DRV8251 4.1A、具有集成电流调节的有刷直流电机驱动器

1 特性

- N 沟道 H 桥有刷直流电机驱动器
- 4.5V 至 48V 工作电源电压范围
- 引脚对引脚、$R_{DS(on)}$、电压和电流检测/调节选项（外部分流电阻器和集成电流镜）
  - DRV8870：6.5V 至 45V、565mΩ 分流电阻器
  - DRV8251：4.5V 至 48V、450mΩ 分流电阻器
  - DRV8251A：4.5V 至 48V、450mΩ 电流镜
  - DRV8231：4.5V 至 33V、600mΩ 分流电阻器
  - DRV8231A：4.5V 至 33V、600mΩ 电流镜
- 高输出电流能力：4.1A 峰值
- PWM 控制接口
- 支持 1.8V、3.3V 和 5V 逻辑输入
- 集成电流调节
- 低功耗睡眠模式
  - 在 V_{VM} = 24V，T_J = 25°C 时，小于 1μA
- 小型封装和外形尺寸
  - 带 PowerPAD™ 的 8 引脚 HSOP 封装，4.9mm × 6.0mm
- 集成型保护特性
  - VM 欠压锁定 (UVLO)
  - 锁存过流保护 (OCP)
  - 热关断 (TSD)

2 应用

- 打印机
- 扫地机器人
- 洗衣机和烘干机
- 咖啡机
- POS 打印机
- 电表
- ATM（自动柜员机）
- 呼吸机
- 外科手术设备
- 电子病床和床控制器
- 健身器

3 说明

DRV8251 器件是一款具有 N 沟道 H 桥、电荷泵、电流调节和保护电路的集成电机驱动器。电荷泵通过支持 N 沟道 MOSFET 半桥和 100% 占空比驱动提升效率。

DRV8251 通过比较模拟输入 VREF 和 ISEN 引脚的电流检测采样电阻上的电压，实现电流调节功能。限制电流的能力可以显著减小电机启动过程中和失速条件下的大电流。

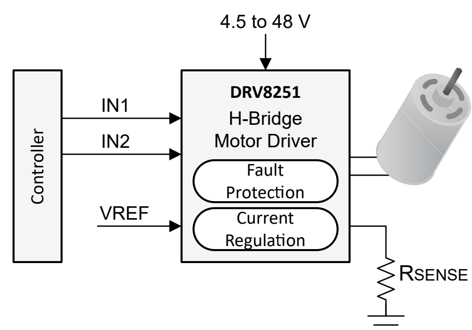
低功耗睡眠模式可通过关断大部分内部电路实现超低静态电流消耗。内部保护功能包括电源欠压锁定、输出过流和器件过热。

DRV8251 所属的器件系列具有引脚对引脚、可扩展 $R_{DS(on)}$ 和电源电压选项，可支持不同负载和电源轨，并尽可能减少设计改动。有关本系列中器件的信息，请参阅节 5。在 ti.com 上查看完整的有刷电机驱动器产品系列。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
DRV8251DDA	HSOP (8)	4.90mm × 6.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化版原理图

English Data Sheet: SLVSFZ6

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
December 2021	*	Initial Release

5 Device Comparison

表 5-1. Device Comparison Table

Device name	Supply voltage (V)	$R_{DS(on)}$ (mΩ)	Current regulation	Current-sense feedback	Overcurrent protection response	Package	Pin-to-pin devices
DRV8870	6.5 to 45	565	External Shunt Resistor	External Amplifier	Automatic Retry	HSOP (4.9x6)	DRV8870, DRV8251, DRV8231
DRV8251	4.5 to 48	450			Latched Disable	HSOP (4.9x6)	
DRV8231	4.5 to 33	600			Automatic Retry	HSOP (4.9x6) WSON (2x2)	
DRV8251A	4.5 to 48	450	Internal current mirror (IPROPI)		Automatic Retry	HSOP (4.9x6)	DRV8251A, DRV8231A
DRV8231A	4.5 to 33	600			Automatic Retry	HSOP (4.9x6) WSON (2x2)	

6 Pin Configuration and Functions

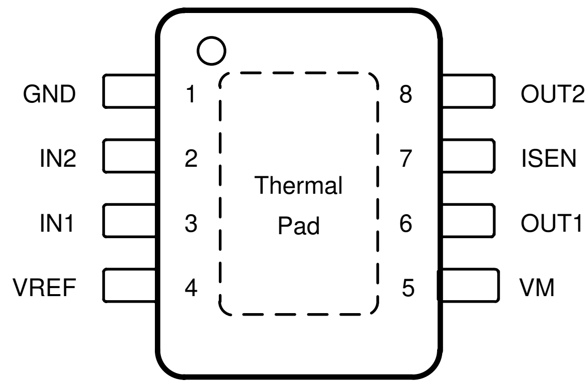


图 6-1. DDA Package 8-Pin HSOP Top View

表 6-1. Pin Functions

PIN NAME	PIN NO.	TYPE	DESCRIPTION
GND	1	PWR	Logic ground. Connect to board ground
IN1	3	I	Logic inputs. Controls the H-bridge output. Has internal pulldowns. See 表 8-2.
IN2	2	I	Logic inputs. Controls the H-bridge output. Has internal pulldowns. See 表 8-2.
ISEN	7	PWR	High-current ground path. If using current regulation, connect ISEN to a resistor (low-value, high-power-rating) to ground. If not using current regulation, connect ISEN directly to ground.
OUT1	6	O	H-bridge output. Connect directly to the motor or other inductive load.
OUT2	8	O	H-bridge output. Connect directly to the motor or other inductive load.
VM	5	PWR	4.5-V to 48-V power supply. Connect a 0.1-μF bypass capacitor to ground, as well as sufficient bulk capacitance, rated for the VM voltage.
VREF	4	I	Analog input. Apply a voltage between 0 to 5 V. For information on current regulation, see the 节 8.4.2 section.
PAD		—	Thermal pad. Connect to board ground. For good thermal dissipation, use large ground planes on multiple layers, and multiple nearby vias connecting those planes.

7 Specifications

7.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Power supply pin voltage	VM	-0.3	50	V
Power supply transient voltage ramp	VM	0	2	V/µs
Logic pin voltage	INx	-0.3	7	V
Reference input pin voltage	VREF	-0.3	6	V
Output pin voltage	OUTx	-0.7	VM + 0.7	V
Current sense input pin voltage	ISEN	-0.5	1	V
Output current	OUTx	Internally Limited	Internally Limited	A
Ambient temperature, T_A		–40	125	°C
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±6000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[2]	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ± 6000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ± 750 V may actually have higher performance.

7.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{VM}	Power supply voltage	VM	4.5		48	V
V_{VREF}	Reference voltage	VREF	0		5	V
V_{IN}	Logic input voltage	INx	0		5.5	V
f_{PWM}	PWM frequency	INx	0		200	kHz
I_{OUT} [1]	Peak output current, $4.5 \leqslant V_{VM} < 5.5$ V	OUTx	0		3.7	A
	Peak output current, $V_{VM} \geqslant 5.5$ V		0		4.1	A
T_A	Operating ambient temperature		–40		125	°C
T_J	Operating junction temperature		–40		150	°C

(1) Power dissipation and thermal limits must be observed

7.4 Thermal Information

THERMAL METRIC[1]		DRV8251 DDA (HSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40.4	°C/W

THERMAL METRIC[(1)]		DRV8251 DDA (HSOP) 8 PINS	UNIT
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	14.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

4.5 V ≤ V_{VM} ≤ 48 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical values are at T_J = 25 °C and V_{VM} = 24 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY (VM)						
I_{VMQ}	VM sleep mode current	V_{VM} = 24 V, IN1 = IN2 = 0, T_J = 25°C			1	μA
I_{VM}	VM active mode current	V_{VM} = 24 V, IN1 = IN2 = 1		3	4	mA
t_{WAKE}	Turnon time	Control signal to active mode			250	μs
t_{SLEEP}	Turnoff time	Control signal to sleep mode	0.8		1.5	ms
LOGIC-LEVEL INPUTS (INx)						
V_{IL}	Input logic low voltage				0.5	V
V_{IH}	Input logic high voltage		1.5			V
V_{HYS}	Input hysteresis			200		mV
I_{IL}	Input logic low current	V_{IN} = 0 V	-1		1	μA
I_{IH}	Input logic high current	V_{IN} = 3.3 V		33	100	μA
R_{PD}	Input pulldown resistance	To GND		100		kΩ
DRIVER OUTPUTS (OUTx)						
$R_{DS(on)\_HS}$	High-side MOSFET on resistance	V_{VM} = 24 V, I = 1 A, f_{PWM} = 25 kHz		225		mΩ
$R_{DS(on)\_LS}$	Low-side MOSFET on resistance	V_{VM} = 24 V, I = 1 A, f_{PWM} = 25 kHz		225		mΩ
V_{SD}	Body diode forward voltage	I_{OUT} = 1 A		0.8		V
t_{RISE}	Output rise time	V_{VM} = 24 V, OUTx rising from 10% to 90%		220		ns
t_{FALL}	Output fall time	V_{VM} = 24 V, OUTx falling from 90% to 10%		220		ns
t_{PD}	Input to output propagation delay	INx to OUTx		0.7	1	μs
t_{DEAD}	Output dead time			200		ns
SHUNT CURRENT SENSE AND REGULATION (ISEN, VREF)						
A_V	ISEN gain	VREF = 2.5 V	9.6	10	10.4	V/V
t_{OFF}	Current regulation off time			25		μs
t_{BLANK}	Current regulation blanking time			2		μs
PROTECTION CIRCUITS						
V_{UVLO}	Supply undervoltage lockout (UVLO)	Supply rising	4.15	4.3	4.45	V
		Supply falling	4.05	4.2	4.35	V
V_{UVLO_HYS}	Supply UVLO hysteresis	Rising to falling threshold		100		mV
t_{UVLO}	Supply undervoltage deglitch time			10		μs
I_{OCP}	Overcurrent protection trip point	4.5 ≤ V_{VM} < 5.5 V	3.7			A
		V_{VM} ≥ 5.5 V	4.1			A

4.5 V ≤ V_{VM} ≤ 48 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical values are at T_J = 25 °C and V_{VM} = 24 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OCP_ISEN}	Overcurrent protection trip point on ISEN pin			0.7		V
t_{OCP}	Overcurrent protection deglitch time			1.5		μs
T_{TSD}	Thermal shutdown temperature		150	175		°C
T_{HYS}	Thermal shutdown hysteresis			40		°C

7.6 Typical Characteristics

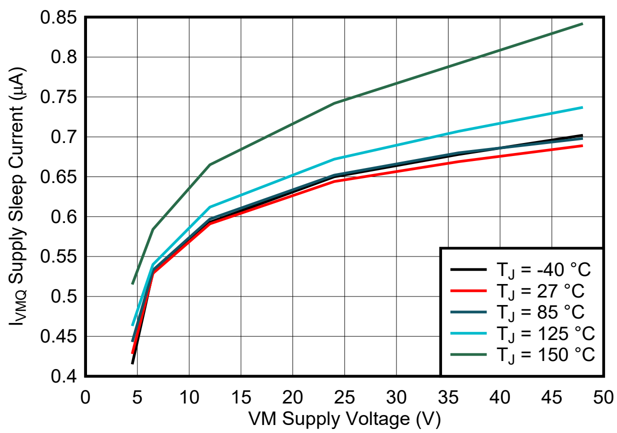


图 7-1. Sleep Current (I_{VMQ}) vs. Supply Voltage (V_{VM})

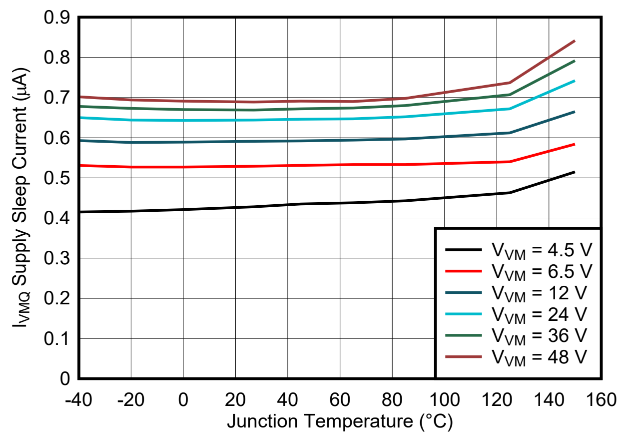


图 7-2. Sleep Current (I_{VMQ}) vs. Junction Temperature (T_J)

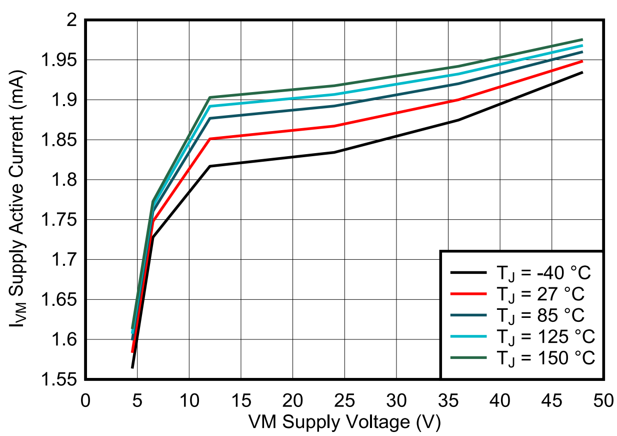


图 7-3. Active Current (I_{VM}) vs. Supply Voltage (V_{VM})

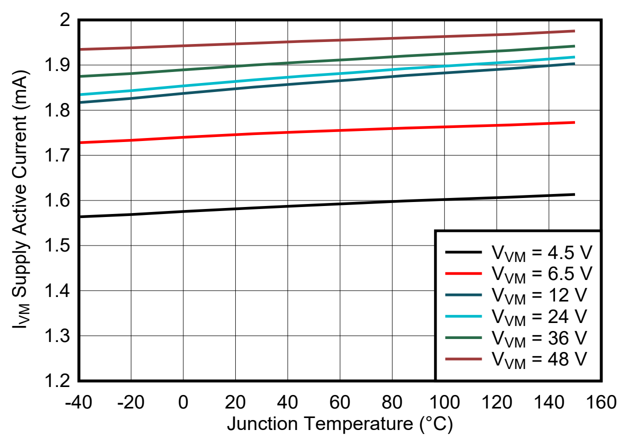


图 7-4. Active Current (I_{VM}) vs. Junction Temperature (T_J)

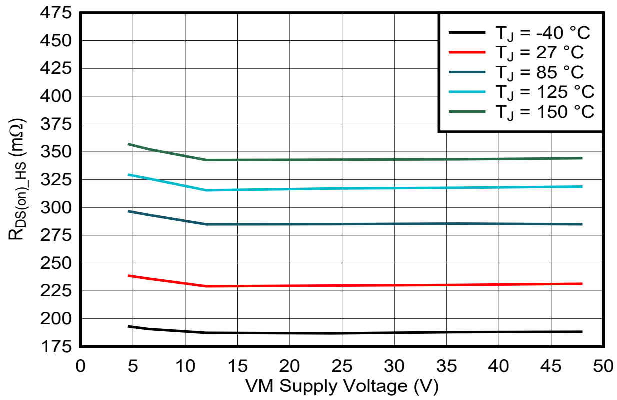


图 7-5. High-Side $R_{DS(on)}$ vs. VM Supply Voltage

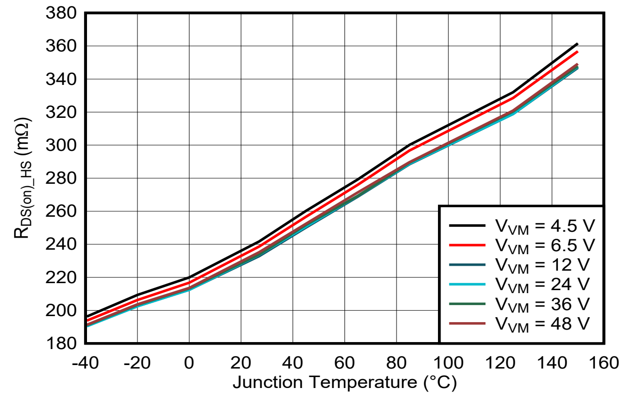


图 7-6. High-Side $R_{DS(on)}$ vs. Junction Temperature (T_J)

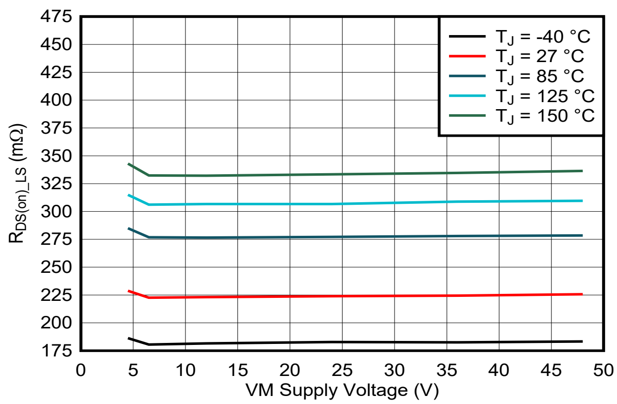


图 7-7. Low-Side $R_{DS(on)}$ vs. VM Supply Voltage

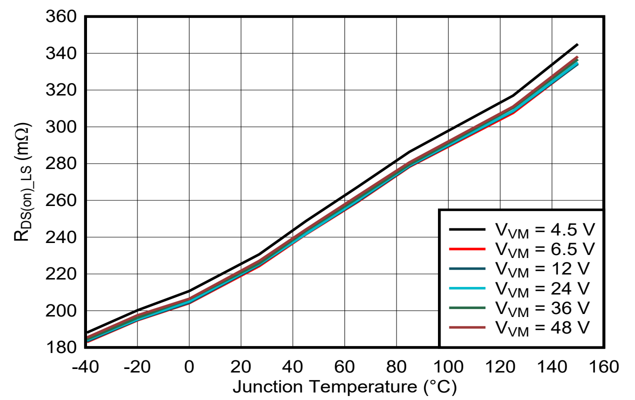
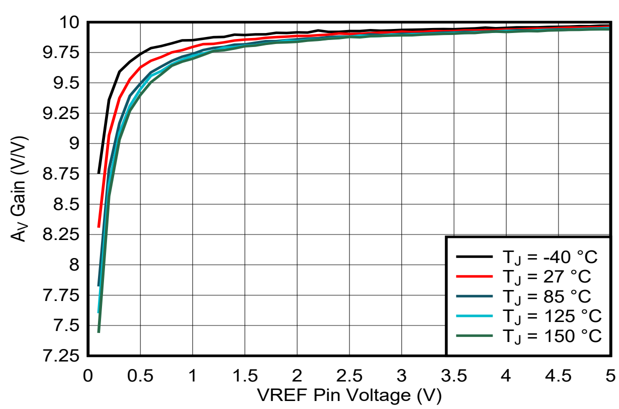


图 7-8. Low-Side $R_{DS(on)}$ vs. Junction Temperature (T_J)



V_{VM} = 24 V

图 7-9. Current Regulation Gain (A_V) vs. Reference Voltage (VREF)

7.7 Timing Diagrams

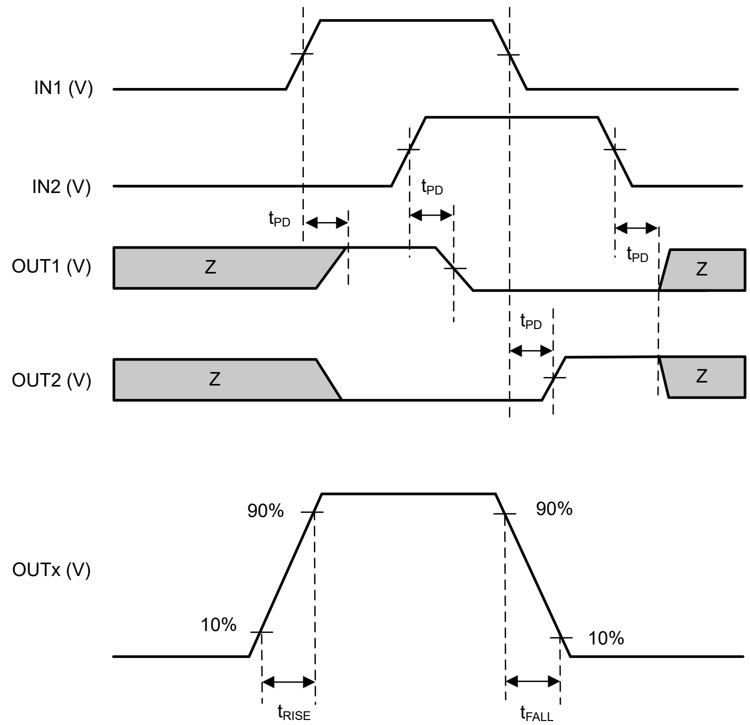


图 7-10. Input-to-Output Timing

8 Detailed Description

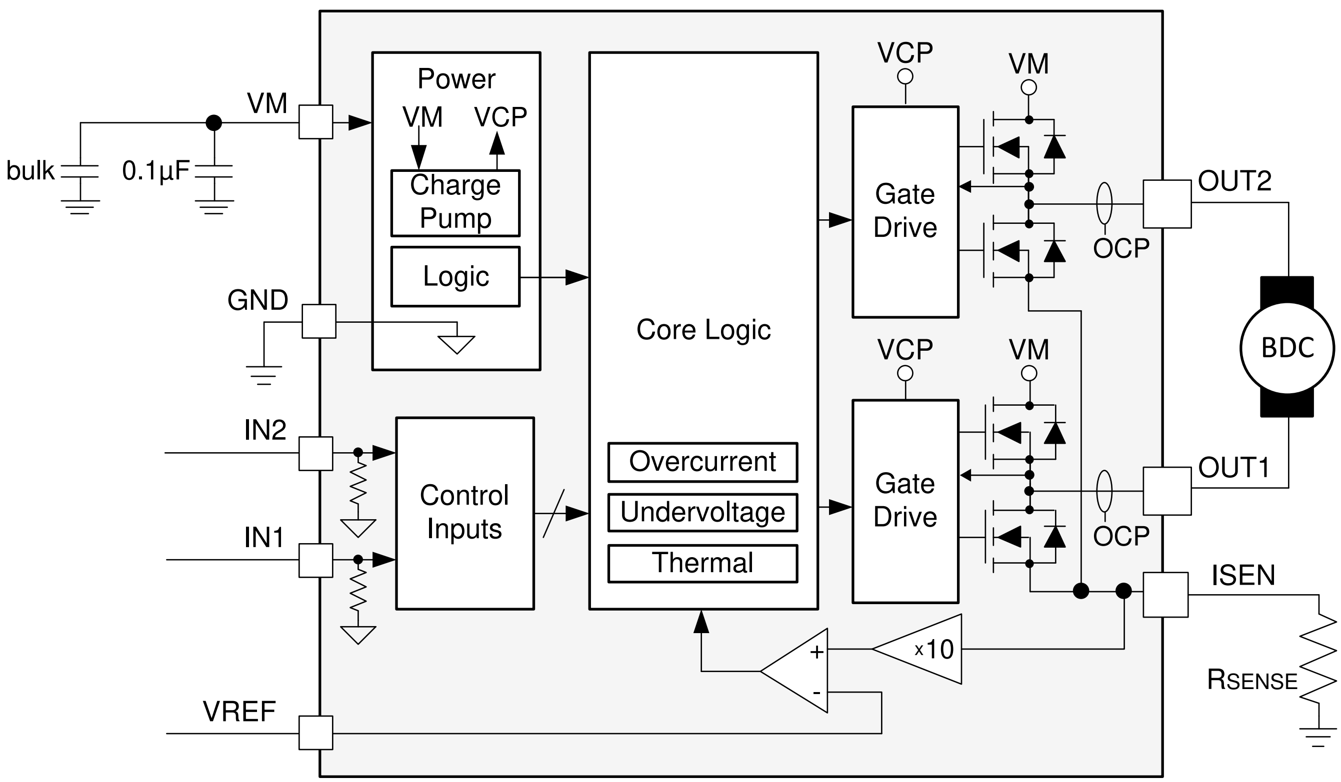
8.1 Overview

The DRV8251 is an 8-pin device for driving brushed DC motors from a 4.5-V to 48-V supply rail. Two logic inputs control the H-bridge driver, which consists of four N-channel MOSFETs that have a typical $R_{DS(on)}$ of 450 mΩ (including one high-side and one low-side FET). A single power input, VM, serves as both device power and the motor winding bias voltage. The integrated charge pump of the device boosts VM internally and fully enhances the high-side FETs. Motor speed can be controlled with pulse-width modulation at frequencies between 0 to 200 kHz. The device enters a low-power sleep mode by bringing both inputs low.

The DRV8251 also integrates current regulation using an external shunt resistor on the ISEN pin. This allows the device to limit the output current with a fixed off-time PWM chopping scheme to limit inrush and stall currents. The current regulation level can be configured during motor operation through the VREF pin to limit the load current accordingly to the system demands.

A variety of integrated protection features protect the device in the case of a system fault. These include undervoltage lockout (UVLO), overcurrent protection (OCP), and overtemperature shutdown (TSD).

8.2 Functional Block Diagram



8.3 External Components

表 8-1 lists the recommended external components for the device.

表 8-1. Recommended external components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	GND	0.1-µF, low ESR ceramic capacitor, VM-rated.
C_{VM2}	VM	GND	节 10.1, VM-rated.

8.4 Feature Description

8.4.1 Bridge Control

The DRV8251 output consists of four N-channel MOSFETs that are designed to drive high current. These outputs are controlled by the two logic inputs IN1 and IN2 as listed in 表 8-2.

表 8-2. H-Bridge Control

IN1	IN2	OUT1	OUT2	DESCRIPTION
0	0	High-Z	High-Z	Coast; H-bridge disabled to High-Z (sleep entered after 1 ms)
0	1	L	H	Reverse (Current OUT2 → OUT1)
1	0	H	L	Forward (Current OUT1 → OUT2)
1	1	L	L	Brake; low-side slow decay

The inputs can be set to static voltages for 100% duty cycle drive, or they can be pulse-width modulated (PWM) for variable motor speed. When using PWM, switching between driving and braking typically works best. For example, to drive a motor forward with 50% of the maximum RPM, IN1 = 1 and IN2 = 0 during the driving period, and IN1 = 1 and IN2 = 1 during the other period. Alternatively, the coast mode (IN1 = 0, IN2 = 0) for *fast current decay* is also available. 图 8-1 shows how the motor current flows through the H-bridge. The input pins can be powered before VM is applied.

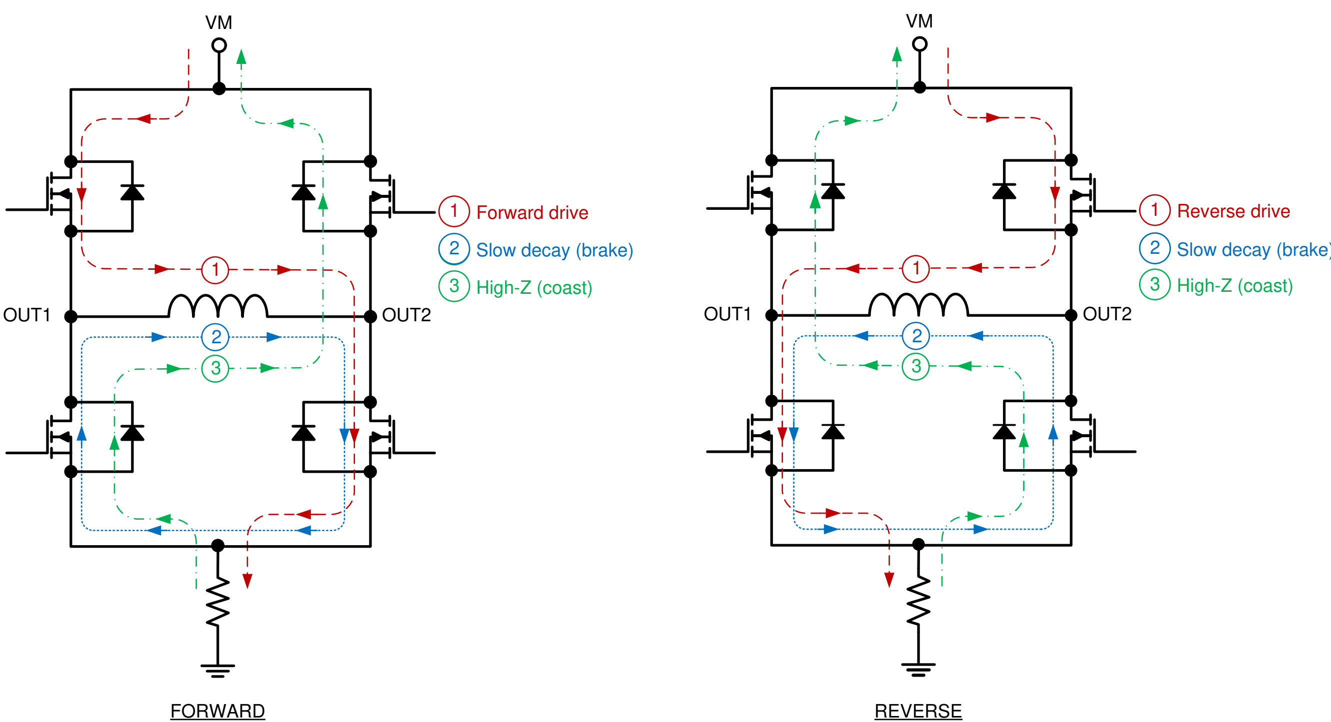


图 8-1. H-Bridge Current Paths

When an output changes from driving high to driving low, or driving low to driving high, dead time is automatically inserted to prevent shoot-through. The t_{DEAD} time is the time in the middle when the output is High-Z. If the output pin is measured during t_{DEAD}, the voltage depends on the direction of current. If the current is leaving the pin, the voltage is a diode drop below ground. If the current is entering the pin, the voltage is a diode drop above VM. This diode is the body diode of the high-side or low-side FET.

The propagation delay time (t_{PD}) is measured as the time between an input edge to output change. This time accounts for input deglitch time and other internal logic propagation delays. The input deglitch time prevents noise on the input pins from affecting the output state. Additional output slew delay timing accounts for FET turn on or turn off times (t_{RISE} and t_{FALL}).

图 8-2 below shows the timing of the inputs and outputs of the motor driver.

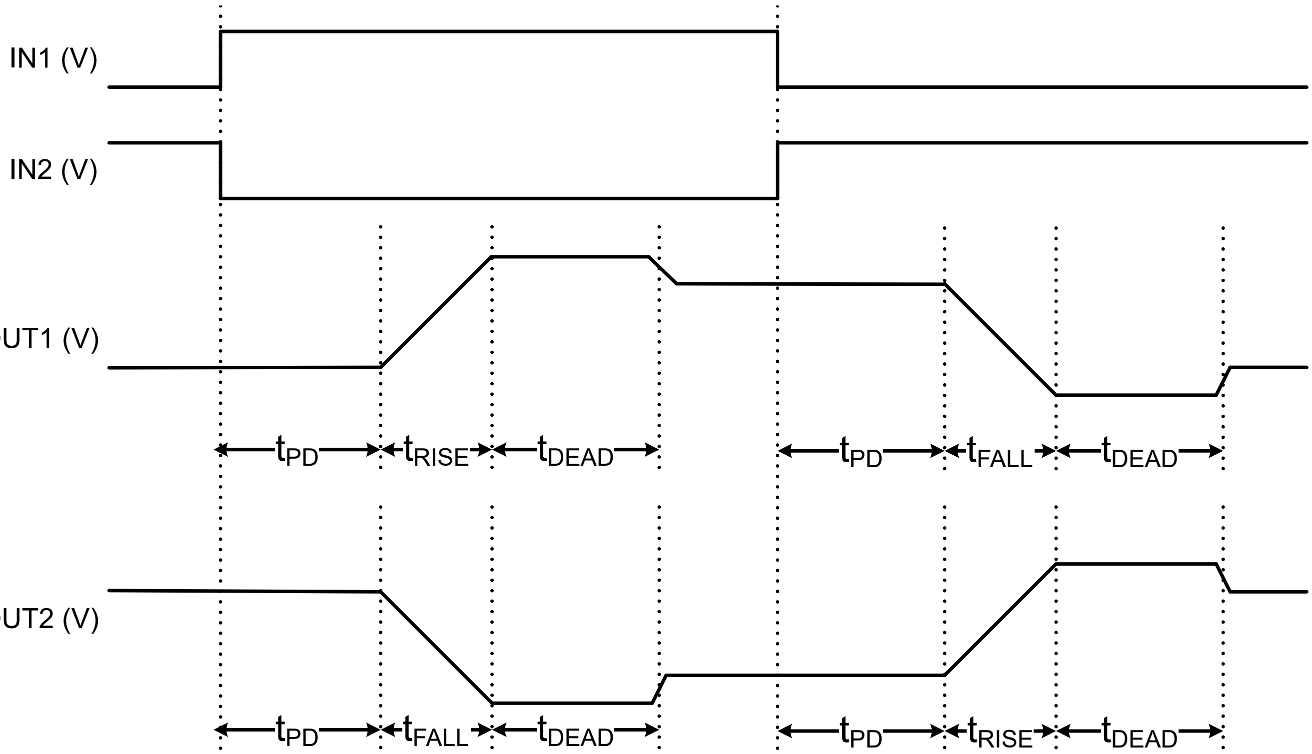


图 8-2. H-Bridge Timing Diagram

8.4.2 Current Regulation

The DRV8251 device limits the output current based on the analog input, VREF, and the resistance of an external sense resistor on the ISEN pin, R_{SENSE}, according to 方程式 1:

$$I_{TRIP} = \frac{VREF}{A_V \times R_{SENSE}} = \frac{VREF}{10 \times R_{SENSE}} \quad (1)$$

By using current regulation, the device input pins can be set for 100% duty cycle, while the device switches the outputs to keep the motor current at the I_{TRIP} level. For example, if VREF = 3.3 V and a R_{SENSE} = 0.15 Ω, the DRV8251 limits motor current to 2.2 A during high torque conditions. For guidelines on selecting a sense resistor, see the *节 9.2.1.2.3* section.

When I_{TRIP} is reached, the device enforces slow current decay by enabling both low-side FETs, and it does this for a time of t_{OFF}.

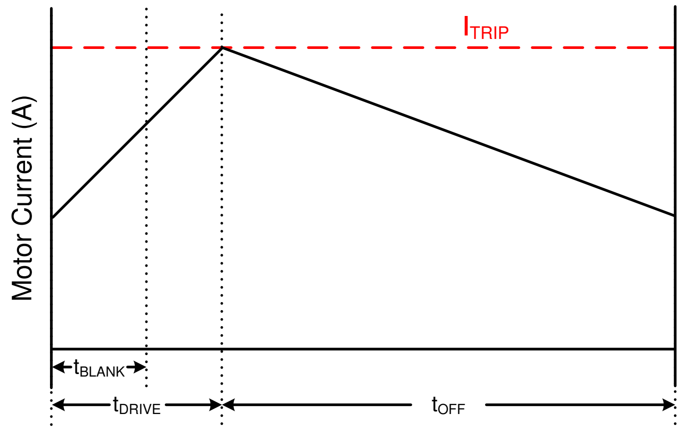


图 8-3. Current-Regulation Time Periods

After t_{OFF} elapses, the output is re-enabled according to the two inputs, INx. The drive time (t_{DRIVE}) until reaching another I_{TRIP} event heavily depends on the VM voltage, the back-EMF of the motor, and the inductance of the motor.

If current regulation is not required, the ISEN pin should be directly connected to the PCB ground plane. The VREF voltage must still be 0.3 V to 5 V, and larger voltages provide greater noise margin. This provides the highest-possible peak current which is up to $I_{OCP,min}$ for a few hundred milliseconds (depending on PCB characteristics and the ambient temperature). If current exceeds $I_{OCP,min}$, the device may enter the fault mode due to overcurrent protection (OCP) or overtemperature shutdown (TSD).

8.4.3 Protection Circuits

The DRV8251 device is fully protected against VM undervoltage, overcurrent, and overtemperature events.

8.4.3.1 Overcurrent Protection (OCP)

If the output current exceeds the OCP threshold, I_{OCP}, for longer than t_{OCP}, the device enters fault mode and all FETs in the H-bridge are disabled. The device remains fault mode until it is reset by putting it into sleep mode with the INx pins or by removing the VM power supply.

Overcurrent conditions are detected independently on both high- and low-side FETs. This means that a short to ground, supply, or across the motor winding will all result in an overcurrent shutdown. The ISEN pin also integrates a separate overcurrent trip threshold specified by V_{OCP_ISEN} for additional protection when the VM voltage is low or the R_{SENSE} resistance on the ISEN pin is high.

8.4.3.2 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge are disabled. After the die temperature has fallen to a safe level, operation automatically resumes.

8.4.3.3 VM Undervoltage Lockout (UVLO)

Whenever the voltage on the VM pin falls below the UVLO falling threshold voltage, V_{UVLO}, all circuitry in the device is disabled, the output FETS are disabled, and all internal logic is reset. Operation continues when the V_{VM} voltage rises above the UVLO rising threshold as shown in 图 8-4.

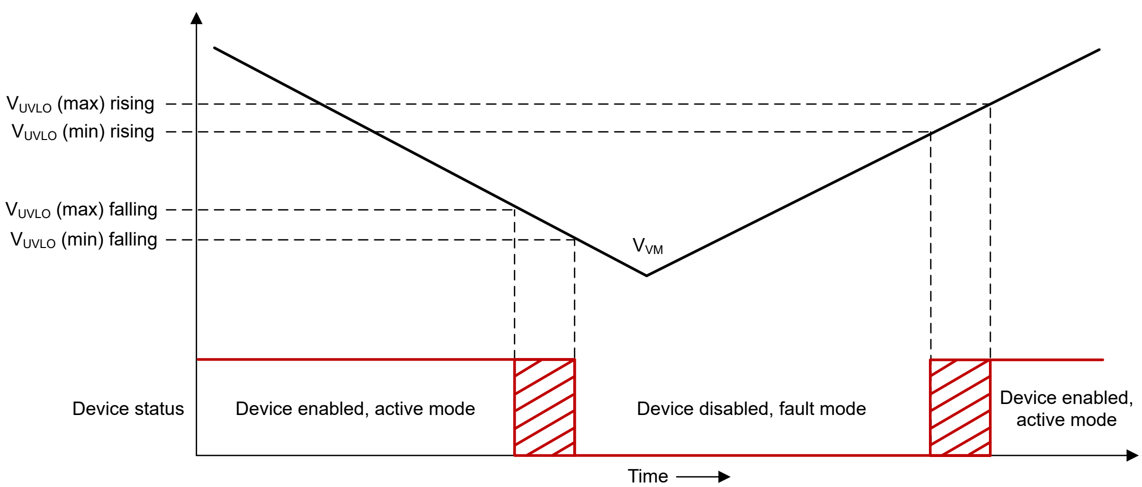


图 8-4. VM UVLO Operation

8.5 Device Functional Modes

表 8-3 summarizes the DRV8251 functional modes described in this section.

表 8-3. Modes of Operation

MODE	CONDITION	H-BRIDGE	INTERNAL CIRCUITS
Active Mode	IN1 or IN2 = logic high	Operating	Operating
Low-Power Sleep Mode	IN1 = IN2 = logic low	Disabled	Disabled
Fault Mode	Any fault condition met	Disabled	See 表 8-4

8.5.1 Active Mode

After the supply voltage on the VM pin has crossed the undervoltage threshold V_{UVLO}, the INx pins are in a state other than IN1 = 0 & IN2 = 0, and t_{WAKE} has elapsed, the device enters active mode. In this mode, the H-bridge, charge pump, and internal logic are active and the device is ready to receive inputs.

8.5.2 Low-Power Sleep Mode

When the IN1 and IN2 pins are both low for time t_{SLEEP}, the DRV8251 device enters a low-power sleep mode. In sleep mode, the outputs remain High-Z and the device draws minimal current from the supply pin (I_{VMQ}). If the device is powered up while all inputs are low, it immediately enters sleep mode. After any of the input pins are set high for longer than the duration of t_{WAKE}, the device becomes fully operational. 图 8-5 shows an example timing diagram for entering and leaving sleep mode.

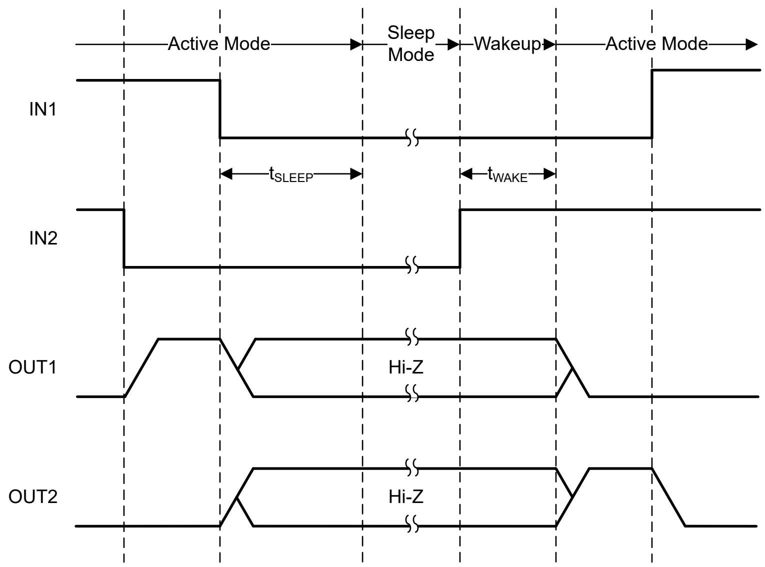


图 8-5. Sleep Mode Entry and Wakeup Timing Diagram

8.5.3 Fault Mode

The DRV8251 device enters a fault mode when a fault is encountered. This is utilized to protect the device and the output load. The device behavior in the fault mode is described in and depends on the fault condition. The device will leave the fault mode and re-enter the active mode when the recovery condition is met.

表 8-4. Fault Conditions Summary

FAULT	CONDITION	H-BRIDGE	INTERNAL CIRCUITS	RECOVERY
VM undervoltage (UVLO)	$V_M < V_{UVLO,falling}$	Disabled	Disabled	$V_M > V_{UVLO,rising}$
Overcurrent (OCP)	$I_{OUT} > I_{OCP}$	Disabled	Operating	$I_{OUT} < I_{OCP}$ and device is power cycled or reset using sleep mode
Thermal Shutdown (TSD)	$T_J > T_{TSD}$	Disabled	Operating	$T_J < T_{TSD} – T_{HYS}$

8.6 Pin Diagrams

8.6.1 Logic-Level Inputs

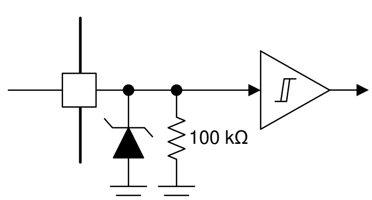


图 8-6. Logic-level input

9 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DRV8251 device is typically used to drive one brushed DC motor.

9.2 Typical Application

9.2.1 Brush DC Motor

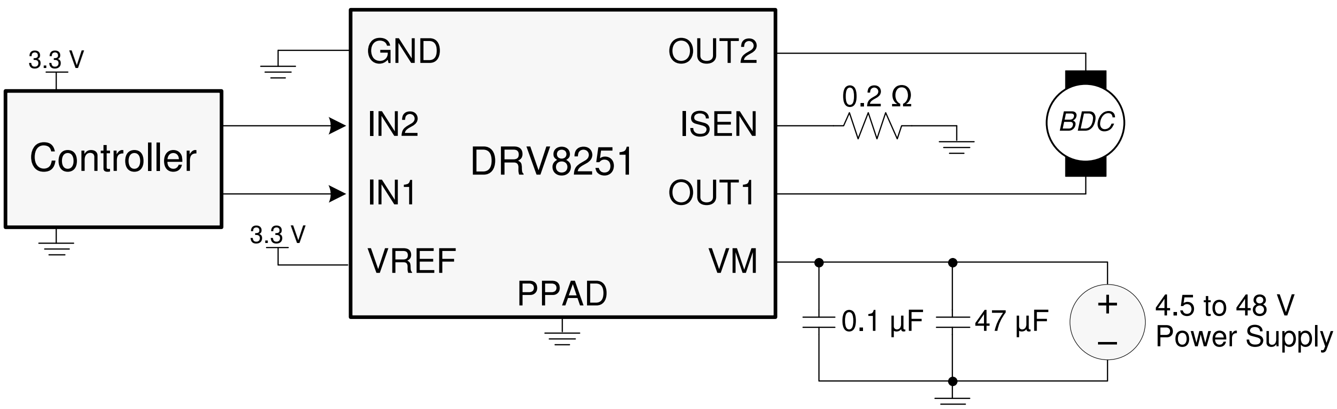


图 9-1. Typical Connections

9.2.1.1 Design Requirements

The table below lists the design parameters.

表 9-1. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor voltage	V_{VM}	12 V
Average motor current	I_{AVG}	0.8 A
Motor inrush (startup) current	I_{INRUSH}	2.1 A
Motor stall current	I_{STALL}	2.1 A
Motor current trip point	I_{TRIP}	1.9 A
VREF voltage	VREF	4 V
Sense resistance	R_{SENSE}	0.2 Ω
PWM frequency	f_{PWM}	20 kHz

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Motor Voltage

The motor voltage to use depends on the ratings of the motor selected and the desired RPM. A higher voltage spins a brushed DC motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive motor windings.

9.2.1.2.2 Motor Current

Motors experience large currents at low speed, initial startup, and stalled rotor conditions. The large current at motor startup is sometimes called inrush current. The current regulation feature in the DRV8251 can help to limit these large currents. 图 9-4 and 图 9-5 show examples of limiting inrush current.

Alternatively, the microcontroller may limit the inrush current by ramping the PWM duty cycle during the startup time.

9.2.1.2.3 Sense Resistor

For optimal performance, the sense resistor must have the following characteristics:

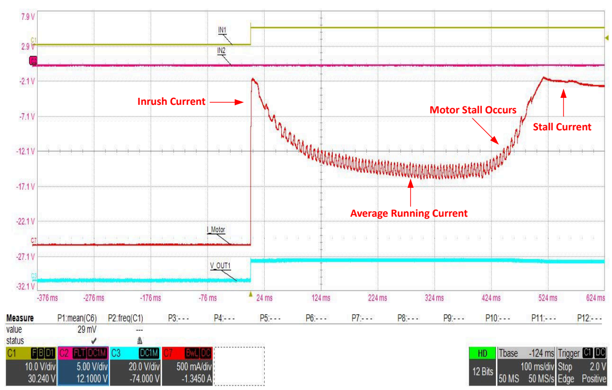
- Surface-mount
- Low inductance
- Rated for high enough power
- Placed closely to the motor driver

The power dissipated by the sense resistor equals $(I_{AVG})^2 \times R$. For example, if peak motor current is 3 A, average motor current is 1.5 A, and a 0.2-Ω sense resistor is used, the resistor dissipates 1.5 $A^2 \times 0.2\ \Omega = 0.45$ W. The power quickly increases with higher current levels.

Resistors typically have a rated power within some ambient temperature range, along with a derated power curve for high ambient temperatures. When a PCB is shared with other components generating heat, the system designer should add margin. Measuring the actual sense resistor temperature in a final system is always best.

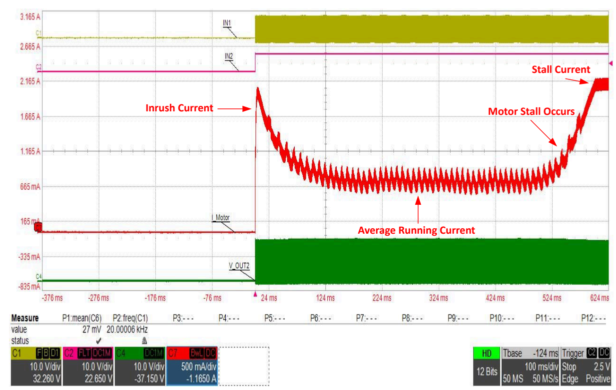
Because power resistors are larger and more expensive than standard resistors, using multiple standard resistors in parallel, between the sense node and ground, is common and distributes the current and heat dissipation.

9.2.1.3 Application Curves



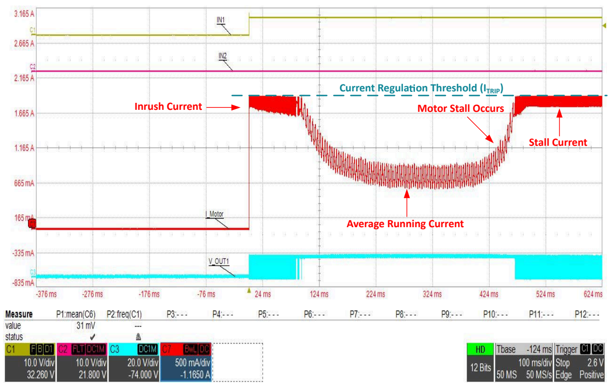
Ch 1 (Yellow) = IN1 Signal Ch 2 (Magenta) = IN2 Signal
Ch 3 (Blue) = OUT1 Voltage Ch 7 (Red) = Motor Current

图 9-2. Motor startup at 100% duty cycle



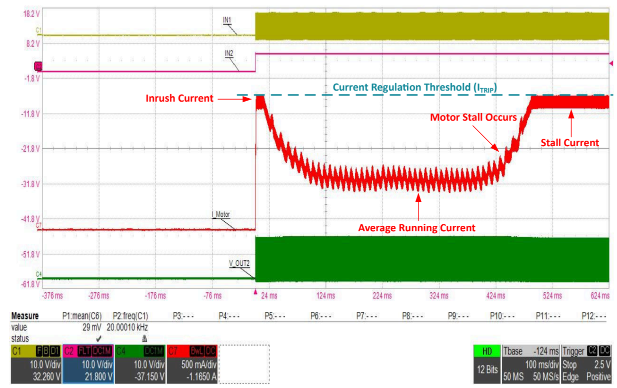
Ch 1 (Yellow) = IN1 Signal Ch 2 (Magenta) = IN2 Signal
Ch 4 (Green) = OUT2 Voltage Ch 7 (Red) = Motor Current

图 9-3. Motor startup at 50% duty cycle



Ch 1 (Yellow) = IN1 Signal　Ch 2 (Magenta) = IN2 Signal
Ch 3 (Blue) = OUT1 Voltage　Ch 7 (Red) = Motor Current

图 9-4. Motor startup at 100% duty cycle with current regulation



Ch 1 (Yellow) = IN1 Signal　Ch 2 (Magenta) = IN2 Signal
Ch 4 (Green) = OUT2 Voltage　Ch 7 (Red) = Motor Current

图 9-5. Motor startup at 50% duty cycle with current regulation

9.2.2 Stall Detection

Some applications require stall detection to notify the microcontroller of a locked rotor condition. A stall could be caused by one of two things: unintended mechanical blockage or the load reaching an end-stop in a constrained travel path. By using current-sense amplifier (CSA) to amplify the voltage on the ISEN pin of the DRV8251, the system can implement a simple stall detection scheme. 图 9-6 shows an example schematic implementation.

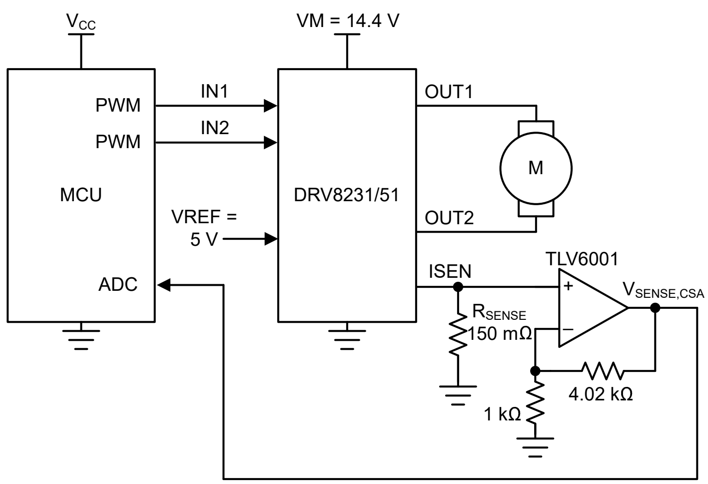


图 9-6. Stall Detection Circuit

The principle of this stall detection scheme relies on the fact that motor current increases during stall conditions as shown in 图 9-7. To implement stall detection, the microcontroller reads the voltage from CSA using an analog-to-digital converter (ADC) and compares it to a stall threshold set in firmware. Alternatively, a comparator peripheral may be used to set this threshold as well.

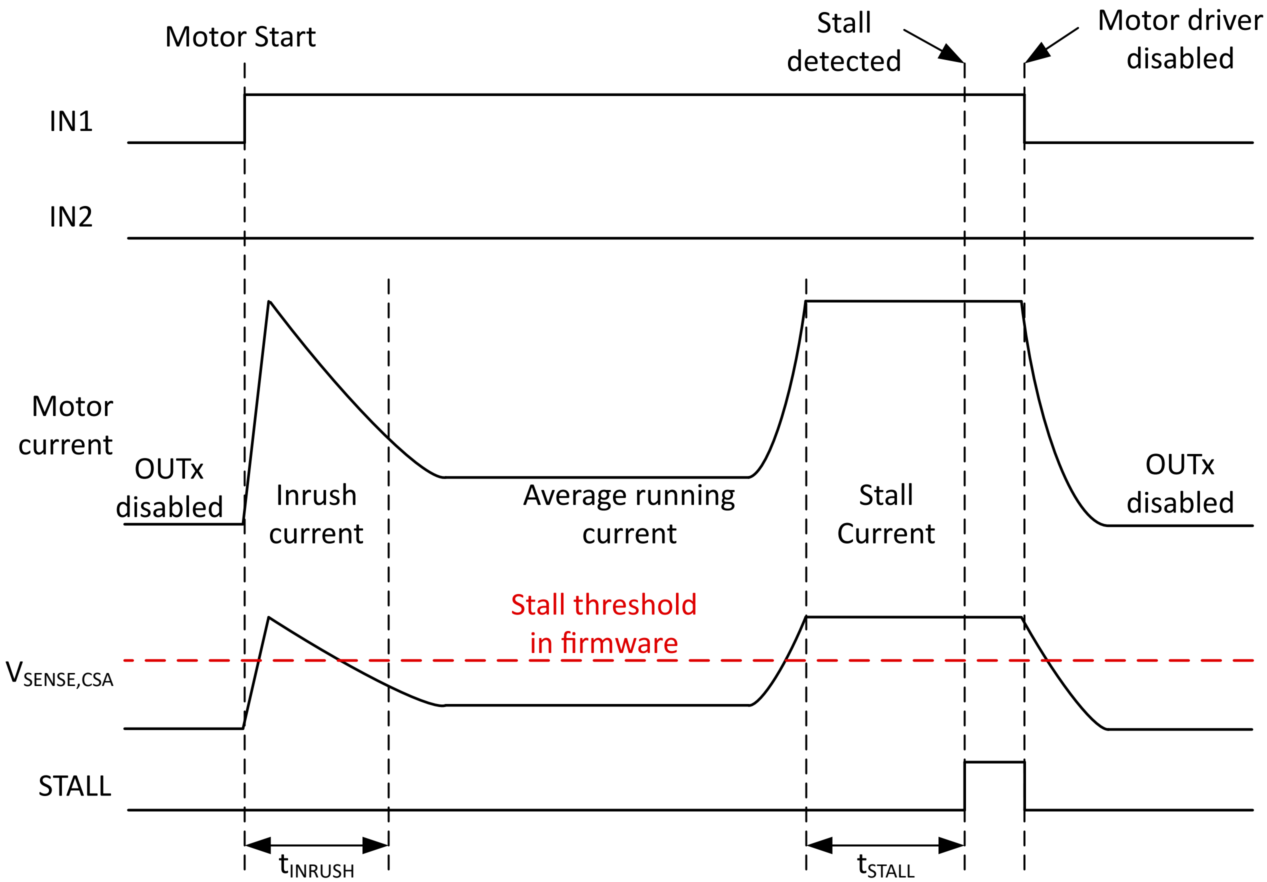


图 9-7. Motor Current Profile with STALL Signal

9.2.2.1 Design Requirements

The table below lists the design parameters.

表 9-2. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor voltage	V_M	14.4 V
VREF voltage	VREF	3.3 V
ISEN resistance	R_{SENSE}	150 mΩ
Stall current	I_{STALL}	1.5 A
Stall detection threshold	$I_{STALL,TH}$	1 A
Inrush current ignore time	t_{INRUSH}	80 ms
Stall detection time	t_{STALL}	80 ms

9.2.2.2 Detailed Design Procedure

9.2.2.2.1 Stall Detection Timing

The microcontroller needs to decide whether or not the $V_{SENSE,CSA}$ signal indicates a motor stall. Large inrush current occurs during motor start up because motor speed is low. As the motor accelerates, the motor current drops to an average level because the back electromotive force (EMF) in the motor increases with speed. The inrush current should not be mistaken for a stall condition. One way to do this is for the microcontroller to ignore the $V_{SENSE,CSA}$ signal above the firmware stall threshold for the duration of the inrush current, t_{INRUSH}, at startup. The t_{INRUSH} timing should be determined experimentally because it depends on motor parameters, supply voltage, and mechanical load response times.

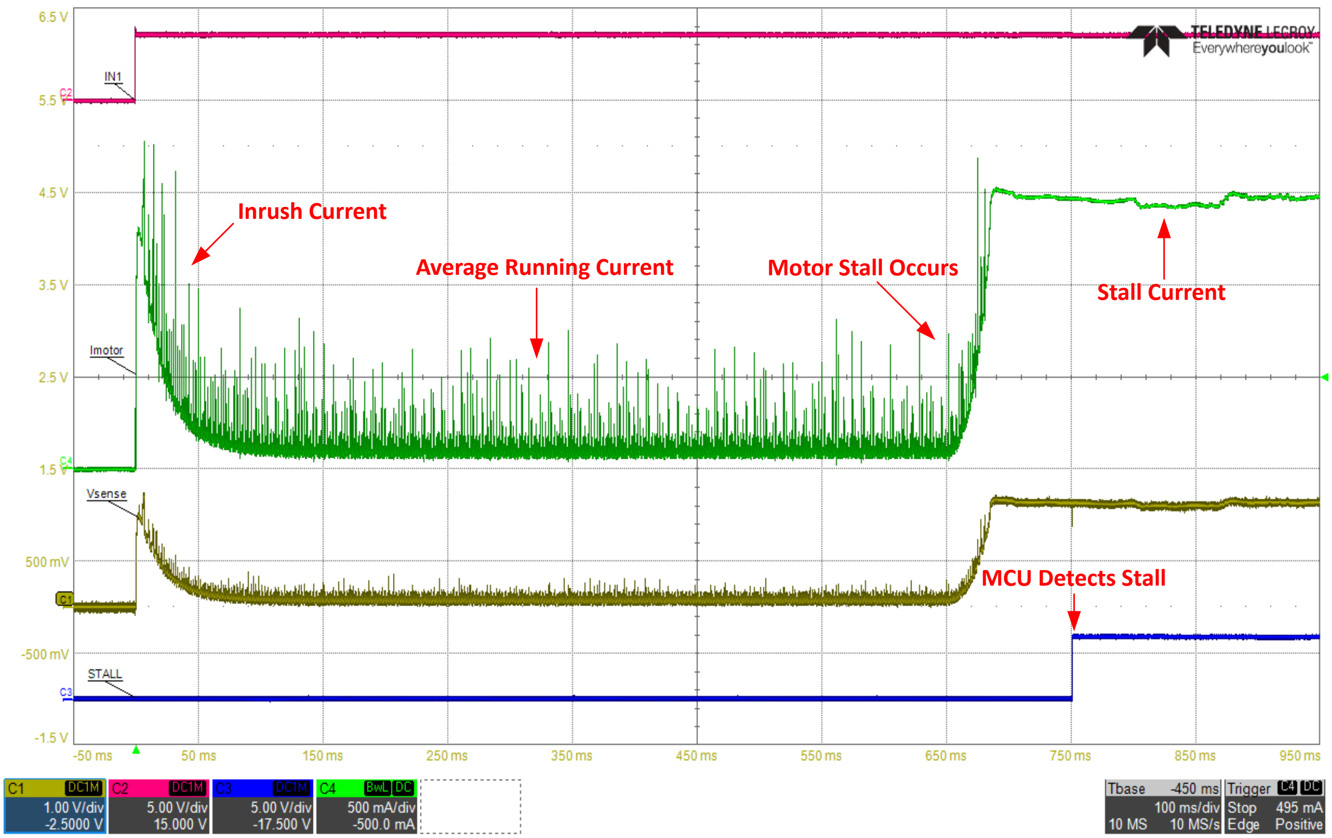
When a stall condition occurs, the motor current will increase from the average running current level because the back EMF is now 0 V. In some cases, it may be desirable to drive at the stall curent for some time in case the motor can clear the blockage on its own. This might be useful for an unintended stall or high-torque condition on the motor. In this case, the system designer can choose a long stall detection time, t_{STALL}, before the microcontroller decides to take action. In other cases, like end-stop detection, a faster response might be desired to reduce power or minimize strong motor torque on the gears or end-stop. This corresponds to setting a shorter t_{STALL} time in the microcontroller.

图 9-7 illustrates the t_{INRUSH} and t_{STALL} timings and how they relate to the motor current waveform.

9.2.2.2.2 Stall Threshold Selection

The stall detection threshold in firmware should be chosen at a current level between the maximum stall current and the average running current of the motor as shown in 图 9-7.

9.2.2.3 Application Curves



Ch 1 (Yellow) = CSA Output Voltage
Ch 2 (Magenta) = IN1 Signal
Ch 3 (Blue) = Stall Detection Indication
Ch 4 (Green) = Motor Current

图 9-8. Example Waveform of Stall Detection

9.2.3 Relay Driving

The PWM interface may also be used to drive single- and dual-coil latching relays, as shown in the figures below.

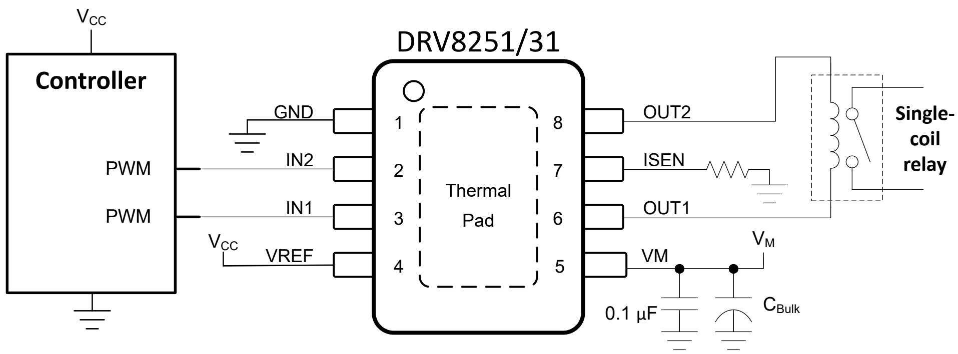


图 9-9. Single-Coil Relay Driving

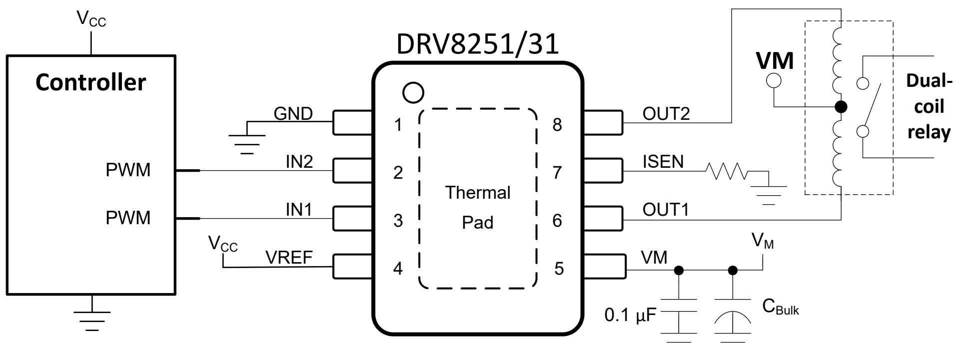


图 9-10. Dual-Coil Relay Driving

9.2.3.1 Design Requirements

表 9-3 provides example requirements for a single- or dual-coil relay application. Current regulation may also be configured to ensure the relay current is within the relay specification. This is important if the VM supply voltage is higher than the voltage rating of the relay.

表 9-3. System design requirements

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor supply voltage	V_M	12 V
Microcontroller supply voltage	V_{CC}	3.3 V
Single coil relay current	I_{Relay}	500 mA pulse for 200 ms
Dual coil relay current	I_{OUT1}, I_{OUT2}	100 mA pulse for 200 ms

9.2.3.2 Detailed Design Procedure

9.2.3.2.1 Control Interface for Single-Coil Relays

The PWM interface can be used to drive single-coil relays. To actuate the relay, the driver needs to drive current with either the forward or reverse states in the PWM table. After driving the relay, the outputs can be disabled (IN1=IN2=0) to put the driver to sleep and save energy. Alternatively, the outputs can be put into brake mode briefly after actuation to avoid back EMF effects from the relay or causing current to flow back from the relay into the VM supply node.

9.2.3.2.2 Control Interface for Dual-Coil Relays

A dual coil relay only require two low-side drivers if the center tap is connected to VM. The body diodes of the unused FETs act as freewheeling diodes, so additional freewheeling diodes are not needed when driving a dual-coil relay with the DRV8251. The PWM interface can be used to control the dual-coil relay. The following figures show the schematic and timing diagram for driving dual-coil relays.

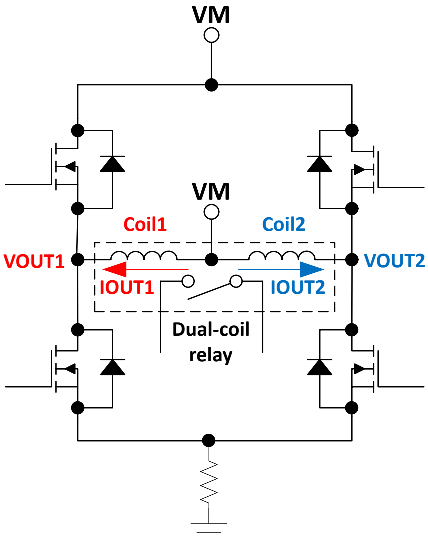


图 9-11. Schematic of dual-coil relay driven by the OUTx H-bridge

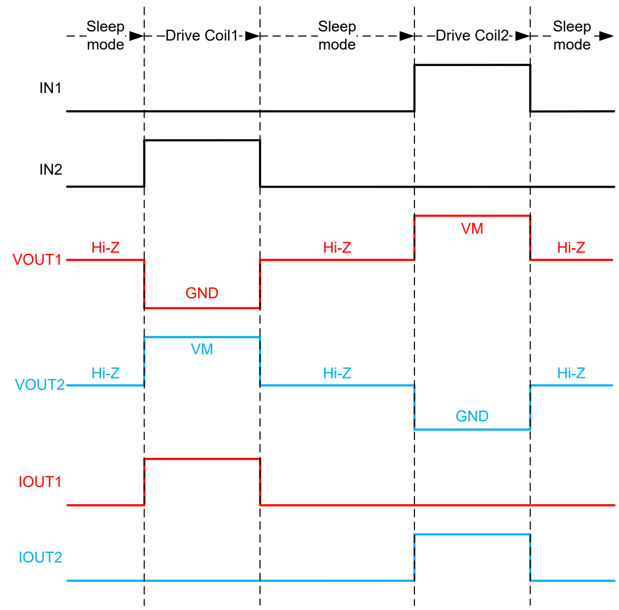


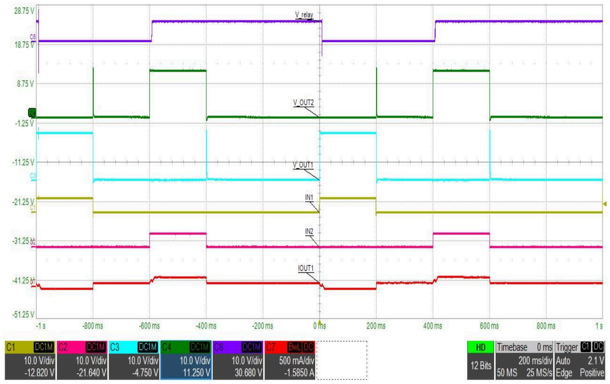
图 9-12. Timing diagram for driving a dual-coil relay with PWM interface

表 9-4 shows the logic table for the PWM interface. The descriptions in this table reflect how the input and output states drive the dual coil relay. When Coil1 is driven (OUT1 voltage is at GND), The voltage at OUT2 will go to VM. Because the center tap of the relay is also at VM, no current flows through Coil2. The same is true when Coil2 is driven; Coil1 shorts to VM. The body diodes of the high-side FETs act as freewheeling diodes, so extra external diodes are not needed. 图 9-15 shows oscilloscope traces for this application.

表 9-4. PWM control table for dual-coil relay driving

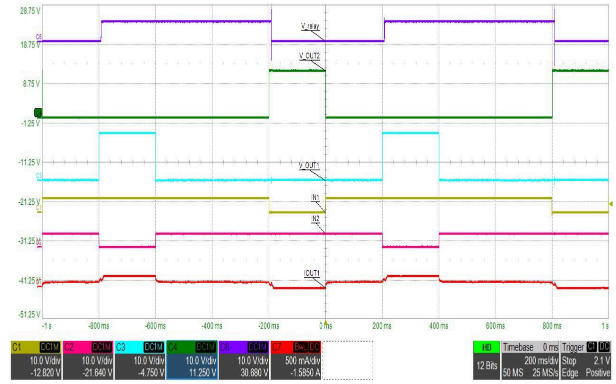
IN1	IN2	OUT1	OUT2	DESCRIPTION
0	0	Hi-Z	Hi-Z	Outputs disabled (H-Bridge Hi-Z)
0	1	L	H	Drive Coil1
1	0	H	L	Drive Coil2
1	1	L	L	Drive Coil1 and Coil2 (invalid state for a dual-coil latching relay)

9.2.3.3 Application Curves



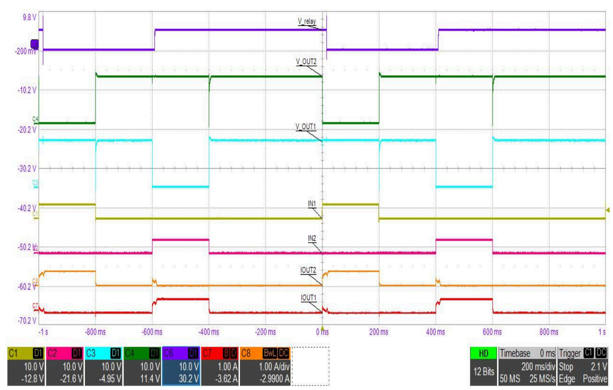
A. Ch 1 = IN1 Ch 2 = IN2 Ch 3 = V_{OUT1} Ch 4 = V_{OUT2} Ch 6 = Relay Switch Ch 7 = Relay Coil Current

图 9-13. PWM driving for a single-coil latching relay with driving profile FORWARD → COAST → REVERSE → COAST



A. Ch 1 = IN1 Ch 2 = IN2 Ch 3 = V_{OUT1} Ch 4 = V_{OUT2} Ch 6 = Relay Switch Ch 7 = Relay Coil Current

图 9-14. PWM driving for a single-coil latching relay with driving profile FORWARD → BRAKE → REVERSE → BRAKE



A. Ch 1 = IN1 Ch 2 = IN2 Ch 3 = V_{OUT1} Ch 4 = V_{OUT2} Ch 6 = Relay Switch Ch 7 = Relay Coil1 Current Ch 8 = Relay Coil2 Current

图 9-15. PWM driving for dual-coil relay

9.2.4 Multi-Sourcing with Standard Motor Driver Pinout

The DRV8870, DRV8251, and DRV8231 devices come in an industry standard package footprint in the DDA package. When the system needs current sensing, a current-sense amplifier may be used across the R_{SENSE} resistor to provide an amplifed signal back to an microcontroller ADC as shown in 图 9-16. To reduce the size of the system bill of materials and cost, the IPROPI function in DRV8231A/51A can replace the current sense amplifer. During the board design process, both solutions, IPROPI and industry standard shunt devices, can be accomodated in the same board layout by placing and not placing (DNP) components as shown in 图 9-17. This allows the system to be flexible for lowest cost with the DRV8231A/51A or for use with second-source devices with the same pinout as DRV8870, DRV8231, and DRV8251.

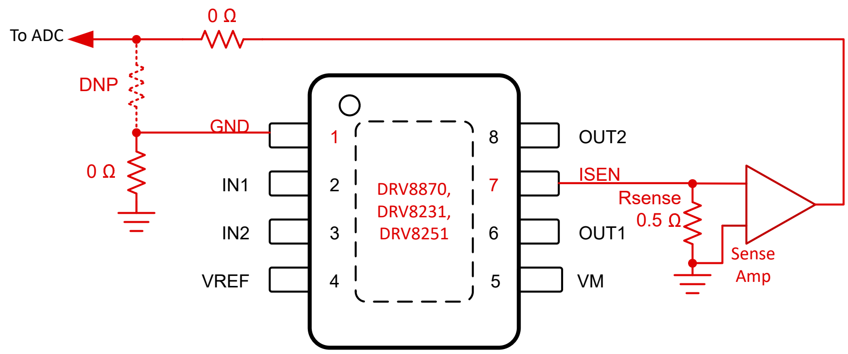


图 9-16. Standard Pinout with Current Sense Amplifier

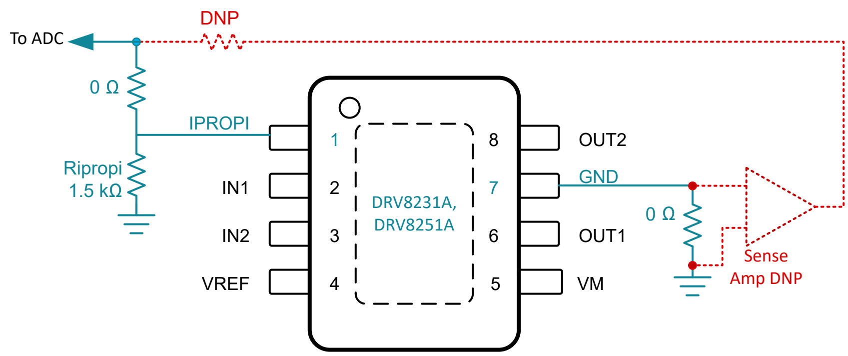


图 9-17. DRV8231A/51A Device Using IPROPI to Integrate The Current Sense Function into The Motor Driver

9.3 Current Capability and Thermal Performance

The output current and power dissipation capabilities of the driver depends heavily on the PCB design and external system conditions. This section provides some guidelines for calculating these values.

9.3.1 Power Dissipation and Output Current Capability

Total power dissipation for the device consists of three main components: quiescent supply current dissipation (P_{VM}), the power MOSFET switching losses (P_{SW}), and the power MOSFET $R_{DS(on)}$ (conduction) losses (P_{RDS}). While other factors may contribute additional power losses, they are typically insignificant compared to the three main items.

$$P_{TOT} = P_{VM} + P_{SW} + P_{RDS} \tag{2}$$

P_{VM} can be calculated from the nominal motor supply voltage (V_{VM}) and the I_{VM} active mode current specification.

$$P_{VM} = V_{VM} \times I_{VM} \tag{3}$$

$$P_{VM} = 96 \text{ mW} = 24 \text{ V} \times 4 \text{ mA} \tag{4}$$

P_{SW} can be calculated from the nominal motor supply voltage (V_{VM}), average output current (I_{AVG}), switching frequency (f_{PWM}) and the device output rise (t_{RISE}) and fall (t_{FALL}) time specifications.

$$P_{SW} = P_{SW\_RISE} + P_{SW\_FALL} \tag{5}$$

$$P_{SW\_RISE} = 0.5 \times V_M \times I_{AVG} \times t_{RISE} \times f_{PWM} \tag{6}$$

$$P_{SW\_FALL} = 0.5 \times V_M \times I_{AVG} \times t_{FALL} \times f_{PWM} \tag{7}$$

$$P_{SW\_RISE} = 26.4\ mW = 0.5 \times 24\ V \times 0.5\ A \times 220\ ns \times 20\ kHz \quad (8)$$

$$P_{SW\_FALL} = 26.4\ mW = 0.5 \times 24\ V \times 0.5\ A \times 220\ ns \times 20\ kHz \quad (9)$$

$$P_{SW} = 53\ mW = 26.4\ mW + 26.4\ mW \quad (10)$$

P_{RDS} can be calculated from the device $R_{DS(on)}$ and average output current (I_{AVG}).

$$P_{RDS} = I_{AVG}^{\ 2} \times (R_{DS(ON)\_HS} + R_{DS(ON)\_LS}) \quad (11)$$

$R_{DS(ON)}$ has a strong correlation with the device temperature. Assuming a device junction temperature of 85 °C, $R_{DS(on)}$ could increase ~1.5x based on the normalized temperature data. The calculation below shows this derating factor. Alternatively, 节 7.6 shows curves that plot how $R_{DS(on)}$ changes with temperature.

$$P_{RDS} = 169\ mW = (0.5\ A)^2 \times (225\ m\Omega \times 1.5 + 225\ m\Omega \times 1.5) \quad (12)$$

Based on the example calculations above, the expressions below calculate the total expected power dissipation for the device.

$$P_{TOT} = P_{VM} + P_{SW} + P_{RDS} \quad (13)$$

$$P_{TOT} = 318\ mW = 96\ mW + 53\ mW + 169\ mW \quad (14)$$

The driver's junction temperature can be estimated using P_{TOT}, device ambient temperature (T_A), and package thermal resistance ($R_{\theta JA}$). The value for $R_{\theta JA}$ depends heavily on the PCB design and copper heat sinking around the device. 节 9.3.2 describes this dependence in greater detail.

$$T_J = (P_{TOT} \times R_{\theta JA}) + T_A \quad (15)$$

$$T_J = 98\ °C = (0.318\ W \times 40.4\ °C/W) + 85°C \quad (16)$$

The device junction temperature should remain below its absolute maximum rating for all system operating conditions. The calculations in this section provide reasonable estimates for junction temperature. However, other methods based on temperature measurements taken during system operation are more realistic and reliable. Additional information on motor driver current ratings and power dissipation can be found in 节 9.3.2 and 节 12.1.1.

9.3.2 Thermal Performance

The datasheet-specified junction-to-ambient thermal resistance, $R_{\theta JA}$, is primarily useful for comparing various drivers or approximating thermal performance. However, the actual system performance may be better or worse than this value depending on PCB stackup, routing, number of vias, and copper area around the thermal pad. The length of time the driver drives a particular current will also impact power dissipation and thermal performance. This section considers how to design for steady-state and transient thermal conditions.

The data in this section was simulated using the following criteria.

表 9-5. Simulation PCB Stackup Summary for HSOP package

Layer	2-layer	4-layer
Top Layer	HSOP footprint with 1- or 2-oz copper thickness. See 表 9-6 for copper area varied in simulation. Thermally connected with vias (2 vias, 1.2-mm spacing, 0.3-mm diameter, 0.025-mm copper plating) from HSOP thermal pad to bottom layer and internal ground plane (4-layer only).	
Layer 2, internal ground plane	N/A	1-oz copper thickness, 74.2 mm x 74.2 mm copper area, thermally connected to HSOP thermal pad through vias.
Layer 3, internal supply plane	N/A	1-oz copper thickness, 74.2 mm x 74.2 mm copper area, not connected to other layers.

表 9-5. Simulation PCB Stackup Summary for HSOP package (continued)

Layer	2-layer	4-layer
Bottom Layer	Ground plane with 1- or 2-oz copper thickness. See 表 9-6 for copper area varied in simulation. Thermally connected to HSOP thermal pad through vias.	1- or 2-oz copper thickness. Copper area fixed at 4.90 mm × 6.00 mm in simulation. Thermally connected to HSOP thermal pad through vias.

图 9-18 shows an example of the simulated board for the HSOP package. 表 9-6 shows the dimensions of the board that were varied for each simulation.

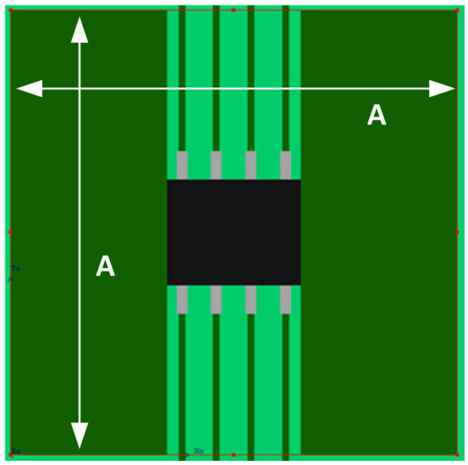


图 9-18. HSOP PCB model top layer

表 9-6. Dimension A for 8-pin HSOP (DDA) package

Cu area (cm^2)	Dimension A (mm)
0.069	Package thermal pad dimensions
2	16.40
4	22.32
8	30.64
16	42.38

9.3.2.1 Steady-State Thermal Performance

"Steady-state" conditions assume that the motor driver operates with a constant average current over a long period of time. The figures in this section show how $R_{\theta JA}$ and Ψ_{JB} (junction-to-board characterization parameter) change depending on copper area, copper thickness, and number of layers of the PCB. More copper area, more layers, and thicker copper planes decrease $R_{\theta JA}$ and Ψ_{JB}, which indicate better thermal performance from the PCB layout.

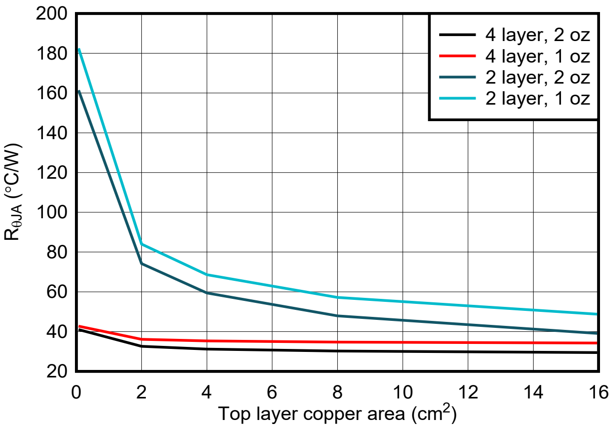


图 9-19. HSOP, PCB junction-to-ambient thermal resistance vs copper area

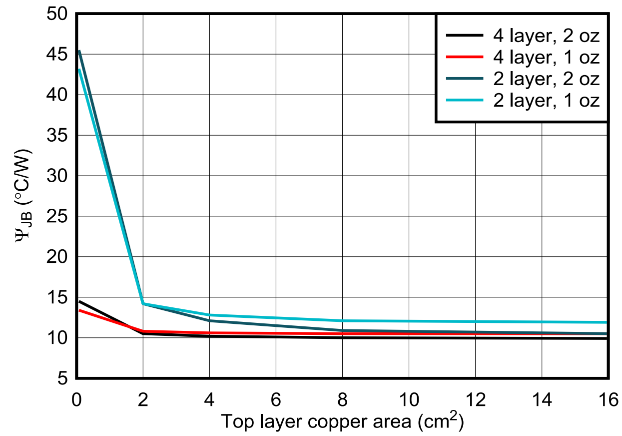


图 9-20. HSOP, junction-to-board characterization parameter vs copper area

9.3.2.2 Transient Thermal Performance

The motor driver may experience different transient driving conditions that cause large currents to flow for a short duration of time. These may include

- Motor start-up when the rotor is initially stationary.
- Fault conditions when there is a supply or ground short to one of the motor outputs, and the overcurrent protection triggers.
- Briefly energizing a motor or solenoid for a limited time, then de-energizing.

For these transient cases, the duration of drive time is another factor that impacts thermal performance in addition to copper area and thickness. In transient cases, the thermal impedance parameter $Z_{\theta JA}$ denotes the junction-to-ambient thermal performance. The figures in this section show the simulated thermal impedances for 1-oz and 2-oz copper layouts for the HSOP package. These graphs indicate better thermal performance with short current pulses. For short periods of drive time, the device die size and package dominates the thermal performance. For longer drive pulses, board layout has a more significant impact on thermal performance. Both graphs show the curves for thermal impedance split due to number of layers and copper area as the duration of the drive pulse duration increases. Long pulses can be considered steady-state performance.

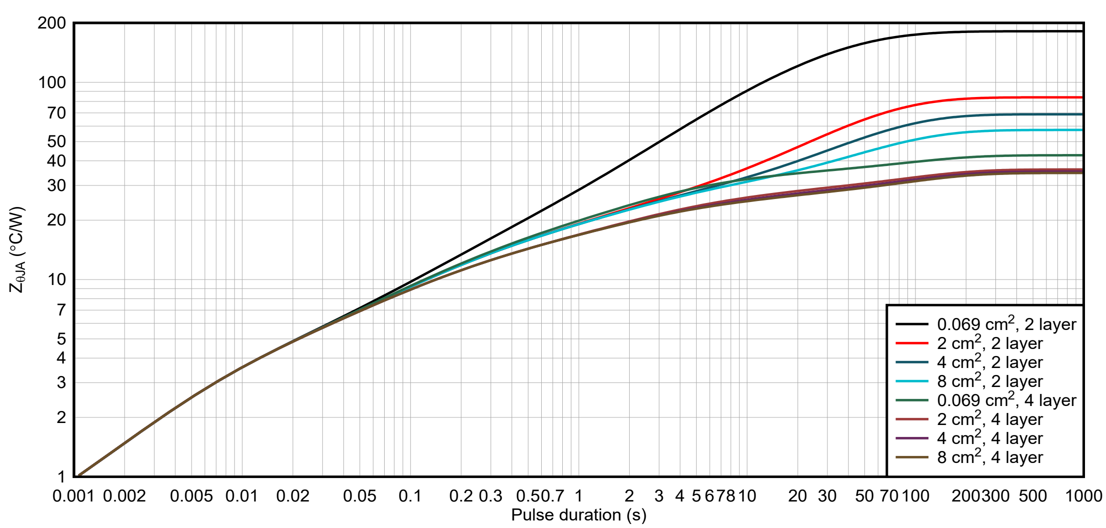


图 9-21. HSOP package junction-to-ambient thermal impedance for 1-oz copper layouts

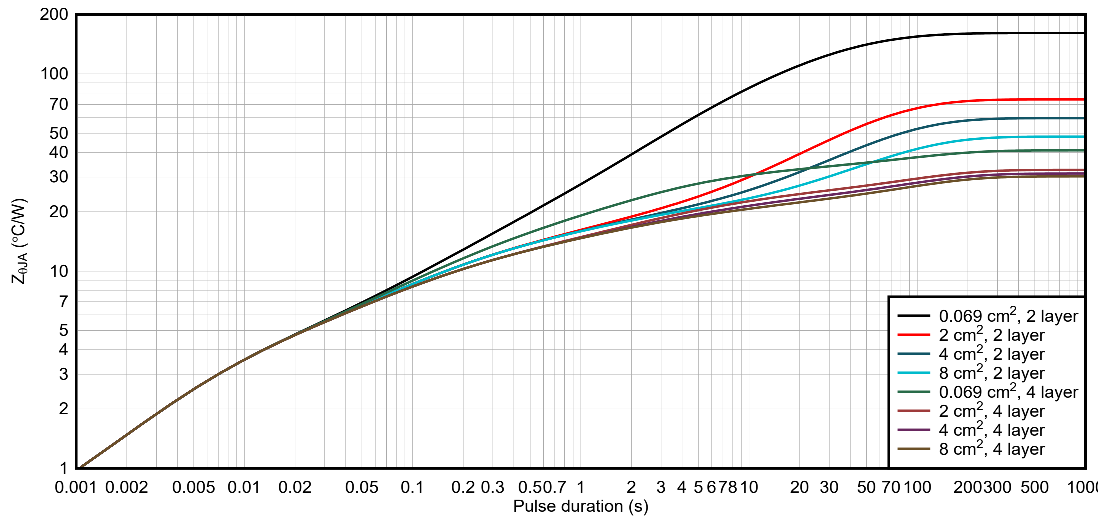


图 9-22. HSOP package junction-to-ambient thermal impedance for 2-oz copper layouts

10 Power Supply Recommendations

10.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. Having more bulk capacitance is generally beneficial, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The capacitance of the power supply and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and motor drive system limits how the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

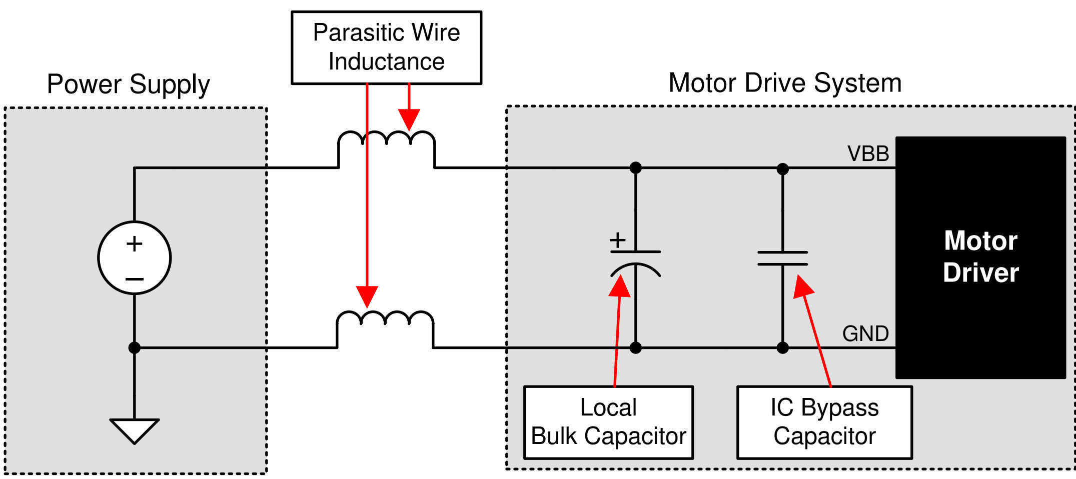


图 10-1. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

11 Layout

11.1 Layout Guidelines

Since the DRV8251 integrates power MOSFETs capable of driving high current, careful attention should be paid to the layout design and external component placement. Some design and layout guidelines are provided below.

- Low ESR ceramic capacitors should be utilized for the VM to GND bypass capacitor. X5R and X7R types are recommended.
- The VM power supply capacitors should be placed as close to the device as possible to minimize the loop inductance.
- The VM power supply bulk capacitor can be of ceramic or electrolytic type, but should also be placed as close as possible to the device to minimize the loop inductance.
- VM, OUT1, OUT2, and PGND carry the high current from the power supply to the outputs and back to ground. Thick metal routing should be utilized for these traces as is feasible.
- The device thermal pad should be attached to the PCB top layer ground plane and internal ground plane (when available) through thermal vias to maximize the PCB heat sinking.
- A recommended land pattern for the thermal vias is provided in the package drawing section.
- The copper plane area attached to the thermal pad should be maximized to ensure optimal heat sinking.

11.2 Layout Example

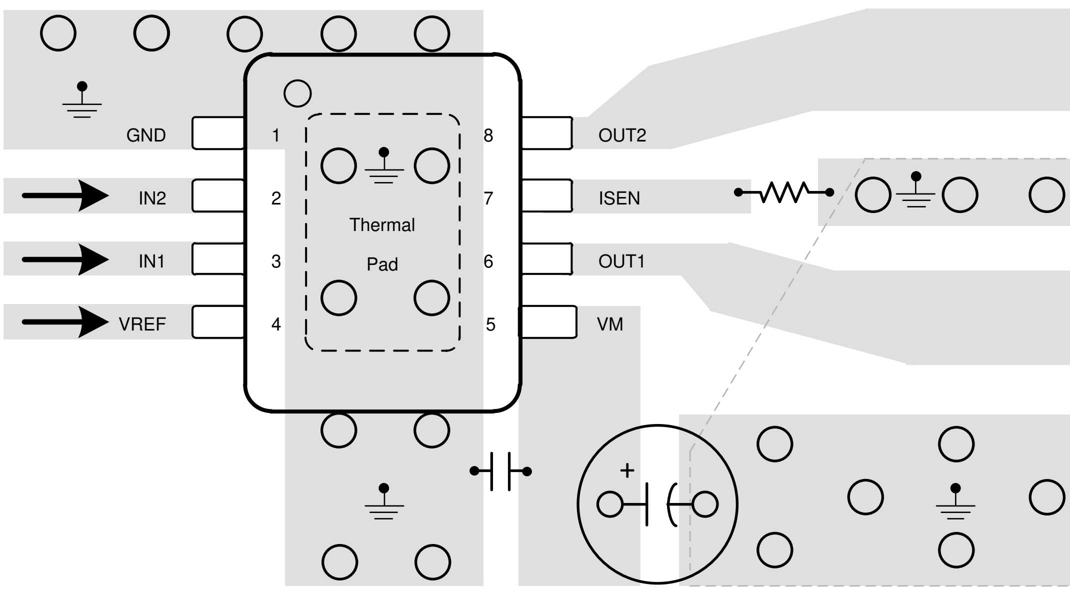


图 11-1. Layout Recommendation

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Calculating Motor Driver Power Dissipation* application report
- Texas Instruments, *Current Recirculation and Decay Modes* application report
- Texas Instruments, *PowerPAD™ Made Easy* application report
- Texas Instruments, *PowerPAD™ Thermally Enhanced Package* application report
- Texas Instruments, *Understanding Motor Driver Current Ratings* application report

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

12.4 Trademarks

PowerPAD™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8251DDAR	Active	Production	SO PowerPAD (DDA) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	DRV8251

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

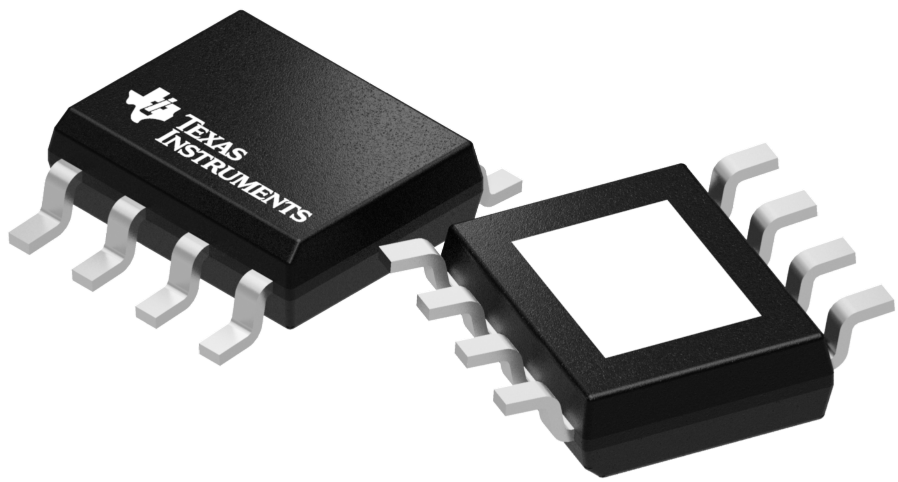
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

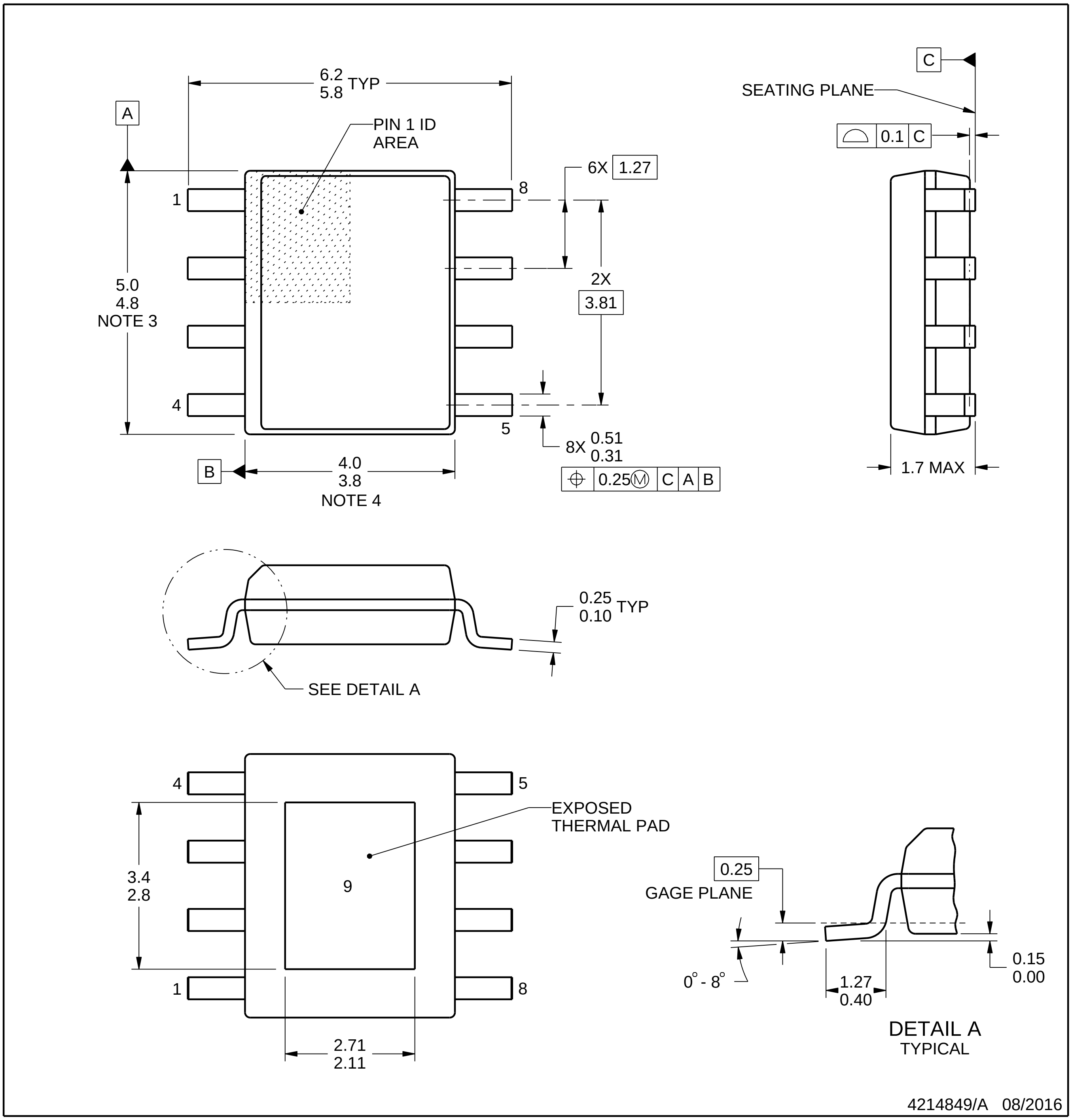
DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



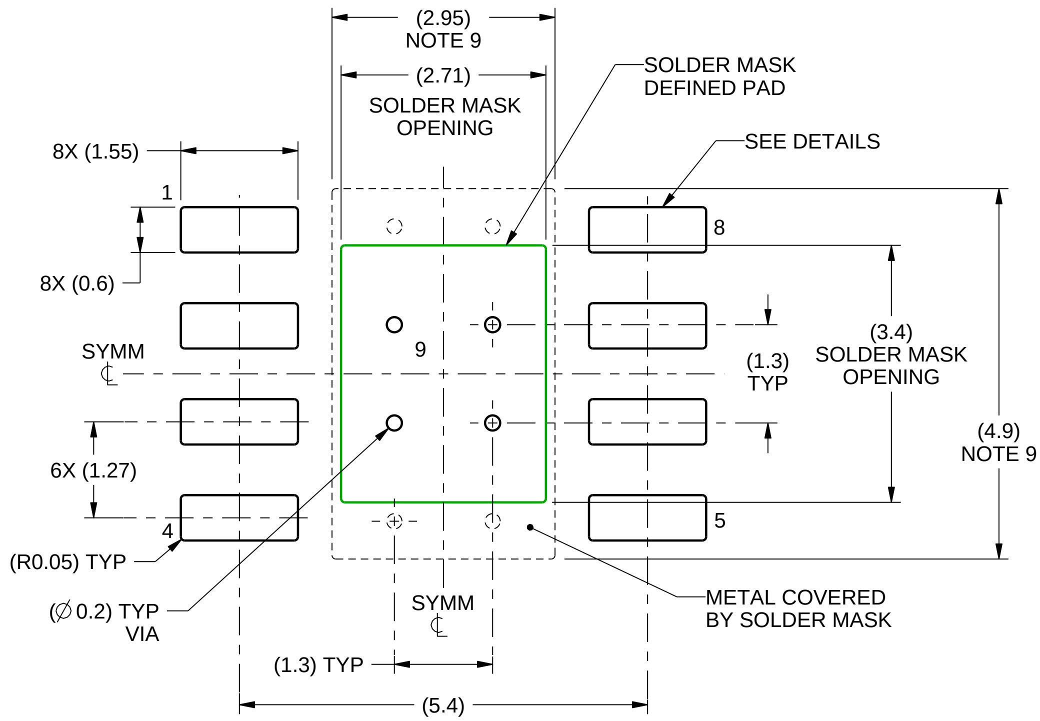
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4202561/G

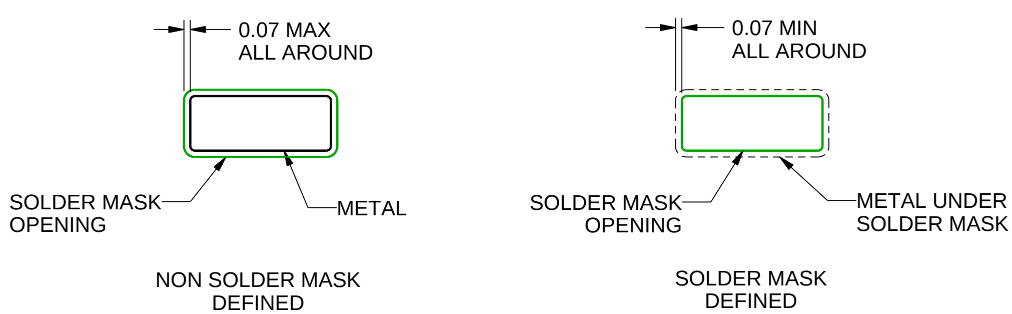


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
PADS 1-8

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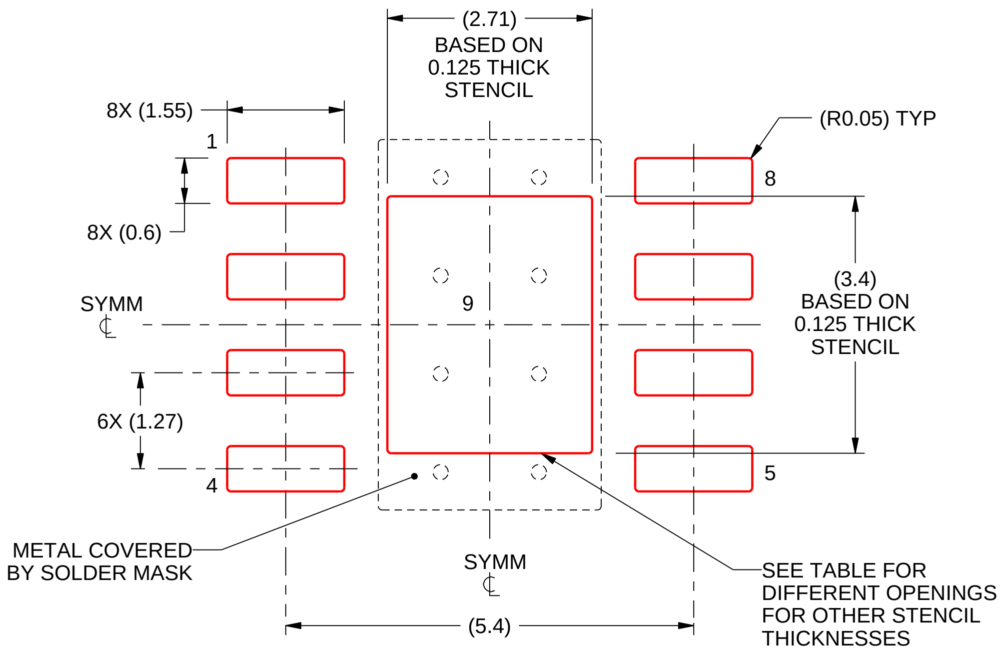
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

4214849/A 08/2016

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265