SBAS192B – MARCH 2001 – REVISED JUNE 2003

Low-Power, Rail-to-Rail Output, 16-Bit Serial Input DIGITAL-TO-ANALOG CONVERTER

FEATURES

- ***micro*Power OPERATION: 250μA at 5V**
- **POWER-ON RESET TO ZERO**
- **POWER SUPPLY: +2.7V to +5.5V**
- **ENSURED MONOTONIC BY DESIGN**
- **SETTLING TIME: 10μs to ±0.003 FSR**
- **LOW-POWER SERIAL INTERFACE WITH SCHMITT-TRIGGERED INPUTS**
- **ON-CHIP OUTPUT BUFFER AMPLIFIER, RAIL-TO-RAIL OPERATION**
- **$\overline{\text{SYNC}}$ INTERRUPT FACILITY**
- **PACKAGES: MSOP-8 and 3x3 SON-8 (same size as QFN)**

APPLICATIONS

- **PROCESS CONTROL**
- **DATA ACQUISITION SYSTEMS**
- **CLOSED-LOOP SERVO-CONTROL**
- **PC PERIPHERALS**
- **PORTABLE INSTRUMENTATION**
- **PROGRAMMABLE ATTENUATION**

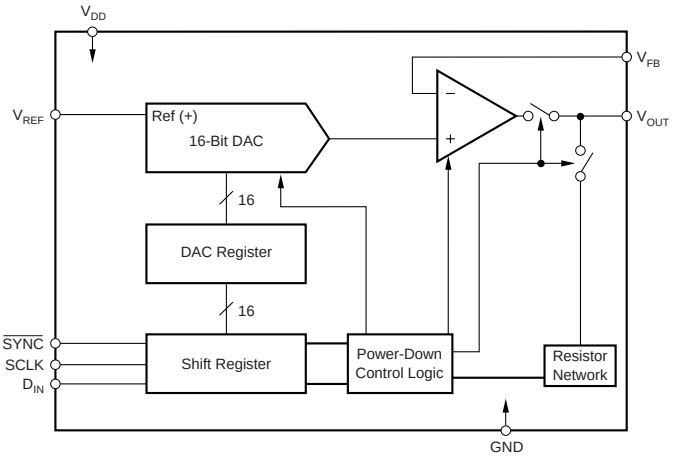
DESCRIPTION

The DAC8531 is a low-power, single, 16-bit buffered voltage output Digital-to-Analog Converter (DAC). Its on-chip precision output amplifier allows rail-to-rail output swing to be achieved. The DAC8531 uses a versatile three-wire serial interface that operates at clock rates up to 30MHz and is compatible with standard SPI™, QSPI™, Microwire™, and Digital Signal Processor (DSP) interfaces.

The DAC8531 requires an external reference voltage to set the output range of the DAC. The DAC8531 incorporates a power-on reset circuit that ensures that the DAC output powers up at 0V and remains there until a valid write takes place to the device. The DAC8531 contains a power-down feature, accessed over the serial interface, that reduces the current consumption of the device to 200nA at 5V.

The low power consumption of this part in normal operation makes it ideally suited to portable battery-operated equipment. The power consumption is 2mW at 5V reducing to 1μW in power-down mode.

The DAC8531 is available in both MSOP-8 and 3x3 SON-8 (same size as QFN) packages.



ABSOLUTE MAXIMUM RATINGS[1]

V_{DD} to GND	–0.3V to +6V
Digital Input Voltage to GND	–0.3V to $+V_{DD}$ + 0.3V
V_{OUT} to GND	–0.3V to $+V_{DD}$ + 0.3V
Operating Temperature Range	–40°C to +105°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature Range (T_J max)	+150°C
Power Dissipation	(T_J max — T_A)/θ_{JA}
θ_{JA} Thermal Impedance	206°C/W
θ_{JC} Thermal Impedance	44°C/W
Lead Temperature, Soldering:	
Vapor Phase (60s)	+215°C
Infrared (15s)	+220°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	MINIMUM RELATIVE ACCURACY (LSB)	DIFFERENTIAL NONLINEARITY (LSB)	PACKAGE-LEAD	PACKAGE DESIGNATOR[1]	SPECIFICATION TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DAC8531E	±64	±1	MSOP-8	DGK	–40°C to +105°C	D31	DAC8531E/250	Tape and Reel, 250
"	"	"	"	"	"	"	DAC8531E/2K5	Tape and Reel, 2500
DAC8531I	±64	±1	SON-8	DRB	–40°C to +105°C	D31	DAC8531IDRBT	Tape and Reel, 250
DAC8531I	"	"	"	"	"	"	DAC8531IDRBR	Tape and Reel, 2500

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

ELECTRICAL CHARACTERISTICS

V_{DD} = +2.7V to +5.5V. –40°C to +105°C, unless otherwise specified.

PARAMETER	CONDITIONS	DAC8531E MIN	DAC8531E TYP	DAC8531E MAX	UNITS
STATIC PERFORMANCE[1]					
Resolution		16			Bits
Relative Accuracy				±0.098	% of FSR
Differential Nonlinearity	Ensured Monotonic by Design			±1	LSB
Zero Code Error	All Zeroes Loaded to DAC Register		+5	+20	mV
Full-Scale Error	All Ones Loaded to DAC Register		–0.15	–1.25	% of FSR
Gain Error				±1.25	% of FSR
Zero Code Error Drift			±20		µV/°C
Gain Temperature Coefficient			±5		ppm of FSR/°C
OUTPUT CHARACTERISTICS[2]					
Output Voltage Range		0		V_{REF}	V
Output Voltage Settling Time	To ±0.003% FSR				
	0200_H to $FD00_H$		8	10	µs
	R_L = 2kΩ; 0pF < C_L < 200pF				
	R_L = 2kΩ; C_L = 500pF		12		µs
Slew Rate			1		V/µs
Capacitive Load Stability	R_L = ∞		470		pF
	R_L = 2kΩ		1000		pF
Code Change Glitch Impulse	1LSB Change Around Major Carry		20		nV-s
Digital Feedthrough			0.5		nV-s
DC Output Impedance			1		Ω
Short-Circuit Current	V_{DD} = +5V		50		mA
	V_{DD} = +3V		20		mA
Power-Up Time	Coming Out of Power-Down Mode				
	V_{DD} = +5V		2.5		µs
	Coming Out of Power-Down Mode				
	V_{DD} = +3V		5		µs
REFERENCE INPUT					
Reference Current	V_{REF} = V_{DD} = +5V		35	45	µA
	V_{REF} = V_{DD} = +3.6V		20	30	µA
Reference Input Range		0		V_{DD}	V
Reference Input Impedance			150		kΩ

NOTES: (1) Linearity calculated using a reduced code range of 485 to 64714; output unloaded. (2) Ensured by design and characterization, not production tested.

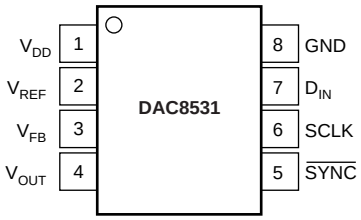
ELECTRICAL CHARACTERISTICS (Cont.)

V_{DD} = +2.7V to +5.5V. –40°C to +105°C, unless otherwise specified.

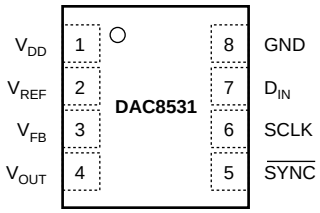
PARAMETER	CONDITIONS	DAC8531E MIN	DAC8531E TYP	DAC8531E MAX	UNITS
LOGIC INPUTS (2)					
Input Current				±1	µA
$V_{IN}L$, Input LOW Voltage	V_{DD} = +5V			0.8	V
$V_{IN}L$, Input LOW Voltage	V_{DD} = +3V			0.6	V
$V_{IN}H$, Input HIGH Voltage	V_{DD} = +5V	2.4			V
$V_{IN}H$, Input HIGH Voltage	V_{DD} = +3V	2.1			V
Pin Capacitance				3	pF
POWER REQUIREMENTS					
V_{DD}		2.7		5.5	V
I_{DD} (normal mode)	DAC Active and Excluding Load Current				
V_{DD} = +3.6V to +5.5V	$V_{IH} = V_{DD}$ and V_{IL} = GND		250	400	µA
V_{DD} = +2.7V to +3.6V	$V_{IH} = V_{DD}$ and V_{IL} = GND		240	390	µA
I_{DD} (all power-down modes)					
V_{DD} = +3.6V to +5.5V	$V_{IH} = V_{DD}$ and V_{IL} = GND		0.2	1	µA
V_{DD} = +2.7V to +3.6V	$V_{IH} = V_{DD}$ and V_{IL} = GND		0.05	1	µA
POWER EFFICIENCY					
I_{OUT}/I_{DD}	I_{LOAD} = 2mA, V_{DD} = +5V		89		%
TEMPERATURE RANGE					
Specified Performance		–40		+105	°C

PIN CONFIGURATIONS

Top View



MSOP-8



SON-8

PIN DESCRIPTION

PIN	NAME	DESCRIPTION
1	V_{DD}	Power-Supply Input, +2.7V to +5.5V.
2	V_{REF}	Reference Voltage Input
3	V_{FB}	Feedback connection for the output amplifier.
4	V_{OUT}	Analog output voltage from DAC. The output amplifier has rail-to-rail operation.
5	$\overline{SYNC}$	Level-triggered control input (active LOW). This is the frame sychronization signal for the input data. When $\overline{SYNC}$ goes LOW, it enables the input shift register and data is transferred in on the falling edges of the following clocks. The DAC is updated following the 24th clock cycle unless $\overline{SYNC}$ is taken HIGH before this edge, in which case the rising edge of $\overline{SYNC}$ acts as an interrupt and the write sequence is ignored by the DAC8531.
6	SCLK	Serial Clock Input. Data can be transferred at rates up to 30MHz.
7	D_{IN}	Serial Data Input. Data is clocked into the 24-bit input shift register on the falling edge of the serial clock input.
8	GND	Ground reference point for all circuitry on the part.

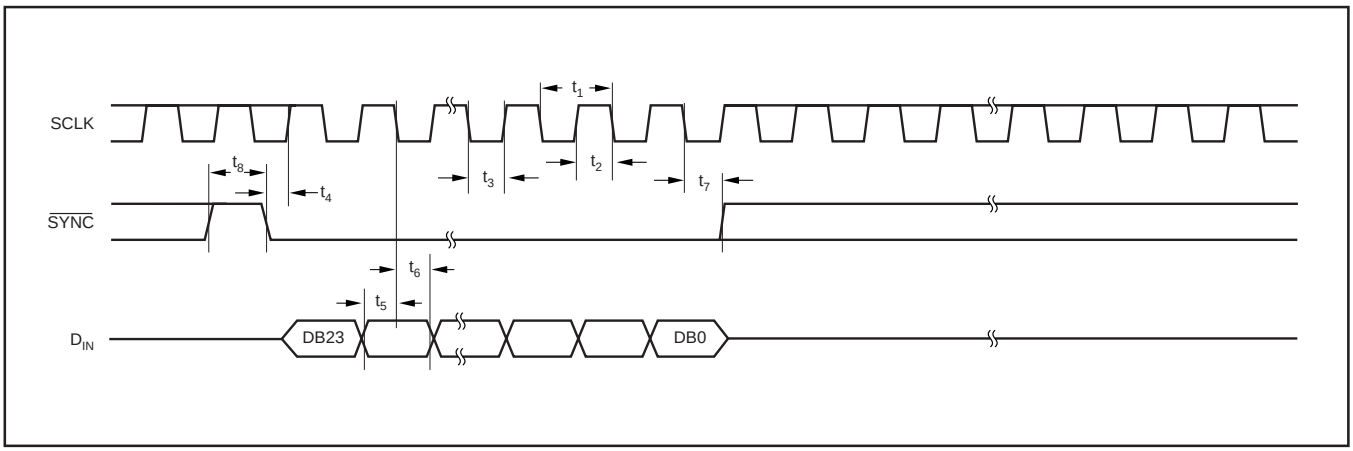
TIMING CHARACTERISTICS(1, 2)

V_{DD} = +2.7V to +5.5V; all specifications –40°C to +105°C unless otherwise noted.

PARAMETER	DESCRIPTION	CONDITIONS	DAC8531E			UNITS
			MIN	TYP	MAX	
t_1(3)	SCLK Cycle Time					
		V_{DD} = 2.7V to 3.6V	50			ns
		V_{DD} = 3.6V to 5.5V	33			ns
t_2	SCLK HIGH Time					
		V_{DD} = 2.7V to 3.6V	13			ns
		V_{DD} = 3.6V to 5.5V	13			ns
t_3	SCLK LOW Time					
		V_{DD} = 2.7V to 3.6V	22.5			ns
		V_{DD} = 3.6V to 5.5V	13			ns
t_4	$\overline{SYNC}$ to SCLK Rising Edge Setup Time					
		V_{DD} = 2.7V to 3.6V	0			ns
		V_{DD} = 3.6V to 5.5V	0			ns
t_5	Data Setup Time					
		V_{DD} = 2.7V to 3.6V	5			ns
		V_{DD} = 3.6V to 5.5V	5			ns
t_6	Data Hold Time					
		V_{DD} = 2.7V to 3.6V	4.5			ns
		V_{DD} = 3.6V to 5.5V	4.5			ns
t_7	SCLK Falling Edge to $\overline{SYNC}$ Rising Edge					
		V_{DD} = 2.7V to 3.6V	0			ns
		V_{DD} = 3.6V to 5.5V	0			ns
t_8	Minimum $\overline{SYNC}$ HIGH Time					
		V_{DD} = 2.7V to 3.6V	50			ns
		V_{DD} = 3.6V to 5.5V	33			ns

NOTES: (1) All input signals are specified with $t_R = t_F$ = 5ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. (2) See Serial Write Operation timing diagram, below. (3) Maximum SCLK frequency is 30MHz at V_{DD} = +3.6V to +5.5V and 20MHz at V_{DD} = +2.7V to +3.6V.

SERIAL WRITE OPERATION

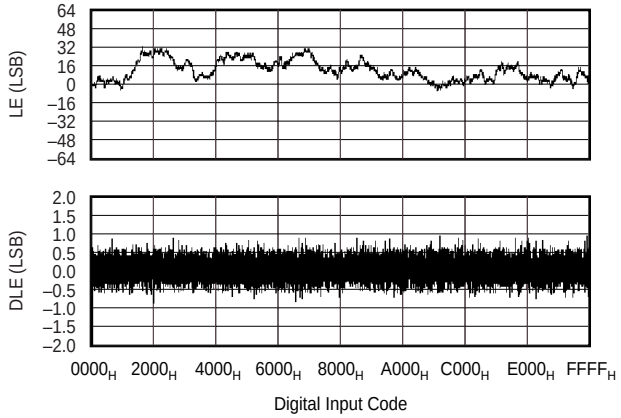


TYPICAL CHARACTERISTICS: V_{DD} = 5V

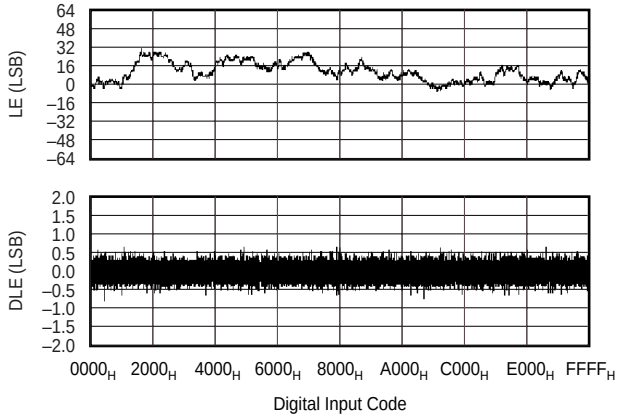
At T_A = +25°C, V_{DD} = 5V, unless otherwise noted.

NOTE: All references to I_{DD} include I_{REF} current.

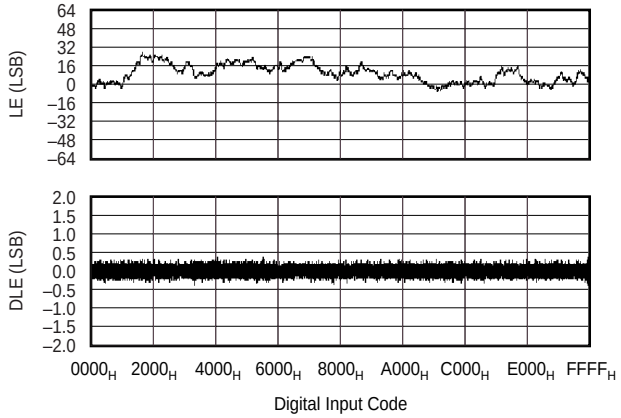
LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE **(–40°C)**



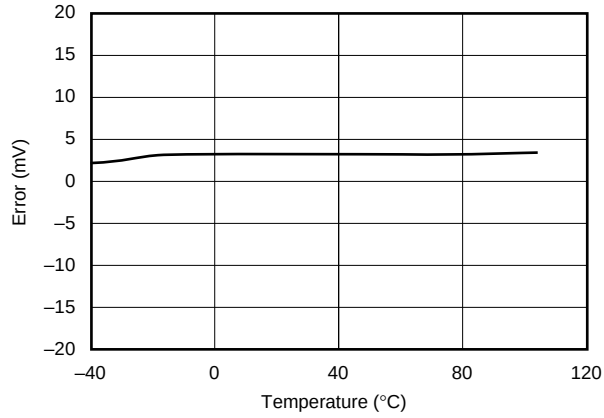
LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE **(+25°C)**



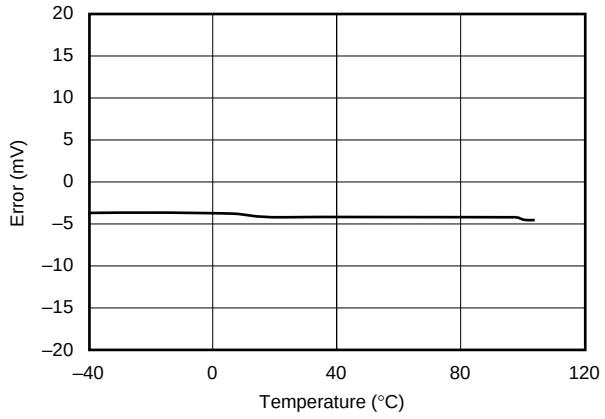
LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE **(+105°C)**



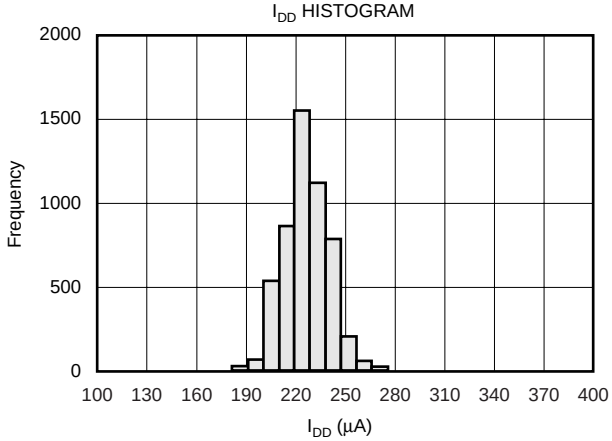
ZERO-SCALE ERROR vs TEMPERATURE



FULL-SCALE ERROR vs TEMPERATURE



I_{DD} HISTOGRAM

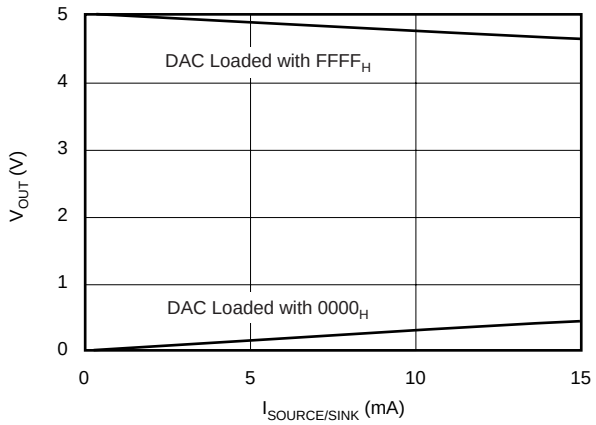


TYPICAL CHARACTERISTICS: V_{DD} = 5V (Cont.)

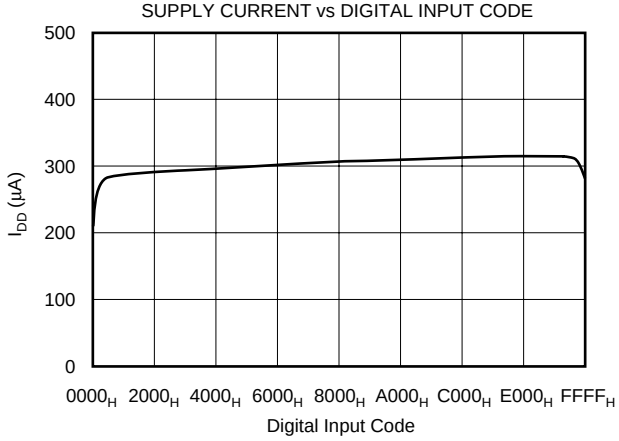
At T_A = +25°C, V_{DD} = 5V, unless otherwise noted.

NOTE: All references to I_{DD} include I_{REF} current.

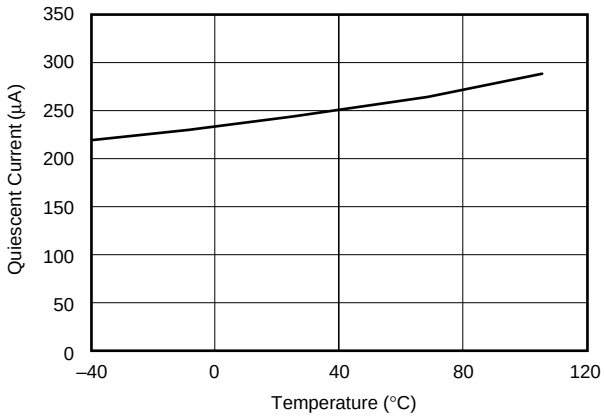
SOURCE AND SINK CURRENT CAPABILITY



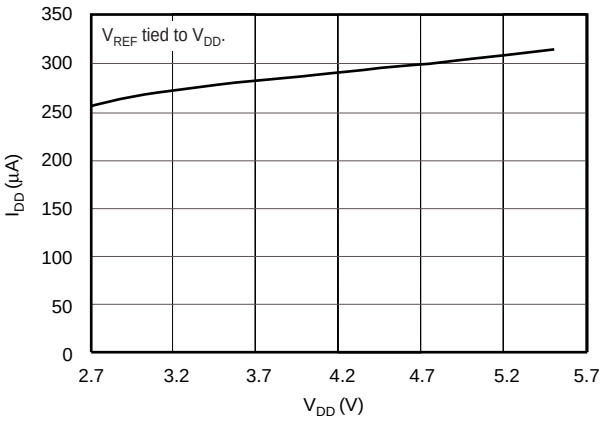
SUPPLY CURRENT vs DIGITAL INPUT CODE



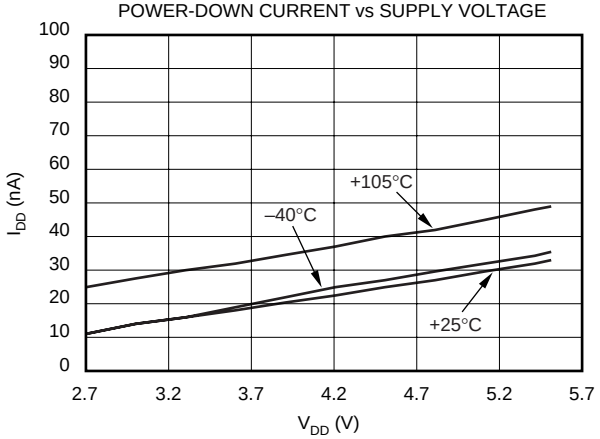
POWER-SUPPLY CURRENT vs TEMPERATURE



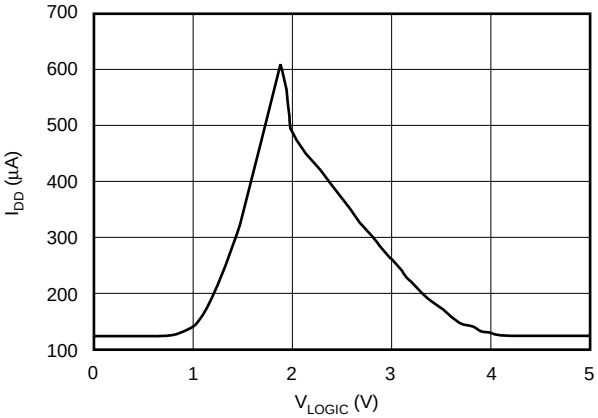
SUPPLY CURRENT vs SUPPLY VOLTAGE



POWER-DOWN CURRENT vs SUPPLY VOLTAGE



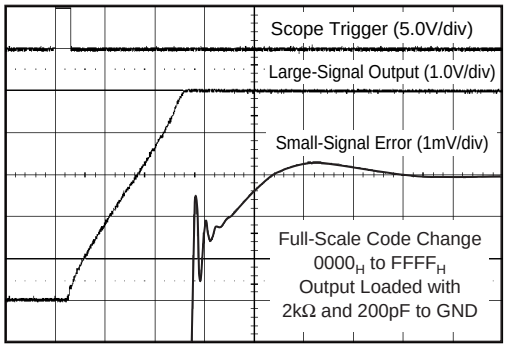
SUPPLY CURRENT vs LOGIC INPUT VOLTAGE



TYPICAL CHARACTERISTICS: V_{DD} = 5V (Cont.)

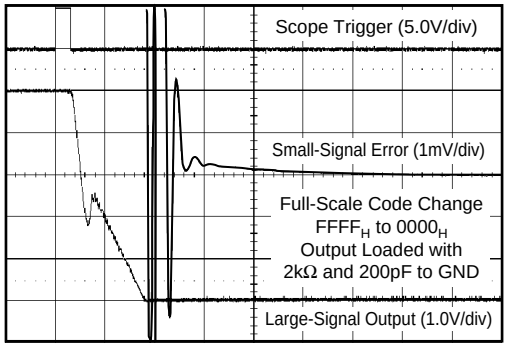
At T_A = +25°C, V_{DD} = 5V, unless otherwise noted.

FULL-SCALE SETTLING TIME



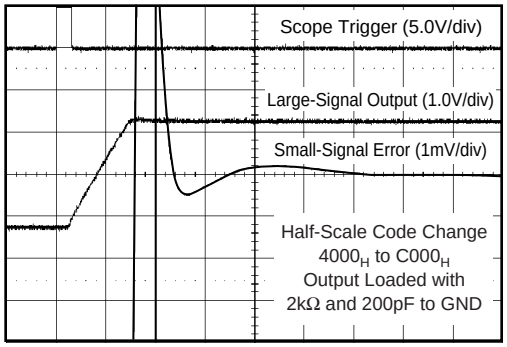
Time (2µs/div)

FULL-SCALE SETTLING TIME



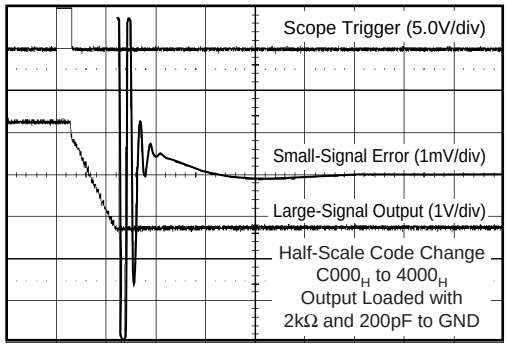
Time (2µs/div)

HALF-SCALE SETTLING TIME



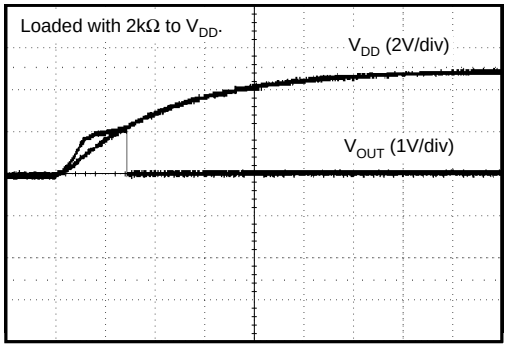
Time (2µs/div)

HALF-SCALE SETTLING TIME



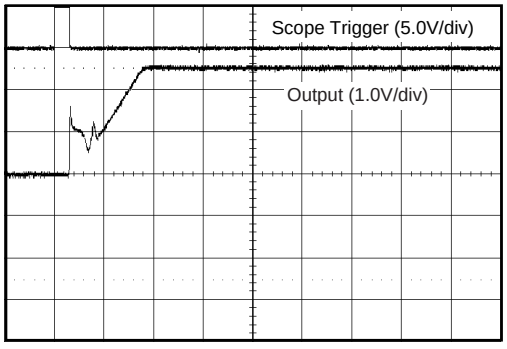
Time (2µs/div)

POWER-ON RESET TO 0V



Time (50µs/div)

EXITING POWER-DOWN
(8000_H Loaded)

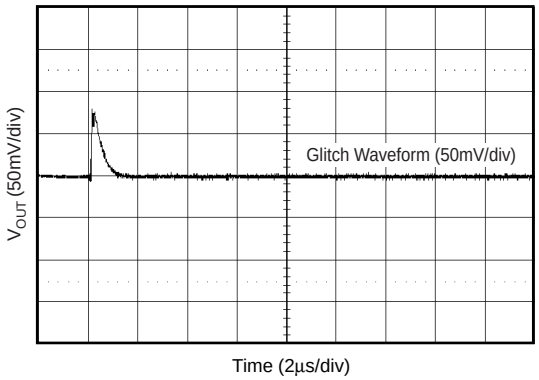


Time (2µs/div)

TYPICAL CHARACTERISTICS: V_{DD} = 5V (Cont.)

At T_A = +25°C, V_{DD} = 5V, unless otherwise noted.

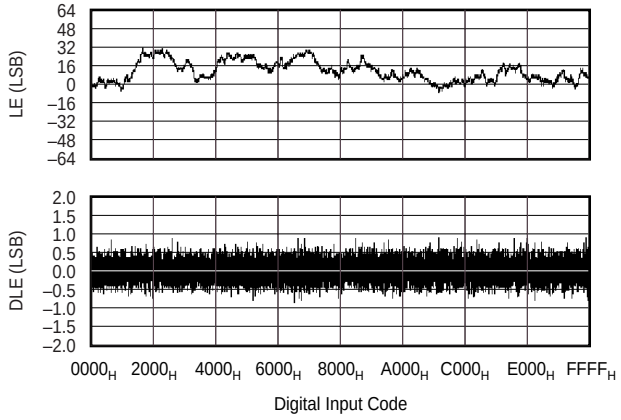
CODE CHANGE GLITCH



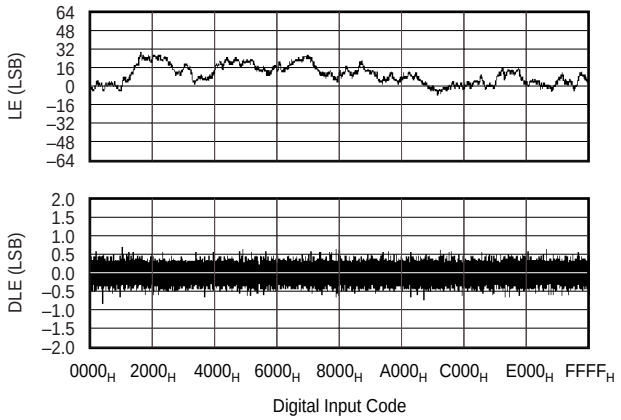
TYPICAL CHARACTERISTICS: V_{DD} = 2.7V

At T_A = +25°C, V_{DD} = 2.7V, unless otherwise noted.

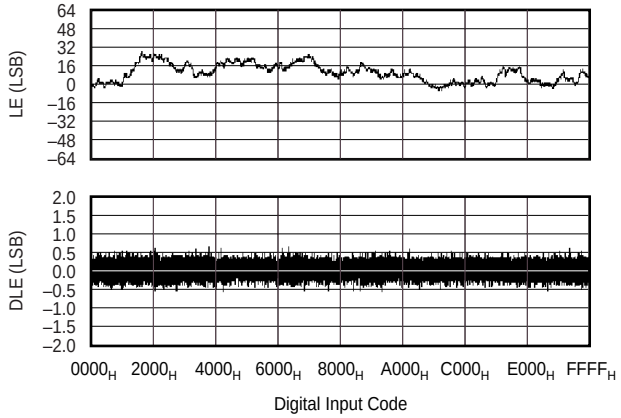
LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE **(–40°C)**



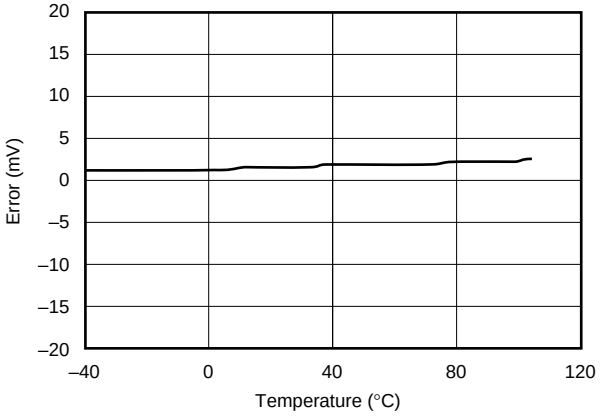
LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE **(+25°C)**



LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE **(+105°C)**



ZERO-SCALE ERROR vs TEMPERATURE

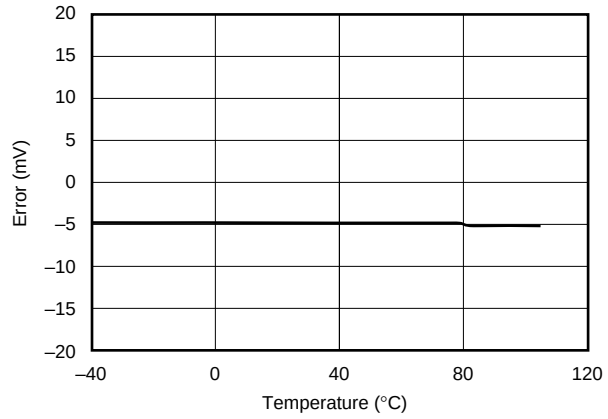


TYPICAL CHARACTERISTICS: V_{DD} = 2.7V

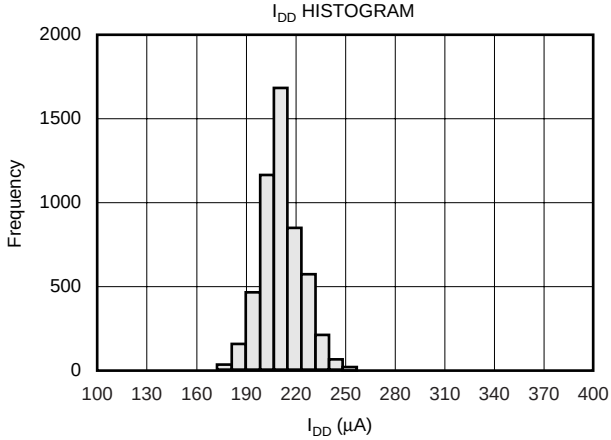
At T_A = +25°C, V_{DD} = 2.7V, unless otherwise noted.

NOTE: All references to I_{DD} include I_{REF} current.

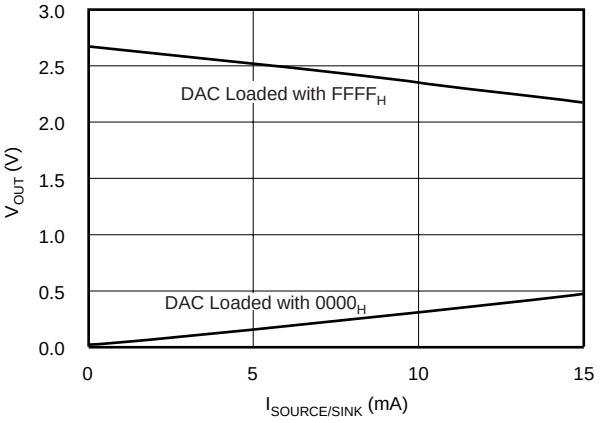
FULL-SCALE ERROR vs TEMPERATURE



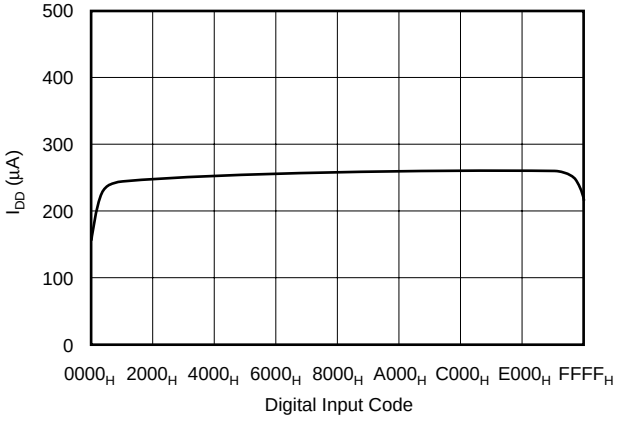
I_{DD} HISTOGRAM



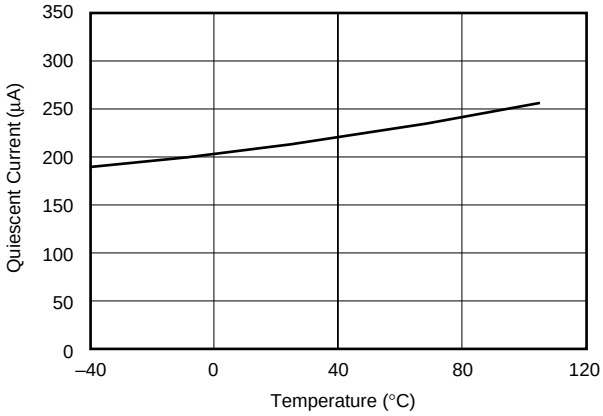
SOURCE AND SINK CURRENT CAPABILITY



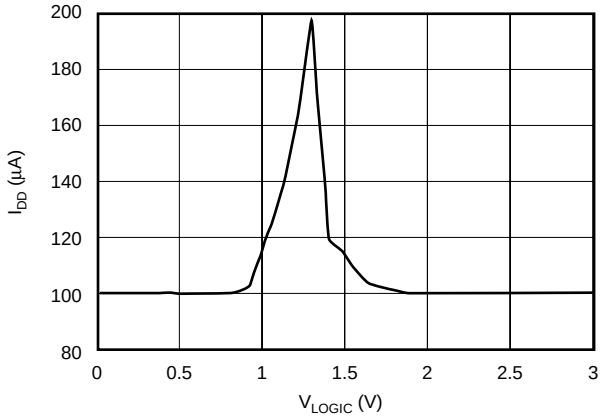
SUPPLY CURRENT vs DIGITAL INPUT CODE



POWER SUPPLY CURRENT vs TEMPERATURE



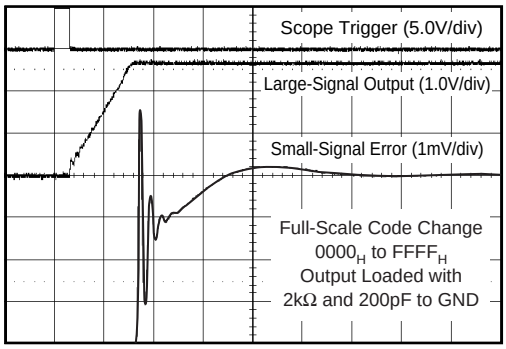
SUPPLY CURRENT vs LOGIC INPUT VOLTAGE



TYPICAL CHARACTERISTICS: V_{DD} = 2.7V (Cont.)

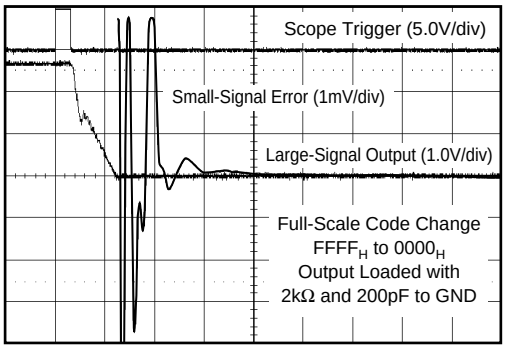
At T_A = +25°C, V_{DD} = 2.7V, unless otherwise noted.

FULL-SCALE SETTLING TIME



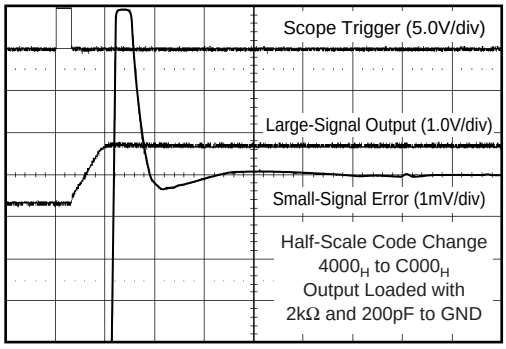
Time (2µs/div)

FULL-SCALE SETTLING TIME



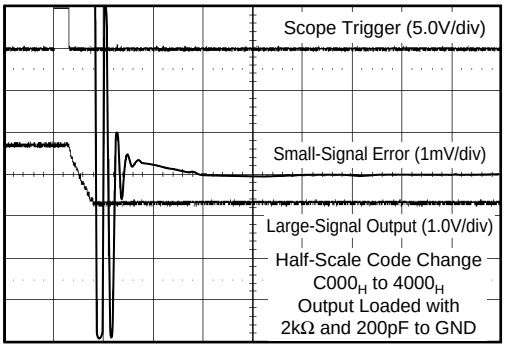
Time (2µs/div)

HALF-SCALE SETTLING TIME



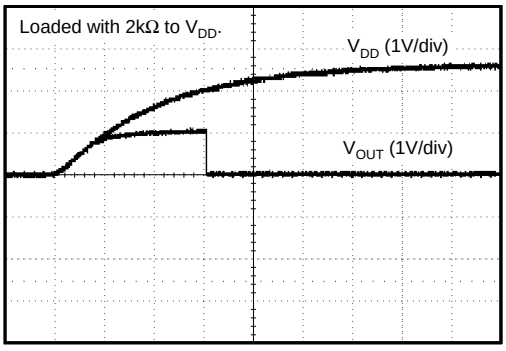
Time (2µs/div)

HALF-SCALE SETTLING TIME



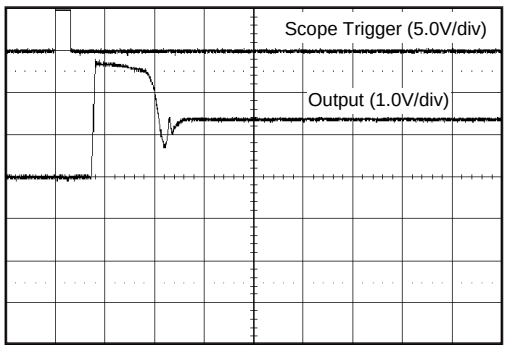
Time (2µs/div)

POWER-ON RESET to 0V



Time (50µs/div)

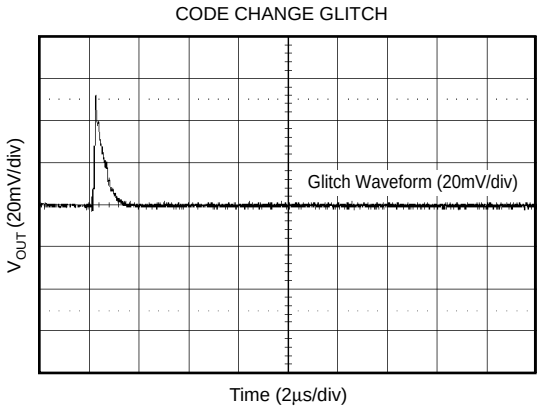
EXITING POWER-DOWN
(8000_H Loaded)



Time (2µs/div)

TYPICAL CHARACTERISTICS: V_{DD} = 2.7V (Cont.)

At T_A = +25°C, V_{DD} = 2.7V, unless otherwise noted.



THEORY OF OPERATION

DAC SECTION

The architecture consists of a string DAC followed by an output buffer amplifier. Figure 1 shows a block diagram of the DAC architecture.

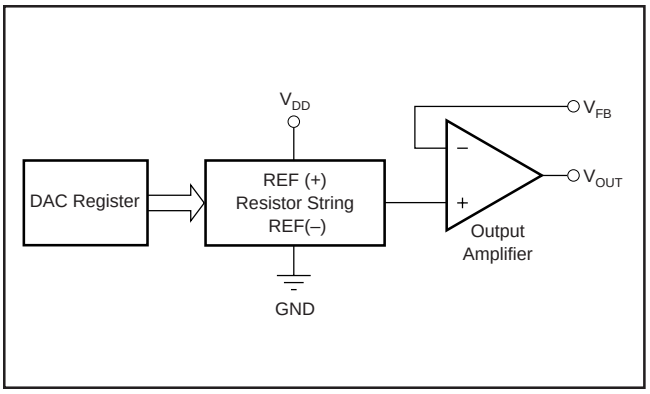


FIGURE 1. DAC8531 Architecture.

The input coding to the DAC8531 is straight binary, so the ideal output voltage is given by:

$$V_{OUT} = V_{REF} \bullet \frac{D}{65536}$$

where D = decimal equivalent of the binary code that is loaded to the DAC register; it can range from 0 to 65535.

RESISTOR STRING

Figure 2 shows the resistor string section. It is simply a string of resistors, each of value R. The code loaded into the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier by closing one of the switches connecting the string to the amplifier. It is ensured monotonic because it is a string of resistors.

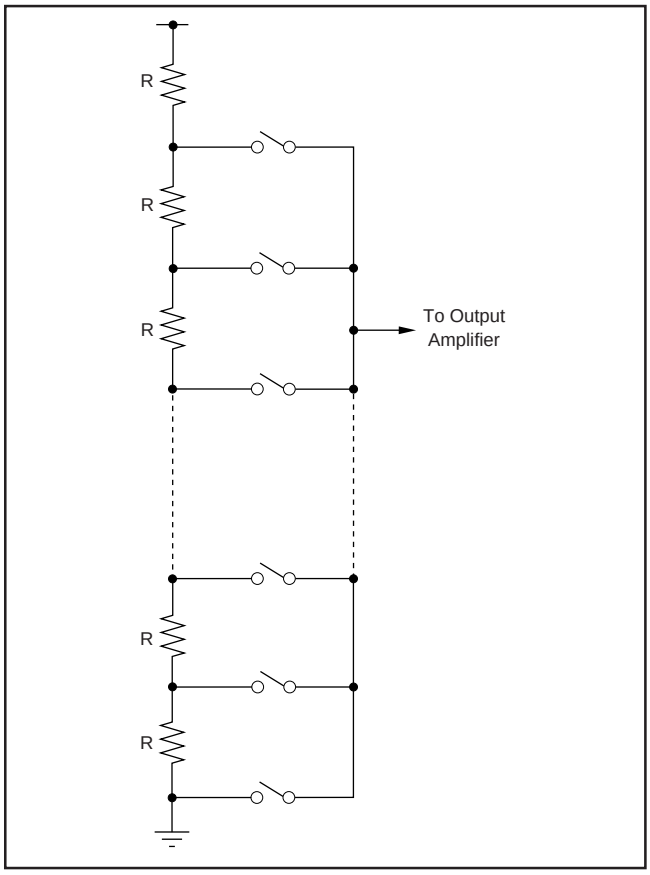


FIGURE 2. Resistor String.

OUTPUT AMPLIFIER

The output buffer amplifier is capable of generating rail-to-rail voltages on its output which gives an output range of 0V to V_{DD}. It is capable of driving a load of 2kΩ in parallel with 1000pF to GND. The source and sink capabilities of the output amplifier can be seen in the typical curves. The slew rate is 1V/µs with a full-scale settling time of 8µs with the output unloaded.

The inverting input of the output amplifier is brought out to the V_{FB} pin. This allows for better accuracy in critical applications by tying the V_{FB} point and the amplifier output together directly at the load. Other signal conditioning circuitry may also be connected between these points for specific applications.

SERIAL INTERFACE

The DAC8531 has a three-wire serial interface ($\overline{SYNC}$, SCLK, and D_{IN}), which is compatible with SPI, QSPI, and Microwire interface standards as well as most DSPs. See the Serial Write Operation timing diagram for an example of a typical write sequence.

The write sequence begins by bringing the $\overline{SYNC}$ line LOW. Data from the D_{IN} line is clocked into the 24-bit shift register on the falling edge of SCLK. The serial clock frequency can be as high as 30MHz, making the DAC8531 compatible with high-speed (DSPs). On the 24th falling edge of the serial clock, the last data bit is clocked in and the programmed function is executed (i.e., a change in DAC register contents and/or a change in the mode of operation).

At this point, the $\overline{SYNC}$ line may be kept LOW or brought HIGH. In either case, it must be brought HIGH for a minimum of 33ns before the next write sequence so that a falling edge of $\overline{SYNC}$ can initiate the next write sequence. Since the $\overline{SYNC}$ buffer draws more current when the $\overline{SYNC}$ signal is HIGH than it does when it is LOW, $\overline{SYNC}$ should be idled LOW between write sequences for lowest power operation of the part. As mentioned above, it must be brought HIGH again just before the next write sequence.

INPUT SHIFT REGISTER

The input shift register is 24 bits wide, as shown in Figure 3. The first six bits are “don’t cares”. The next two bits (PD1 and PD0) are control bits that control which mode of operation the part is in (normal mode or any one of three power-down modes). There is a more complete description of the various modes in the Power-Down Modes section. The next 16 bits are the data bits. These are transferred to the DAC register on the 24th falling edge of SCLK.

$\overline{SYNC}$ INTERRUPT

In a normal write sequence, the $\overline{SYNC}$ line is kept LOW for at least 24 falling edges of SCLK and the DAC is updated on the 24th falling edge. However, if $\overline{SYNC}$ is brought HIGH before the 24th falling edge, this acts as an interrupt to the write sequence. The shift register is reset and the write sequence is seen as invalid. Neither an update of the DAC register contents or a change in the operating mode occurs, as shown in Figure 4.

POWER-ON RESET

The DAC8531 contains a power-on reset circuit that controls the output voltage during power-up. On power-up, the DAC register is filled with zeros and the output voltage is 0V; it remains there until a valid write sequence is made to the DAC. This is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up.

DB23																							DB0
X	X	X	X	X	X	PD1	PD0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

FIGURE 3. Data Input Register.

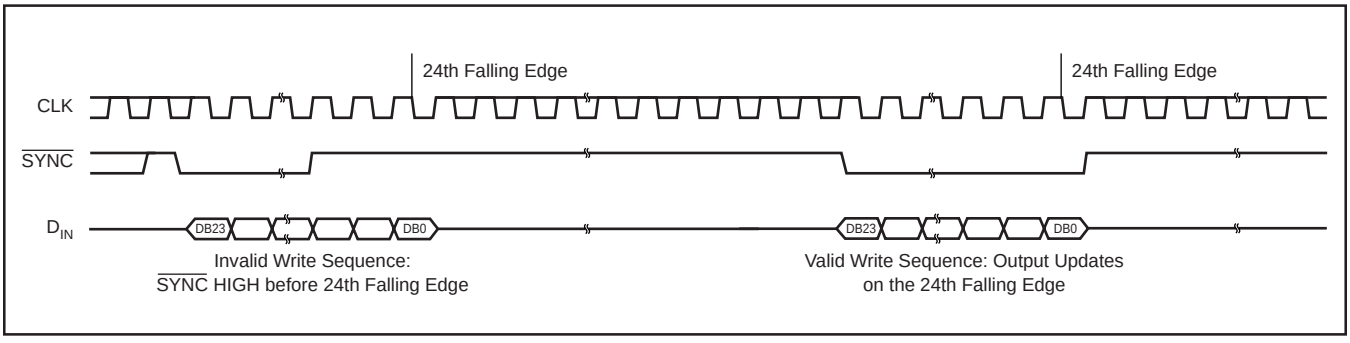


FIGURE 4. $\overline{SYNC}$ Interrupt Facility.

POWER-DOWN MODES

The DAC8531 supports four separate modes of operation. These modes are programmable by setting two bits (PD1 and PD0) in the control register. Table I shows how the state of the bits corresponds to the mode of operation of the device.

PD1 (DB17)	PD0 (DB16)	OPERATING MODE
0	0	Normal Operation
—	—	Power-Down Modes
0	1	Output 1kΩ to GND
1	0	Output 100kΩ to GND
1	1	High-Z

TABLE I. Modes of Operation for the DAC8531.

When both bits are set to 0, the part works normally with its typical current consumption of 250μA at 5V. However, for the three power-down modes, the supply current falls to 200nA at 5V (50nA at 3V). Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the part is known while the part is in power-down mode. There are three different options. The output is connected internally to GND through a 1kΩ resistor, a 100kΩ resistor, or it is left open-circuited (High-Z). The output stage is illustrated in Figure 5.

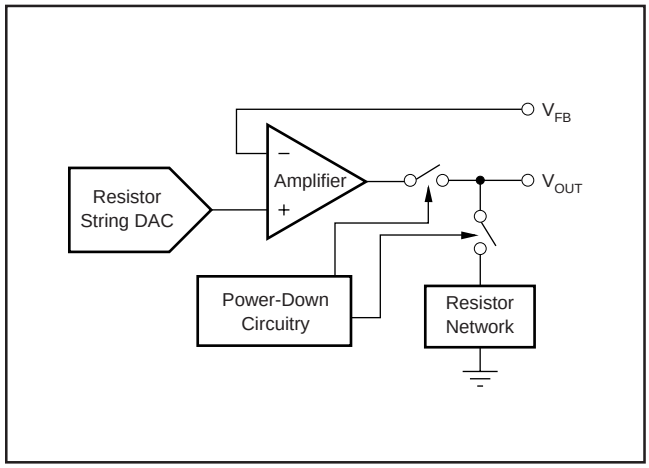


FIGURE 5. Output Stage During Power-Down.

All linear circuitry is shut down when the power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 2.5μs for V_{DD} = 5V, and 5μs for V_{DD} = 3V. See the Typical Characteristics for more information.

MICROPROCESSOR INTERFACING

DAC8531 TO 8051 INTERFACE

Figure 6 shows a serial interface between the DAC8531 and a typical 8051-type microcontroller. The setup for the interface is as follows: TXD of the 8051 drives SCLK of the DAC8531, while RXD drives the serial data line of the part. The $\overline{SYNC}$ signal is derived from a bit-programmable pin on the port. In this case, port line P3.3 is used. When data is to be transmitted to the DAC8531, P3.3 is taken LOW. The 8051 transmits data only in 8-bit bytes; thus only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left LOW after the first eight bits are transmitted and a second write cycle is initiated to transmit the second byte of data. P3.3 is taken HIGH following the completion of the third write cycle. The 8051 outputs the serial data in a format which has the LSB first. The DAC8531 requires its data with the MSB as the first bit received. The 8051 transmit routine must therefore take this into account, and “mirror” the data as needed.

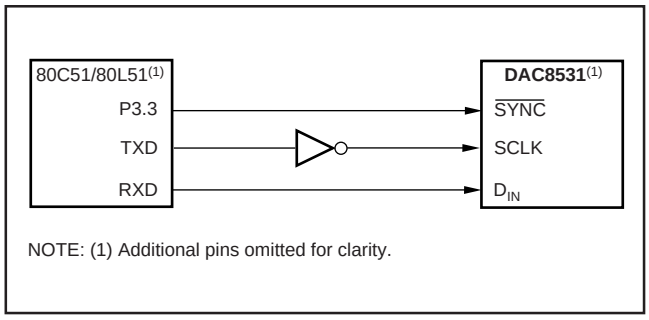


FIGURE 6. DAC8531 to 80C51/80L51 Interface.

DAC8531 TO Microwire INTERFACE

Figure 7 shows an interface between the DAC8531 and any Microwire compatible device. Serial data is shifted out on the falling edge of the serial clock and is clocked into the DAC8531 on the rising edge of the SK signal.

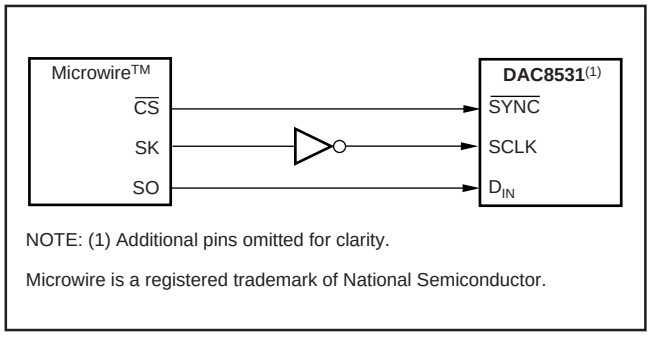


FIGURE 7. DAC8531 to Microwire Interface.

DAC8531 TO 68HC11 INTERFACE

Figure 8 shows a serial interface between the DAC8531 and the 68HC11 microcontroller. SCK of the 68HC11 drives the SCLK of the DAC8531, while the MOSI output drives the serial data line of the DAC. The $\overline{SYNC}$ signal is derived from a port line (PC7), similar to what was done for the 8051.

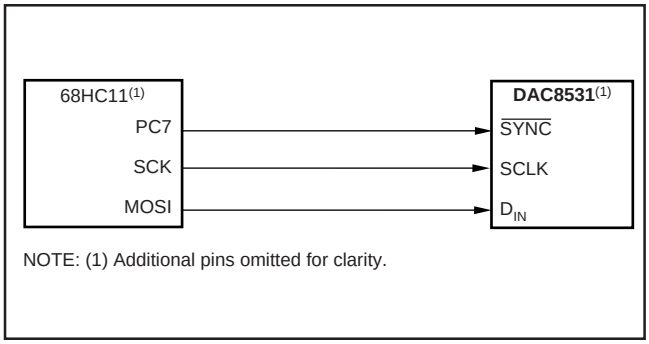


FIGURE 8. DAC8531 to 68HC11 Interface.

The 68HC11 should be configured so that its CPOL bit is a 0 and its CPHA bit is a 1. This configuration causes data appearing on the MOSI output to be valid on the falling edge of SCK. When data is being transmitted to the DAC, the $\overline{SYNC}$ line is taken LOW (PC7). Serial data from the 68HC11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. In order to load data to the DAC8531, PC7 is left LOW after the first eight bits are transferred, then a second and third serial write operation is performed to the DAC and PC7 is taken HIGH at the end of this procedure.

APPLICATIONS

USING REF02 AS A POWER SUPPLY FOR THE DAC8531

Due to the extremely low supply current required by the DAC8531, an alternative option is to use a REF02 +5V precision voltage reference to supply the required voltage to the part, as shown in Figure 9. This is especially useful if the power supply is quite noisy or if the system supply voltages are at some value other than 5V. The REF02 will output a steady supply voltage for the DAC8531. If the REF02 is used, the typical current it needs to supply to the DAC8531 is 250µA. This is with no load on the output of the DAC. When the DAC output is loaded, the REF02 also needs to supply the current to the load. The total current required (with a 5kΩ load on the DAC output) is:

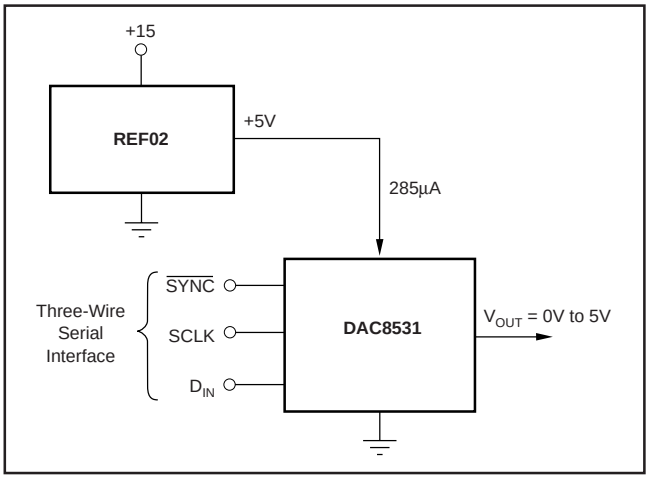


FIGURE 9. REF02 as a Power Supply to the DAC8531.

$$250\mu A + (5V/5k\Omega) = 1.29mA$$

The load regulation of the REF02 is typically 0.005%/mA, which results in an error of 322µV for the 1.29mA current drawn from it. This corresponds to a 4.2LSB error.

BIPOLAR OPERATION USING THE DAC8531

The DAC8531 has been designed for single-supply operation but a bipolar output range is also possible using the circuit in Figure 10. The circuit shown will give an output voltage range of $\pm V_{REF}$. Rail-to-rail operation at the amplifier output is achievable using an OPA703 as the output amplifier.

The output voltage for any input code can be calculated as follows:

$$V_O = \left[V_{REF} \bullet \left(\frac{D}{65536} \right) \bullet \left(\frac{R_1 + R_2}{R_1} \right) - V_{REF} \bullet \left(\frac{R_2}{R_1} \right) \right]$$

where D represents the input code in decimal (0–65535).

With V_{REF} = 5V, $R_1 = R_2$ = 10kΩ:

$$V_O = \left(\frac{10 \bullet D}{65536} \right) - 5V$$

This is an output voltage range of ±5V with 0000_H corresponding to a –5V output and $FFFF_H$ corresponding to a +5V output. Similarly, using V_{REF} = 2.5V, ±2.5V output voltage raw can be achieved.

LAYOUT

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies.

As the DAC8531 offers single-supply operation, it will often be used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it will be to keep digital noise from appearing at the output.

Due to the single ground pin of the DAC8531, all return currents, including digital and analog return currents, must flow through the GND pin. Ideally, GND would be connected directly to an analog ground plane. This plane would be separate from the ground connection for the digital components until they were connected at the power-entry point of the system.

The power applied to V_{DD} should be well regulated and low noise. Switching power supplies and DC/DC converters will often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output.

As with the GND connection, V_{DD} should be connected to a +5V power-supply plane or trace that is separate from the connection for digital logic until they are connected at the power-entry point. In addition, the 1µF to 10µF and 0.1µF bypass capacitors are strongly recommended. In some situations, additional bypassing may be required, such as a 100µF electrolytic capacitor or even a "Pi" filter made up of inductors and capacitors—all designed to essentially low-pass filter the +5V supply, removing the high-frequency noise.

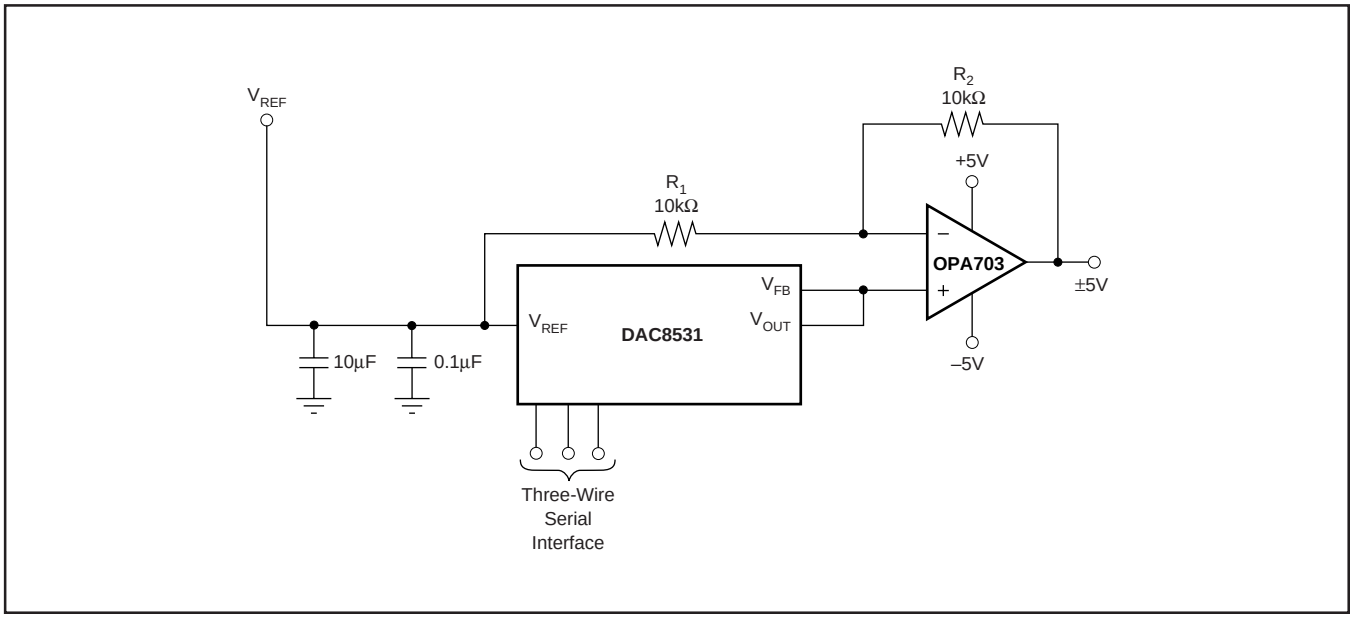
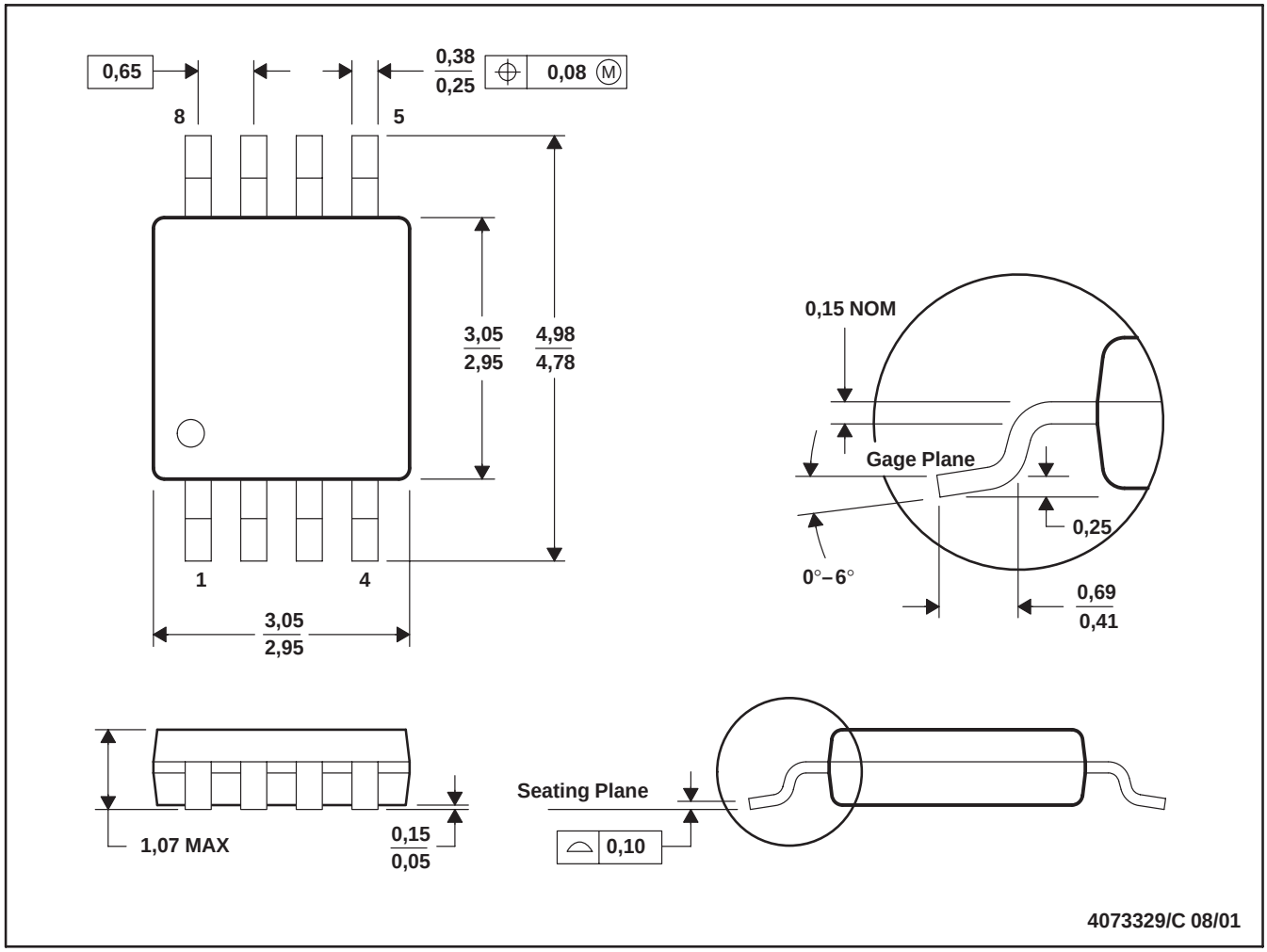


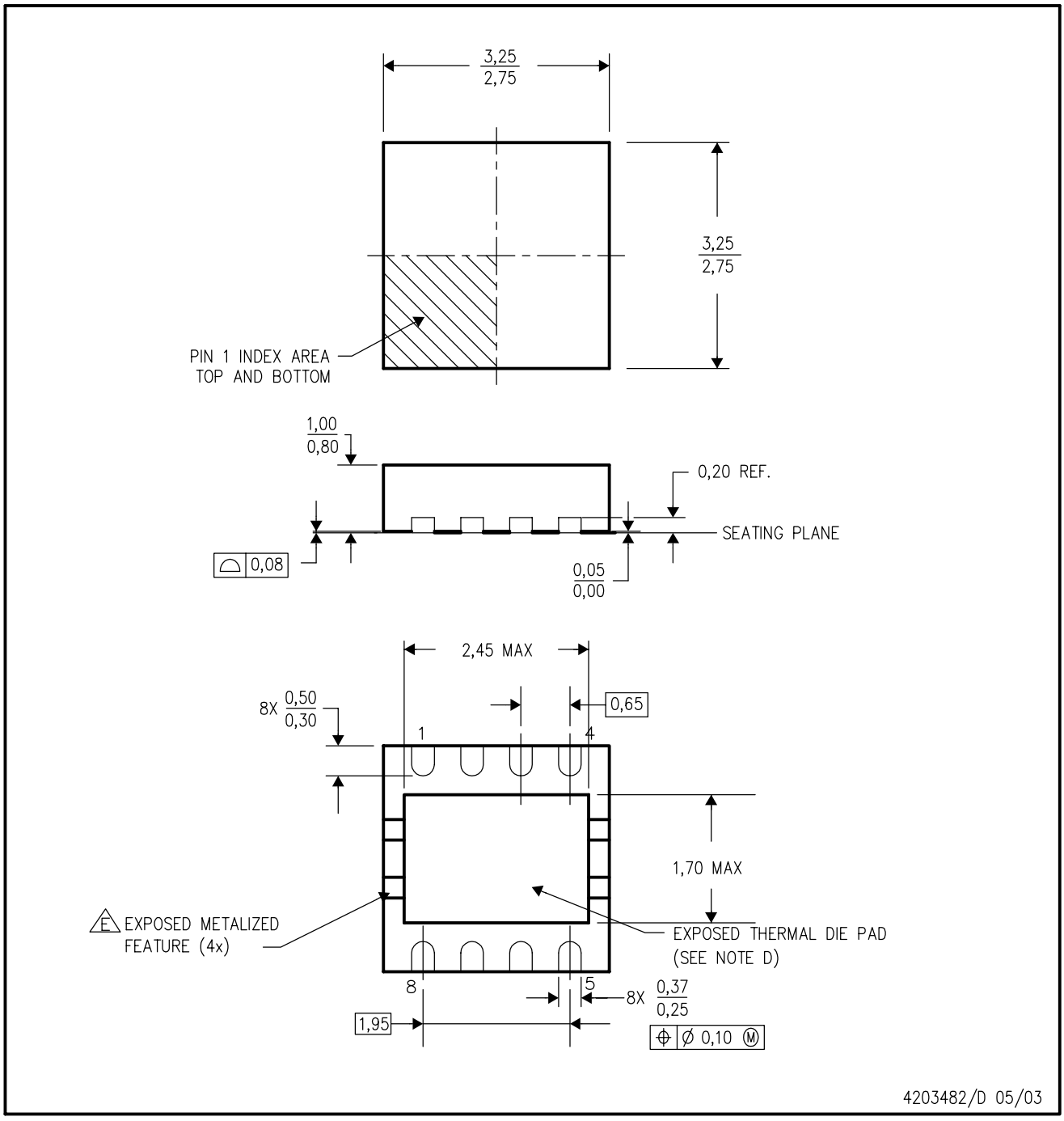
FIGURE 10. Bipolar Operation with the DAC8531.

DGK (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-187

DRB (S–PDSO–N8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane.
E. Metalized features are supplier options and may not be on the package.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC8531E/250	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 105	D31
DAC8531E/250G4	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 105	D31
DAC8531E/2K5	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 105	D31
DAC8531E/2K5G4	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 105	D31
DAC8531IDRBR	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	D31
DAC8531IDRBT	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	D31

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

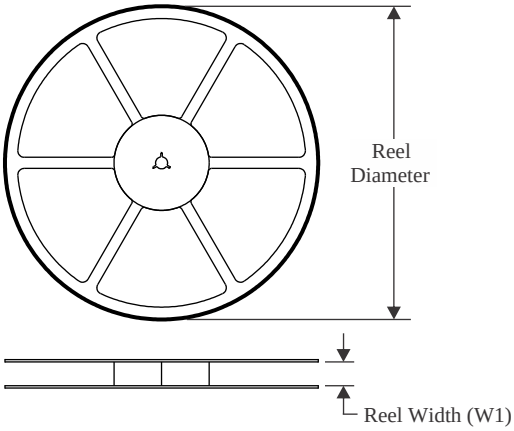
(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

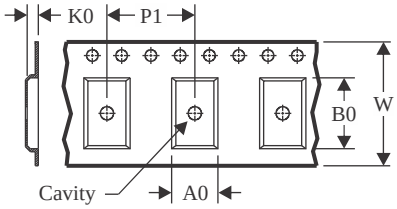
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

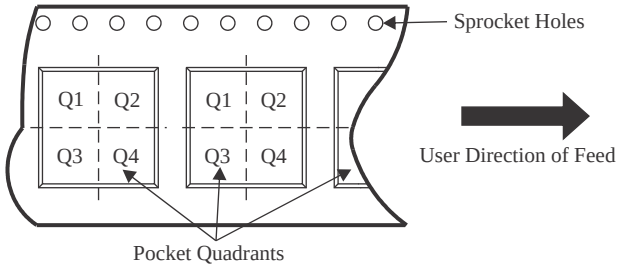


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

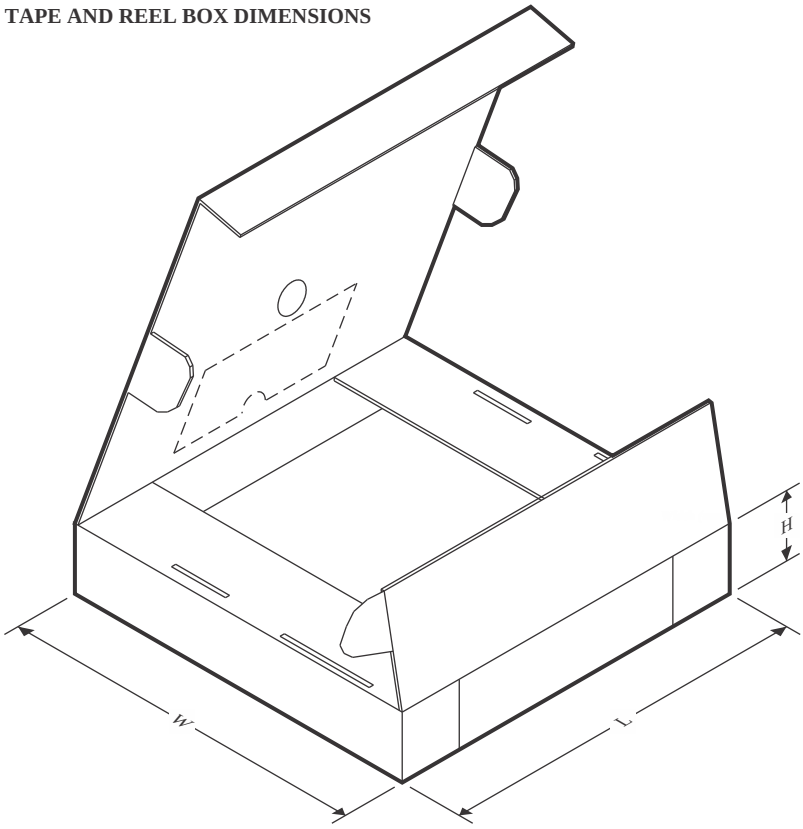
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC8531IDRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DAC8531IDRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC8531IDRBR	SON	DRB	8	3000	356.0	356.0	35.0
DAC8531IDRBT	SON	DRB	8	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DRB 8

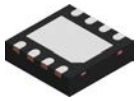
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203482/L

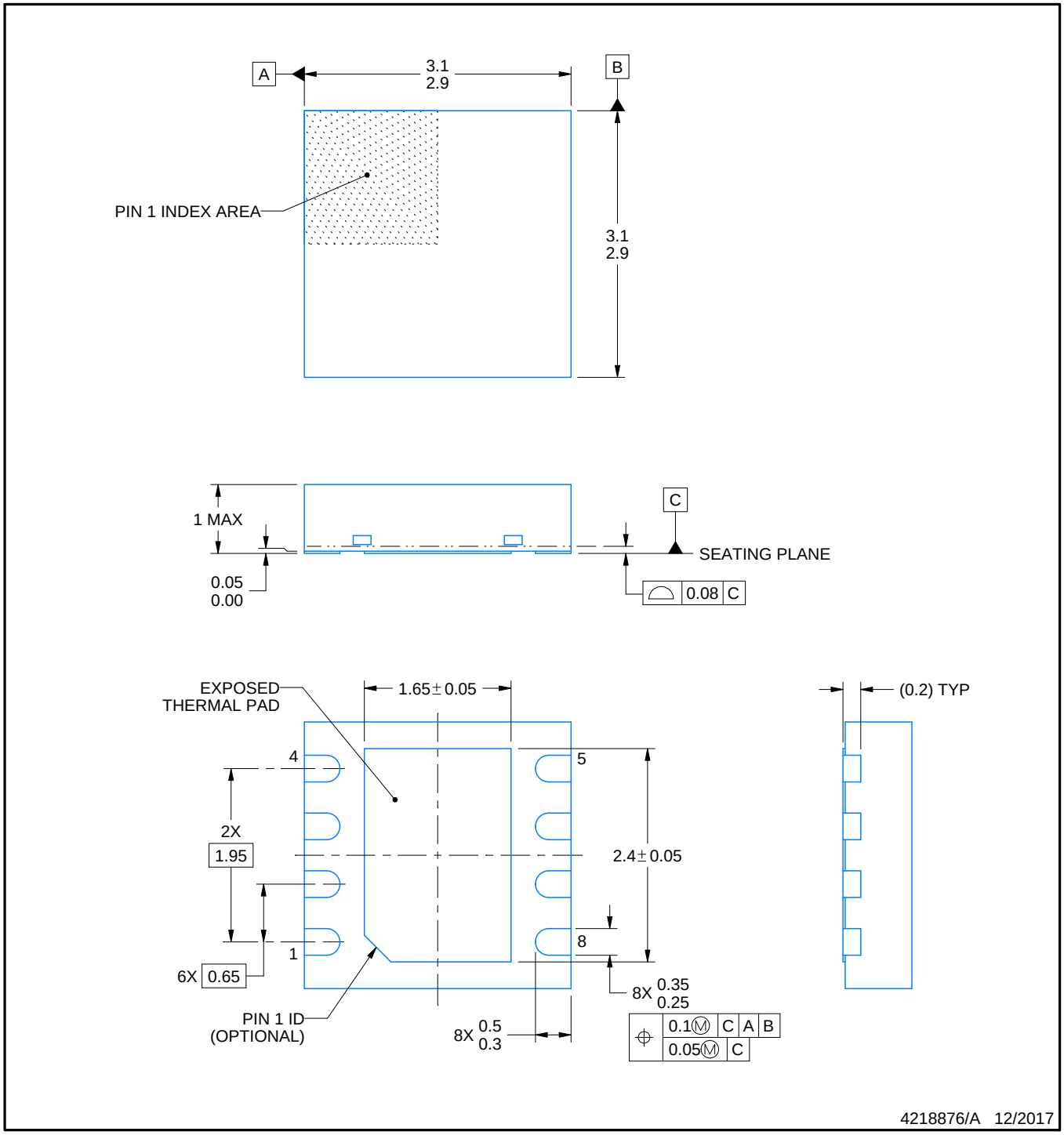
DRB0008B



PACKAGE OUTLINE

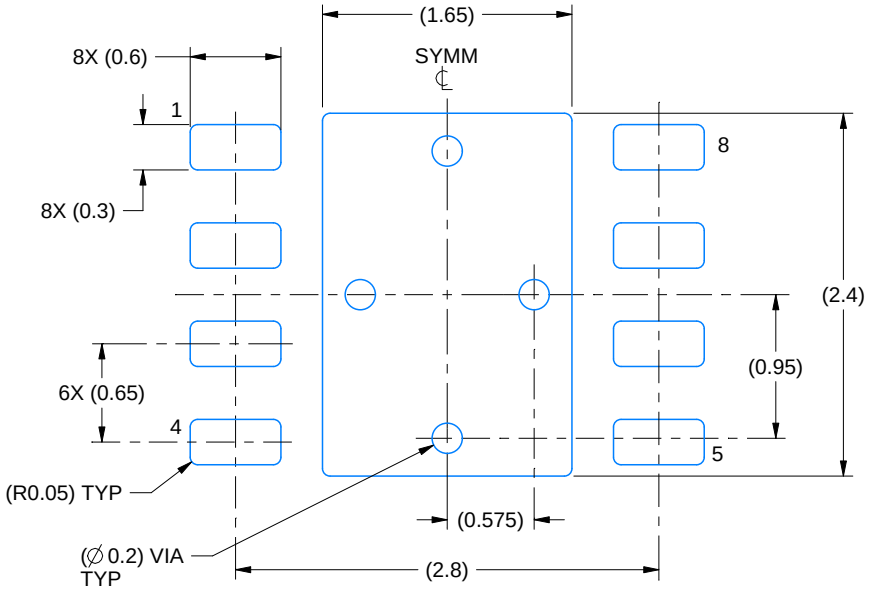
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

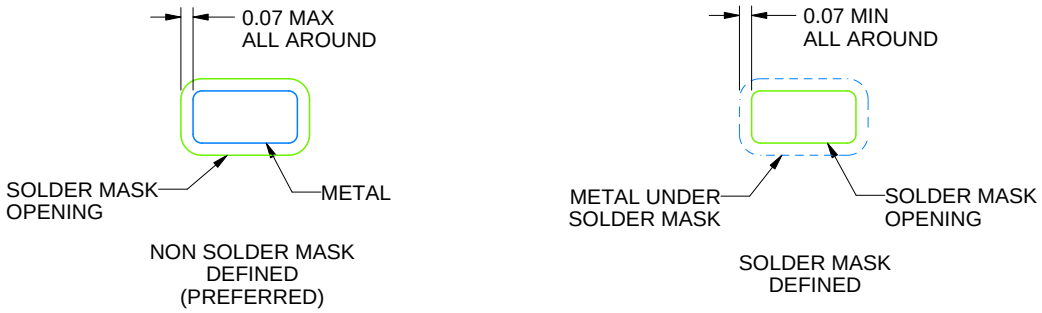


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

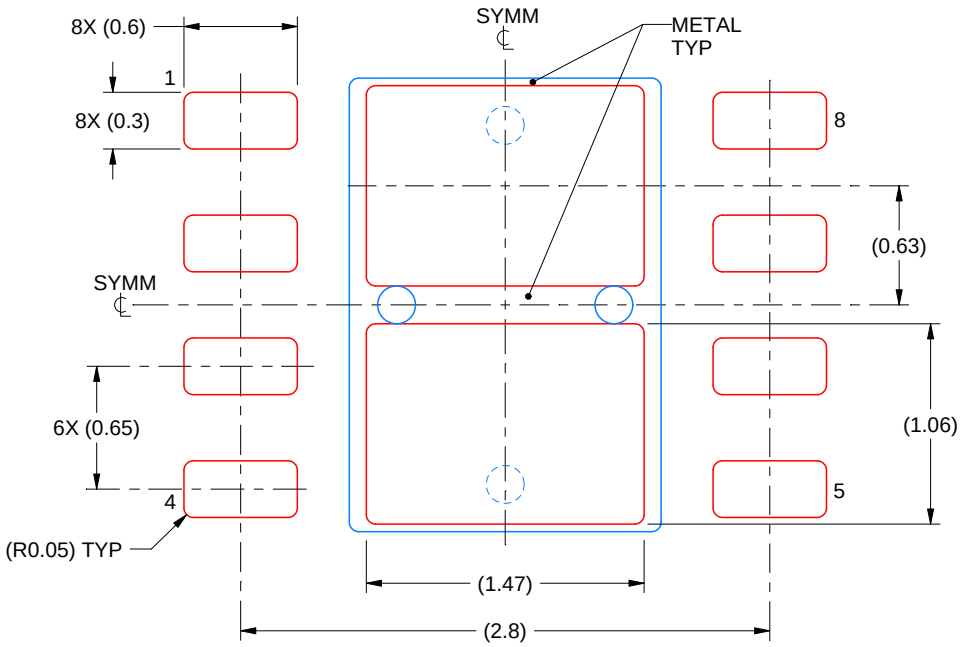


SOLDER MASK DETAILS

4218876/A 12/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218876/A 12/2017

NOTES: (continued)

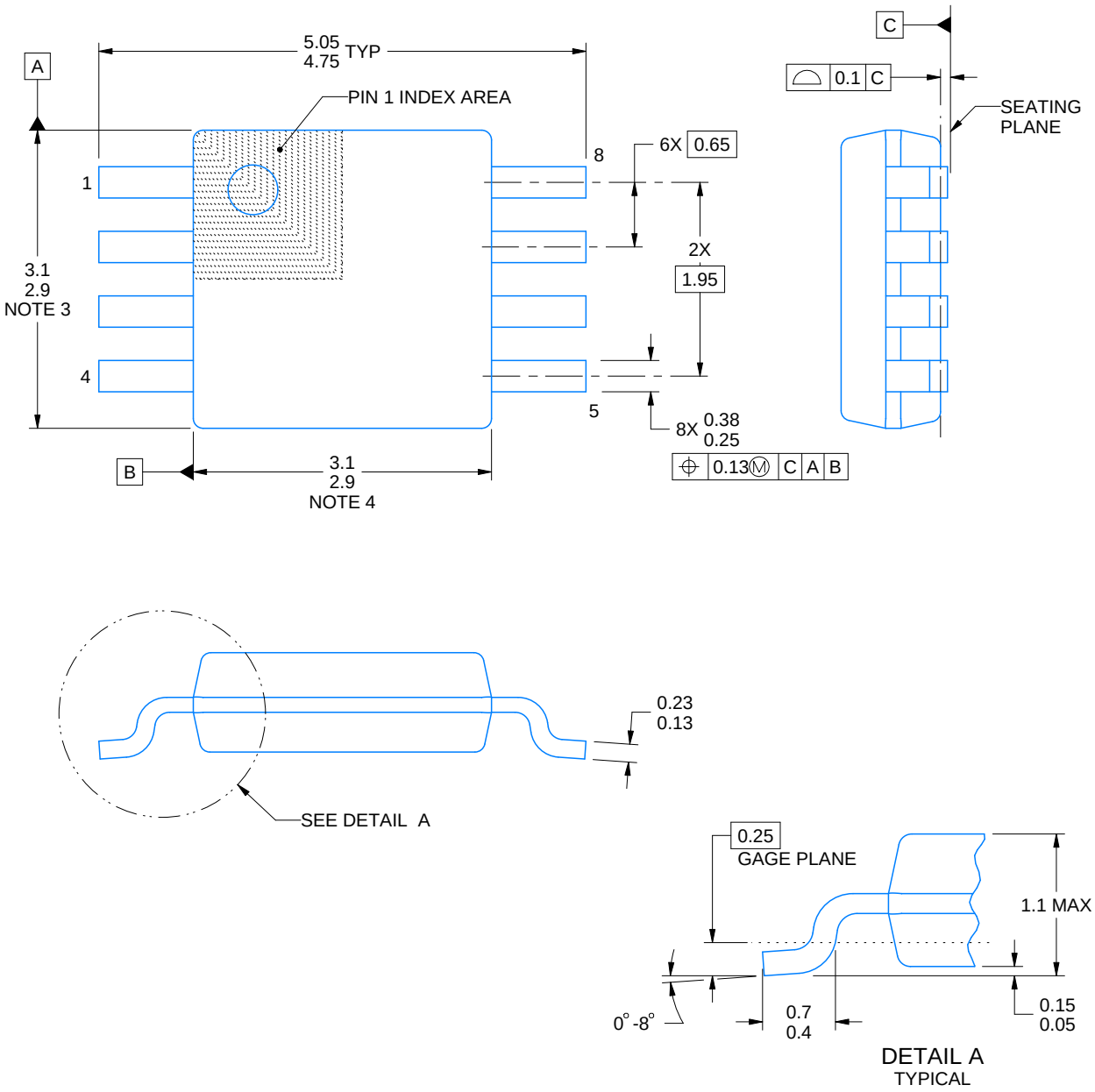
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

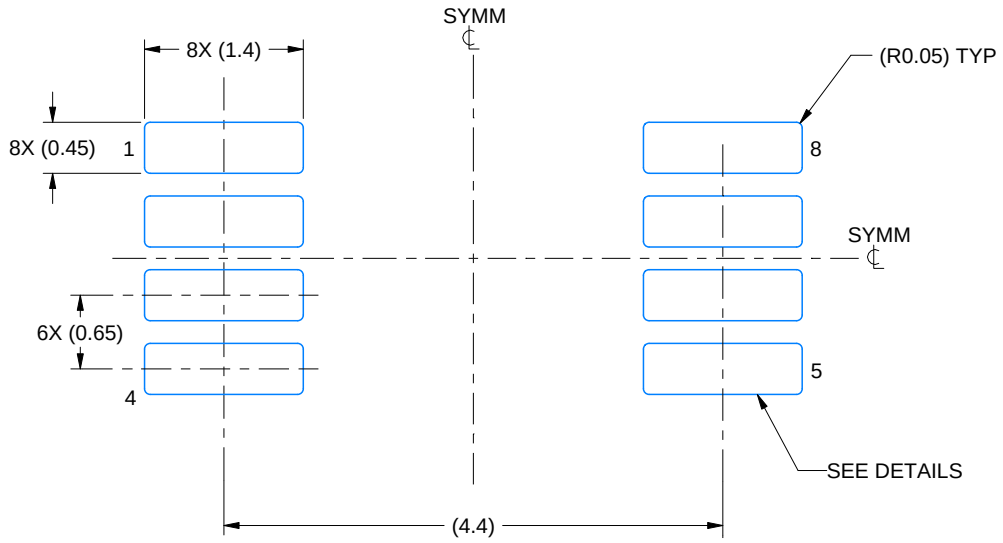
SMALL OUTLINE PACKAGE



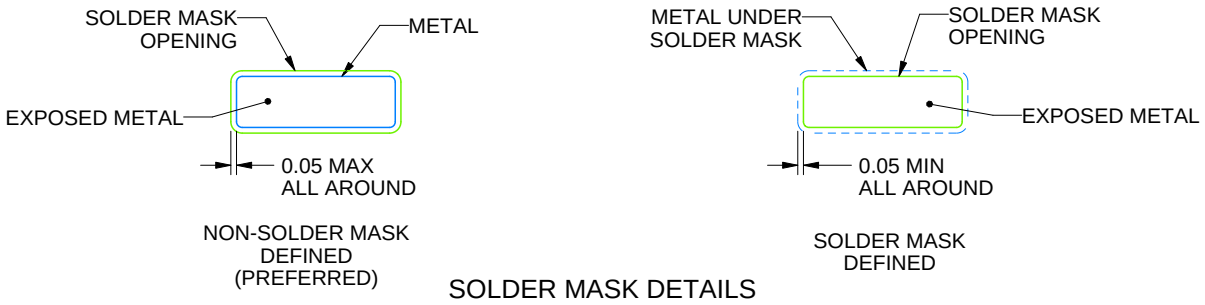
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

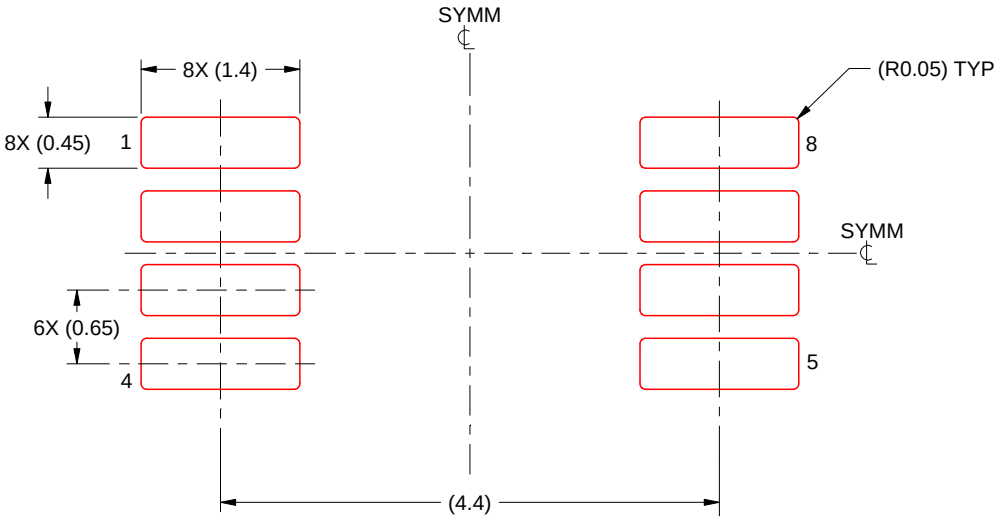


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265