

INA260

具有低漂移、高精度集成分流器的精密电流和功率监测计

1 特性

- 集成精密分流电阻：
 - 电流感测电阻：2mΩ
 - 等效容差为 0.1%
 - 15A 持续电流（-40°C 至 +85°C）
 - 10ppm/°C 温度系数（0°C 至 +125°C）
- 感测的总线电压范围：0V 至 36V
- 高侧或低侧感测
- 报告电流、电压和功率
- 高精度：
 - ±0.15% 系统增益误差（最大值）
 - 5mA 偏移（最大值）
- 可配置的取平均值选项
- 16 个可编程地址
- 由 2.7V 至 5.5V 电源供电
- 16 引脚薄型小尺寸 (TSSOP) 封装

2 应用

- 测试设备
- 服务器
- 电信设备
- 计算
- 电源管理
- 电池充电器
- 电源

3 说明

INA260 是一款数字输出电流、功率和电压监测计，具有一个集成高精度分流电阻的 I²C 和 SMBus™ 兼容接口。该器件支持高精度电流和功率测量并在独立于电源电压的共模电压范围内（0V 至 36V）实现过流检测。该器件是一款双向、低侧/高侧分流监测计，可测量流经内部电流感测电阻的电流。集成的精密电流感测电阻可使器件获得校准级别的测量精度以及超低温漂，并确保始终可实施针对感测电阻而优化的 Kelvin 布局。

INA260 在同一 I²C 兼容接口中具有多达 16 个可编程地址。数字接口允许通过编程设定报警阈值，可实现模数转换器 (ADC) 转换时间并求取平均值。为便于使用，可使用内部乘法器直接读取电流值（单位为安培）和功率值（单位为瓦）。

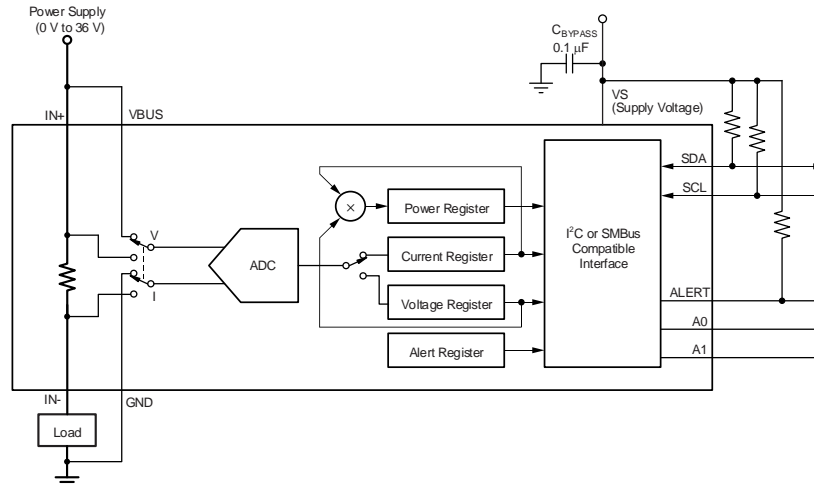
该器件由一个 2.7V 至 5.5V 单电源供电，电源电流为 310μA（典型值）。INA260 在 -40°C 至 +125°C 温度范围内额定运行，采用 16 引脚薄型小外形尺寸 (TSSOP) 封装。

器件信息⁽¹⁾

| 器件型号 | 封装 | 封装尺寸（标称值） |
|--------|------------|-----------------|
| INA260 | TSSOP (16) | 5.00mm x 4.40mm |

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

高侧感测应用



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

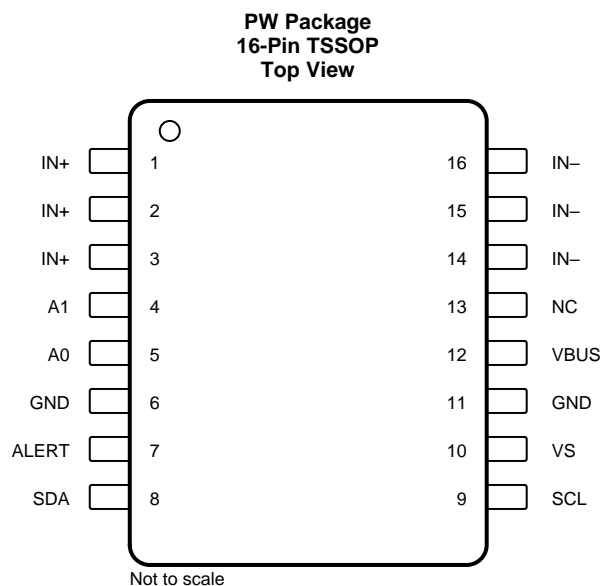
| Changes from Revision B (December 2016) to Revision C | Page |
|--|----------|
| • 已更改 parameter symbol for current sense offset from: V_{OS} to: I_{OS} in <i>Electrical Characteristics</i> table | 8 |

| Changes from Revision A (August 2016) to Revision B | Page |
|---|----------|
| • 已更改 器件状态至“量产数据” | 1 |

5 Related Products

| DEVICE | DESCRIPTION |
|--|--|
| INA250 | 36-V, Low- or High-Side, Bidirectional, Zero-Drift Current-Shunt Monitor with Precision Integrated Shunt Resistor |
| INA226 | High-Side or Low-Side Measurement, Bi-Directional Current and Power Monitor with I ² C Compatible Interface |
| INA230 | High- or Low-Side Measurement, Bidirectional Current/Power Monitor with I ² C Interface |
| INA210 , INA211 , INA212 , INA213 , INA214 , INA215 | Voltage Output, Low- or High-Side Measurement, Bidirectional, Zero-Drift Series, Current-Shunt Monitors |

6 Pin Configuration and Functions



Pin Functions

| PIN | | I/O | DESCRIPTION |
|-------|------------|----------------|---|
| NAME | NO. | | |
| A0 | 5 | Digital input | Address pin. Connect to GND, SCL, SDA, or VS. 表 2 shows pin settings and corresponding addresses. |
| A1 | 4 | Digital input | Address pin. Connect to GND, SCL, SDA, or VS. 表 2 shows pin settings and corresponding addresses. |
| ALERT | 7 | Digital output | Multi-functional alert, open-drain output. |
| GND | 6, 11 | Analog | Ground pin for both analog and digital circuits. |
| IN+ | 1, 2, 3 | Analog input | Connect to supply for high side current sensing or to load ground for low side sensing. |
| IN– | 14, 15, 16 | Analog input | Connect to load for high side current sensing or to board ground for low side sensing. |
| NC | 13 | — | No internal connection. Can be grounded or left floating. |
| SCL | 9 | Digital input | Serial bus clock line input. |
| SDA | 8 | Digital I/O | Serial bus data line, open-drain input/output. |
| VBUS | 12 | Analog input | Bus voltage monitor input. |
| VS | 10 | Analog | Power supply input, connect a 2.7 V to 5.5 V supply to this pin. |

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|-------------------------|---|------|----------|------|
| Analog input current | Continuous Conduction | | ±15 | A |
| Analog inputs: IN+, IN– | Common-mode ($V_{IN+} + V_{IN-}$) / 2 | –0.3 | 40 | V |
| Voltage | Supply, VS | | 6 | V |
| | VBUS pin | –0.3 | 40 | |
| | SDA, SCL, ALERT | –0.3 | 6 | |
| | Address Pins, A0, A1 | –0.3 | VS + 0.3 | |
| | Open-drain digital output current, I _{OUT} | | 10 | mA |
| Temperature | Junction, T _J | | 150 | °C |
| | Storage, T _{stg} | –65 | 150 | |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

| | | VALUE | UNIT |
|--|--|-------|------|
| V _(ESD) Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 | V |
| | Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±1000 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|-----------------|--------------------------------|-----|-----|-----|------|
| V _{CM} | Common-mode input voltage | 0 | | 36 | V |
| VS | Operating supply voltage | 2.7 | | 5.5 | V |
| T _A | Operating free-air temperature | –40 | | 125 | °C |

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | INA260 | UNIT |
|-------------------------------|--|------------|------|
| | | PW (TSSOP) | |
| | | 16 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 115.6 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 50.1 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 46.8 | °C/W |
| ψ _{JT} | Junction-to-top characterization parameter | 3.3 | °C/W |
| ψ _{JB} | Junction-to-board characterization parameter | 46.5 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | N/A | °C/W |

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = 3.3\text{ V}$, $V_{IN+} = 12\text{ V}$, $V_{SENSE} = (V_{IN+} - V_{IN-}) = 0\text{ mV}$ and $V_{VBUS} = 12\text{ V}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------|--|--|-----|--------|-------|--------|
| INPUT | | | | | | |
| V _{CM} | Common-mode input range | | 0 | | 36 | V |
| | Bus voltage input range ⁽¹⁾ | | 0 | | 36 | V |
| CMRR | Common-mode rejection | 0 V ≤ V _{IN+} ≤ 36 V | | 0 | 150 | μA/V |
| I _{OS} | Current sense offset, RTI ⁽²⁾ | | | ±1.25 | ±5 | mA |
| | Current sense offset drift, RTI ⁽²⁾ | −40°C ≤ T _A ≤ 125°C | | 1 | 50 | μA/°C |
| PSRR | Current sense offset voltage, RTI ⁽²⁾ vs power supply | 2.7 V ≤ V _S ≤ 5.5 V | | 1.6 | 3 | mA/V |
| V _{OS} | Bus offset voltage, RTI ⁽²⁾ | | | ±1.25 | ±7.5 | mV |
| | Bus offset voltage, RTI ⁽²⁾ vs temperature | −40°C ≤ T _A ≤ 125°C | | 0.6 | 40 | μV/°C |
| PSRR | Bus offset voltage, RTI ⁽²⁾ vs power supply | | | 1.5 | | mV/V |
| I _B | Input bias current (I _{IN+} , I _{IN−} pins) | (IN+ pin) + (IN− pin), I _{SENSE} = 0A | | 17 | | μA |
| | VBUS input impedance | | | 830 | | kΩ |
| | Input leakage ⁽³⁾ | (IN+ pin) + (IN− pin), power-down mode | | 0.1 | 0.5 | μA |
| DC ACCURACY | | | | | | |
| System current sense gain error | | I _{SENSE} = −15 A to 15 A, T _A = 25°C | | 0.02% | 0.15% | ppm/°C |
| | | I _{SENSE} = −10 A to 10 A, −40°C ≤ T _A ≤ 125°C | | 0.2% | 0.5% | |
| | | −40°C ≤ T _A ≤ 125°C | | 10 | 35 | |
| Bus voltage gain error | | V _{BUS} = 0 V to 36 V, T _A = 25°C | | 0.02% | 0.1% | ppm/°C |
| | | V _{BUS} = 0 V to 36 V, −40°C ≤ T _A ≤ 125°C | | 0.1% | 0.4% | |
| | | −40°C ≤ T _A ≤ 125°C | | 15 | 40 | |
| INTEGRATED ADC | | | | | | |
| ADC native resolution | | | | 16 | | Bits |
| 1-LSB step size | | Current | | 1.25 | | mA |
| | | Bus voltage | | 1.25 | | mV |
| | | Power | | 10 | | mW |
| t _{CT} | ADC conversion time | CT bit = 000 | | 140 | 154 | μs |
| | | CT bit = 001 | | 204 | 224 | |
| | | CT bit = 010 | | 332 | 365 | |
| | | CT bit = 011 | | 588 | 646 | |
| | | CT bit = 100 | | 1.1 | 1.21 | ms |
| | | CT bit = 101 | | 2.116 | 2.328 | |
| | | CT bit = 110 | | 4.156 | 4.572 | |
| | | CT bit = 111 | | 8.244 | 9.068 | |
| Differential nonlinearity | | | | ±0.1 | | LSB |
| INTEGRATED SHUNT | | | | | | |
| Package resistance | | IN+ to IN− | | 4.5 | | mΩ |
| Maximum continuous current | | −40°C ≤ T _A ≤ 85°C | | | ±15 | A |
| Short time overload change | | I _{SENSE} = 30 A for 5 seconds | | ±0.05% | | |

- (1) Although the input range is 36 V, the full-scale range of the ADC scaling is 40.96 V; see the [Basic ADC Functions](#) section. Do not apply more than 36 V.
- (2) RTI = Referred-to-input.
- (3) Input leakage is positive (current flowing into the pin) for the conditions shown at the top of this table. Negative leakage currents can occur under different input conditions.

Electrical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 3.3\text{ V}$, $V_{IN+} = 12\text{ V}$, $V_{SENSE} = (V_{IN+} - V_{IN-}) = 0\text{ mV}$ and $V_{VBUS} = 12\text{ V}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|------------------|---------------|------------------|---------------|
| Change due to thermal shock | $-65^\circ\text{C} \leq T_A \leq 150^\circ\text{C}$, 500 cycles | | $\pm 0.1\%$ | | |
| Resistance change to solder heat | 260°C solder, 10 s | | $\pm 0.1\%$ | | |
| High temperature exposure change | 1000 hours, $T_A = 150^\circ\text{C}$ | | $\pm 0.15\%$ | | |
| Cold temperature storage change | 24 hours, $T_A = -65^\circ\text{C}$ | | $\pm 0.025\%$ | | |
| SMBus | | | | | |
| SMBus timeout ⁽⁴⁾ | | | 28 | 35 | ms |
| DIGITAL INPUT/OUTPUT | | | | | |
| Input capacitance | | | 3 | | pF |
| Leakage input current | $0\text{ V} \leq V_{SCL} \leq V_S$, $0\text{ V} \leq V_{SDA} \leq V_S$, $0\text{ V} \leq V_{ALERT} \leq V_S$, $0\text{ V} \leq V_{A0} \leq V_S$, $0\text{ V} \leq V_{A1} \leq V_S$ | | 0.1 | 1 | μA |
| V_{IH} High-level input voltage | | $0.7 \times V_S$ | | 6 | V |
| V_{IL} Low-level input voltage | | 0 | | $0.3 \times V_S$ | V |
| V_{OL} Low-level output voltage, SDA, ALERT | $I_{OL} = 3\text{ mA}$ | 0 | | 0.4 | V |
| SDA, SCL Hysteresis | | | 500 | | mV |
| POWER SUPPLY | | | | | |
| Operating supply range | | 2.7 | | 5.5 | V |
| I_Q Quiescent current | | | 310 | 420 | μA |
| Quiescent current, power-down (shutdown) mode | | | 0.5 | 2 | μA |
| V_{POR} Power-on reset threshold | | | 2 | | V |

(4) SMBus timeout in the INA260 resets the interface any time SCL is low for more than 28 ms.

7.6 Typical Characteristics

At $T_A = 25^\circ\text{C}$, $V_S = 3.3\text{ V}$, $V_{IN+} = 12\text{ V}$, $V_{SENSE} = (V_{IN+} - V_{IN-}) = 0\text{ mV}$ and $V_{VBUS} = 12\text{ V}$, unless otherwise noted.

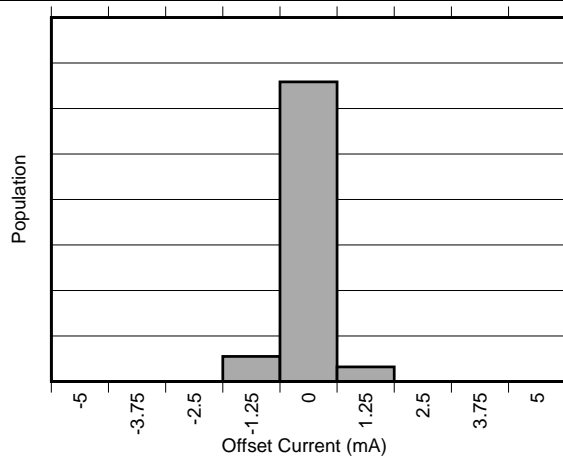


图 1. Current Sense Offset Production Distribution

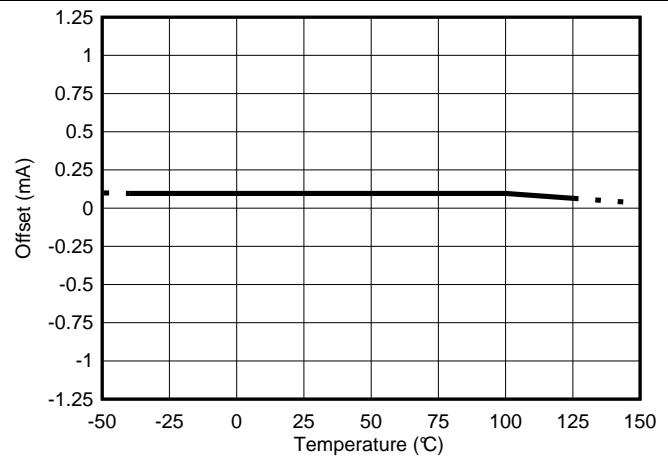


图 2. Current Sense Offset vs Temperature

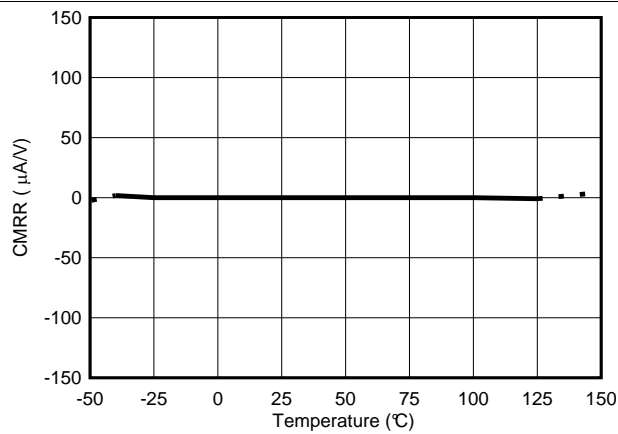


图 3. Current Sense Common-Mode Rejection Ratio vs Temperature

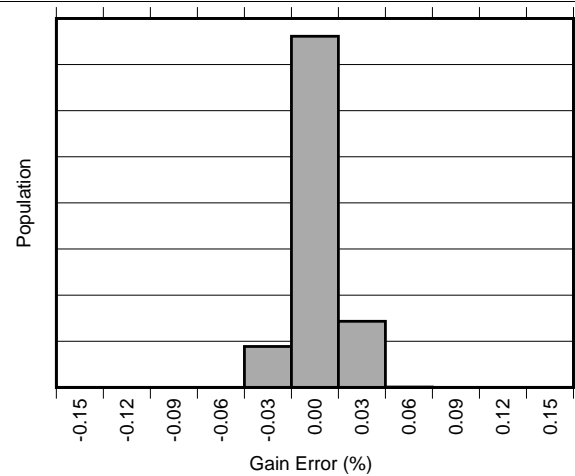


图 4. Current Sense Gain Error Production Distribution

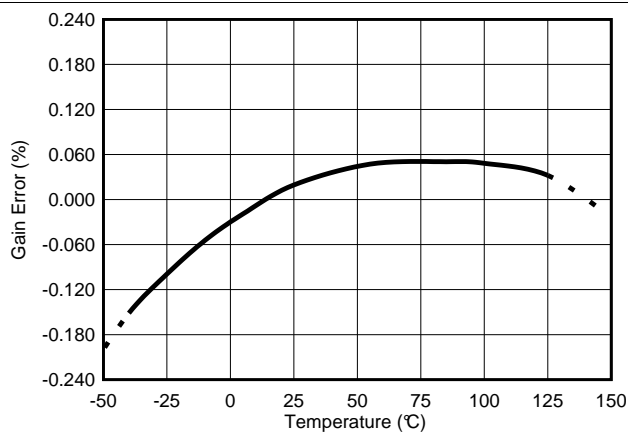


图 5. Current Sense Gain Error vs Temperature

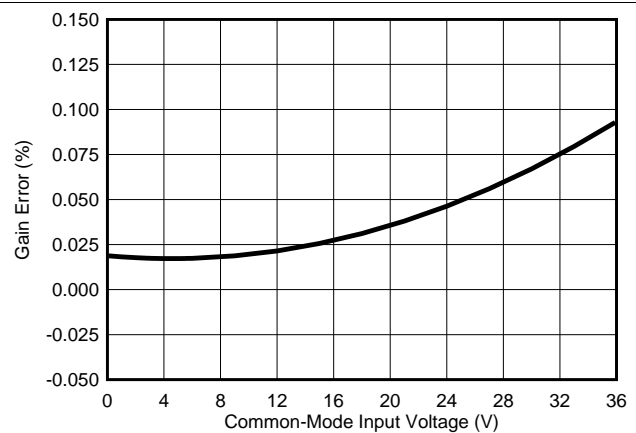


图 6. Current Sense Gain Error vs Common-Mode Voltage

Typical Characteristics (接下页)

At $T_A = 25^\circ\text{C}$, $V_S = 3.3\text{ V}$, $V_{IN+} = 12\text{ V}$, $V_{SENSE} = (V_{IN+} - V_{IN-}) = 0\text{ mV}$ and $V_{VBUS} = 12\text{ V}$, unless otherwise noted.

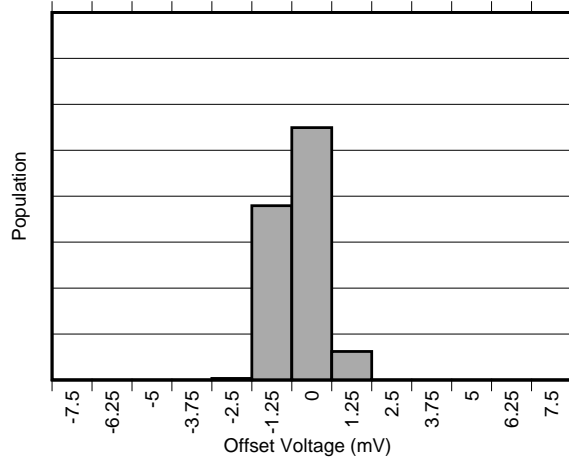


图 7. Bus Offset Voltage Production Distribution

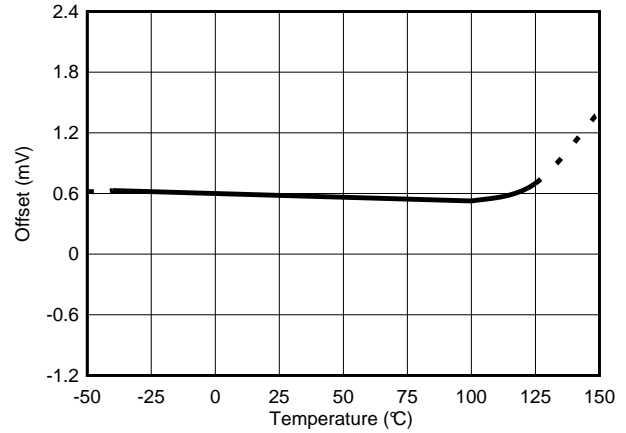


图 8. Bus Offset Voltage vs Temperature

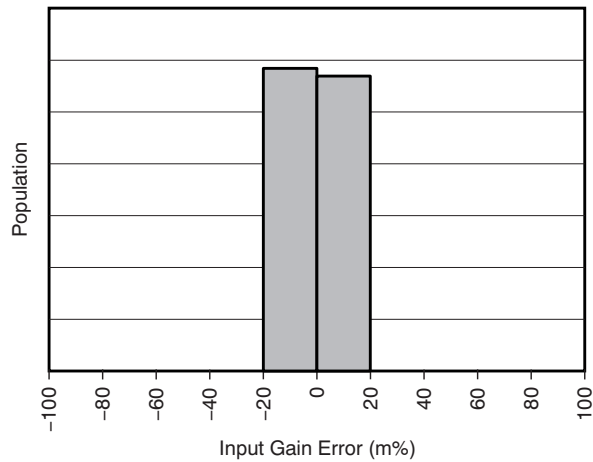


图 9. Bus Gain Error Production Distribution

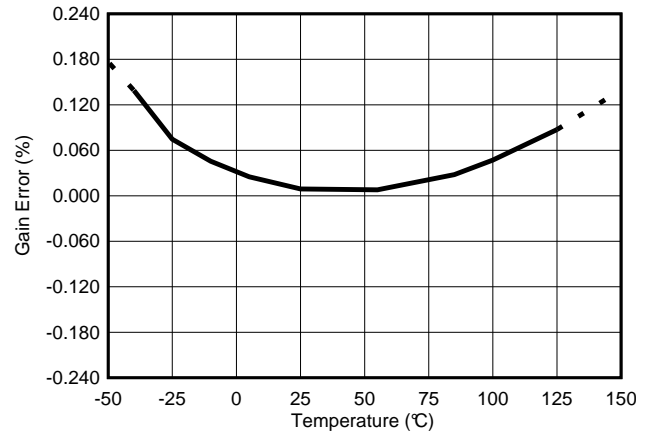


图 10. Bus Gain Error vs Temperature

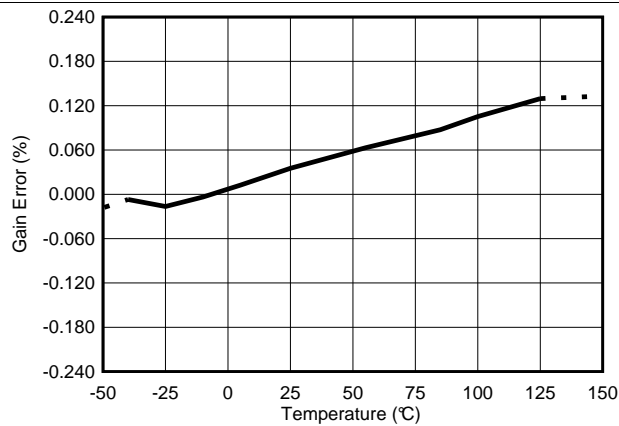


图 11. Power Gain Error vs Temperature

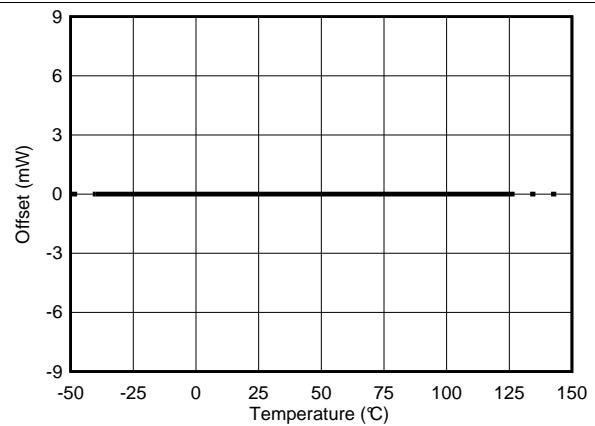


图 12. Power Offset Error vs Temperature

Typical Characteristics (接下页)

At $T_A = 25^\circ\text{C}$, $V_S = 3.3\text{ V}$, $V_{IN+} = 12\text{ V}$, $V_{SENSE} = (V_{IN+} - V_{IN-}) = 0\text{ mV}$ and $V_{VBUS} = 12\text{ V}$, unless otherwise noted.

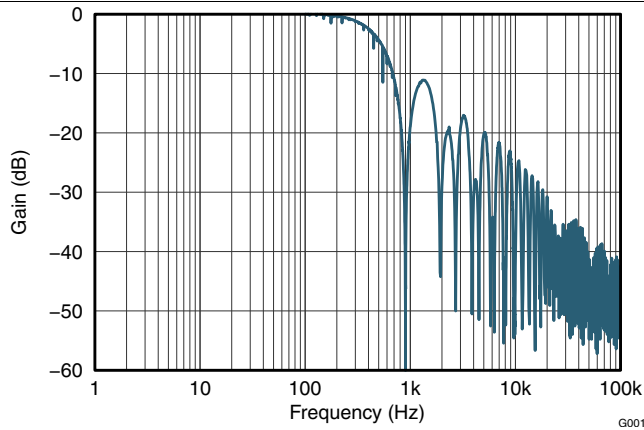


图 13. Frequency Response

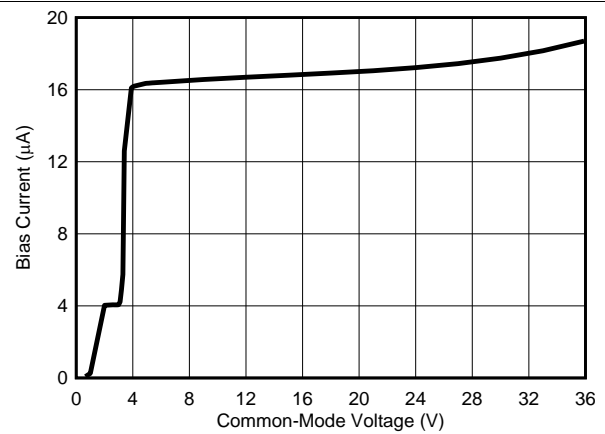


图 14. Input Bias Current vs Common-Mode Voltage (Both Inputs, IN+ and IN-)

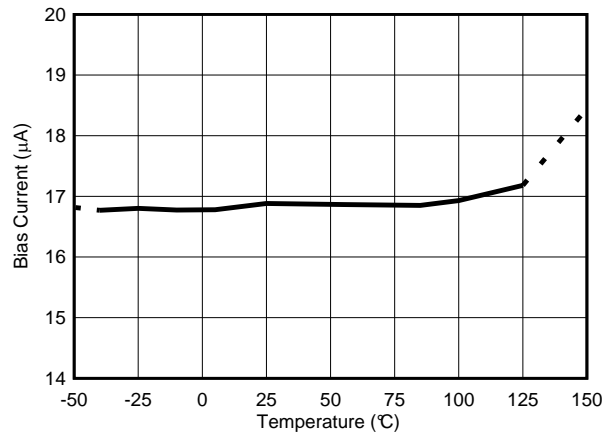


图 15. Input Bias Current vs Temperature (Both Inputs, IN+ and IN-)

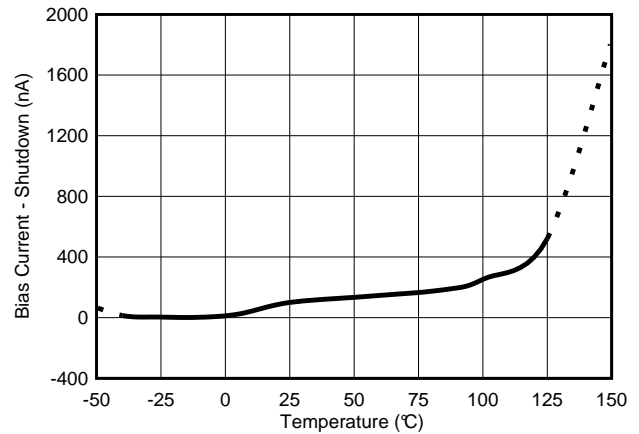


图 16. Input Bias Current vs Temperature, Shutdown (Both Inputs, IN+ and IN-)

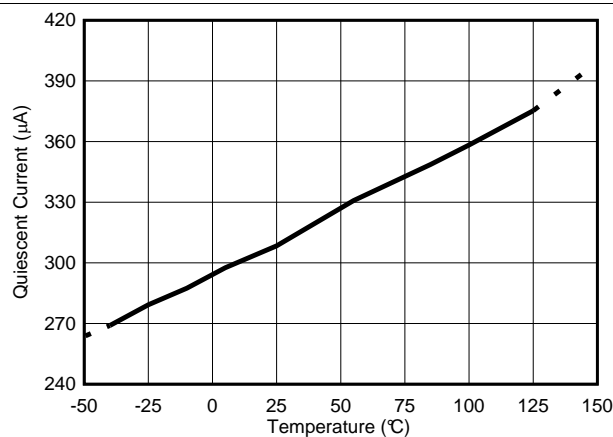


图 17. Active I_Q vs Temperature

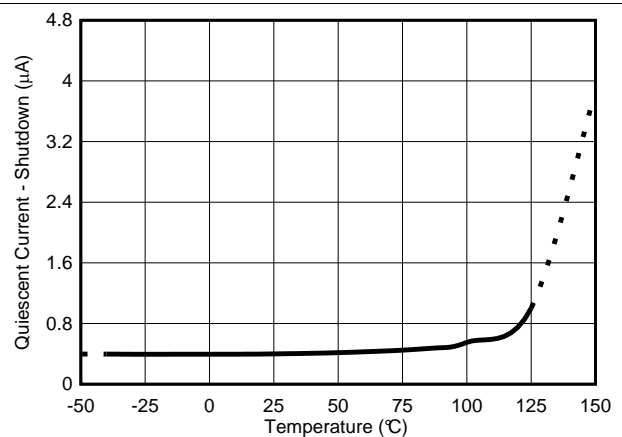


图 18. Shutdown I_Q vs Temperature

Typical Characteristics (接下页)

At $T_A = 25^\circ\text{C}$, $V_S = 3.3\text{ V}$, $V_{IN+} = 12\text{ V}$, $V_{SENSE} = (V_{IN+} - V_{IN-}) = 0\text{ mV}$ and $V_{VBUS} = 12\text{ V}$, unless otherwise noted.

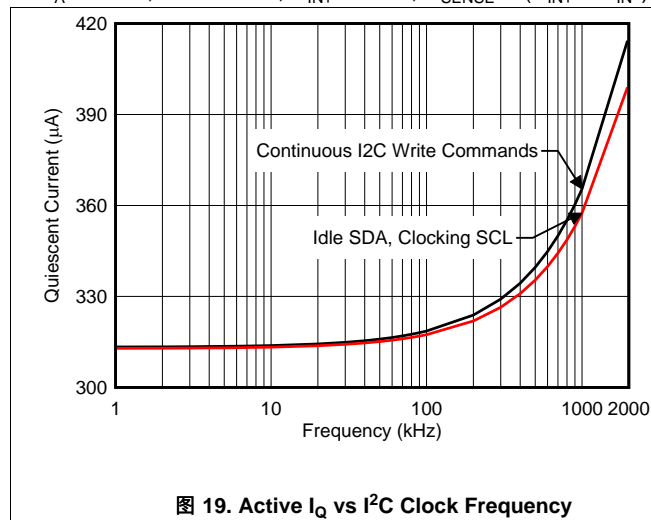


图 19. Active I_Q vs I²C Clock Frequency

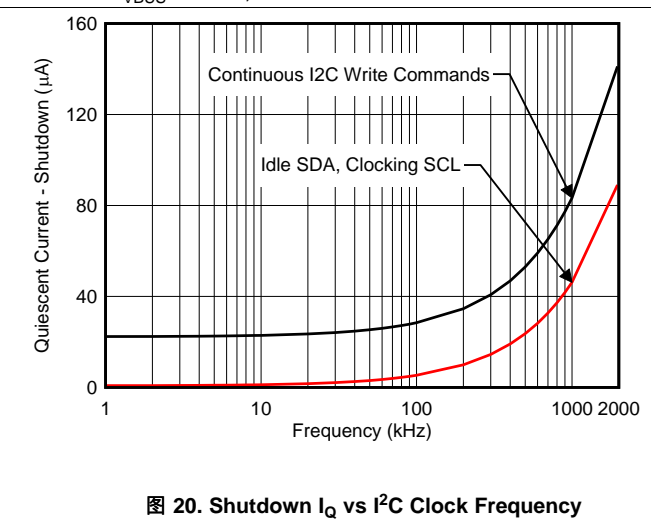


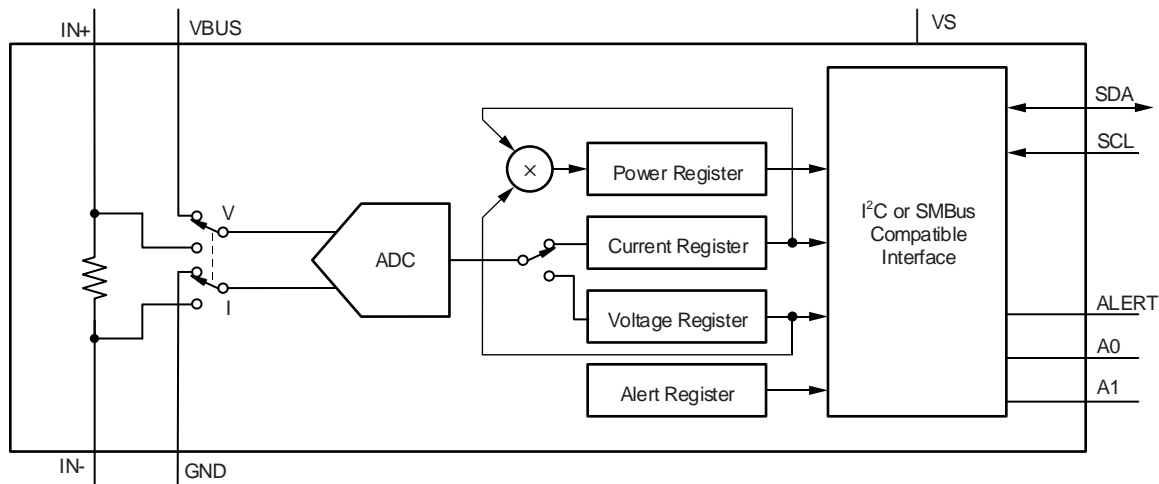
图 20. Shutdown I_Q vs I²C Clock Frequency

8 Detailed Description

8.1 Overview

The INA260 is an integrated shunt digital current sense amplifier with an I²C- and SMBus-compatible interface. It provides digital current, voltage, and power readings necessary for accurate decision-making in precisely-controlled systems. Programmable registers allow flexible configuration for conversion times as well as continuous-versus-triggered operation. Detailed register information appears at the end of this data sheet, beginning with 表 4. See the [Functional Block Diagram](#) section for a block diagram of the INA260 device.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Integrated Shunt Resistor

The INA260 features a precise, low-drift, current-sensing resistor to allow for precision measurements over the entire specified temperature range of -40°C to $+125^{\circ}\text{C}$. The integrated current-sensing resistor ensures measurement stability over temperature as well as simplifying printed-circuit board (PCB) layout difficulties common in high precision current sensing measurements.

The onboard current-sensing resistor is designed as a 4-wire (or Kelvin) connected resistor that enables accurate measurements through a force-sense connection. The Kelvin connections to the shunt are done internally eliminating many of the parasitic impedances commonly found in typical very-low sensing-resistor level measurements. Although the shunt resistor can be accessed through the IN+ and IN- pins, this resistor is not intended to be used as a stand-alone component. The INA260 is internally calibrated to ensure that the current-sensing resistor and current-sensing amplifier are both precisely matched to one another.

The INA260 has approximately $4.5\text{ m}\Omega$ of total resistance between the IN+ and IN- pins. $2\text{ m}\Omega$ of this total package resistance is a precisely-controlled resistance from the Kelvin-connected current-sensing resistor used by the internal analog to digital converter (ADC). The power dissipation requirements of the system and package are based on the total $4.5\text{-m}\Omega$ package resistance. The heat dissipated across the package when current flows through the device ultimately determines the maximum current that can be safely handled by the package. The current consumption of the silicon is relatively low, leaving the total package resistance carrying the high load current as the primary contributor to the total power dissipation of the package. The maximum safe-operating current level is set to ensure that the heat dissipated across the package is limited so that no damage to the resistor or the package itself occurs or that the internal junction temperature of the silicon does not exceed a 150°C limit.

Feature Description (接下页)

External factors (such as ambient temperature, external air flow, and PCB layout) can contribute to how effectively the heat developed as a result of the current flowing through the total package resistance can be removed from within the device. Under the conditions of no air flow, a maximum ambient temperature of 85°C, and 1-oz. copper input power planes, the INA260 can accommodate continuous current levels up to 15 A. As shown in 图 21, the current handling capability is derated at temperatures above the 85°C level with safe operation up to 10 A at a 125°C ambient temperature. With air flow and larger 2-oz. copper input power planes, the INA260 can safely accommodate continuous current levels up to 15 A over the entire –40°C to +125°C temperature range.

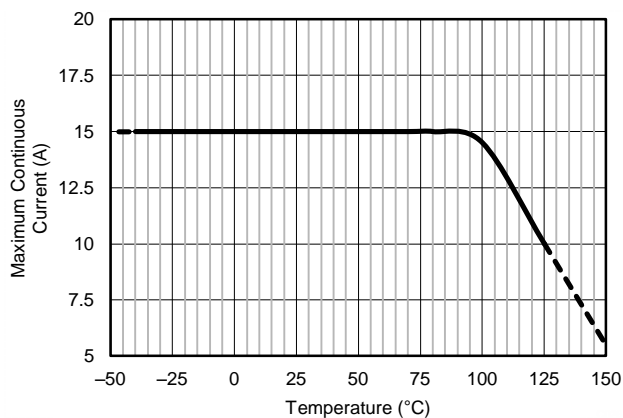


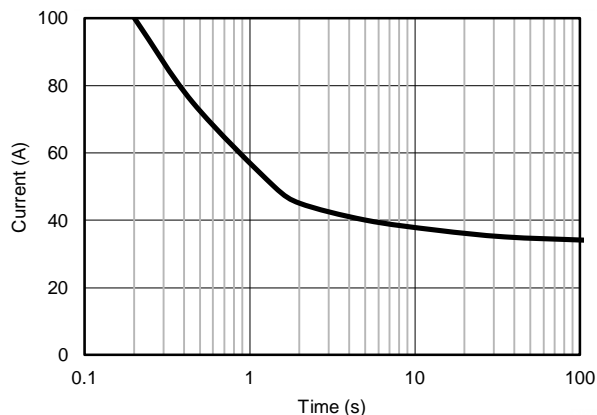
图 21. Maximum Current vs Temperature

8.3.2 Over-Current Capability

The INA260 features a physical shunt resistance that is able to withstand current levels higher than the continuous handling limit of 15 A without sustaining damage to the current-sensing resistor or the current-sensing amplifier if the excursions are very brief. 图 22 shows the maximum overload current versus time curve for the INA260.

CAUTION

Operation at or above this curve, 图 22, can result in device damage or permanent erroneous current readings.



$T_A = 25^\circ\text{C}$

图 22. Maximum Overload Current vs Time

Feature Description (接下页)

8.3.3 Basic ADC Functions

The INA260 device performs two measurements on the power-supply bus of interest. The current which is internally calculated by measuring the voltage developed across a known internal shunt resistor, and the power supply bus voltage from the external VBUS pin to ground.

The device is typically powered by a separate supply that can range from 2.7 V to 5.5 V. The bus that is being monitored can range in voltage from 0 V to 36 V. Based on the fixed 1.25-mV LSB for the Bus Voltage Register that a full-scale register results in a 40.96 V value.

注

Do not apply more than 36 V of actual voltage to the input pins.

There are no special considerations for power-supply sequencing because the common-mode input range and power-supply voltage are independent of each other; therefore, the bus voltage can be present with the supply voltage off, and vice-versa.

The device has two operating modes, continuous and triggered, that determine how the ADC operates following these conversions. When the device is in the normal operating mode (that is, MODE bits of the Configuration Register (00h) are set to '111'), it continuously converts an internal shunt voltage reading followed by a bus voltage reading. After the measurement of the internal shunt voltage reading, the current value is calculated. This current value is then used to calculate the power result. These values are subsequently stored in an accumulator, and the measurement/calculation sequence repeats until the number of averages set in the Configuration Register (00h) is reached. Following every sequence, the present set of values, measured and calculated, are appended to previously collected values. After all of the averaging has been completed, the final values for bus voltage, current, and power are updated in the corresponding registers that can then be read. These values remain in the data output registers until they are replaced by the next fully completed conversion results. Reading the data output registers does not affect a conversion in progress.

The mode control in the Configuration Register (00h) also permits selecting modes to convert only the current or the bus voltage in order to further allow the user to configure the monitoring function to fit the specific application requirements.

In triggered mode, writing any of the triggered convert modes into the Configuration Register (00h) (that is, MODE bits of the Configuration Register (00h) are set to '001', '010', or '011') triggers a single-shot conversion. This action produces a single set of measurements; thus, to trigger another single-shot conversion, the Configuration Register (00h) must be written to a second time, even if the mode does not change.

In addition to the two operating modes (continuous and triggered), the device also has a power-down mode that reduces the quiescent current and turns off current into the device inputs, reducing the impact of supply drain when the device is not being used. Full recovery from power-down mode requires 40 μ s. The registers of the device can be written to and read from while the device is in power-down mode. The device remains in power-down mode until one of the active modes settings are written into the Configuration Register (00h) .

Although the device can be read at any time, and the data from the last conversion remain available, the Conversion Ready flag bit (Mask/Enable Register, CVRF bit) is provided to help coordinate one-shot or triggered conversions. The Conversion Ready flag (CVRF) bit is set after all conversions, averaging, and multiplication operations are complete.

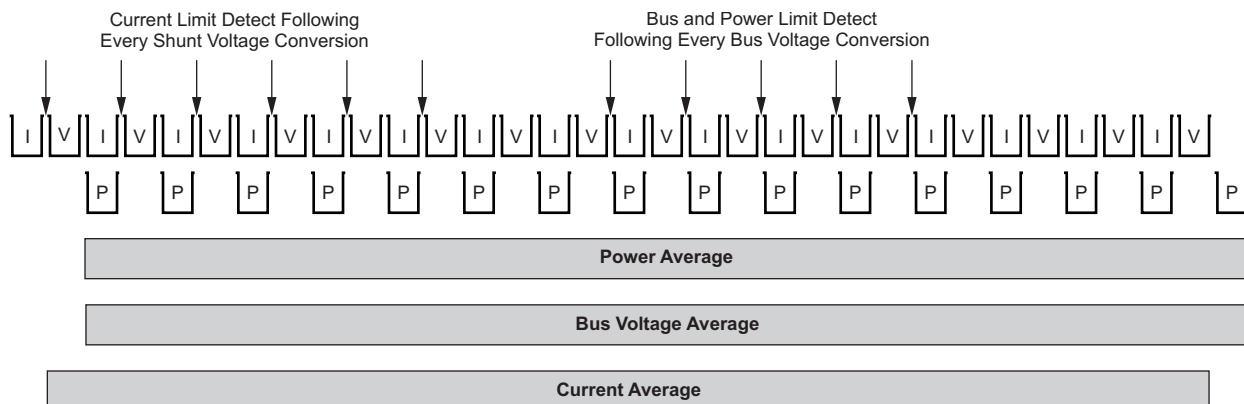
The Conversion Ready flag (CVRF) bit clears under these conditions:

- Writing to the Configuration Register (00h), except when configuring the MODE bits for power-down mode; or
- Reading the Mask/Enable Register (06h)

8.3.3.1 Power Calculation

The power is calculated following current and bus voltage measurements; see 图 23. Calculations for both the current and power are performed in the background and do not add to the overall conversion time. These current and power values are considered intermediate results (unless the averaging is set to 1) and are stored in an internal accumulation register, not the corresponding output registers. Following every measured sample, the newly-calculated values for current and power are appended to this accumulation register until all of the samples have been measured and averaged based on the number of averages set in the Configuration Register (00h).

Feature Description (接下页)



NOTE: I = current, V = voltage, and P = power.

图 23. Power Calculation Scheme

In addition to the current and power accumulating after every sample, the bus voltage measurement is also collected. After all of the samples have been measured and the corresponding current and power calculations have been made, the accumulated average for each of these parameters is then loaded to the corresponding output registers, where they can be read.

8.3.3.2 ALERT Pin

The INA260 has a single Alert Limit Register (07h), that allows the ALERT pin to be programmed to respond to a single user-defined event or to a Conversion Ready notification if desired. The Mask/Enable Register allows the user to select from one of the five available functions to monitor as well as setting the Conversion Ready bit to control the response of the ALERT pin. Based on the function being monitored, enter a value into the Alert Limit Register to set the corresponding threshold value that asserts the ALERT pin.

The ALERT pin allows for one of several available alert functions to be monitored to determine if a user-defined threshold has been exceeded. The five alert functions that can be monitored are:

- Shunt Over Current-Limit (OCL)
- Shunt Under Current-Limit (UCL)
- Bus Voltage Over-Limit (BOL)
- Bus Voltage Under-Limit (BUL)
- Power Over-Limit (POL)

The ALERT pin is an open-drain output. This pin is asserted when the alert function selected in the Mask/Enable Register exceeds the value programmed into the Alert Limit Register. Only one of these alert functions can be enabled and monitored at a time. If multiple alert functions are enabled, the selected function in the highest significant bit position takes priority and responds to the Alert Limit Register value. For example, if the shunt over and under current limit functions are both selected, the Alert pin asserts when the shunt current exceeds the value in the Alert Limit Register.

The Conversion Ready state of the device can also be monitored at the ALERT pin to inform the user when the device has completed the previous conversion and is ready to begin a new conversion. Conversion Ready can be monitored at the ALERT pin along with one of the alert functions. If an alert function and the Conversion Ready are both enabled to be monitored at the ALERT pin, after the ALERT pin is asserted, the Mask/Enable Register must be read following the alert to determine the source of the alert. By reading the Conversion Ready Flag (CVRF, bit 3), and the Alert Function Flag (AFF, bit 4) in the Mask/Enable Register, the source of the alert can be determined. If the Conversion Ready feature is not desired and the CNVR bit is not set, the ALERT pin only responds to an exceeded alert limit based on the alert function enabled.

If the alert function is not used, the ALERT pin can be left floating without impacting the operation of the device.

Feature Description (接下页)

Refer to 图 23 to see the relative timing of when the value in the Alert Limit Register is compared to the corresponding converted value. For example, if the alert function that is enabled is Shunt Overcurrent-Limit (OCL), following every shunt current conversion the value in the Alert Limit Register is compared to the measured shunt voltage to determine if the measurements has exceeded the programmed limit. The AFF, bit 4 of the Mask/Enable Register, asserts high any time the measured voltage exceeds the value programmed into the Alert Limit Register. In addition to the AFF being asserted, the Alert pin is asserted based on the Alert Polarity Bit (APOL, bit 1 of the Mask/Enable Register). If the Alert Latch is enabled, the AFF and Alert pin remain asserted until either the Configuration Register (00h) is written to or the Mask/Enable Register is read.

The Bus Voltage alert functions compare the measured bus voltage to the Alert Limit Register following every bus voltage conversion and assert the AFF bit and ALERT pin if the limit threshold is exceeded.

The Power Over-Limit alert function is also compared to the calculated power value following every bus voltage measurement conversion and asserts the AFF bit and ALERT pin if the limit threshold is exceeded.

8.4 Device Functional Modes

8.4.1 Averaging and Conversion Time Considerations

The INA260 device offers programmable conversion times (t_{CT}) for both the shunt current and bus voltage measurements. The conversion times for these measurements can be selected from as fast as 140 μ s to as long as 8.244 ms. The conversion time settings, along with the programmable averaging mode, allow the device to be configured to optimize the available timing requirements in a given application. For example, if a system requires that data be read every 5 ms, the device could be configured with the conversion times set to 588 μ s for both shunt and bus voltage measurements and the averaging mode set to 4. This configuration results in the data updating approximately every 4.7 ms. The device could also be configured with a different conversion time setting for the shunt and bus voltage measurements. This type of approach is common in applications where the bus voltage tends to be relatively stable. This situation allows reduced time focused on the bus voltage measurement relative to the shunt voltage measurement. The shunt voltage conversion time could be set to 4.156 ms with the bus voltage conversion time set to 588 μ s and with the averaging mode set to 1. This configuration also results in data updating approximately every 4.7 ms.

There are trade-offs associated with the settings for conversion time and the averaging mode used. The averaging feature can significantly improve the measurement accuracy by effectively filtering the signal. This approach allows the device to reduce any noise in the measurement that may be caused by noise coupling into the signal. A greater number of averages enables the device to be more effective in reducing the noise component of the measurement.

The conversion times selected can also have an impact on the measurement accuracy. 图 24 shows multiple conversion times to illustrate the impact of noise on the measurement. To achieve the highest accuracy measurement possible, use a combination of the longest allowable conversion times and highest number of averages, based on the timing requirements of the system.

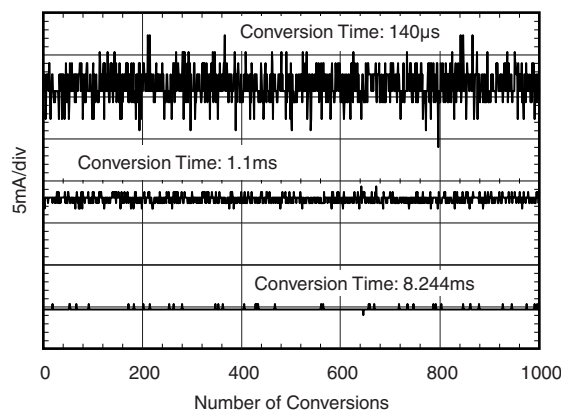


图 24. Noise vs Conversion Time

8.5 Programming

8.5.1 Calculating Returned Values

The LSB size for the Bus Voltage Register (02h), Current Register, and Power Register are fixed and are shown in 表 1. To calculate any of the values for current, voltage or power take the decimal value returned by the device and multiply that value by the LSB size. For example, the LSB for the bus voltage is 1.25 mV/bit, if the device returns a decimal value of 9584 (2570h), the value of the bus voltage is calculated to be $1.25 \text{ mV} \times 9584 = 11.98 \text{ V}$. Because the INA260 supports current measurements in either direction, the returned value for negative currents (currents flowing from IN- to IN+) is represented in two's complement format. Returned values for power will always be positive even when the current is negative.

表 1. Calculating Current and Power⁽¹⁾

| REGISTER NAME | ADDRESS | CONTENTS | DEC | LSB | VALUE |
|----------------------|---------|----------|-------|---------|----------|
| Current Register | 01h | 2710h | 10000 | 1.25 mA | 12.5 A |
| Bus Voltage Register | 02h | 2570h | 9584 | 1.25 mV | 11.98 V |
| Power Register | 03h | 3A7Fh | 14975 | 10 mW | 149.75 W |

(1) Conditions: Load = 12.5 A, $V_{CM} = 11.98 \text{ V}$.

8.5.2 Default Settings

The default power-up states of the registers are shown in the [Register Maps](#) section of this data sheet. These registers are volatile, and if programmed to a value other than the default values shown in 表 4, they must be re-programmed at every device power-up.

8.5.3 Communications Bus Overview

The INA260 offers compatibility with both I²C and SMBus interfaces. The I²C and SMBus protocols are essentially compatible with one another.

The I²C interface is used throughout this data sheet as the primary example, with SMBus protocol specified only when a difference between the two systems is discussed. Two lines, SCL and SDA, connect the device to the bus. Both SCL and SDA connect to the bus and require external pullup resistors.

The device that initiates a data transfer is called a *master*, and the devices controlled by the master are *slaves*. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates START and STOP conditions. The SCL pin on the INA260 is an input only and will not stretch the clock by holding the clock line low.

To address a specific device, the master initiates a start condition by pulling the data signal line (SDA) from a high to a low logic level while SCL is high. All slaves on the bus shift in the slave address byte on the rising edge of SCL, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA low.

Data transfer is then initiated and eight bits of data are sent, followed by an *Acknowledge* bit. During data transfer, SDA must remain stable while SCL is high. Any change in SDA while SCL is high is interpreted as a start or stop condition.

After all data have been transferred, the master generates a stop condition, indicated by pulling SDA from low to high while SCL is high. The device includes a 28-ms timeout on its interface to prevent locking up the bus.

8.5.3.1 Serial Bus Address

To communicate with the device, the master must first address the INA260 through a slave address byte. The slave address byte consists of seven address bits and a direction bit that indicates whether the action is to be a read or write operation.

The device has two address pins, A0 and A1 that can be connected to GND, VS, SCL or SDA to set the desired address. 表 2 lists the pin connections for each of the 16 possible addresses. The device samples the state of pins A0 and A1 on every bus communication in order to establish the pin states before any activity on the interface occurs.

表 2. Address Pins and Slave Addresses

| A1 | A0 | SLAVE ADDRESS |
|-----|-----|---------------|
| GND | GND | 1000000 |
| GND | VS | 1000001 |
| GND | SDA | 1000010 |
| GND | SCL | 1000011 |
| VS | GND | 1000100 |
| VS | VS | 1000101 |
| VS | SDA | 1000110 |
| VS | SCL | 1000111 |
| SDA | GND | 1001000 |
| SDA | VS | 1001001 |
| SDA | SDA | 1001010 |
| SDA | SCL | 1001011 |
| SCL | GND | 1001100 |
| SCL | VS | 1001101 |
| SCL | SDA | 1001110 |
| SCL | SCL | 1001111 |

8.5.3.2 Serial Interface

The INA260 operates only as a slave device on both the I²C bus and the SMBus. Connections to the bus are made through the open-drain SDA and SCL lines. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. Although the device integrates spike suppression into the digital I/O lines, proper layout techniques help minimize the amount of coupling into the communication lines. This noise introduction could occur from capacitively coupling signal edges between the two communication lines themselves or from other switching noise sources present in the system. Routing traces in parallel with ground in between layers on a PCB typically reduces the effects of coupling between the communication lines. Shielded communication lines reduces the possibility of unintended noise coupling into the digital I/O lines that could be incorrectly interpreted as start or stop commands.

The INA260 supports the transmission protocol for fast mode (1 kHz to 400 kHz) and high-speed mode (1 kHz to 2.94 MHz). All data bytes are transmitted most significant byte first.

8.5.3.3 Writing to and Reading From the INA260

Accessing a specific register on the INA260 is accomplished by writing the appropriate value to the register pointer. See 表 4 for a complete list of registers and corresponding addresses. The value for the register pointer (as shown in 图 28) is the first byte transferred after the slave address byte with the R/W bit low. Every write operation to the device requires a value for the register pointer.

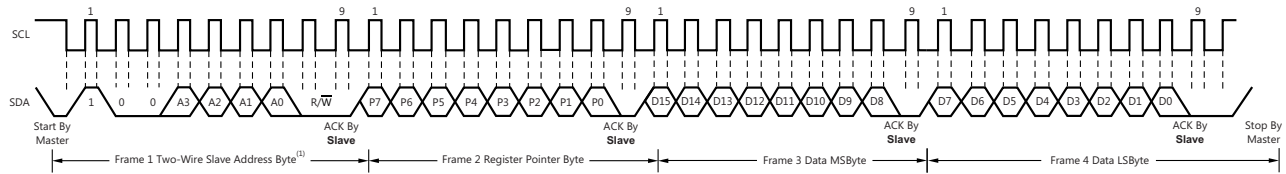
Writing to a register begins with the first byte transmitted by the master. This byte is the slave address, with the R/W bit low. The device then acknowledges receipt of a valid address. The next byte transmitted by the master is the address of the register which data is written to. This register address value updates the register pointer to the desired register. The next two bytes are written to the register addressed by the register pointer. The device acknowledges receipt of each data byte. The master may terminate data transfer by generating a start or stop condition.

When reading from the device, the last value stored in the register pointer by a write operation determines which register is read during a read operation. To change the register pointer for a read operation, a new value must be written to the register pointer. This write is accomplished by issuing a slave address byte with the R/W bit low, followed by the register pointer byte. No additional data are required. The master then generates a start condition and sends the slave address byte with the R/W bit high to initiate the read command. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the register pointer. This byte is followed by an *Acknowledge* from the master; then the slave transmits the least significant byte. The master acknowledges receipt of the data byte. The master may terminate data transfer by generating a *Not-Acknowledge* after receiving any data byte, or generating a start or stop condition. If repeated reads from the same register are desired, it is not necessary to continually send the register pointer bytes; the device retains the register pointer value until it is changed by the next write operation.

图 25 shows the write operation timing diagram. 图 26 shows the read operation timing diagram.

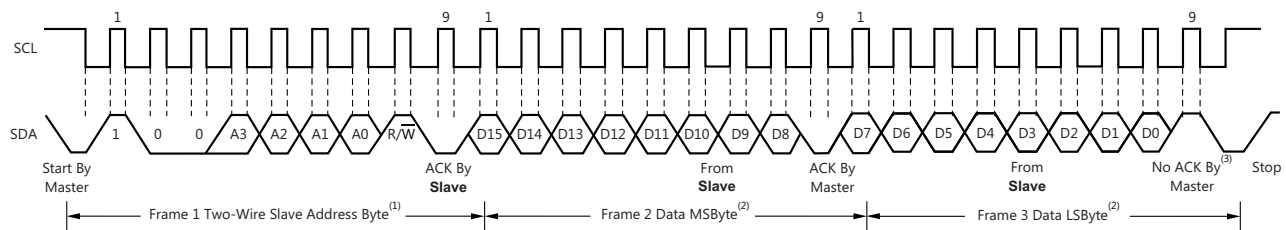
注

Register bytes are sent most-significant byte first, followed by the least significant byte.



- (1) The value of the Slave Address byte is determined by the settings of the A0 and A1 pins. See 表 2.

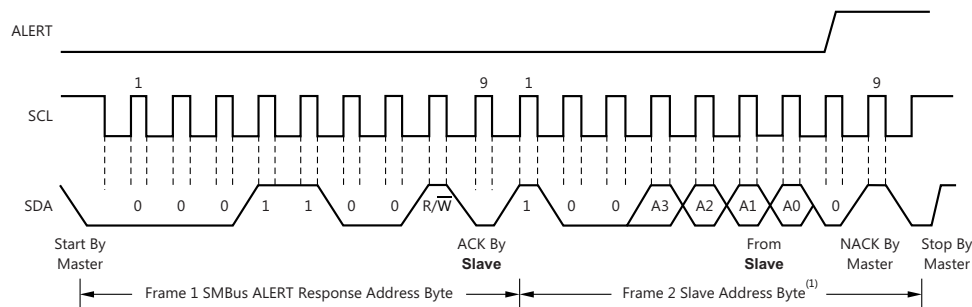
图 25. Timing Diagram for Write Word Format



- (1) The value of the Slave Address byte is determined by the settings of the A0 and A1 pins. See 表 2.
(2) Read data is from the last register pointer location. If a new register is desired, the register pointer must be updated. See 图 28.
(3) ACK by Master can also be sent.

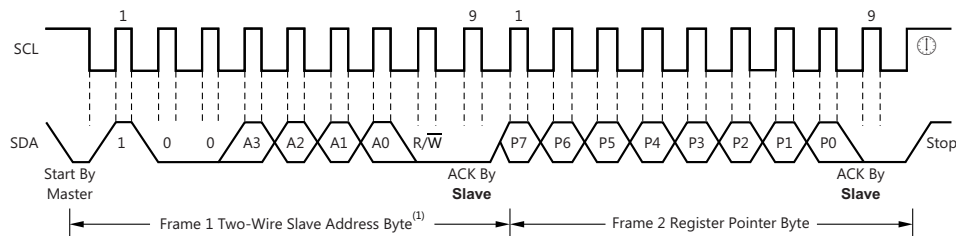
图 26. Timing Diagram for Read Word Format

图 27 provides a timing diagram for the SMBus Alert response operation. 图 28 illustrates a typical register pointer configuration.



- (1) The value of the Slave Address Byte is determined by the settings of the A0 and A1 pins. See 表 2.

图 27. Timing Diagram for SMBus ALERT Response



- (1) The value of the Slave Address Byte is determined by the settings of the A0 and A1 pins. See 表 2.

图 28. Typical Register Pointer Set

8.5.3.3.1 High-Speed I²C Mode

To initiate high-speed mode operation, the master generates a start condition followed by a valid serial byte containing high-speed (HS) master code 00001XXX. This transmission is made in fast (400 kHz) or standard (100 kHz) (F/S) mode at no more than 400 kHz. When the INA260 receives the high-speed code it does not send an acknowledgement but does change the internal logic deglitch filters to support high-speed operation.

The master then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S mode, except that transmission speeds up to 2.94 MHz are allowed. Instead of using a stop condition, use repeated start conditions to secure the bus in HS-mode. A stop condition ends the HS-mode and switches all the internal filters of the device to support the F/S mode. See 图 29 and 表 3 for relevant fast mode and high-speed mode timing requirements.

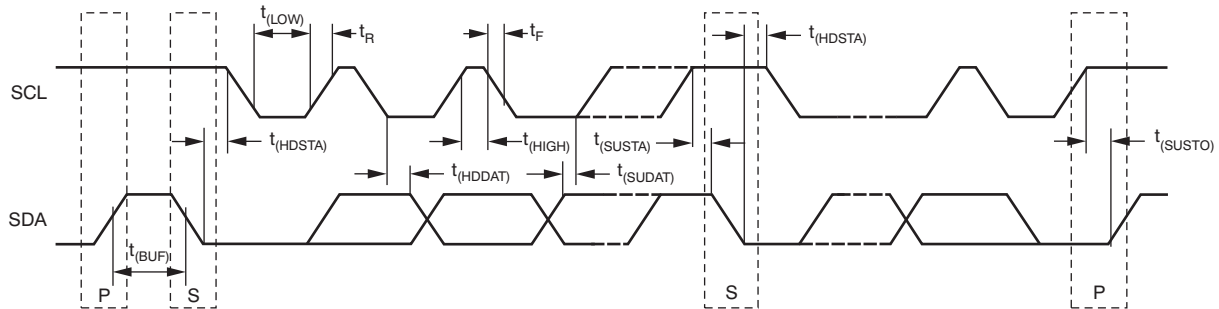


图 29. Bus Timing Diagram

表 3. Bus Timing Diagram Definitions⁽¹⁾

| PARAMETER | | FAST MODE | | HIGH-SPEED MODE | | UNIT |
|--|---------------|-----------|------|-----------------|------|------|
| | | MIN | MAX | MIN | MAX | |
| SCL operating frequency | $f_{(SCL)}$ | 0.001 | 0.4 | 0.001 | 2.94 | MHz |
| Bus free time between stop and start conditions | $t_{(BUF)}$ | 600 | | 160 | | ns |
| Hold time after repeated START condition. After this period, the first clock is generated. | $t_{(HDSTA)}$ | 100 | | 100 | | ns |
| Repeated start condition setup time | $t_{(SUSTA)}$ | 100 | | 100 | | ns |
| STOP condition setup time | $t_{(SUSTO)}$ | 100 | | 100 | | ns |
| Data hold time | $t_{(HDDAT)}$ | 10 | 900 | 10 | 100 | ns |
| Data setup time | $t_{(SUDAT)}$ | 100 | | 20 | | ns |
| SCL clock low period | $t_{(LOW)}$ | 1300 | | 200 | | ns |
| SCL clock high period | $t_{(HIGH)}$ | 600 | | 60 | | ns |
| Data fall time | t_F | | 300 | | 80 | ns |
| Clock fall time | t_F | | 300 | | 40 | ns |
| Clock rise time | t_R | | 300 | | 40 | ns |
| Clock/data rise time for $SCLK \leq 100kHz$ | t_R | | 1000 | | — | ns |

(1) Values based on a statistical analysis of a one-time sample of devices. Minimum and maximum values are specified by design, but not production tested.

8.5.3.4 SMBus Alert Response

When SMBus Alerts are latched, the INA260 is designed to respond to the SMBus Alert Response address. The SMBus Alert Response provides a quick fault identification for simple slave devices. When an Alert occurs, the master can broadcast the Alert Response slave address (0001 100) with the Read/Write bit set high. Following this Alert Response, any slave device that generates an alert identifies itself by acknowledging the Alert Response and sending its address on the bus.

The Alert Response can activate several different slave devices simultaneously, similar to the I²C General Call. If more than one slave attempts to respond, bus arbitration rules apply and the device with the lowest address will win and be serviced first. The losing devices do not generate an Acknowledge and continues to hold the Alert line low until the interrupt is cleared. The winning device responds with its address and releases the SMBus alert line. Even though the INA260 releases the SMBus line the internal error flags are not cleared until done so by the host.

8.6 Register Maps

The INA260 uses a bank of registers for holding configuration settings, measurement results, minimum/maximum limits, and status information. 表 4 summarizes the device registers; see the [Functional Block Diagram](#) section for an illustration of the registers.

表 4. Register Set Summary

| POINTER ADDRESS | REGISTER NAME | FUNCTION | POWER-ON RESET | | TYPE ⁽¹⁾ |
|-----------------|--------------------------|---|-------------------|------|---------------------|
| | | | BINARY | HEX | |
| 00h | Configuration Register | All-register reset, shunt voltage and bus voltage ADC conversion times and averaging, operating mode. | 01100001 00100111 | 6127 | R/ \overline{W} |
| 01h | Current Register | Contains the value of the current flowing through the shunt resistor. | 00000000 00000000 | 0000 | R |
| 02h | Bus Voltage Register | Bus voltage measurement data. | 00000000 00000000 | 0000 | R |
| 03h | Power Register | Contains the value of the calculated power being delivered to the load. | 00000000 00000000 | 0000 | R |
| 06h | Mask/Enable Register | Alert configuration and Conversion Ready flag. | 00000000 00000000 | 0000 | R/ \overline{W} |
| 07h | Alert Limit Register | Contains the limit value to compare to the selected Alert function. | 00000000 00000000 | 0000 | R/ \overline{W} |
| FEh | Manufacturer ID Register | Contains unique manufacturer identification number. | 0101010001001001 | 5449 | R |
| FFh | Die ID Register | Contains unique die identification number. | 0010001001110000 | 2270 | R |

(1) Type: R = Read-Only, R/ \overline{W} = Read/Write.

8.6.1 Configuration Register (00h) (Read/Write)

The Configuration Register settings control the operating modes for the device. This register controls the conversion time settings for both shunt current and bus voltage measurements as well as the averaging mode used. The operating mode that controls what signals are selected to be measured is also programmed in the Configuration Register.

The Configuration Register can be read from at any time without impacting or affecting the device settings or a conversion in progress. Writing to the Configuration Register halts any conversion in progress until the write sequence is completed resulting in a new conversion starting based on the new contents of the Configuration Register (00h). This halt prevents any uncertainty in the conditions used for the next completed conversion.

图 30. Configuration Register (00h) (Read/Write)

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---------|---------|--------|--------|--------|-------|-------|---------|
| RST | — | — | — | AVG2 | AVG1 | AVG0 | VBUSCT2 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| R/W | R | | | R/W | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VBUSCT1 | VBUSCT0 | ISHCT2 | ISHCT1 | ISHCT0 | MODE3 | MODE2 | MODE1 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 |
| R/W | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 5. Configuration Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------|------|-------|---|
| 15 | RST | R/W | 0 | Reset Bit Setting this bit to '1' generates a system reset that is the same as power-on reset. Resets all registers to default values; this bit self-clears. |
| 14–12 | — | R | 110 | |
| 11–9 | AVG | R/W | 000 | Averaging Mode Determines the number of samples that are collected and averaged. The following shows all the AVG bit settings and related number of averages for each bit setting. AVG2 = 0, AVG1 = 0, AVG0 = 0, number of averages = 1 ⁽¹⁾ AVG2 = 0, AVG1 = 0, AVG0 = 1, number of averages = 4 AVG2 = 0, AVG1 = 1, AVG0 = 0, number of averages = 16 AVG2 = 0, AVG1 = 1, AVG0 = 1, number of averages = 64 AVG2 = 1, AVG1 = 0, AVG0 = 0, number of averages = 128 AVG2 = 1, AVG1 = 0, AVG0 = 1, number of averages = 256 AVG2 = 1, AVG1 = 1, AVG0 = 0, number of averages = 512 AVG2 = 1, AVG1 = 1, AVG0 = 1, number of averages = 1024 |
| 8–6 | VBUSCT | R/W | 100 | Bus Voltage Conversion Time Sets the conversion time for the bus voltage measurement. The following shows the VBUSCT bit options and related conversion times for each bit setting. VBUSCT2 = 0, VBUSCT1 = 0, VBUSCT0 = 0, conversion time = 140 μ s VBUSCT2 = 0, VBUSCT1 = 0, VBUSCT0 = 1, conversion time = 204 μ s VBUSCT2 = 0, VBUSCT1 = 1, VBUSCT0 = 0, conversion time = 332 μ s VBUSCT2 = 0, VBUSCT1 = 1, VBUSCT0 = 1, conversion time = 588 μ s VBUSCT2 = 1, VBUSCT1 = 0, VBUSCT0 = 0, conversion time = 1.1 ms ⁽¹⁾ VBUSCT2 = 1, VBUSCT1 = 0, VBUSCT0 = 1, conversion time = 2.116 ms VBUSCT2 = 1, VBUSCT1 = 1, VBUSCT0 = 0, conversion time = 4.156 ms VBUSCT2 = 1, VBUSCT1 = 1, VBUSCT0 = 1, conversion time = 8.244 ms |
| 5–3 | ISHCT | R/W | 100 | Shunt Current Conversion Time The following shows the ISHCT bit options and related conversion times for each bit setting. ISHCT2 = 0, ISHCT1 = 0, ISHCT0 = 0, conversion time = 140 μ s ISHCT2 = 0, ISHCT1 = 0, ISHCT0 = 1, conversion time = 204 μ s ISHCT2 = 0, ISHCT1 = 1, ISHCT0 = 0, conversion time = 332 μ s ISHCT2 = 0, ISHCT1 = 1, ISHCT0 = 1, conversion time = 588 μ s ISHCT2 = 1, ISHCT1 = 0, ISHCT0 = 0, conversion time = 1.1 ms ⁽¹⁾ ISHCT2 = 1, ISHCT1 = 0, ISHCT0 = 1, conversion time = 2.116 ms ISHCT2 = 1, ISHCT1 = 1, ISHCT0 = 0, conversion time = 4.156 ms ISHCT2 = 1, ISHCT1 = 1, ISHCT0 = 1, conversion time = 8.244 ms |
| 2–0 | MODE | R/W | 111 | Operating Mode Selects continuous, triggered, or power-down mode of operation. These bits default to continuous shunt and bus measurement mode. The following shows mode settings. MODE2 = 0, MODE1 = 0, MODE0 = 0, mode = Power-Down (or Shutdown) MODE2 = 0, MODE1 = 0, MODE0 = 1, mode = Shunt Current, Triggered MODE2 = 0, MODE1 = 1, MODE0 = 0, mode = Bus Voltage, Triggered MODE2 = 0, MODE1 = 1, MODE0 = 1, mode = Shunt Current and Bus Voltage, Triggered MODE2 = 1, MODE1 = 0, MODE0 = 0, mode = Power-Down (or Shutdown) MODE2 = 1, MODE1 = 0, MODE0 = 1, mode = Shunt Current, Continuous MODE2 = 1, MODE1 = 1, MODE0 = 0, mode = Bus Voltage, Continuous MODE2 = 1, MODE1 = 1, MODE0 = 1, mode = Shunt Current and Bus Voltage, Continuous ⁽¹⁾ |

(1) These values are default.

8.6.2 Current Register (01h) (Read-Only)

The value in the current register is represented in two's complement format to support negative current values. The LSB size for the current register is set to 1.25 mA. If averaging is enabled, this register will report the averaged value.

图 31. Current Register (01h) (Read-Only)

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------|------|------|------|------|------|-----|-----|
| CSIGN | CD14 | CD13 | CD12 | CD11 | CD10 | CD9 | CD8 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CD7 | CD6 | CD5 | CD4 | CD3 | CD2 | CD1 | CD0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

8.6.3 Bus Voltage Register (02h) (Read-Only)

The Bus Voltage Register stores the most recent bus voltage reading, VBUS.

If averaging is enabled, this register reports the averaged value.

Full-scale range = 40.96 V (decimal = 32767); LSB = 1.25 mV.

图 32. Bus Voltage Register (02h) (Read-Only)

| 15 ⁽¹⁾ | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------------------|------|------|------|------|------|-----|-----|
| — | BD14 | BD13 | BD12 | BD11 | BD10 | BD9 | BD8 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BD7 | BD6 | BD5 | BD4 | BD3 | BD2 | BD1 | BD0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

(1) Bit 15 is always zero because bus voltage can only be positive.

8.6.4 Power Register (03h) (Read-Only)

If averaging is enabled, this register reports the averaged value.

The Power Register LSB is fixed to 10 mW.

The Power Register records power in Watts by multiplying the decimal values of the Current Register with the decimal value of the Bus Voltage Register. Values stored in the power register will always be positive regardless of the direction of current flow. The maximum value that can be returned by the power register is A3D7h or 419.43 W.

图 33. Power Register (03h) (Read-Only)

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|------|------|------|------|------|-----|-----|
| PD15 | PD14 | PD13 | PD12 | PD11 | PD10 | PD9 | PD8 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

8.6.5 Mask/Enable Register (06h) (Read/Write)

The Mask/Enable Register selects the function that is enabled to control the ALERT pin as well as how that pin functions. If multiple functions are enabled, the highest significant bit position Alert Function (D15-D11) takes priority and responds to the Alert Limit Register.

图 34. Mask/Enable Register (06h) (Read/Write)

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----|-----|-----|-----|------|------|------|-----|
| OCL | UCL | BOL | BUL | POL | CNVR | — | — |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | | | | | | R | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| — | — | — | AFF | CVRF | OVF | APOL | LEN |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | | | | | | R/W | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 6. Mask/Enable Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|---|
| 15 | OCL | R/W | 0 | Over Current Limit Setting this bit high configures the ALERT pin to be asserted if the current measurement following a conversion exceeds the value programmed in the Alert Limit Register. |
| 14 | UCL | R/W | 0 | Under Current Limit Setting this bit high configures the ALERT pin to be asserted if the current measurement following a conversion drops below the value programmed in the Alert Limit Register. |
| 13 | BOL | R/W | 0 | Bus Voltage Over-Voltage Setting this bit high configures the ALERT pin to be asserted if the bus voltage measurement following a conversion exceeds the value programmed in the Alert Limit Register. |
| 12 | BUL | R/W | 0 | Bus Voltage Under-Voltage Setting this bit high configures the ALERT pin to be asserted if the bus voltage measurement following a conversion drops below the value programmed in the Alert Limit Register. |
| 11 | POL | R/W | 0 | Power Over-Limit Setting this bit high configures the ALERT pin to be asserted if the Power calculation made following a bus voltage measurement exceeds the value programmed in the Alert Limit Register. |
| 10 | CNVR | R/W | 0 | Conversion Ready Setting this bit high configures the ALERT pin to be asserted when the Conversion Ready Flag, Bit 3, is asserted indicating that the device is ready for the next conversion. |
| 9–5 | — | R | 00000 | Not used. |
| 4 | AFF | R | 0 | Alert Function Flag While only one Alert Function can be monitored at the ALERT pin at a time, the Conversion Ready can also be enabled to assert the ALERT pin. Reading the Alert Function Flag following an alert allows the user to determine if the Alert Function was the source of the Alert. When the Alert Latch Enable bit is set to Latch mode, the Alert Function Flag bit clears only when the Mask/Enable Register is read. When the Alert Latch Enable bit is set to Transparent mode, the Alert Function Flag bit is cleared following the next conversion that does not result in an Alert condition. |
| 3 | CVRF | R | 0 | Conversion Ready Although the device can be read at any time, and the data from the last conversion is available, the Conversion Ready Flag bit is provided to help coordinate one-shot or triggered conversions. The Conversion Ready Flag bit is set after all conversions, averaging, and multiplications are complete. Conversion Ready Flag bit clears under the following conditions: 1.) Writing to the Configuration Register (except for Power-Down selection) 2.) Reading the Mask/Enable Register |

表 6. Mask/Enable Register Field Descriptions (接下页)

| Bit | Field | Type | Reset | Description |
|-----|-------|------------------|-------|--|
| 2 | OVF | R | 0 | Math Overflow Flag This bit is set to '1' if an arithmetic operation resulted in an overflow error. It indicates that power data may have exceeded the maximum reportable value of 419.43 W. |
| 1 | APOL | R \overline{W} | 0 | Alert Polarity bit 1 = Inverted (active-high open collector) 0 = Normal (active-low open collector) (default) |
| 0 | LEN | R \overline{W} | 0 | Alert Latch Enable; configures the latching feature of the ALERT pin and Alert Flag bits. 1 = Latch enabled 0 = Transparent (default) When the Alert Latch Enable bit is set to Transparent mode, the ALERT pin and Flag bit resets to the idle states when the fault has been cleared. When the Alert Latch Enable bit is set to Latch mode, the ALERT pin and Alert Flag bit remains active following a fault until the Mask/Enable Register has been read. |

8.6.6 Alert Limit Register (07h) (Read/Write)

The Alert Limit Register contains the value used to compare to the register selected in the Mask/Enable Register to determine if a limit has been exceeded. The format for this register will match the format of the register that is selected for comparison.

图 35. Alert Limit Register (07h) (Read/Write)

| | | | | | | | |
|------------------|-------|-------|-------|-------|-------|------|------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| AUL15 | AUL14 | AUL13 | AUL12 | AUL11 | AUL10 | AUL9 | AUL8 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R \overline{W} | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AUL7 | AUL6 | AUL5 | AUL4 | AUL3 | AUL2 | AUL1 | AUL0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R \overline{W} | | | | | | | |

LEGEND: R \overline{W} = Read/Write; R = Read only; -n = value after reset

8.6.7 Manufacturer ID Register (FEh) (Read-Only)

The Manufacturer ID Register stores a unique identification number for the manufacturer.

图 36. Manufacturer ID Register (FEh) (Read-Only)

| | | | | | | | |
|------|------|------|------|------|------|-----|-----|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ID15 | ID14 | ID13 | ID12 | ID11 | ID10 | ID9 | ID8 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| R | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID7 | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| R | | | | | | | |

LEGEND: R \overline{W} = Read/Write; R = Read only; -n = value after reset

表 7. Manufacturer ID Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|--------------------|--|
| 15–0 | ID | R | 5449h / TI (ascii) | Manufacturer ID Stores the manufacturer identification bits |

8.6.8 Die ID Register (FFh) (Read-Only)

The Die ID Register stores a unique identification number and the revision ID for the die.

图 37. Die ID Register (FFh) (Read-Only)

| | | | | | | | |
|-------|-------|------|------|------|------|------|------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DID11 | DID10 | DID9 | DID8 | DID7 | DID6 | DID5 | DID4 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| R | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DID3 | DID2 | DID1 | DID0 | RID3 | RID2 | RID1 | RID0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| R | | | | | | | |

LEGEND: $\overline{R/\overline{W}}$ = Read/Write; R = Read only; -n = value after reset

表 8. Die ID Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|--|
| 15–4 | DID | R | 227h | Device ID Stores the device identification bits. |
| 3–0 | RID | R | 0h | Die Revision ID Stores the device revision identification bits. |

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Validate and test the design implementation to confirm system functionality.

9.1 Application Information

The INA260 is a current shunt and power monitor with an I²C-compatible interface. The device monitors both a shunt current and bus supply voltage. The internally calibrated integrated current sense resistor combined with an internal multiplier, enable direct readouts of current in amperes and power in watts.

9.2 Typical Application

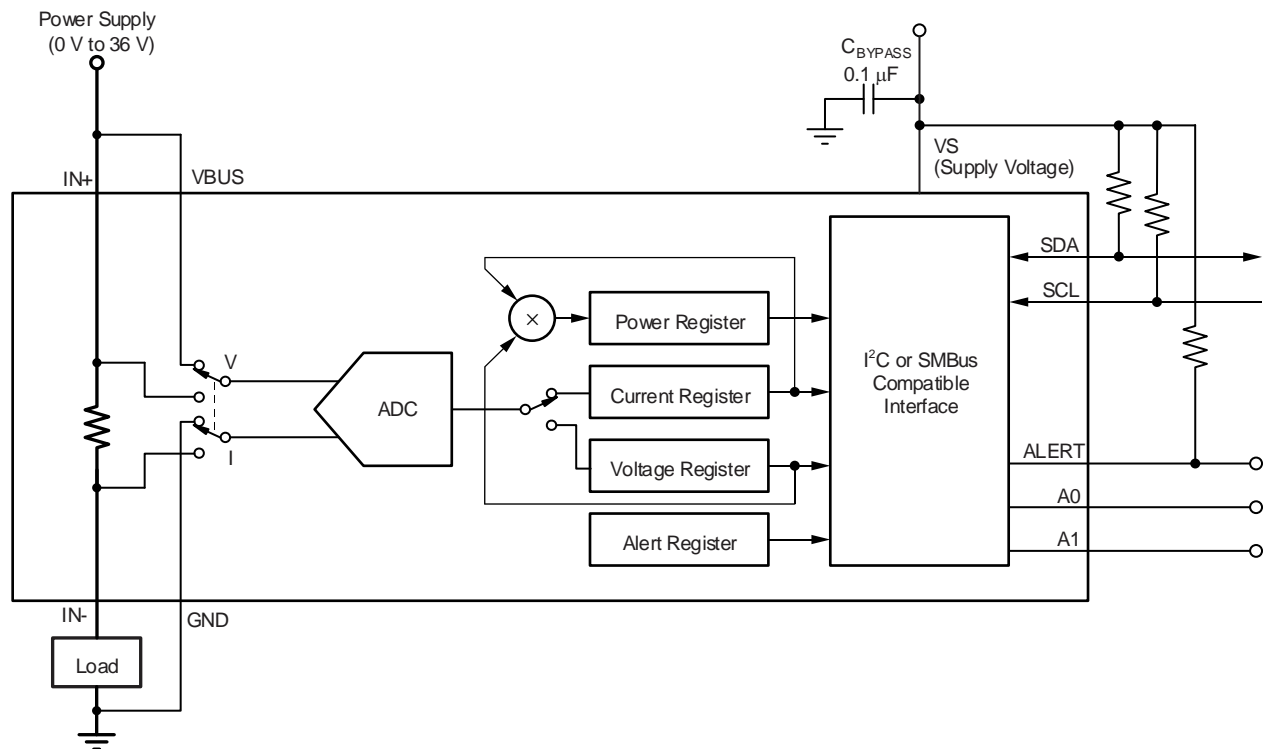


图 38. Typical Circuit Configuration, INA260

9.2.1 Design Requirements

The INA260 measures current and the bus supply voltage and calculates power. It comes with alert capability where the ALERT pin can be programmed to respond to a user-defined event or to a conversion ready notification. This design illustrates the ability of the ALERT pin to respond to a set threshold.

Typical Application (接下页)

9.2.2 Detailed Design Procedure

The ALERT pin can be configured to respond to one of the five alert functions described in the [ALERT Pin](#) section. The ALERT pin must be pulled up to the VS pin voltage through an external pullup resistor. The configuration register is set based on the required conversion time and averaging. The Mask/Enable Register is set to identify the required alert function and the Alert Limit Register is set to the limit value used for comparison.

9.2.3 Application Curves

图 40 shows the ALERT pin response to a bus over voltage limit of 5.5 V for a conversion time (t_{CT}) of 1.1 ms and averaging set to 1. 图 39 shows the response for the same limit but with the conversion time reduced to 140 μ s. For the scope shots shown in these figures, persistence was enabled on the ALERT channel. This shows how the ALERT response time can vary depending on when the fault condition occurs relative to the internal ADC clock of the INA260. For fault conditions that are just exceeding the limit threshold the response time for the ALERT pin can vary from 1 to 2 conversion cycles. As mentioned, the variation is due to the timing on when the fault event occurs relative to the start time of the internal ADC conversion cycle. For fault events that greatly exceed the limit threshold it is possible for the alert to respond in less than one conversion cycle. This is because it takes fewer samples for the average to exceed the limit threshold value.

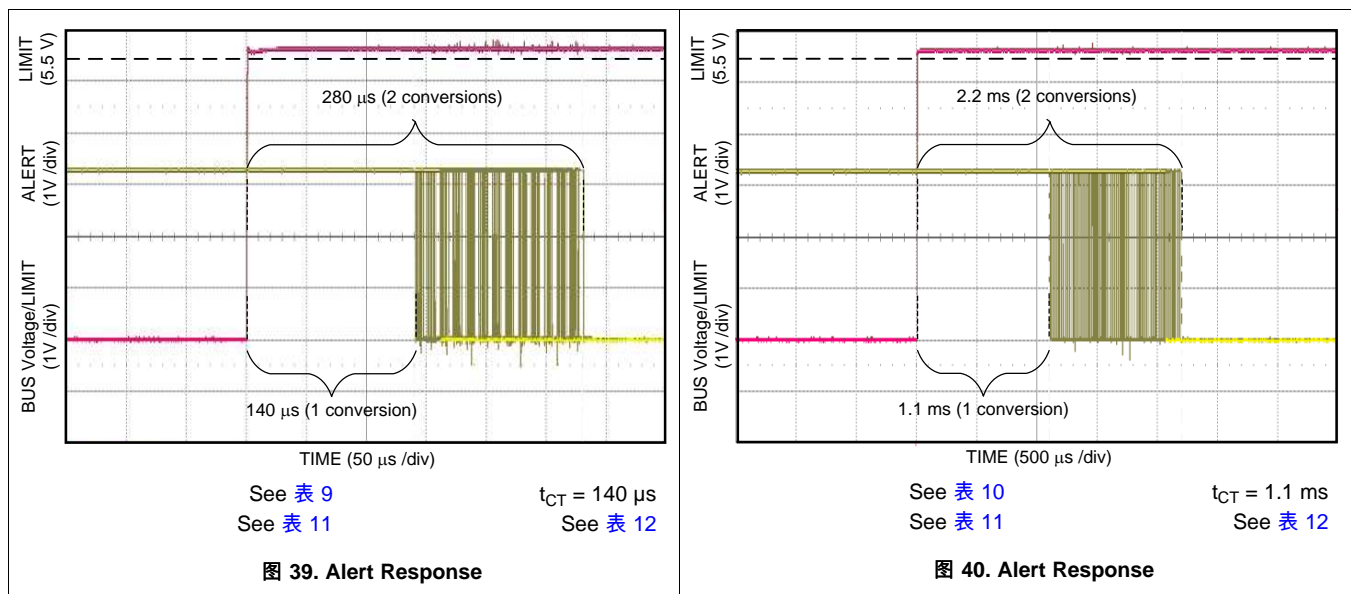


表 9. Configuration Register (00h) Settings for 图 39 (Value = 6006h)

| BIT # | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|-----|----|----|----|------|------|------|----------|----------|----------|--------|--------|--------|-------|-------|-------|
| BIT NAME | RST | — | — | — | AVG2 | AVG1 | AVG0 | VBUSC T2 | VBUSC T1 | VBUSC T0 | ISHCT2 | ISHCT1 | ISHCT0 | MODE3 | MODE2 | MODE1 |
| POR VALUE | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

表 10. Configuration Register (00h) Settings for 图 40 (Value = 6126h)

| BIT # | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|-----|----|----|----|------|------|------|----------|----------|----------|--------|--------|--------|-------|-------|-------|
| BIT NAME | RST | — | — | — | AVG2 | AVG1 | AVG0 | VBUSC T2 | VBUSC T1 | VBUSC T0 | ISHCT2 | ISHCT1 | ISHCT0 | MODE3 | MODE2 | MODE1 |
| POR VALUE | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |

表 11. Mask/Enable Register (06h) Settings for 图 39 and 图 40 (Value = 2008h)

| BIT # | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|-----|-----|-----|-----|-----|------|---|---|---|---|---|-----|------|-----|------|-----|
| BIT NAME | OCL | UCL | BOL | BUL | POL | CNVR | — | — | — | — | — | AFF | CVRF | OVF | APOL | LEN |
| POR VALUE | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

表 12. Alert Limit Register (07h) Settings for 图 39 and 图 40 (Value = 1130h)

| BIT # | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|
| BIT NAME | AUL15 | AUL14 | AUL13 | AUL12 | AUL11 | AUL10 | AUL9 | AUL8 | AUL7 | AUL6 | AUL5 | AUL4 | AUL3 | AUL2 | AUL1 | AUL0 |
| POR VALUE | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

10 Power Supply Recommendations

The input circuitry of the device can accurately measure signals on common-mode voltages beyond its power supply voltage, V_{VS} . For example, the voltage applied to the power supply terminal (VS) can be 5 V, whereas the load power-supply voltage being monitored (the common-mode voltage) can be as high as 36 V. Note also that the device can withstand the full 0-V to 36-V range at the input terminals, regardless of whether the device has power applied or not.

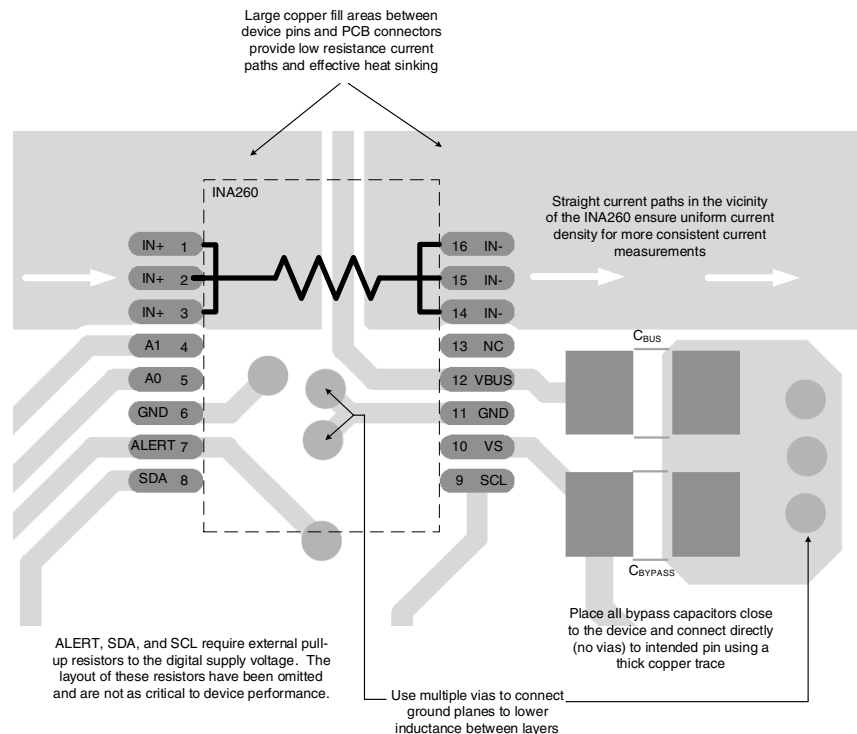
Place the required power-supply bypass capacitors as close as possible to the supply and ground terminals of the device. A typical value for this supply bypass capacitor is 0.1 μ F. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise.

11 Layout

11.1 Layout Guidelines

Connections to the internal shunt resistor should be connected directly into and out of the shunt resistor pins to encourage uniform current flow through the device. The trace width should be sized correctly to handle the desired current flow. Place the power-supply bypass capacitor as close as possible to the supply and ground pins. Use of multiple vias to connect the device ground to the bypass capacitor grounds is recommended if there is not direct connection on the top layer.

11.2 Layout Example



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NOTE: Connect the VBUS pin to the power supply rail.

图 41. INA260 Layout Example

12 器件和文档支持

12.1 器件支持

12.1.1 Third-Party Products Disclaimer

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12.2 文档支持

12.2.1 相关文档

相关文档请参见以下部分：

《[INA260EVM 评估板和软件教程](#)》用户指南（文献编号：SBOU113）

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| INA260AIPW | Last Time Buy | Production | TSSOP (PW) 16 | 90 TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | I260AI |
| INA260AIPWR | Active | Production | TSSOP (PW) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | I260AI |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| INA260AIPWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

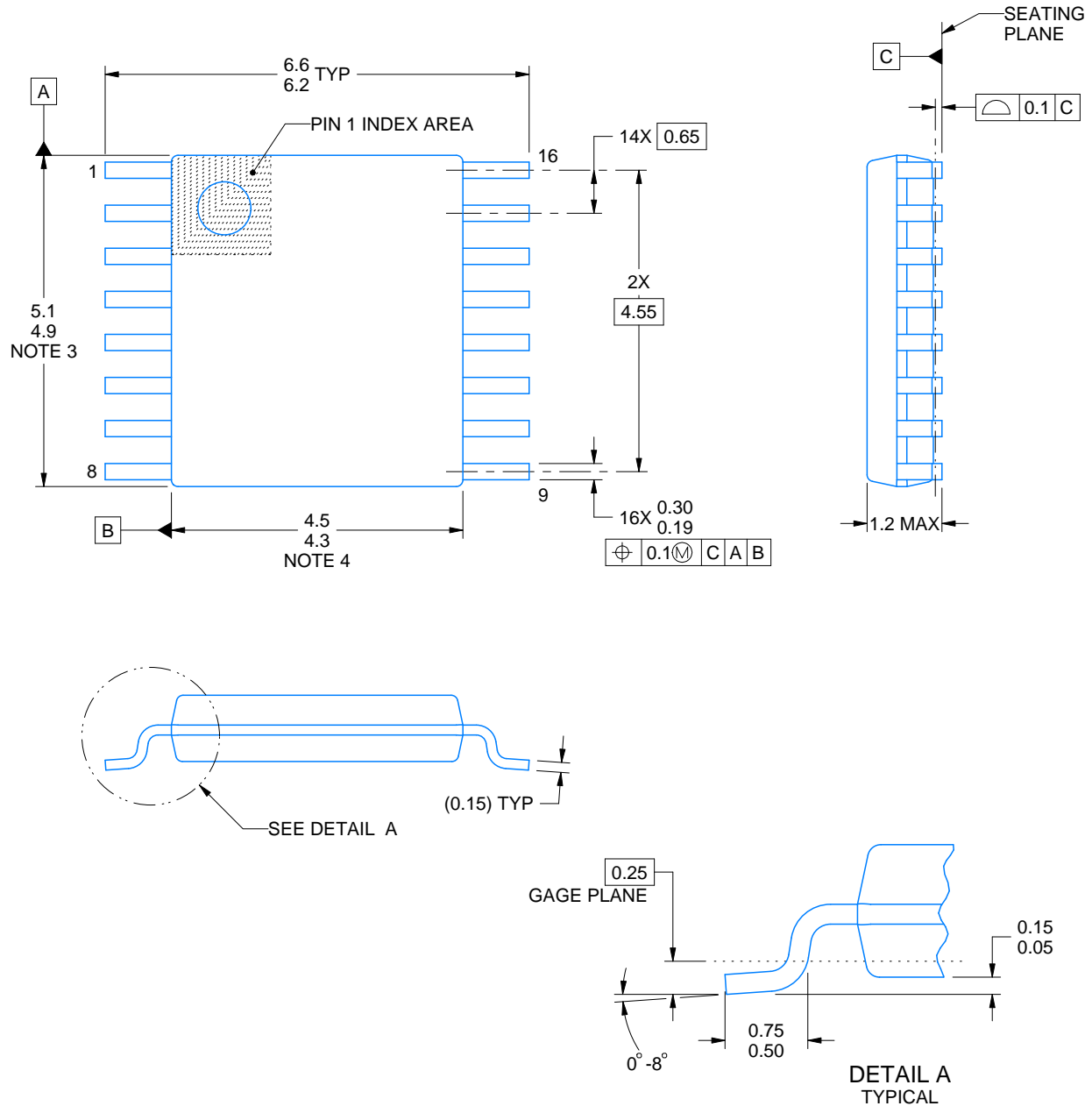
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| INA260AIPWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |

TUBE



*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| INA260AIPW | PW | TSSOP | 16 | 90 | 530 | 10.2 | 3600 | 3.5 |



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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