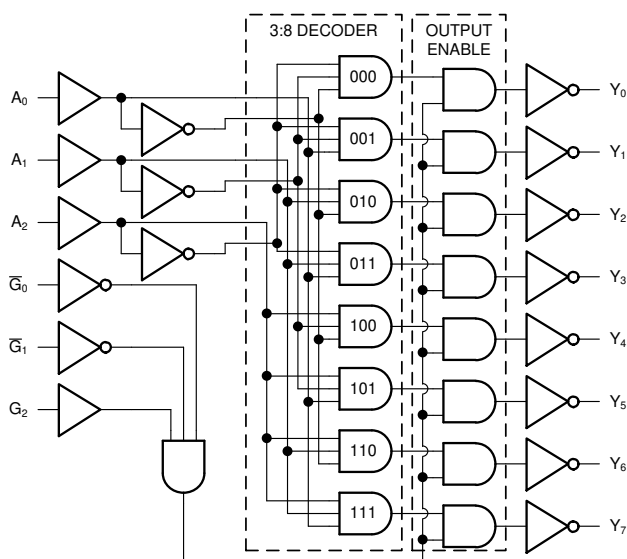


# CDx4HC138、CDx4HCT138、CDx4HC238、CDx4HCT238 高速 CMOS 逻辑 3 线至 8 线解码器/多路解复用器（反向和同向）

## 1 特性

- 选择一个数据输出（共八个）：
  - 针对 '138 的低电平有效
  - 针对 '238 的高电平有效
- I/O 端口或存储器选择器
- 三个使能输入以简化级联
- 当  $V_{CC} = 5V$ ,  $C_L = 15pF$ ,  $T_A = 25^\circ C$  时的传播延迟典型值为 13ns
- 扇出（在温度范围内）
  - 总线驱动器输出：15 个 LSTTL 负载
  - 标准输出：10 个 LSTTL 负载
- 宽工作温度范围： $-55^\circ C$  至  $125^\circ C$
- 平衡的传播延迟及转换时间
- 与 LSTTL 逻辑 IC 相比，可显著降低功耗
- HC 类型
  - 工作电压为 2V 至 6V
  - 高抗噪性：当  $V_{CC} = 5V$  时， $N_{IL} = 30\%$ ,  $N_{IH} = V_{CC}$  的 30%
- HCT 类型
  - 4.5V 至 5.5V 工作电压
  - 直接 LSTTL 输入逻辑兼容性， $V_{IL} = 0.8V$ （最大值）， $V_{IH} = 2V$ （最小值）
  - CMOS 输入兼容性，当电压为  $V_{OL}$ 、 $V_{OH}$  时， $I_i \leq 1\mu A$



功能框图 '138

## 2 说明

CDx4HC(T)138 和 '238 是 3 线至 8 线解码器，具有一个标准输出选通 ( $G_2$ ) 和两个低电平有效的输出选通 ( $\overline{G}_1$  和  $\overline{G}_0$ )。当输出受到任何选通输入控制时，这些输出全都强制进入高电平状态。当选通输入未禁用输出时，只有选定输出为低电平，而所有其他输出为高电平。

CDx4HC(T)238 是 3 线至 8 线解码器，具有一个标准输出选通 ( $G_2$ ) 和两个低电平有效的输出选通 ( $\overline{G}_1$  和  $\overline{G}_0$ )。当输出受到任何选通输入控制时，这些输出全都强制进入低电平状态。当选通输入未禁用输出时，只有选定输出为高电平，而所有其他输出为低电平。

### 器件信息

| 器件型号         | 封装 <sup>(1)</sup>    | 封装尺寸 (标称值)       |
|--------------|----------------------|------------------|
| CD74HC138E   | PDIP (16)            | 25.40mm × 6.35mm |
| CD74HCT138E  | PDIP (16)            | 25.40mm × 6.35mm |
| CD74HCT238E  | PDIP (16)            | 25.40mm × 6.35mm |
| CD74HC138M   | SOIC (16)            | 9.90mm × 3.90mm  |
| CD74HCT238M  | SOIC (16)            | 9.90mm × 3.90mm  |
| CD74HC238NS  | SO (16)              | 10.20mm × 5.30mm |
| CD74HC238PW  | TSSOP (16)           | 5.00mm × 4.40mm  |
| CD74HCT238PW | TSSOP (16)           | 5.00mm × 4.40mm  |
| CD54HC138F   | 陶瓷双列直插封装 (CDIP) (16) | 21.34mm × 6.92mm |
| CD54HCT138F  | 陶瓷双列直插封装 (CDIP) (16) | 21.34mm × 6.92mm |
| CD54HCT238F  | 陶瓷双列直插封装 (CDIP) (16) | 21.34mm × 6.92mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



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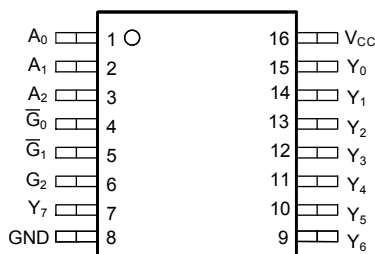
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## 3 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision I (August 2004) to Revision J (November 2021)                                                                    | Page |
|----------------------------------------------------------------------------------------------------------------------------------------|------|
| • 更新了整个文档中的编号、格式、表格、图和交叉参考，以反映现代数据表标准.....                                                                                             | 1    |
| • 更新了引脚名称，以符合现行的 TI 命名约定 E <sub>3</sub> 现在是 G <sub>2</sub> ，E <sub>2</sub> 现在是 G <sub>1</sub> ，E <sub>1</sub> 现在是 G <sub>0</sub> ..... | 1    |

## 4 Pin Configuration and Functions



**J, N, D, NS, or PW package**  
**16-Pin CDIP, PDIP, SOIC, SO, or TSSOP**  
**Top View**

### Pin Functions

| PIN               |                  | I/O <sup>(1)</sup> | DESCRIPTION                 |
|-------------------|------------------|--------------------|-----------------------------|
| SOIC or TSSOP NO. | NAME             |                    |                             |
| 1                 | A <sub>0</sub>   | I                  | Address select 0            |
| 2                 | A <sub>1</sub>   | I                  | Address select 1            |
| 3                 | A <sub>2</sub>   | I                  | Address select 2            |
| 4                 | $\overline{G}_0$ | I                  | Output strobe 0, active low |
| 5                 | $\overline{G}_1$ | I                  | Output strobe 1, active low |
| 6                 | G <sub>2</sub>   | I                  | Output strobe 2             |
| 7                 | Y <sub>7</sub>   | O                  | Output 7                    |
| 8                 | GND              | —                  | Ground                      |
| 9                 | Y <sub>6</sub>   | O                  | Output 6                    |
| 10                | Y <sub>5</sub>   | O                  | Output 5                    |
| 11                | Y <sub>4</sub>   | O                  | Output 4                    |
| 12                | Y <sub>3</sub>   | O                  | Output 3                    |
| 13                | Y <sub>2</sub>   | O                  | Output 2                    |
| 14                | Y <sub>1</sub>   | O                  | Output 1                    |
| 15                | Y <sub>0</sub>   | O                  | Output 0                    |
| 16                | V <sub>CC</sub>  | —                  | Positive supply             |

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|           |                                                          |                                            | MIN  | MAX      | UNIT |
|-----------|----------------------------------------------------------|--------------------------------------------|------|----------|------|
| $V_{CC}$  | Supply voltage                                           |                                            | -0.5 | 7        | V    |
| $I_{IK}$  | Input clamp diode current                                | For $V_I < 0.5V$ or $V_I > V_{CC} + 0.5V$  |      | $\pm 20$ | mA   |
| $I_{OK}$  | Output clamp diode current                               | For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ |      | $\pm 20$ | mA   |
| $I_O$     | Output source or sink current per output pin             | For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ |      | $\pm 25$ | mA   |
|           | Continuous current through $V_{CC}$ or GND               |                                            |      | $\pm 50$ | mA   |
| $T_J$     | Junction temperature                                     |                                            |      | 150      | °C   |
| $T_{stg}$ | Storage temperature range                                |                                            | -65  | 150      | °C   |
|           | Lead temperature (Soldering 10s) (SOIC - Lead Tips Only) |                                            |      | 300      | °C   |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 5.2 Recommended Operating Conditions

|          |                          |                 | MIN | MAX      | UNIT |
|----------|--------------------------|-----------------|-----|----------|------|
| $V_{CC}$ | Supply voltage range     | HC types        | 2   | 6        | V    |
|          |                          | HCT types       | 4.5 | 5.5      |      |
| $V_I$    | Input voltage            |                 | 0   | $V_{CC}$ | V    |
| $V_O$    | Output voltage           |                 | 0   | $V_{CC}$ | V    |
| $t_t$    | Input rise and fall time | $V_{CC} = 2V$   |     | 1000     | ns   |
|          |                          | $V_{CC} = 4.5V$ |     | 500      |      |
|          |                          | $V_{CC} = 6V$   |     | 400      |      |
| $T_A$    | Temperature range        |                 | -55 | 125      | °C   |

### 5.3 Thermal Information

| THERMAL METRIC  |                                                       | CD74HC(T)138, CD74HC(T)238 |             |             |               | UNIT |
|-----------------|-------------------------------------------------------|----------------------------|-------------|-------------|---------------|------|
|                 |                                                       | N<br>(PDIP)                | D<br>(SOIC) | NS<br>(SOP) | PW<br>(TSSOP) |      |
|                 |                                                       | 16 Pins                    | 16 Pins     | 16 Pins     | 16 Pins       |      |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance <sup>(1)</sup> | 67                         | 73          | 64          | 108           | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

## 5.4 Electrical Characteristics

| PARAMETER        |                                         | TEST CONDITIONS <sup>(1)</sup>                                           | V <sub>CC</sub> (V) | 25°C    |     |     | -40°C to 85°C |     | -55°C to 125°C |     | UNIT |
|------------------|-----------------------------------------|--------------------------------------------------------------------------|---------------------|---------|-----|-----|---------------|-----|----------------|-----|------|
|                  |                                         |                                                                          |                     | MIN     | TYP | MAX | MIN           | MAX | MIN            | MAX |      |
| HC TYPES         |                                         |                                                                          |                     |         |     |     |               |     |                |     |      |
| V <sub>IH</sub>  | High-level input voltage                |                                                                          | 2                   | 1.5     |     |     | 1.5           |     | 1.5            |     | V    |
|                  |                                         |                                                                          | 4.5                 | 3.15    |     |     | 3.15          |     | 3.15           |     | V    |
|                  |                                         |                                                                          | 6                   | 4.2     |     |     | 4.2           |     | 4.2            |     | V    |
| V <sub>IL</sub>  | Low-level input voltage                 |                                                                          | 2                   | 0.5     |     |     | 0.5           |     | 0.5            |     | V    |
|                  |                                         |                                                                          | 4.5                 | 1.35    |     |     | 1.35          |     | 1.35           |     | V    |
|                  |                                         |                                                                          | 6                   | 1.8     |     |     | 1.8           |     | 1.8            |     | V    |
| V <sub>OH</sub>  | High-level output voltage               | I <sub>OH</sub> = - 20 μA                                                | 2                   | 1.9     |     |     | 1.9           |     | 1.9            |     | V    |
|                  |                                         | I <sub>OH</sub> = - 20 μA                                                | 4.5                 | 4.4     |     |     | 4.4           |     | 4.4            |     | V    |
|                  |                                         | I <sub>OH</sub> = - 20 μA                                                | 6                   | 5.9     |     |     | 5.9           |     | 5.9            |     | V    |
|                  | High-level output voltage               | I <sub>OH</sub> = - 4 mA                                                 | 4.5                 | 3.98    |     |     | 3.84          |     | 3.7            |     | V    |
|                  |                                         | I <sub>OH</sub> = - 5.2 mA                                               | 6                   | 5.48    |     |     | 5.34          |     | 5.2            |     | V    |
| V <sub>OL</sub>  | Low-level output voltage                | I <sub>OL</sub> = 20 μA                                                  | 2                   | 0.1     |     |     | 0.1           |     | 0.1            |     | V    |
|                  |                                         | I <sub>OL</sub> = 20 μA                                                  | 4.5                 | 0.1     |     |     | 0.1           |     | 0.1            |     | V    |
|                  |                                         | I <sub>OL</sub> = 20 μA                                                  | 6                   | 0.1     |     |     | 0.1           |     | 0.1            |     | V    |
|                  | Low-level output voltage                | I <sub>OL</sub> = 4 mA                                                   | 4.5                 | 0.26    |     |     | 0.33          |     | 0.4            |     | V    |
|                  |                                         | I <sub>OL</sub> = 5.2 mA                                                 | 6                   | 0.26    |     |     | 0.33          |     | 0.4            |     | V    |
| I <sub>I</sub>   | Input leakage current                   | V <sub>I</sub> = V <sub>CC</sub> or GND                                  | 6                   | ±0.1    |     |     | ±1            |     | ±1             |     | μA   |
| I <sub>CC</sub>  | Supply current                          | V <sub>I</sub> = V <sub>CC</sub> or GND                                  | 6                   | 8       |     |     | 80            |     | 160            |     | μA   |
| HCT TYPES        |                                         |                                                                          |                     |         |     |     |               |     |                |     |      |
| V <sub>IH</sub>  | High-level input voltage                |                                                                          | 4.5 to 5.5          | 2       |     |     | 2             |     | 2              |     | V    |
| V <sub>IL</sub>  | Low-level input voltage                 |                                                                          | 4.5 to 5.5          | 0.8     |     |     | 0.8           |     | 0.8            |     | V    |
| V <sub>OH</sub>  | High-level output voltage               | I <sub>OH</sub> = - 20 μA                                                | 4.5                 | 4.4     |     |     | 4.4           |     | 4.4            |     | V    |
|                  | High-level output voltage               | I <sub>OH</sub> = - 4 mA                                                 | 4.5                 | 3.98    |     |     | 3.84          |     | 3.7            |     | V    |
| V <sub>OL</sub>  | Low-level output voltage                | I <sub>OL</sub> = 20 μA                                                  | 4.5                 | 0.1     |     |     | 0.1           |     | 0.1            |     | V    |
|                  | Low-level output voltage                | I <sub>OH</sub> = 4 mA                                                   | 4.5                 | 0.26    |     |     | 0.33          |     | 0.4            |     | V    |
| I <sub>I</sub>   | Input leakage current                   | V <sub>I</sub> = V <sub>CC</sub> and GND                                 | 5.5                 | ±0.1    |     |     | ±1            |     | ±1             |     | μA   |
| I <sub>CC</sub>  | Supply current                          | V <sub>I</sub> = V <sub>CC</sub> and GND                                 | 5.5                 | 8       |     |     | 80            |     | 160            |     | μA   |
| ΔI <sub>CC</sub> | Additional supply current per input pin | A <sub>0</sub> - A <sub>2</sub> inputs held at V <sub>CC</sub> - 2.1 V   | 4.5 to 5.5          | 100 540 |     |     | 675           |     | 735            |     | μA   |
|                  |                                         | G <sub>0</sub> and G <sub>1</sub> inputs held at V <sub>CC</sub> - 2.1 V | 4.5 to 5.5          | 100 450 |     |     | 562.5         |     | 612.5          |     | μA   |
|                  |                                         | G <sub>2</sub> input held at V <sub>CC</sub> - 2.1 V                     | 4.5 to 5.5          | 100 360 |     |     | 450           |     | 490            |     | μA   |

(1) V<sub>I</sub> = V<sub>IH</sub> or V<sub>IL</sub>, unless otherwise noted.

## 5.5 Switching Characteristics<sup>(2)</sup>

Input  $t_i = 6\text{ns}$ . (See [Parameter Measurement Information](#))

| PARAMETER       |                                                                                  | TEST CONDITIONS       | V <sub>CC</sub> (V) | 25°C |                   |     | -40°C to 85°C |     | -55°C to 125°C |     | UNIT |
|-----------------|----------------------------------------------------------------------------------|-----------------------|---------------------|------|-------------------|-----|---------------|-----|----------------|-----|------|
|                 |                                                                                  |                       |                     | MIN  | TYP               | MAX | MIN           | MAX | MIN            | MAX |      |
| HC TYPES        |                                                                                  |                       |                     |      |                   |     |               |     |                |     |      |
| t <sub>pd</sub> | Address to output                                                                | C <sub>L</sub> = 50pF | 2                   |      |                   | 150 |               | 190 |                | 225 | ns   |
|                 |                                                                                  |                       | 4.5                 |      | 13 <sup>(3)</sup> | 30  |               | 38  |                | 45  |      |
|                 |                                                                                  | C <sub>L</sub> = 50pF | 6                   |      |                   | 26  |               | 33  |                | 38  |      |
|                 | Strobe $\overline{G}_0$ , $\overline{G}_1$ , G <sub>2</sub> to output HC/HCT 138 | C <sub>L</sub> = 50pF | 2                   |      |                   | 150 |               | 190 |                | 265 | ns   |
|                 |                                                                                  |                       | 4.5                 |      |                   | 30  |               | 38  |                | 53  |      |
|                 |                                                                                  |                       | 6                   |      |                   | 26  |               | 33  |                | 45  |      |
| t <sub>t</sub>  | Output transition time                                                           | C <sub>L</sub> = 50pF | 2                   |      |                   | 75  |               | 95  |                | 110 | MHz  |
|                 |                                                                                  |                       | 4.5                 |      |                   | 15  |               | 19  |                | 22  |      |
|                 |                                                                                  |                       | 6                   |      |                   | 13  |               | 16  |                | 19  |      |
| C <sub>pd</sub> | Power dissipation capacitance <sup>(1)</sup>                                     | C <sub>L</sub> = 15pF | 5                   |      | 67                |     |               |     |                |     | pF   |
| C <sub>i</sub>  | Input capacitance                                                                |                       |                     |      |                   | 10  |               | 10  |                | 10  | pF   |
| HCT TYPES       |                                                                                  |                       |                     |      |                   |     |               |     |                |     |      |
| t <sub>pd</sub> | Address to output                                                                | C <sub>L</sub> = 50pF | 4.5                 |      | 14 <sup>(3)</sup> | 35  |               | 44  |                | 53  | ns   |
|                 | Strobe G <sub>2</sub> to output HC/HCT138                                        | C <sub>L</sub> = 50pF | 4.5                 |      |                   | 35  |               | 44  |                | 53  | ns   |
|                 | Strobe $\overline{G}_0$ , $\overline{G}_1$ to output HC/HCT238                   | C <sub>L</sub> = 15pF | 4.5                 |      |                   | 40  |               | 50  |                | 60  | ns   |
| t <sub>t</sub>  | Output transition time                                                           | C <sub>L</sub> = 15pF | 4.5                 |      |                   | 15  |               | 19  |                | 22  |      |
| C <sub>pd</sub> | Power dissipation capacitance <sup>(1)</sup>                                     | C <sub>L</sub> = 15pF | 5                   |      | 67                |     |               |     |                |     | pF   |
| C <sub>i</sub>  | Input capacitance                                                                |                       |                     |      |                   | 10  |               | 10  |                | 10  | pF   |

(1)  $C_{PD}$  is used to determine the dynamic power consumption, per gate.

(2) For details on power calculation, see [SCAA035B](#)

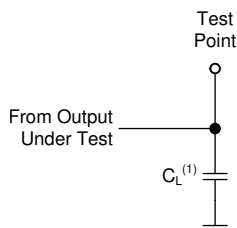
(3)  $C_L = 15\text{pF}$  and  $V_{CC} = 5$

## 6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_f < 6 \text{ ns}$ .

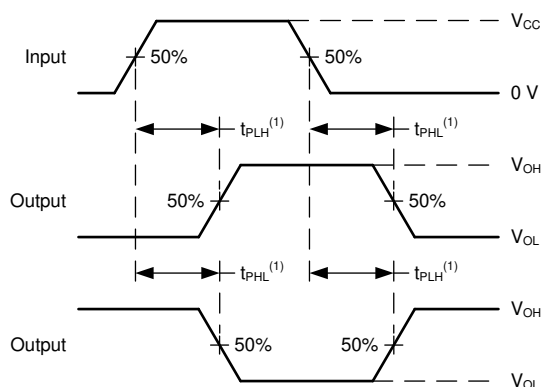
For clock inputs,  $f_{\text{max}}$  is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



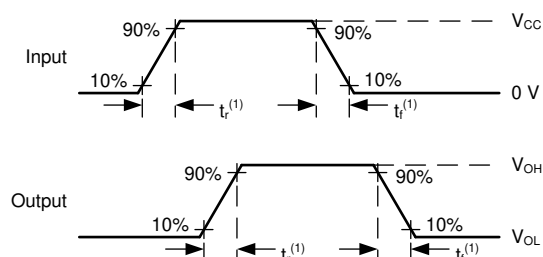
(1)  $C_L$  includes probe and test-fixture capacitance.

**图 6-1. Load Circuit for Push-Pull Outputs**



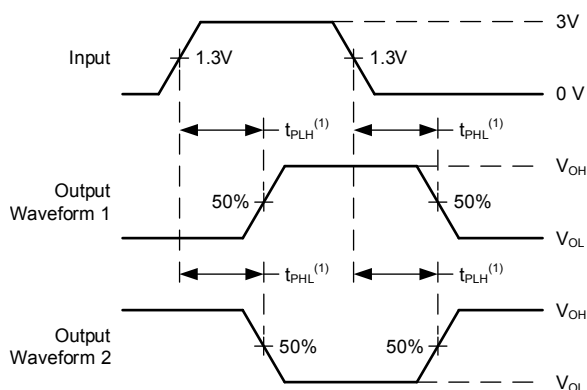
(1) The greater between  $t_{PLH}$  and  $t_{PHL}$  is the same as  $t_{pd}$ .

**图 6-2. Voltage Waveforms, Propagation Delays for Standard CMOS Inputs**



(1) The greater between  $t_r$  and  $t_f$  is the same as  $t_t$ .

**图 6-3. Voltage Waveforms, Input and Output Transition Times for Standard CMOS Inputs**



(1) The greater between  $t_{PLH}$  and  $t_{PHL}$  is the same as  $t_{pd}$ .

**图 6-4. Voltage Waveforms, Propagation Delays for TTL-Compatible Inputs**

## 7 Detailed Description

### 7.1 Overview

The CDx4HC(T)138 and '238 are high speed silicon gate CMOS decoders well suited to memory address decoding or data routing applications. They contain a single 3:8 decoder.

The CDx4HC(T)138 and '238 have three address select inputs ( $A_2$ ,  $A_1$ , and  $A_0$ ). The circuit functions as a normal one-of-eight decoder.

Three strobe inputs ( $G_2$ ,  $\overline{G}_1$  and  $\overline{G}_0$ ) are provided to simplify cascading and to facilitate demultiplexing. When any input strobe is active, all outputs are forced into the high state for the '138 function. When any input strobe is active, all outputs are forced into the low state for the '238 function.

The demultiplexing function is accomplished by first using the select inputs to choose the desired output, and then using one of the strobe inputs as the data input.

The outputs for the CDx4HC(T)138 are normally low when selected. The outputs for the CDxHC(T)238 are normally high when selected.

### 7.2 Functional Block Diagram

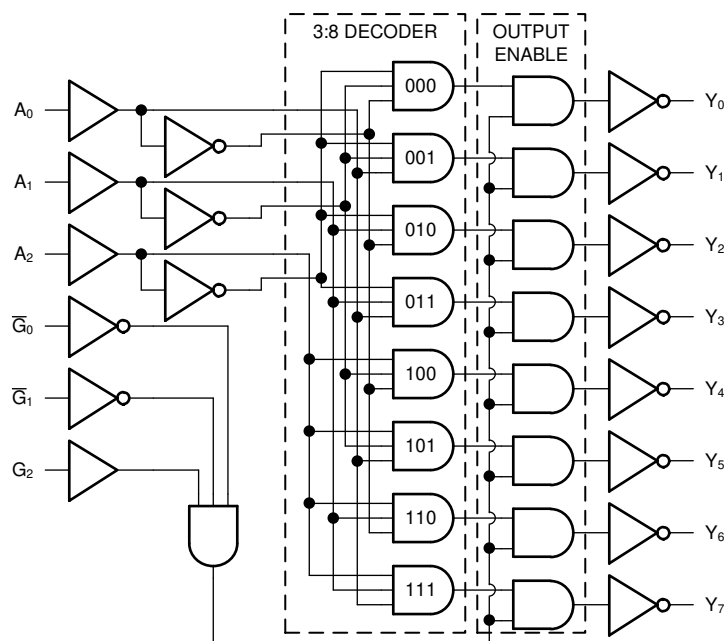


图 7-1. Functional Block Diagram '138

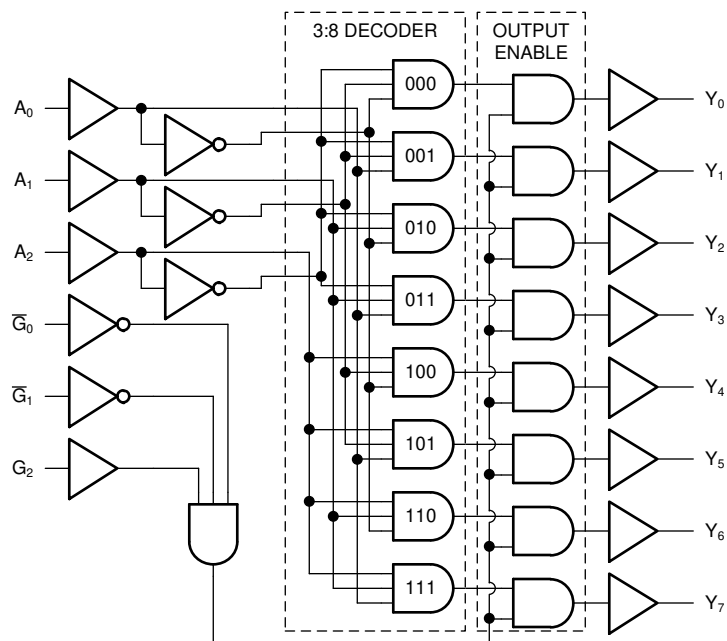


图 7-2. Functional Block Diagram '238

## 7.3 Device Functional Modes

表 7-1. Function Table 'HC138, 'HCT138

| INPUTS |    |    |                |                |                | OUTPUTS        |                |                |                |                |                |                |                |
|--------|----|----|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| STROBE |    |    | ADDRESS        |                |                |                |                |                |                |                |                |                |                |
| G2     | G1 | G0 | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> | Y <sub>0</sub> | Y <sub>1</sub> | Y <sub>2</sub> | Y <sub>3</sub> | Y <sub>4</sub> | Y <sub>5</sub> | Y <sub>6</sub> | Y <sub>7</sub> |
| X      | X  | H  | X              | X              | X              | H              | H              | H              | H              | H              | H              | H              | H              |
| L      | X  | X  | X              | X              | X              | H              | H              | H              | H              | H              | H              | H              | H              |
| X      | H  | X  | X              | X              | X              | H              | H              | H              | H              | H              | H              | H              | H              |
| H      | L  | L  | L              | L              | L              | L              | H              | H              | H              | H              | H              | H              | H              |
| H      | L  | L  | L              | L              | H              | H              | L              | H              | H              | H              | H              | H              | H              |
| H      | L  | L  | L              | H              | L              | H              | H              | L              | H              | H              | H              | H              | H              |
| H      | L  | L  | L              | H              | H              | H              | H              | H              | L              | H              | H              | H              | H              |
| H      | L  | L  | H              | L              | L              | H              | H              | H              | H              | L              | H              | H              | H              |
| H      | L  | L  | H              | L              | H              | H              | H              | H              | H              | H              | L              | H              | H              |
| H      | L  | L  | H              | H              | L              | H              | H              | H              | H              | H              | H              | L              | H              |
| H      | L  | L  | H              | H              | H              | H              | H              | H              | H              | H              | H              | H              | L              |

H = High Voltage Level, L = Low Voltage Level, X = Don't Care

表 7-2. Function Table 'HC238, 'HCT238

| INPUTS |    |    |                |                |                | OUTPUTS        |                |                |                |                |                |                |                |
|--------|----|----|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| STROBE |    |    | ADDRESS        |                |                |                |                |                |                |                |                |                |                |
| G2     | G1 | G0 | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> | Y <sub>0</sub> | Y <sub>1</sub> | Y <sub>2</sub> | Y <sub>3</sub> | Y <sub>4</sub> | Y <sub>5</sub> | Y <sub>6</sub> | Y <sub>7</sub> |
| X      | X  | H  | X              | X              | X              | L              | L              | L              | L              | L              | L              | L              | L              |
| L      | X  | X  | X              | X              | X              | L              | L              | L              | L              | L              | L              | L              | L              |
| X      | H  | X  | X              | X              | X              | L              | L              | L              | L              | L              | L              | L              | L              |
| H      | L  | L  | L              | L              | L              | H              | L              | L              | L              | L              | L              | L              | L              |
| H      | L  | L  | L              | L              | H              | L              | H              | L              | L              | L              | L              | L              | L              |
| H      | L  | L  | L              | H              | L              | L              | L              | H              | L              | L              | L              | L              | L              |
| H      | L  | L  | L              | H              | H              | L              | L              | L              | H              | L              | L              | L              | L              |
| H      | L  | L  | H              | L              | L              | L              | L              | L              | L              | H              | L              | L              | L              |
| H      | L  | L  | H              | L              | H              | L              | L              | L              | L              | L              | H              | L              | L              |
| H      | L  | L  | H              | H              | L              | L              | L              | L              | L              | L              | L              | H              | L              |
| H      | L  | L  | H              | H              | H              | L              | L              | L              | L              | L              | L              | L              | H              |

H = High Voltage Level, L = Low Voltage Level, X = Don't Care

## 8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- $\mu$ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 9 Layout

### 9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

## 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 10.1 Documentation Support

#### 10.1.1 Related Documentation

### 10.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 10.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

### 10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

### 10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number          | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)             |
|--------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------------------|
| <a href="#">5962-8688401EA</a> | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8688401EA<br>CD54HC238F3A  |
| <a href="#">CD54HC138F</a>     | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CD54HC138F                      |
| <a href="#">CD54HC138F3A</a>   | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 8406201EA<br>CD54HC138F3A       |
| <a href="#">CD54HC238F3A</a>   | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8688401EA<br>CD54HC238F3A  |
| <a href="#">CD54HCT138F</a>    | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CD54HCT138F                     |
| <a href="#">CD54HCT138F3A</a>  | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 8550401EA<br>CD54HCT138F3A      |
| <a href="#">CD54HCT238F3A</a>  | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8974501EA<br>CD54HCT238F3A |
| <a href="#">CD74HC138E</a>     | Active        | Production           | PDIP (N)   16   | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74HC138E                      |
| <a href="#">CD74HC138M</a>     | Obsolete      | Production           | SOIC (D)   16   | -                     | -           | Call TI                              | Call TI                           | -55 to 125   | HC138M                          |
| <a href="#">CD74HC138M96</a>   | Active        | Production           | SOIC (D)   16   | 2500   LARGE T&R      | Yes         | NIPDAU   SN                          | Level-1-260C-UNLIM                | -55 to 125   | HC138M                          |
| <a href="#">CD74HC138M96E4</a> | Active        | Production           | null (null)     | 2500   LARGE T&R      | -           | Call TI                              | Call TI                           | -55 to 125   |                                 |
| <a href="#">CD74HC138MT</a>    | Obsolete      | Production           | SOIC (D)   16   | -                     | -           | Call TI                              | Call TI                           | -55 to 125   | HC138M                          |
| <a href="#">CD74HC238E</a>     | Active        | Production           | PDIP (N)   16   | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74HC238E                      |
| <a href="#">CD74HC238M</a>     | Obsolete      | Production           | SOIC (D)   16   | -                     | -           | Call TI                              | Call TI                           | -55 to 125   | HC238M                          |
| <a href="#">CD74HC238M96</a>   | Active        | Production           | SOIC (D)   16   | 2500   LARGE T&R      | Yes         | NIPDAU   SN                          | Level-1-260C-UNLIM                | -55 to 125   | (CD4051BM, HC238M)              |
| <a href="#">CD74HC238MT</a>    | Obsolete      | Production           | SOIC (D)   16   | -                     | -           | Call TI                              | Call TI                           | -55 to 125   | HC238M                          |
| <a href="#">CD74HC238NSR</a>   | Active        | Production           | SOP (NS)   16   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | HC238M                          |
| <a href="#">CD74HC238PW</a>    | Obsolete      | Production           | TSSOP (PW)   16 | -                     | -           | Call TI                              | Call TI                           | -55 to 125   | HJ238                           |
| <a href="#">CD74HC238PWR</a>   | Active        | Production           | TSSOP (PW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU   SN                          | Level-1-260C-UNLIM                | -55 to 125   | HJ238                           |
| <a href="#">CD74HC238PWT</a>   | Obsolete      | Production           | TSSOP (PW)   16 | -                     | -           | Call TI                              | Call TI                           | -55 to 125   | HJ238                           |
| <a href="#">CD74HCT138E</a>    | Active        | Production           | PDIP (N)   16   | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74HCT138E                     |
| <a href="#">CD74HCT138M</a>    | Obsolete      | Production           | SOIC (D)   16   | -                     | -           | Call TI                              | Call TI                           | -55 to 125   | HCT138M                         |
| <a href="#">CD74HCT138M96</a>  | Active        | Production           | SOIC (D)   16   | 2500   LARGE T&R      | Yes         | NIPDAU   SN                          | Level-1-260C-UNLIM                | -55 to 125   | HCT138M                         |
| <a href="#">CD74HCT238E</a>    | Active        | Production           | PDIP (N)   16   | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74HCT238E                     |
| <a href="#">CD74HCT238M</a>    | Obsolete      | Production           | SOIC (D)   16   | -                     | -           | Call TI                              | Call TI                           | -55 to 125   | HCT238M                         |

| Orderable part number         | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">CD74HCT238M96</a> | Active        | Production           | SOIC (D)   16   | 2500   LARGE T&R      | Yes         | NIPDAU   SN                          | Level-1-260C-UNLIM                | -55 to 125   | HCT238M             |
| <a href="#">CD74HCT238PW</a>  | Obsolete      | Production           | TSSOP (PW)   16 | -                     | -           | Call TI                              | Call TI                           | -55 to 125   | HK238               |
| <a href="#">CD74HCT238PWR</a> | Active        | Production           | TSSOP (PW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU   SN   NIPDAU                 | Level-1-260C-UNLIM                | -55 to 125   | HK238               |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## OTHER QUALIFIED VERSIONS OF CD54HC138, CD54HC238, CD54HCT138, CD54HCT238, CD74HC138, CD74HC238, CD74HCT138, CD74HCT238 :

• Catalog : [CD74HC138](#), [CD74HC238](#), [CD74HCT138](#), [CD74HCT238](#)

• Automotive : [CD74HC138-Q1](#), [CD74HC138-Q1](#)

- Military : [CD54HC138](#), [CD54HC238](#), [CD54HCT138](#), [CD54HCT238](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74HC138M96  | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| CD74HC238M96  | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| CD74HC238M96  | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| CD74HC238NSR  | SOP          | NS              | 16   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |
| CD74HC238PWR  | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| CD74HC238PWR  | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| CD74HCT138M96 | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| CD74HCT238M96 | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| CD74HCT238PWR | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| CD74HCT238PWR | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74HC138M96  | SOIC         | D               | 16   | 2500 | 356.0       | 356.0      | 35.0        |
| CD74HC238M96  | SOIC         | D               | 16   | 2500 | 340.5       | 336.1      | 32.0        |
| CD74HC238M96  | SOIC         | D               | 16   | 2500 | 340.5       | 336.1      | 32.0        |
| CD74HC238NSR  | SOP          | NS              | 16   | 2000 | 356.0       | 356.0      | 35.0        |
| CD74HC238PWR  | TSSOP        | PW              | 16   | 2000 | 356.0       | 356.0      | 35.0        |
| CD74HC238PWR  | TSSOP        | PW              | 16   | 2000 | 356.0       | 356.0      | 35.0        |
| CD74HCT138M96 | SOIC         | D               | 16   | 2500 | 356.0       | 356.0      | 35.0        |
| CD74HCT238M96 | SOIC         | D               | 16   | 2500 | 356.0       | 356.0      | 35.0        |
| CD74HCT238PWR | TSSOP        | PW              | 16   | 2000 | 356.0       | 356.0      | 35.0        |
| CD74HCT238PWR | TSSOP        | PW              | 16   | 2000 | 356.0       | 356.0      | 35.0        |

## TUBE



\*All dimensions are nominal

| Device       | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|--------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| CD74HC138E   | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HC138E   | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HC238E   | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HC238E   | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HC238EE4 | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HC238EE4 | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HCT138E  | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HCT138E  | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HCT238E  | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HCT238E  | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |



# PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

## NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.





SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL  
 SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

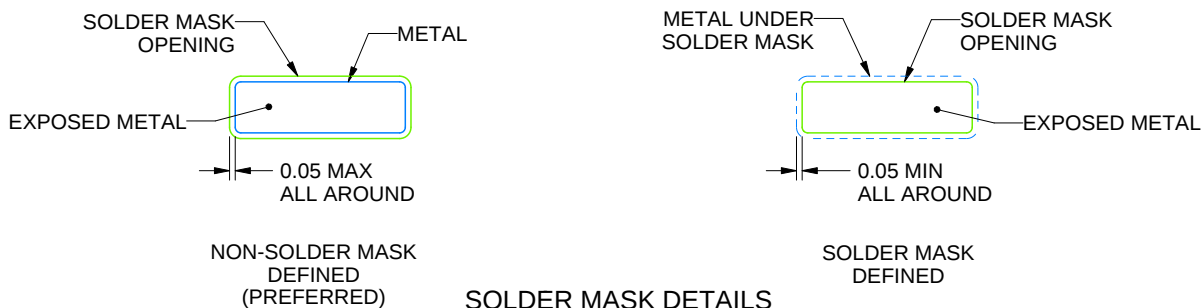
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

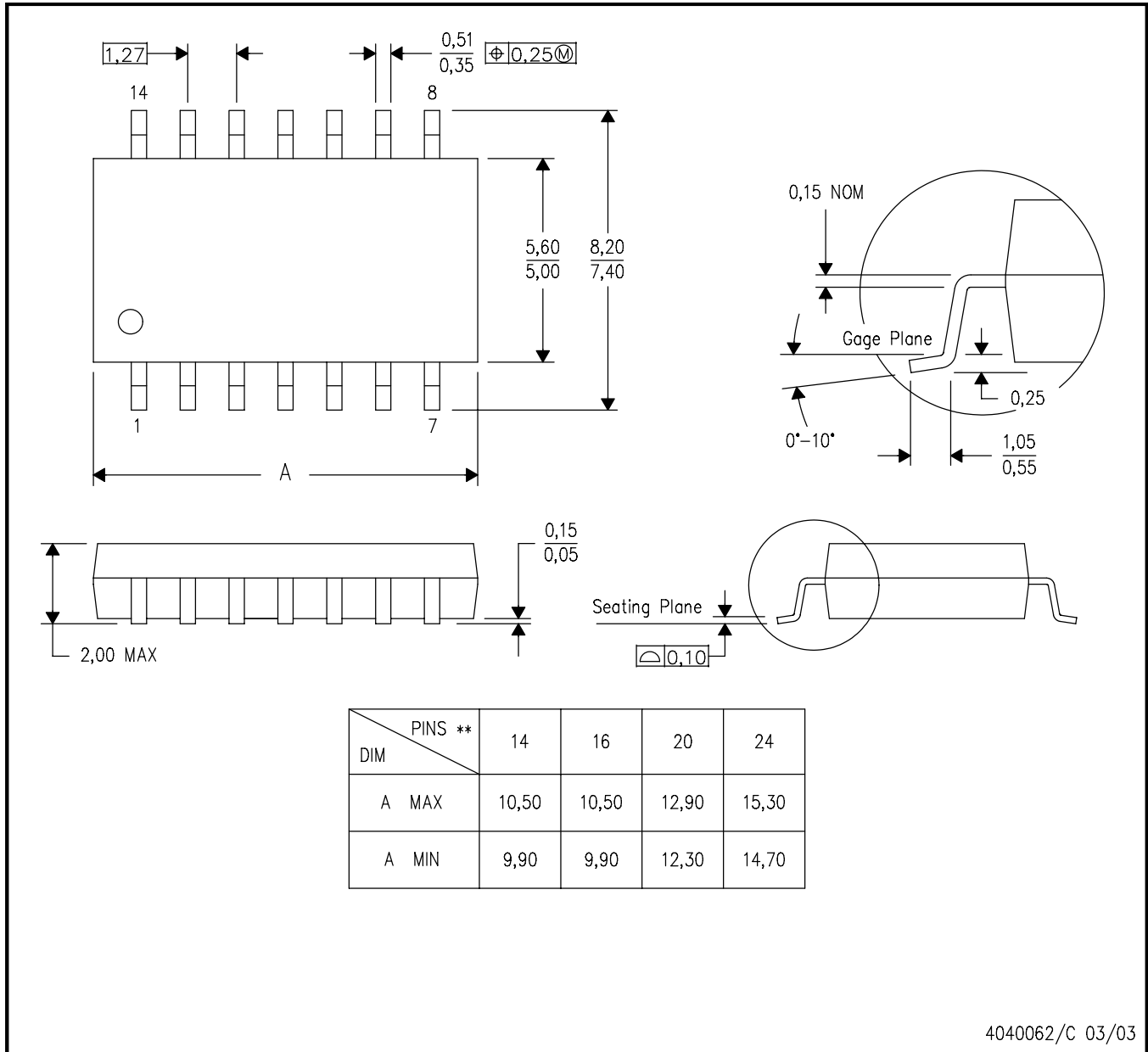
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



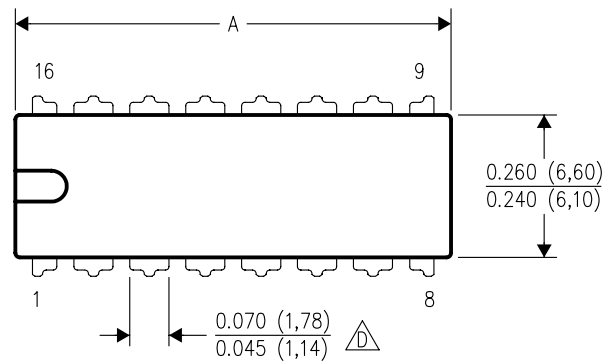
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

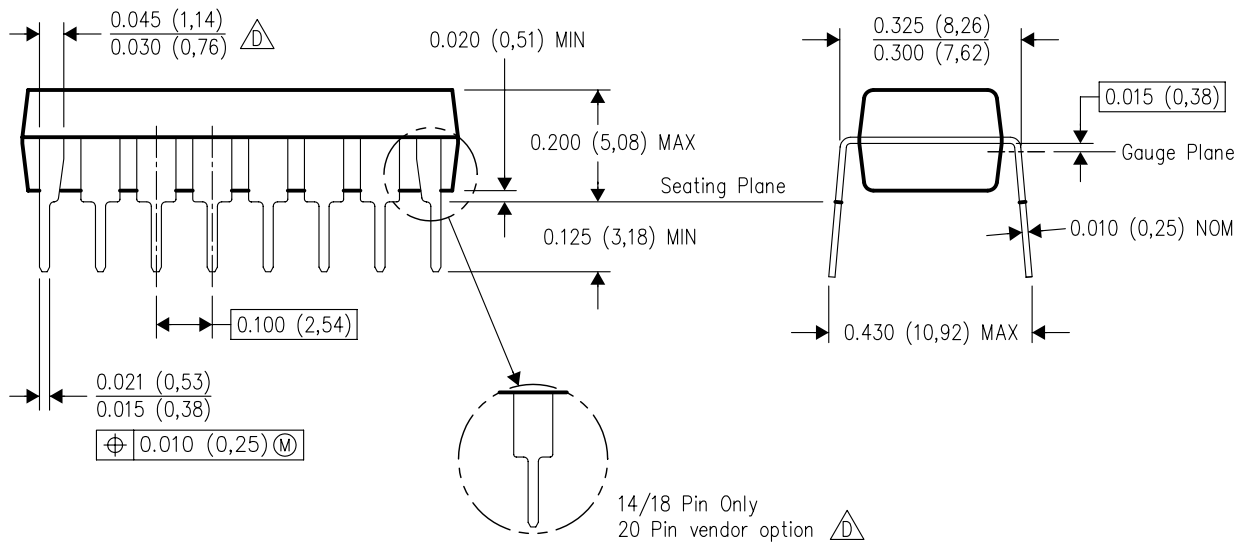
N (R-PDIP-T\*\*)

16 PINS SHOWN

# PLASTIC DUAL-IN-LINE PACKAGE



| DIM \ PINS **       | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

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