

具有可控接通功能的超小型、低导通电阻负载开关

查询样品: [TPS22912](#)

特性

- 集成单负载开关
- 0.9mm x 0.9mm**, 锡球/焊盘间距 **0.5mm**, 超小型晶片比例 **(CSP)-4** 封装
- 输入电压范围: **1.4V 至 5.5V**
- 低导通电阻
 - 在输入电压(VIN) = 5V时, rON = 60mΩ
 - 在输入电压(VIN) = 3.3V时, rON = 61mΩ
 - 在输入电压(VIN) = 1.8V时, rON = 74mΩ
 - 在输入电压(VIN) = 1.5V时, rON = 84mΩ
- 2A** 最大持续开关电流
- 低阈值控制输入
- 可控转换率选项
- 欠压闭锁
- 反向电流保护

应用范围

- 便携式工业/医疗设备
- 便携式媒体播放器
- POS** 机终端
- 全球卫星定位系统 **(GPS)** 导航器件
- 数码摄像机
- 便携式仪表
- 智能电话 / 无线手持终端

说明

TPS22912 是一款具有可控接通功能的小型、低 rON 负载开关, 此开关包含一个可在 1.4V 至 5.5V 的输入电压范围内运行的 P 通道金属氧化物半导体场效应晶体管 (MOSFET)。此开关由一个高电平输入 (ON) 控制, 此输入能够与低压控制信号直接接口相连。

为了避免涌入电流, 此器件的转换率由内部控制。TPS22912 系列产品有多重上升时间选项并且工作态高电平启用。(参见表 1)

TPS22912 通过在反向电压情况期间锁存电源开关来提供电路断路器功能。一个内部反向电压比较器在输出电压 (VOUT) 高于输入电压 (VIN) 时禁用此电源开关。这一过程能够快速 (典型值为 10μs) 阻止流向开关输入端的电流。反向电流保护一直有效, 即便当器件被禁用时也是如此。此外, 如果此输入电压过低, 欠压闭锁 (UVLO) 保护会将此开关关闭。

TPS22912 采用超小型、节省空间的 4 引脚 CSP 封装并可在 -40°C 至 85°C 的大气环境温度范围内运行。

典型应用

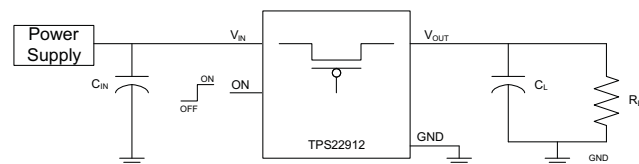


表 1. 特性列表

器件	3.3V 时的 rON (典型值)	3.3V (典型值) 时的上升时间	快速输出放电 (1)	最大输出电压	使能
TPS22912A (2)	61mΩ	1μs	否	2A	高电平有效
TPS22912B (2)	61mΩ	100μs	否	2A	高电平有效
TPS22912C	61mΩ	1000μs	否	2A	高电平有效
TPS22912D (2)	61mΩ	4500μs	否	2A	高电平有效

(1) 此特性可通过一个 150Ω 电阻器将开关的输出放电至接地水平, 从而防止此输出悬空。

(2) 请向当地销售商/分销商或者厂家查询产品供货信息。



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2012, Texas Instruments Incorporated
English Data Sheet: [SLVSB78](#)

TPS22912

ZHCS850 –APRIL 2012

www.ti.com.cn



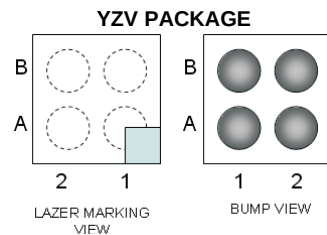
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING/ STATUS ⁽²⁾
–40°C to 85°C	YZV (0.5mm pitch)	Tape and Reel	TPS22912AYZVR	Contact factory for availability
–40°C to 85°C	YZV (0.5mm pitch)	Tape and Reel	TPS22912BYZVR	Contact factory for availability
–40°C to 85°C	YZV (0.5mm pitch)	Tape and Reel	TPS22912CZVR	– – – – 78
–40°C to 85°C	YZV (0.5mm pitch)	Tape and Reel	TPS22912DYZVR	Contact factory for availability

- (1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
- (2) Contact factory for details and availability for PREVIEW devices, minimum order quantities may apply.

DEVICE INFORMATION



TERMINAL ASSIGNMENTS

B	ON	GND
A	V _{IN}	V _{OUT}
	2	1

PIN FUNCTIONS

TPS22912	PIN NAME	DESCRIPTION
YZV		
B1	GND	Ground
B2	ON	Switch control input, active high. Do not leave floating
A1	V _{OUT}	Switch output
A2	V _{IN}	Switch input. Use ceramic capacitor to GND for bypass.

BLOCK DIAGRAM

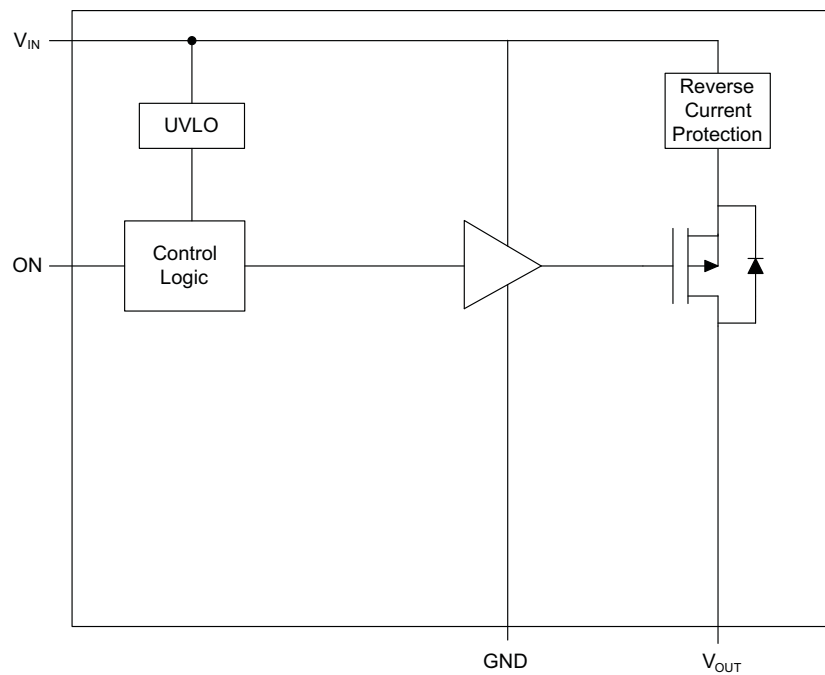


Table 2. FUNCTION TABLE

ON	VIN to VOUT
L	OFF
H	ON

ABSOLUTE MAXIMUM RATINGS

		VALUE	UNIT
V _{IN}	Input voltage range	–0.3 to 6	V
V _{OUT}	Output voltage range	–0.3 to 6	V
V _{ON}	Input voltage range	–0.3 to 6	V
I _{MAX}	Maximum continuous switch current	2	A
I _{PLS}	Maximum pulsed switch current, pulse ≤500 ms, 50% duty cycle	3	A
T _A	Operating free-air temperature range	–40 to 85	°C
T _J	Maximum junction temperature	125	°C
T _{STG}	Storage temperature range	–65 to 150	°C
T _{LEAD}	Maximum lead temperature (10-s soldering time)	300	°C
ESD	Electrostatic discharge protection	Human-Body Model (HBM) (VIN, VOUT, GND pins)	V
		Charged-Device Model (CDM) (VIN, VOUT, ON, GND pins)	

TPS22912

ZHCS850 –APRIL 2012

www.ti.com.cn

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾		TPS22912	UNITS
		CSP	
		4 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	189.1	°C/W
θ_{JCTop}	Junction-to-case (top) thermal resistance	1.9	
θ_{JB}	Junction-to-board thermal resistance	36.8	
ψ_{JT}	Junction-to-top characterization parameter	11.3	
ψ_{JB}	Junction-to-board characterization parameter	36.8	
θ_{JCbott}	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_{IN}	Input voltage range	1.4	5.5	V
V_{ON}	ON voltage range	0	5.5	V
V_{OUT}	Output voltage range (Note: V_{OUT} greater than V_{IN} will cause the reverse current protection of this device to trigger. See application section.)	$V_{IN}^{(1)}$		
V_{IH}	High-level input voltage, ON	VIN = 3.61 V to 5.5 V		V
		VIN = 1.4 V to 3.6 V		V
V_{IL}	Low-level input voltage, ON	VIN = 3.61 V to 5.5 V		0.6
		VIN = 1.4 V to 3.6V		0.4
C_{IN}	Input Capacitor	1 ⁽¹⁾		μF

(1) Refer to the application section.

ELECTRICAL CHARACTERISTICS

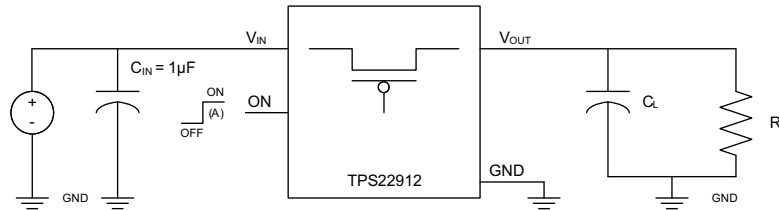
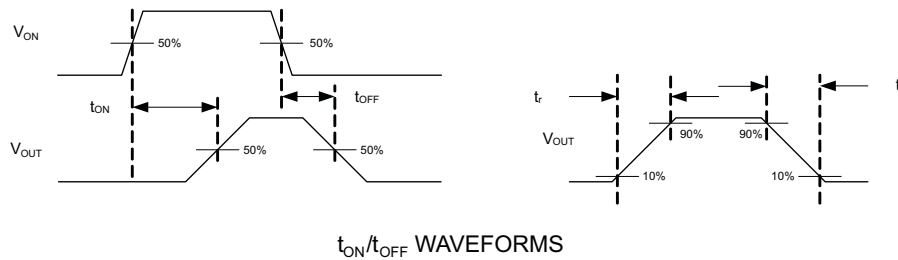
V_{IN} = 1.4 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T _A	MIN	TYP	MAX	UNIT
I _{IN} Quiescent current	I _{OUT} = 0, V _{ON} = V _{IN} = 5.25 V	Full		2	10	μA
	I _{OUT} = 0, V _{ON} = V _{IN} = 4.2 V			2	7.0	
	I _{OUT} = 0, V _{ON} = V _{IN} = 3.6 V			2	7.0	
	I _{OUT} = 0, V _{ON} = V _{IN} = 2.5 V			0.9	5	
	I _{OUT} = 0, V _{ON} = V _{IN} = 1.5 V			0.7	5	
I _{IN(off)} ⁽¹⁾ Off supply current	R _L = 1 MΩ, V _{IN} = 5.25 V, V _{ON} = GND	Full		1.2	10	μA
	R _L = 1 MΩ, V _{IN} = 4.2 V, V _{ON} = GND			0.2	7.0	
	R _L = 1 MΩ, V _{IN} = 3.6 V, V _{ON} = GND			0.1	7.0	
	R _L = 1 MΩ, V _{IN} = 2.5 V, V _{ON} = GND			0.1	5	
	R _L = 1 MΩ, V _{IN} = 1.5 V, V _{ON} = GND			0.1	5	
I _{IN(Leakage)} Leakage current	V _{OUT} = 0, V _{IN} = 5.25 V, V _{ON} = GND	Full		1.2	10	μA
	V _{OUT} = 0, V _{IN} = 4.2 V, V _{ON} = GND			0.2	7.0	
	V _{OUT} = 0, V _{IN} = 3.6 V, V _{ON} = GND			0.1	7.0	
	V _{OUT} = 0, V _{IN} = 2.5 V, V _{ON} = GND			0.1	5	
	V _{OUT} = 0, V _{IN} = 1.5 V, V _{ON} = GND			0.1	5	
r _{ON} On-resistance	V _{IN} = 5.25 V, I _{OUT} = –200 mA	25°C		60	80	mΩ
		Full			110	
	V _{IN} = 5.0 V, I _{OUT} = –200 mA	25°C		60	80	
		Full			110	
	V _{IN} = 4.2 V, I _{OUT} = –200 mA	25°C		60	80	
		Full			110	
	V _{IN} = 3.3 V, I _{OUT} = –200 mA	25°C		60.7	80	
		Full			110	
	V _{IN} = 2.5 V, I _{OUT} = –200 mA	25°C		63.4	90	
		Full			120	
	V _{IN} = 1.8 V, I _{OUT} = –200 mA	25°C		74.2	100	
		Full			130	
UVLO Under voltage lockout	V _{IN} increasing, V _{ON} = 3.6 V, I _{OUT} = –100 mA	Full			1.2	V
	V _{IN} decreasing, V _{ON} = 3.6 V, I _{OUT} = –100 mA		0.50			
I _{ON} ON input leakage current	V _{ON} = 1.4 V to 5.25 V or GND	Full			1	μA
V _{RCP} Reverse Current Voltage Threshold	V _{OUT} > V _{IN}	25°C		54		mV
I _{RCP(leak)} Reverse Current Protection Leakage after Reverse Current event	V _{OUT} – V _{IN} > V _{RCP}	25°C		0.3		μA
t _{DELAY} Reverse Current Response Delay	V _{IN} = 5V			10		μs

(1) Verified by characterization, not production tested.

SWITCHING CHARACTERISTICS

PARAMETER		TEST CONDITION	TPS22912	UNIT
			TYP	
VIN = 5 V, TA = 25°C (unless otherwise noted)				
tON	Turn-ON time	RL = 10 Ω, CL = 0.1 μF	840	μs
tOFF	Turn-OFF time	RL = 10 Ω, CL = 0.1 μF	6.6	
tR	VOUT rise time	RL = 10 Ω, CL = 0.1 μF	912	
tF	VOUT fall time	RL = 10 Ω, CL = 0.1 μF	3	
VIN = 3.3 V, TA = 25°C (unless otherwise noted)				
tON	Turn-ON time	RL = 10 Ω, CL = 0.1 μF	1147	μs
tOFF	Turn-OFF time	RL = 10 Ω, CL = 0.1 μF	8.6	
tR	VOUT rise time	RL = 10 Ω, CL = 0.1 μF	1030	
tF	VOUT fall time	RL = 10 Ω, CL = 0.1 μF	3	
VIN = 1.5 V, TA = 25°C (unless otherwise noted)				
tON	Turn-ON time	RL = 10 Ω, CL = 0.1 μF	2513	μs
tOFF	Turn-OFF time	RL = 10 Ω, CL = 0.1 μF	17.4	
tR	VOUT rise time	RL = 10 Ω, CL = 0.1 μF	1970	
tF	VOUT fall time	RL = 10 Ω, CL = 0.1 μF	6.5	

PARAMETRIC MEASUREMENT INFORMATION

TEST CIRCUIT


(A) Rise and fall times of the control signal is 100ns.

A. Rise and fall times of the control signal are 100 ns.

Figure 1. Test Circuit and t_{ON}/t_{OFF} Waveforms

TYPICAL CHARACTERISTICS

ON-STATE RESISTANCE
vs
INPUT VOLTAGE

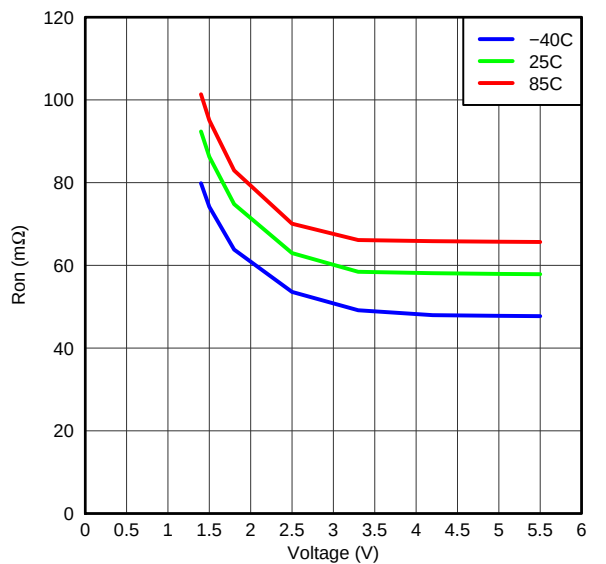


Figure 2.

ON INPUT THRESHOLD

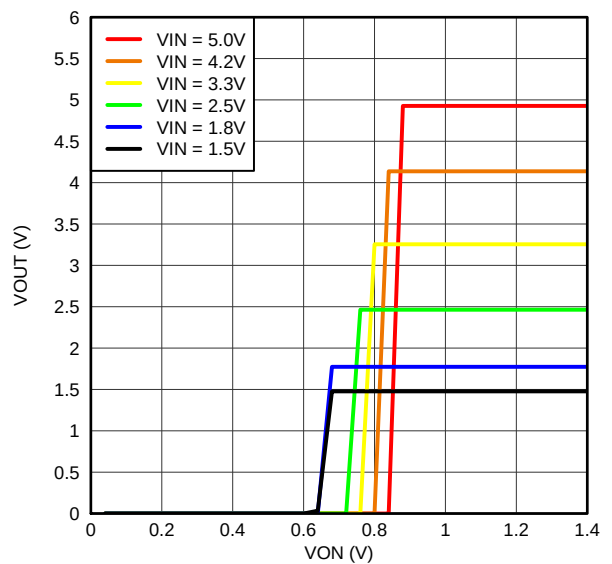


Figure 3.

INPUT CURRENT, QUIESCENT
vs
INPUT VOLTAGE

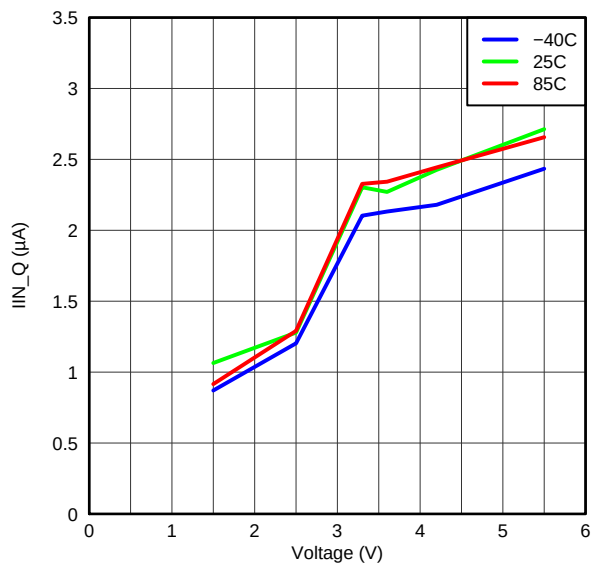


Figure 4.

INPUT CURRENT, LEAK
vs
INPUT VOLTAGE

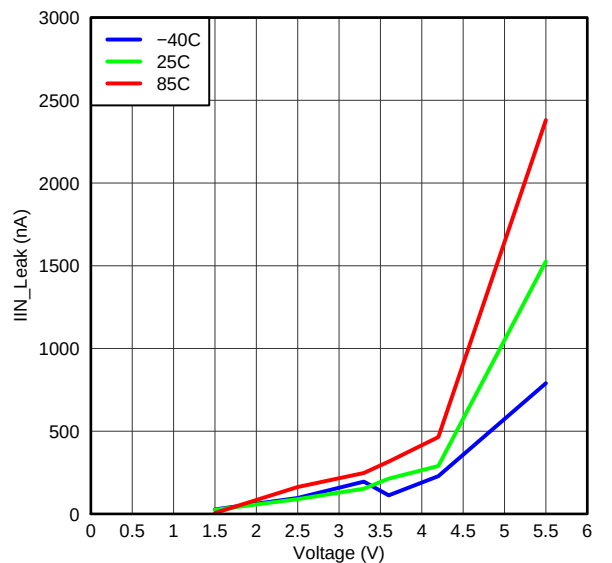


Figure 5.

TYPICAL CHARACTERISTICS (continued)

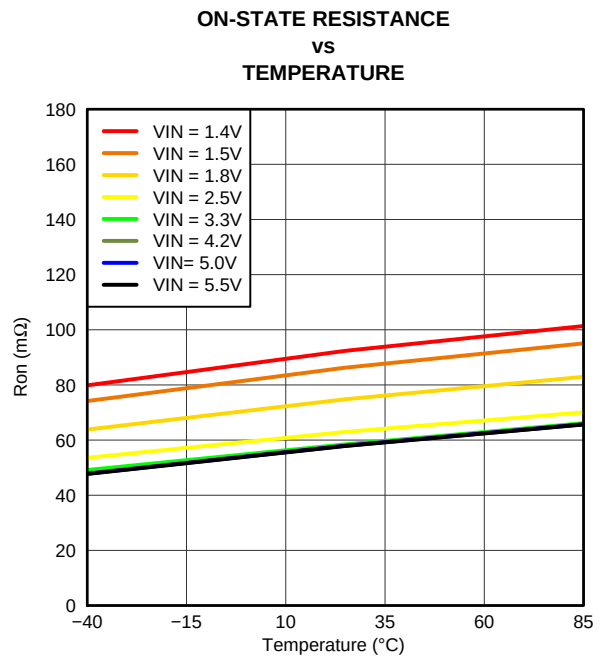


Figure 6.

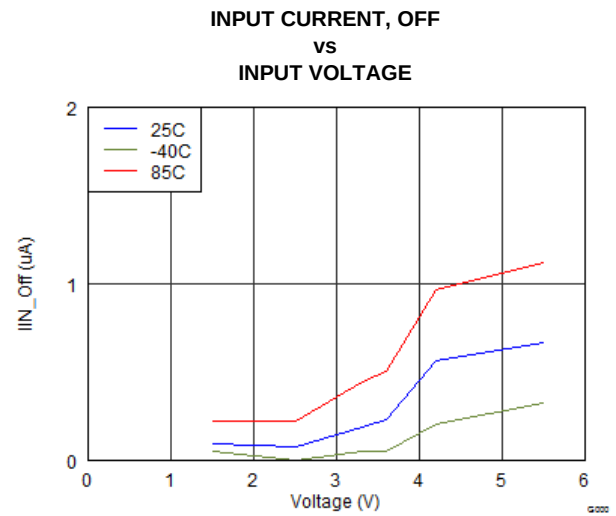


Figure 7.

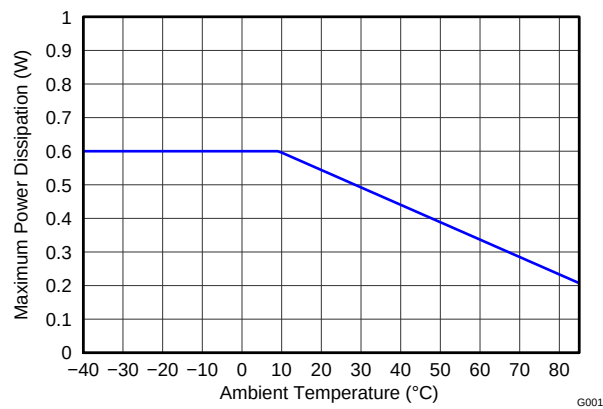


Figure 8. Allowable Power Dissipation

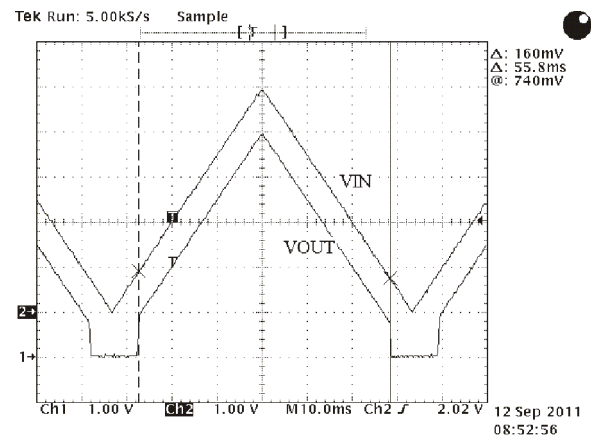


Figure 9. ULVO Response $I_{OUT} = -100\text{mA}$

TYPICAL CHARACTERISTICS (continued)

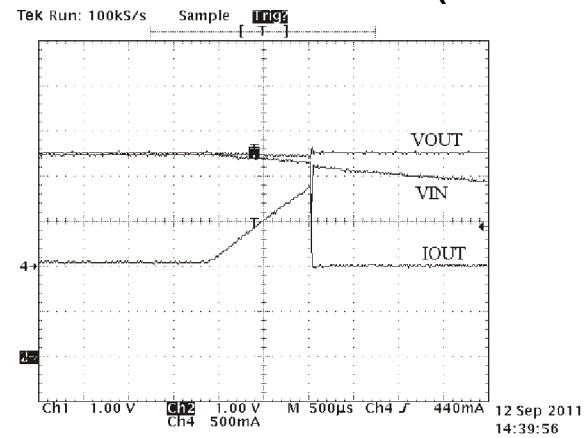


Figure 10. Reverse Current Protection $V_{OUT} = 3.3V$, $V_{IN} = 3.3V$ Decreasing to 0V

TYPICAL AC CHARACTERISTICS FOR TPS22912C

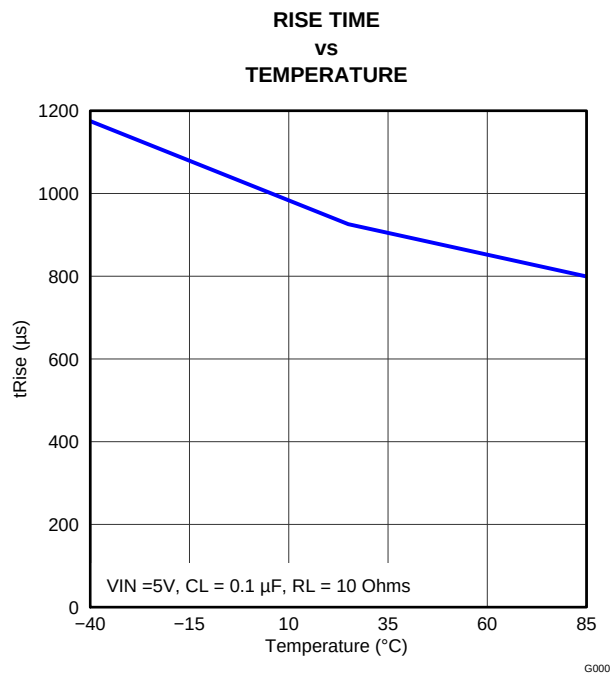


Figure 11.

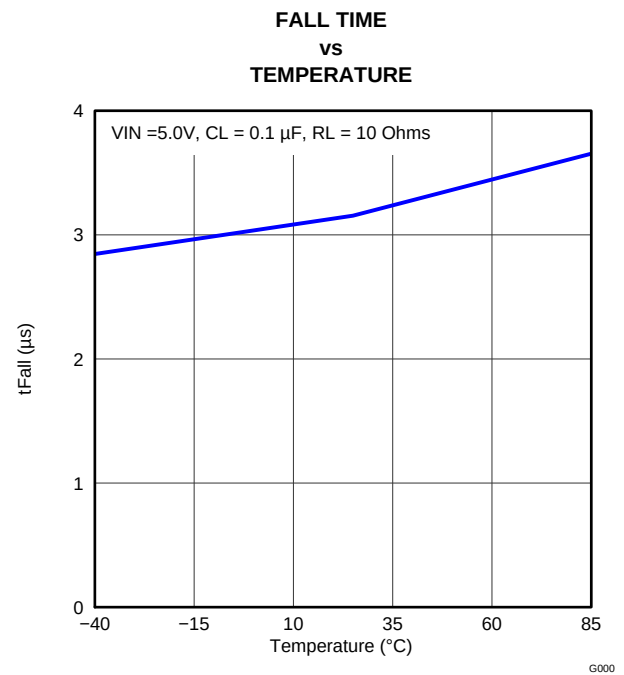


Figure 12.

TYPICAL CHARACTERISTICS (continued)

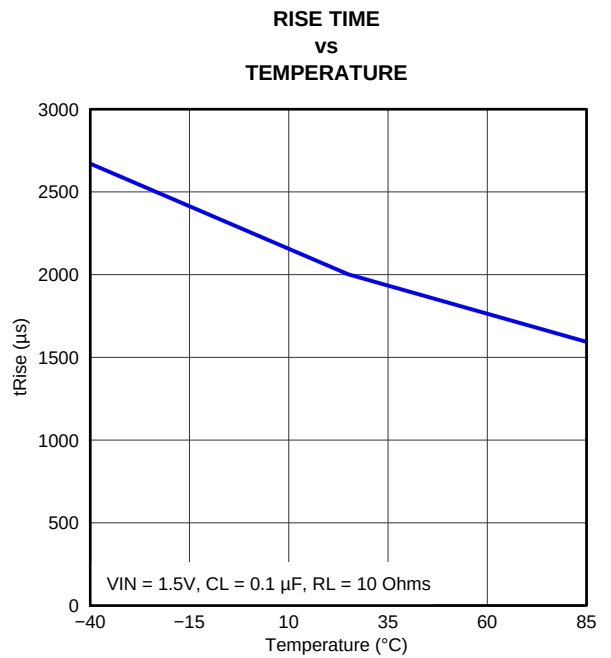


Figure 13.

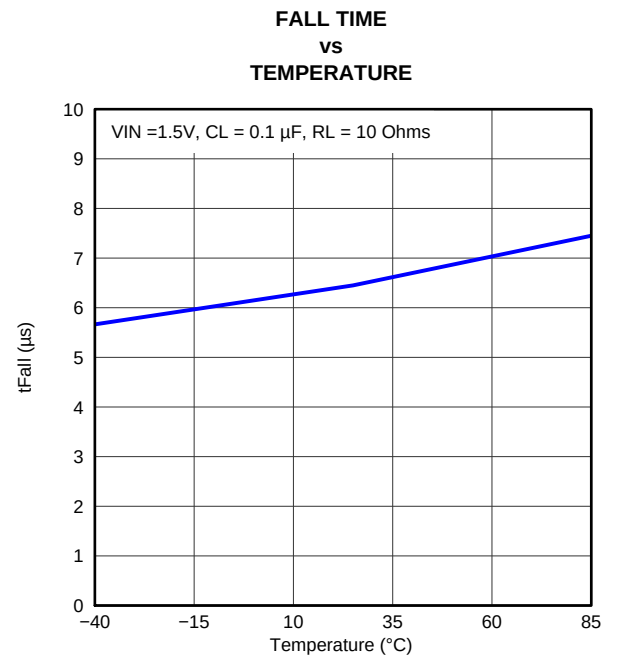


Figure 14.

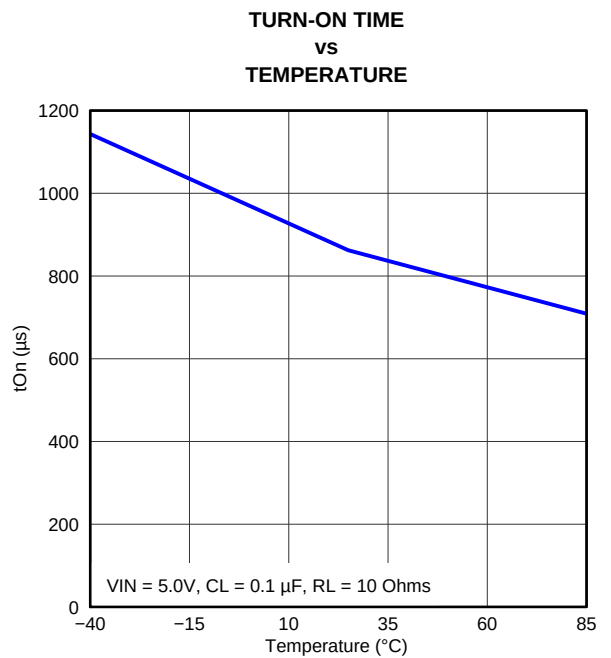


Figure 15.

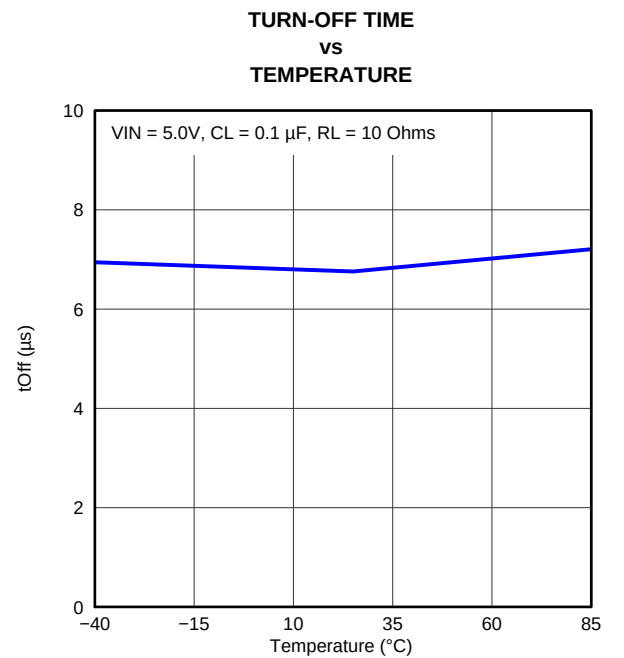


Figure 16.

TYPICAL CHARACTERISTICS (continued)

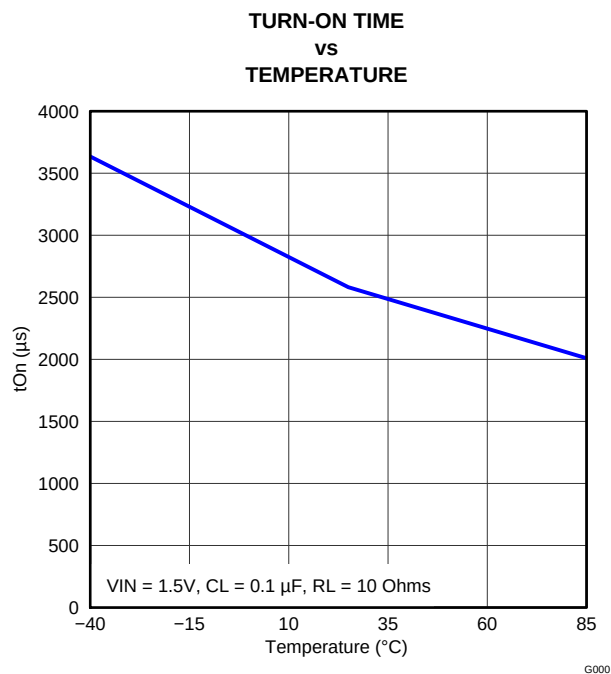


Figure 17.

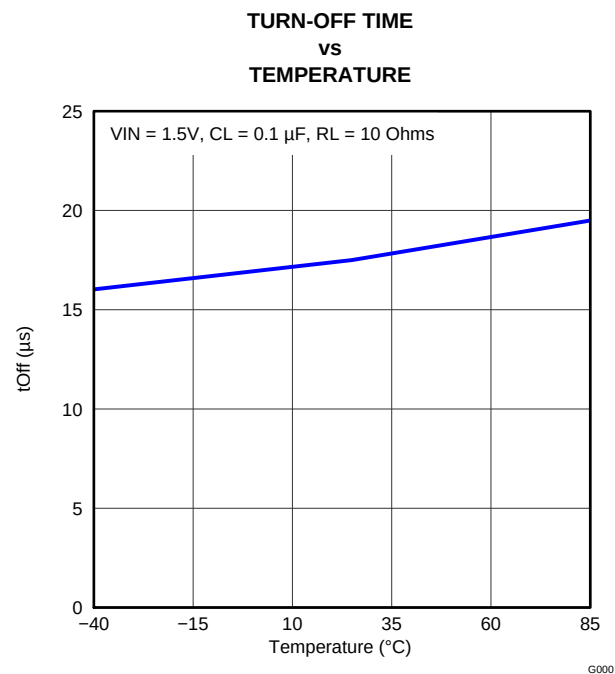


Figure 18.

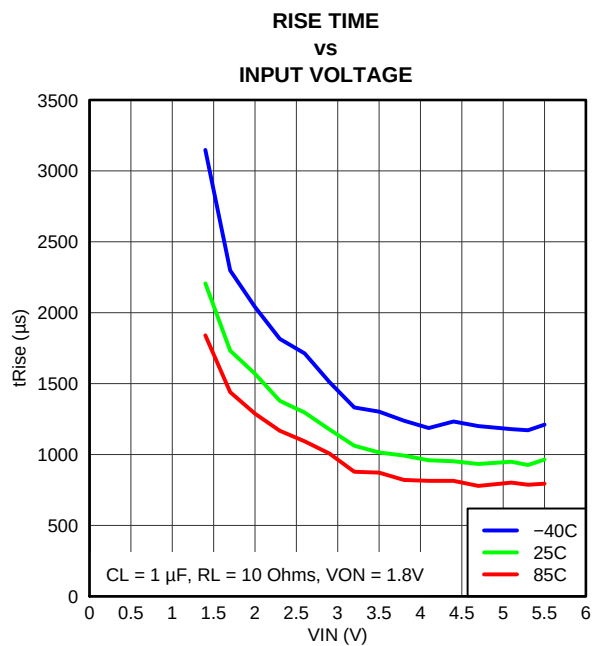


Figure 19.

TYPICAL CHARACTERISTICS (continued)

TURN-ON RESPONSE

$V_{IN} = 5V$, $T_A = 25^\circ C$, $C_{IN} = 1\mu F$, $C_L = 0.1\mu F$, $R_L = 10\Omega$

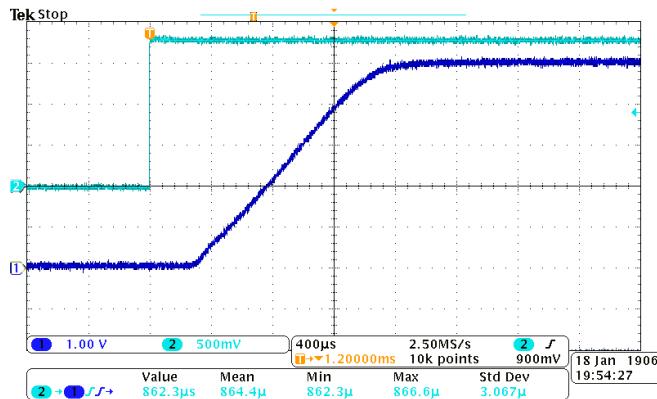


Figure 20.

TURN-OFF RESPONSE

$V_{IN} = 5V$, $T_A = 25^\circ C$, $C_{IN} = 1\mu F$, $C_L = 0.1\mu F$, $R_L = 10\Omega$

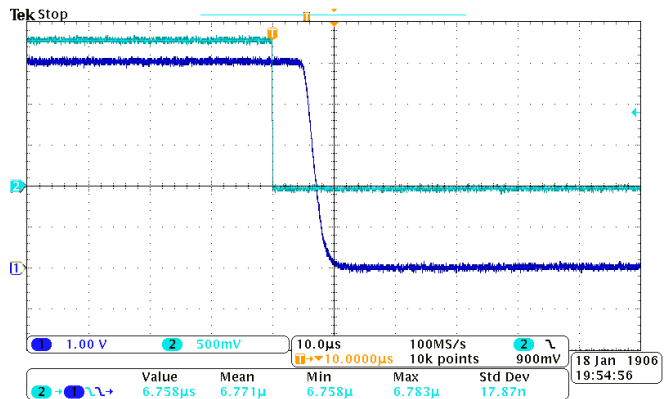


Figure 21.

TURN-ON RESPONSE TIME

$V_{IN} = 5V$, $T_A = 25^\circ C$, $C_{IN} = 10\mu F$, $C_L = 1\mu F$, $R_L = 10\Omega$

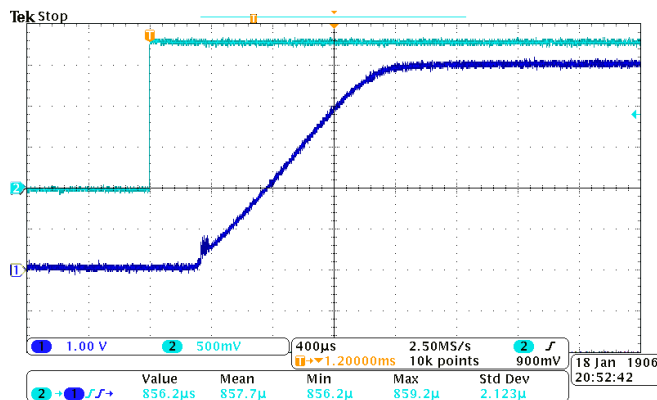


Figure 22.

TURN-OFF RESPONSE TIME

$V_{IN} = 5V$, $T_A = 25^\circ C$, $C_{IN} = 10\mu F$, $C_L = 1\mu F$, $R_L = 10\Omega$

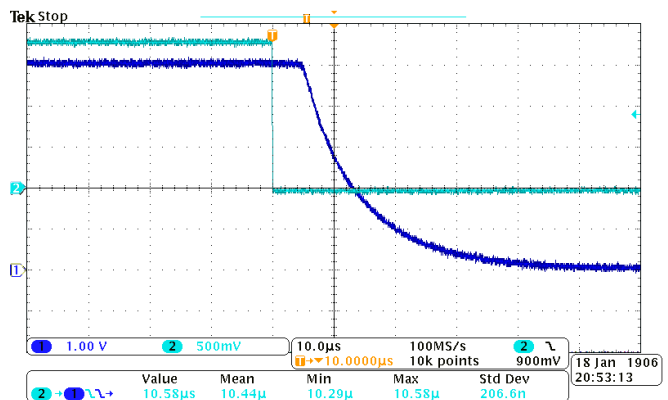


Figure 23.

TURN-ON RESPONSE TIME

$V_{IN} = 1.5V$, $T_A = 25^\circ C$, $C_{IN} = 1\mu F$, $C_L = 0.1\mu F$, $R_L = 10\Omega$

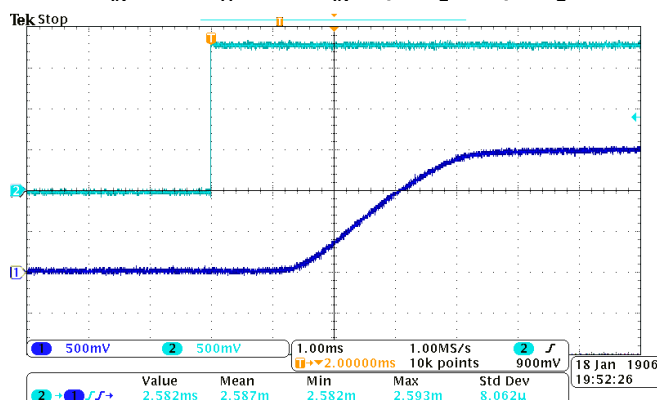


Figure 24.

TURN-OFF RESPONSE TIME

$V_{IN} = 1.5V$, $T_A = 25^\circ C$, $C_{IN} = 1\mu F$, $C_L = 0.1\mu F$, $R_L = 10\Omega$

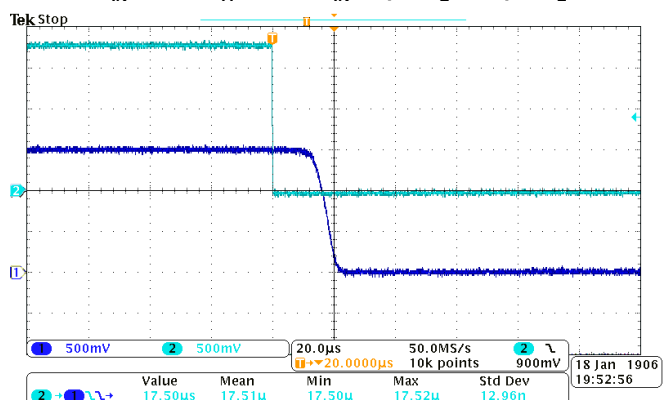


Figure 25.

TYPICAL CHARACTERISTICS (continued)

TURN-ON RESPONSE TIME

$V_{IN} = 1.5V$, $T_A = 25^\circ C$, $C_{IN} = 10\mu F$, $C_L = 1\mu F$, $R_L = 10\Omega$

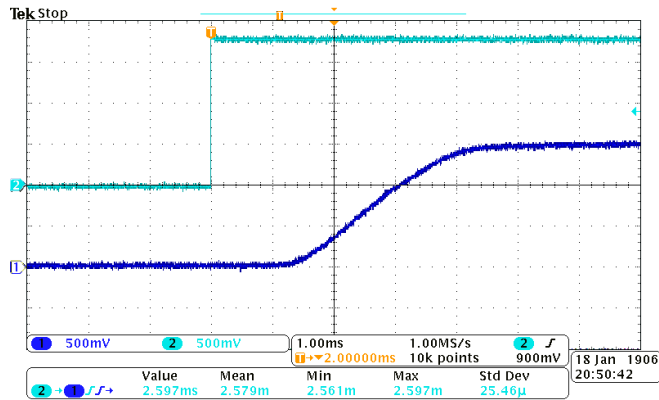


Figure 26.

TURN-OFF RESPONSE TIME

$V_{IN} = 1.5V$, $T_A = 25^\circ C$, $C_{IN} = 10\mu F$, $C_L = 1\mu F$, $R_L = 10\Omega$

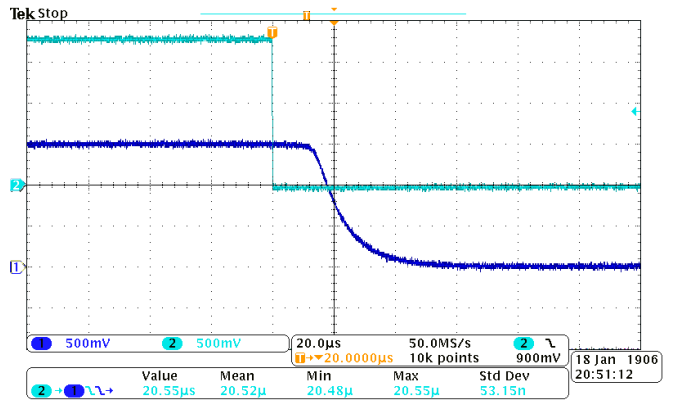


Figure 27.

APPLICATION INFORMATION

On/Off Control

The ON pin controls the state of the switch. Asserting ON high enables the switch. ON is active high and has a low threshold, making the pin capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2-V, 1.8-V, 2.5-V or 3.3-V GPIO.

Input Capacitor

To limit the voltage drop on the input supply caused by transient inrush currents, a capacitor needs to be placed between VIN and GND. A 1- μ F ceramic capacitor, C_{IN}, placed close to the pins is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop.

Output Capacitor

A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup. Devices with faster rise times may require a larger ratio to minimize V_{IN} dip.

Under-Voltage Lockout

Under-voltage lockout protection turns off the switch if the input voltage is below the under-voltage lockout threshold. During under-voltage lockout (UVLO), if the voltage level at V_{OUT} exceeds the voltage level at V_{IN} by the Reverse Current Voltage Threshold (V_{RVP}), the body diode will be disengaged to prevent any current flow to V_{IN}. With the ON pin active, the input voltage rising above the under-voltage lockout threshold will cause a controlled turn-on of the switch to limit current over-shoot.

Reverse Current Protection

In a scenario where V_{OUT} is greater than V_{IN} , there is potential for reverse current to flow through the pass FET or the body diode. The TPS22912 monitors V_{IN} and V_{OUT} voltage levels. When the reverse current voltage threshold (V_{RCP}) is exceeded, the switch is disabled (within 10 μ s typ). Additionally, the body diode is disengaged so as to prevent any reverse current flow to V_{IN} . The FET, and the output (V_{OUT}), will resume normal operation when the reverse current scenario is no longer present. The peak instantaneous reverse current is the current it takes to trip the reverse current protection. After the reverse current protection has tripped due to the peak instantaneous reverse current, the DC (off-state) leakage current from V_{OUT} and V_{IN} is referred to as $I_{RCP(LEAK)}$ (see figure below).

Use the following formula to calculate the amount of peak instantaneous reverse current for a particular application:

$$I_{RC} = \frac{V_{RCP}}{R_{ON(VIN)}}$$

Where,

I_{RC} is the amount of reverse current,

$R_{ON(VIN)}$ is the on-resistance at the V_{IN} of the reverse current condition.

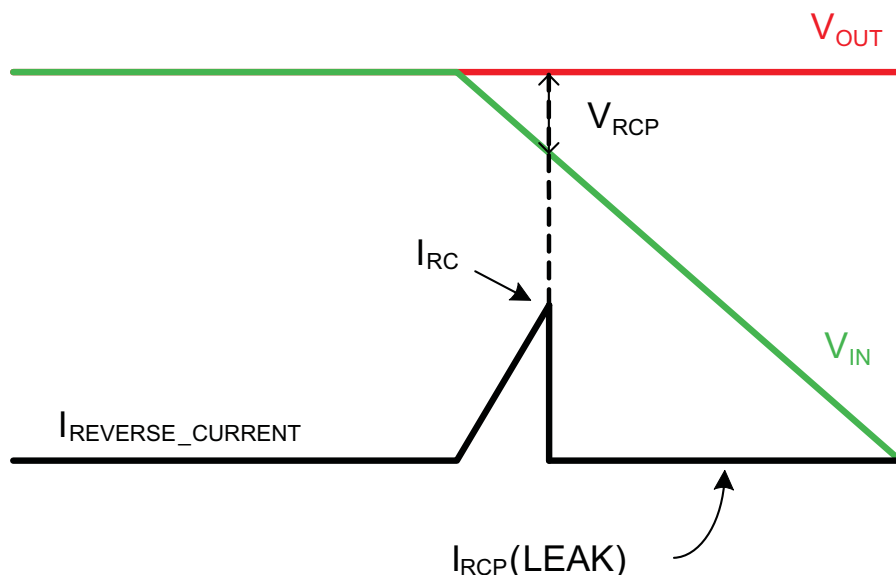


Figure 28. Reverse Current

Board Layout

For best performance, all traces should be as short as possible. The input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for V_{IN} , V_{OUT} , and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS22912CYZVR	Active	Production	DSBGA (YZV) 4	3000 LARGE T&R	Yes	SAC396	Level-1-260C-UNLIM	-40 to 85	78
TPS22912CYZVT	Active	Production	DSBGA (YZV) 4	250 SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	78

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

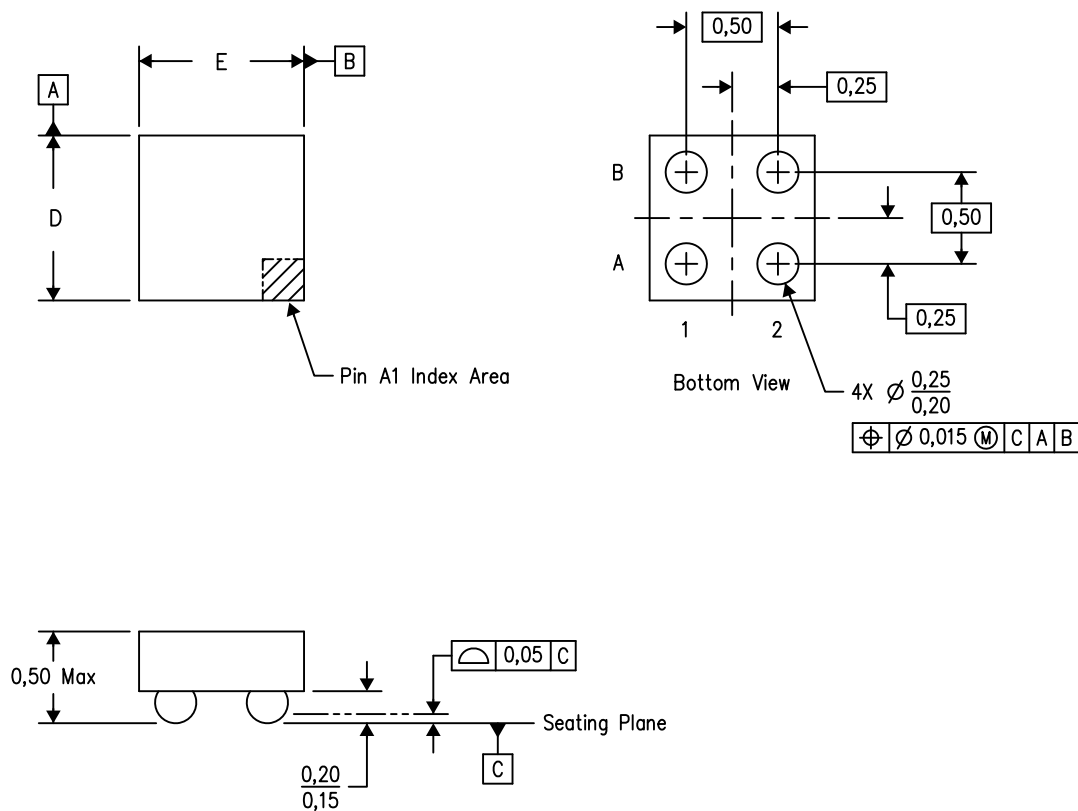
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

YZV (S-XBGA-N4)

DIE-SIZE BALL GRID ARRAY



4206083/C 07/13

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
版权所有 © 2025，德州仪器 (TI) 公司