JWH5046

17V/6A Synchronous Step-Down Converter

DESCRIPTION

The JW®H5046 is a current mode monolithic buck voltage converter. Operating with an input range of 4.5V-17V, the JWH5046 delivers 6A of continuous output current with two integrated N-Channel MOSFETs. The internal synchronous power switches provide high efficiency without the use of an external Schottky diode.

The JWH5046 guarantees robustness with short circuit protection, thermal protection, current run-away protection, output over-voltage protection and input under voltage lockout.

The JWH5046 is available in a QFN3.5x3.5-14 package, which provides a compact solution with minimal external components.

FEATURES

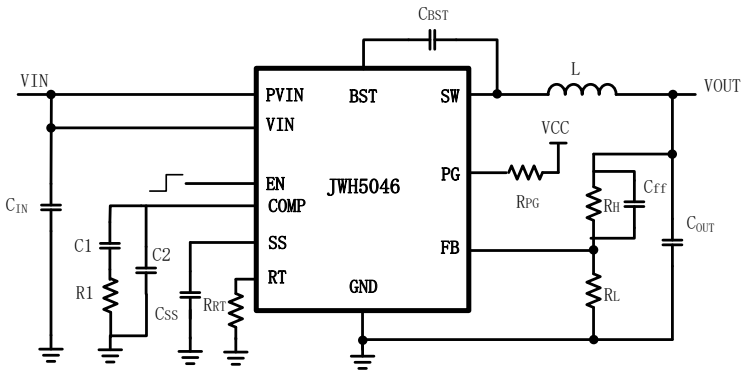
- 4.5V to 17V Operating Input Range
  6A Output Current
- 0.6V±1% FB Voltage Over-Temperature
- Adjustable Soft-start and Power Sequencing
- Adjustable Switching Frequency from 210kHz to 1.77MHz
- UV and OV Power Good Indicator
- Over Current Protection and Hiccup
- Output Over Voltage Protection
- Thermal Protection
- Available in QFN3.5x3.5-14 Package

APPLICATIONS

- Distributed Power Systems
- Networking Systems
- FPGA, DSP, ASIC Power Supplies
- Green Electronics/ Appliances
- Notebook Computers

TYPICAL APPLICATION

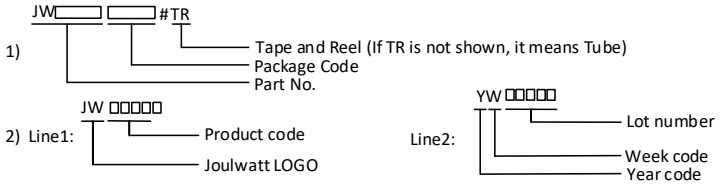
6A Step Down Regulators



ORDER INFORMATION

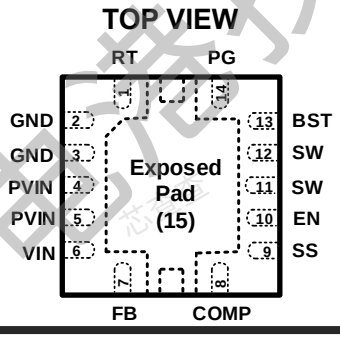
DEVICE[1)]	PACKAGE	TOP MARKING[2)]	ENVIRONMENTAL[3)]
JWH5046QFNZA#TR	QFN3.5x3.5-14	JWH5046 YW□□□□□	Green

Notes:



3) All Joulwatt products are packaged with Pb-free and Halogen-free materials and compliant to RoHS standards.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATING[1)]

VIN, PVIN, EN, Pins ..... -0.3V to 20V
SW Pin ..... -0.3V(-7V for 10ns, -10V for 5ns) to 20V(26V for 10ns)
BST Pin ..... SW-0.3V to SW+4V
RT, SS, COMP,FB Pins ..... -0.3V to 4V
PG Pin ..... -0.3V to 6V
Junction Temperature[2)] 150ºC
Lead Temperature 260ºC
Storage Temperature ..... -65ºC to +150 ºC
ESD (HBM) .....±2000V
ESD (CDM) .....±750V

RECOMMENDED OPERATING CONDITIONS[3)]

Input Voltage VIN .....4.5V to 17V
Output Voltage VOUT .....VOUT≤VIN×(T_{period}-300ns)/ T_{period}
Junction Temperature Range .....-40ºC to 125ºC
Ambient Temperature Range .....-40ºC to 85ºC

THERMAL PERFORMANCE[4)]

	θ_{JA}	θ_{Jcbot}	θ_{Jctop}
QFN3.5x3.5-14	40	1.8	34.4 ºC /W

Note:

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.

2) The JWH5046 includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

3) The device is not guaranteed to function outside of its operating conditions

4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

PVIN=12V, T_J=-40℃ to 125℃，Unless otherwise stated。

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
V_{IN} Under Voltage Lock-out Threshold	V_{IN_MIN}	V_{IN} rising		4.2	4.45	V
V_{IN} Under voltage Lockout Hysteresis	$V_{IN\_MIN\_HYST}$			250		mV
Shutdown Supply Current	I_{SD}	V_{EN}=0V			5	μA
Supply Current	I_Q	Non switching		380	460	μA
Feedback Voltage	V_{FB}		594	600	606	mV
Top Switch Resistance	$R_{DS(ON)T}$			20		mΩ
Bottom Switch Resistance	$R_{DS(ON)B}$			16		mΩ
Top Switch Leakage Current	I_{LEAK_TOP}	V_{IN}=17V, V_{EN}=0V, V_{SW}=0V			2	μA
Bottom Switch Leakage Current	I_{LEAK_BOT}	V_{IN}=17V, V_{EN}=0V, V_{SW}=17V			2	μA
Top Switch Current Limit	I_{LIM_TOP}		8	11	14	A
Bottom Switch Current Limit	I_{LIM_BOT}		6.5	9.5	12.5	A
Negative Current Limit	I_{LIM_NEG}		-2.5	-4	-5.5	A
Minimum On Time[5)]	T_{ON_MIN}			100		ns
Minimum Off Time	T_{OFF_MIN}	V_{FB}=0.42V		130		ns
EN Rising Threshold	V_{EN_H}	V_{EN} rising		1.22	1.26	V
EN Falling Threshold	V_{EN_L}	V_{EN} falling	1.1	1.17		V
EN Pull Up Current	I_{ENPULL}	EN = 1.1 V		1.4		uA
EN Hysteresis Current	$I_{EN\ HYS}$	EN = 1.3 V		3.3		uA
Minimum Switching Frequency	fsw_min	R_{RT}=240K(1%)	170	210	250	kHz
Switching Frequency	fsw	R_{RT}=100K(1%)	430	510	590	kHz
Maximum Switching Frequency	fsw_max	R_{RT}=29K(1%)	1550	1770	1980	kHz
Error Amplifier Transconductance	g_M			1300		uA/V
Error Amplifier DC Gain[5)]	Gain			3100		V/V
Error Amplifier Source/Sink	I_{EA}			165		uA
COMP to SW Current Transconductance	g_{CS}			16		A/V
Power Good Upper Threshold	PG_{TH_Upper}	FB rising		106%		V_{REF}
		FB falling		104%		V_{REF}
Power Good Lower Threshold	PG_{TH_lower}	FB rising		94%		V_{REF}
		FB falling		92%		V_{REF}
Power Good Sink Current	I_{PG}	PG=0.3V	2			mA
Minimum Vin for Valid PG Output	V_{IN_PG}			0.8	1	V

Minimum SS Voltage for PG	V_{SS_PG}				1.4	V
Soft-start Charge Current	I_{ss_CHAR}			2.3		uA
Thermal Shutdown[5)]	T_{TSD}			175		°C
Thermal Shutdown Hysteresis[5)]	T_{TSD_HYST}			10		°C
Thermal Shutdown Hiccup Time[5)]	T_{TSD_Time}			16384		cycle

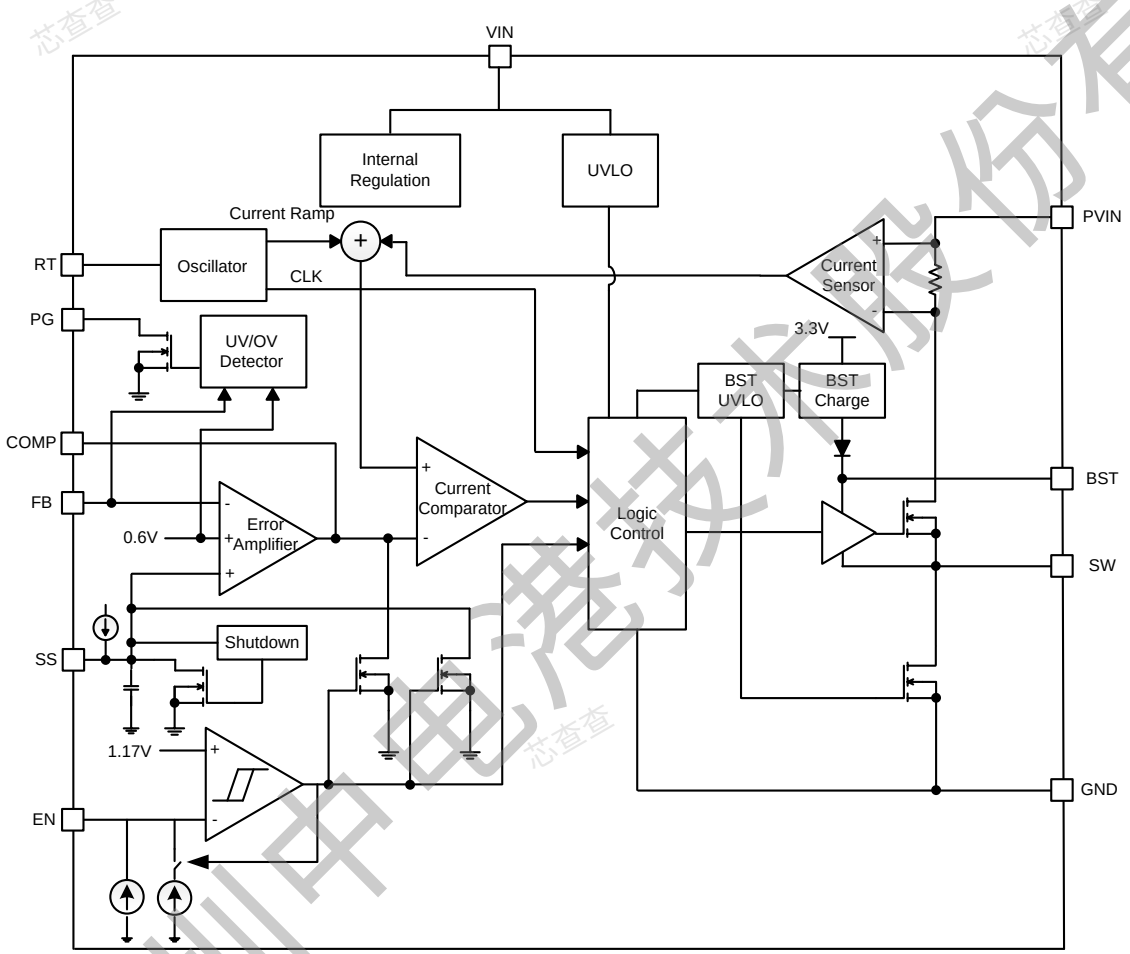
Note:

5) Guaranteed by design.

PIN DESCRIPTION

QFN3.5x3.5-14	Name	Description
1	RT	Switching frequency program. Connect an external resistor from RT pin to ground to set the switching frequency.
2,3	GND	Ground.
4,5	PVIN	Power input. Supplies the power switches of the power converter
6	VIN	Supplies the control circuitry of the power converter.
7	FB	Output feedback pin. FB senses the output voltage and is regulated by the control loop to 600mV. Connect a resistive divider at FB.
8	COMP	Error amplifier output and input to the output switch current (PWM) comparator. Connect frequency compensation components to this pin.
9	SS	Soft-start control pin. Connect to a capacitor to set soft start time.
10	EN	Drive EN pin high to turn on the regulator and low to turn off the regulator.
11,12	SW	SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
13	BST	Bootstrap pin for top switch.
14	PG	Open drain output for power-good flag. Use a 10kΩ to 100kΩ pull-up resistor to logic rail or other DC voltage no higher than 5V.
15	Exposed Thermal PAD	Thermal pad of the package and signal ground and it must be soldered down for proper operation.

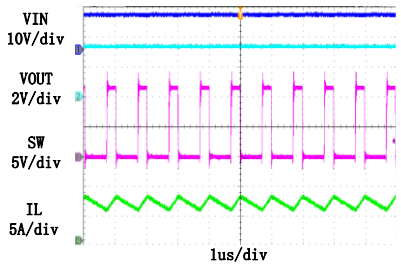
BLOCK DIAGRAM



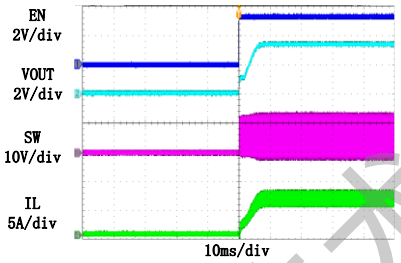
TYPICAL PERFORMANCE CHARACTERISTICS

VIN = 12V, VOUT = 3.3V, L = 1μH, C_{OUT} = 47μF×2, T_A = +25°C, unless otherwise noted.

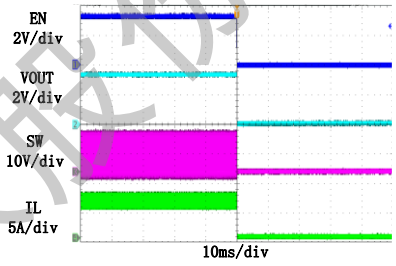
Steady State Test
VIN=12V, VOUT=3.3V
IOUT=6A



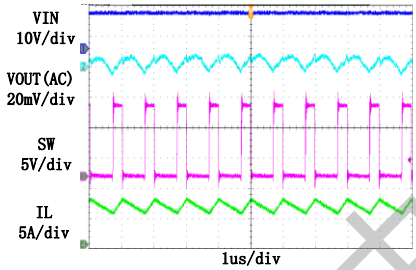
Startup through Enable
VIN=12V, VOUT=3.3V
IOUT=6A (Resistive load)



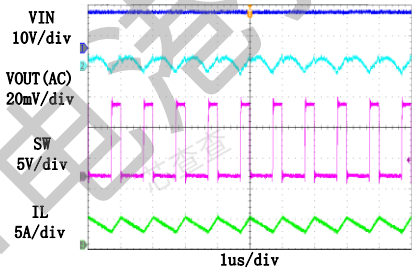
Shutdown through Enable
VIN=12V, VOUT=3.3V
IOUT=6A (Resistive load)



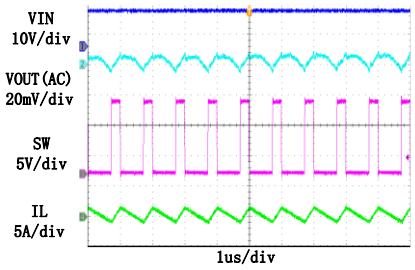
Heavy Load Operation
6A LOAD



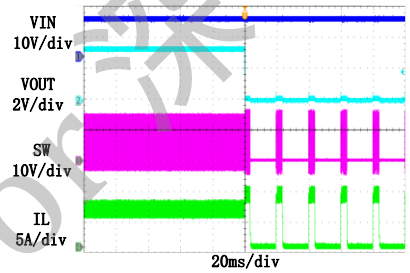
Medium Load Operation
3A LOAD



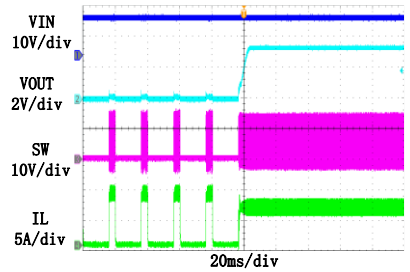
Light Load Operation
0A LOAD



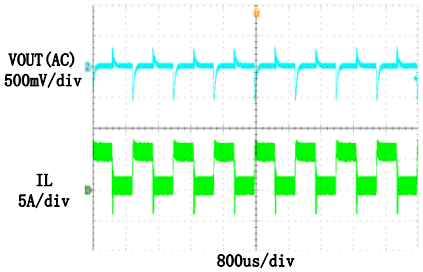
Short Circuit Protection
VIN=12V, VOUT=3.3V
IOUT=6A→Short



Short Circuit Recovery
VIN=12V, VOUT=3.3V
IOUT=Short→6A



Load Transient
VIN=12V, VOUT=3.3V
0.6A LOAD→6A LOAD→0.6A LOAD



TYPICAL PERFORMANCE CHARACTERISTICS

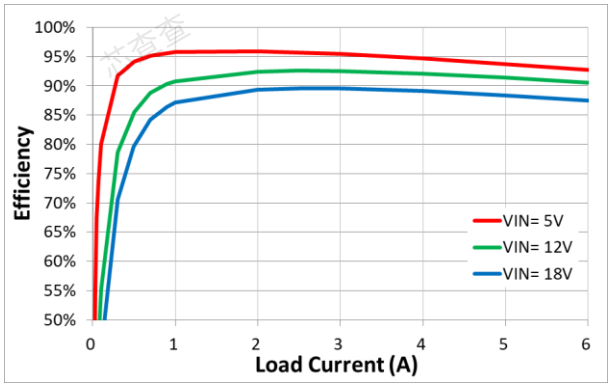


Figure 1. Efficiency vs. Load Current

(VOUT=3.3V, L=1μH)

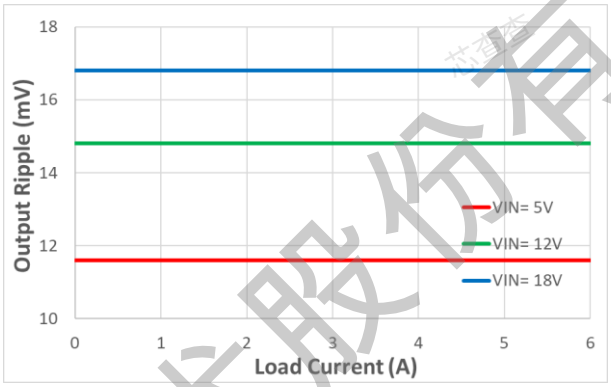


Figure 2. Output Ripple vs. Load Current

(VOUT=3.3V, L=1μH)

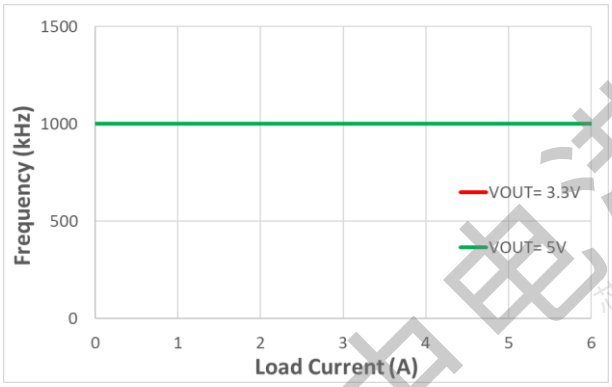


Figure 3. Frequency vs. Load Current

(VIN=12V, L=1μH)

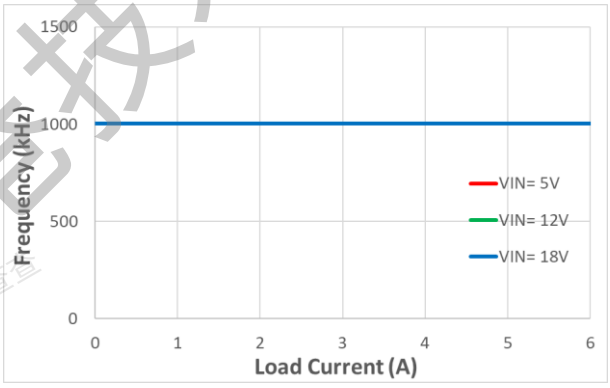


Figure 4. Frequency vs. Load Current

(VOUT=3.3V, L=1μH)

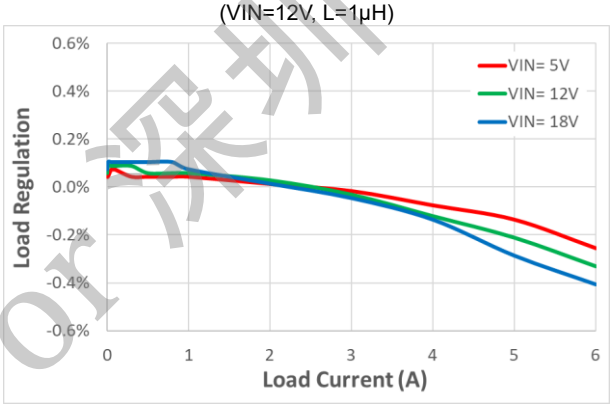


Figure 5. Load Regulation

(VOUT=3.3V, L=1μH)

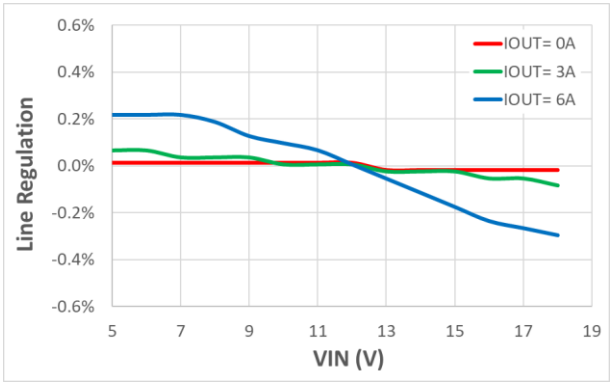


Figure 6. Line Regulation

(VOUT=3.3V, L=1μH)

TYPICAL PERFORMANCE CHARACTERISTICS

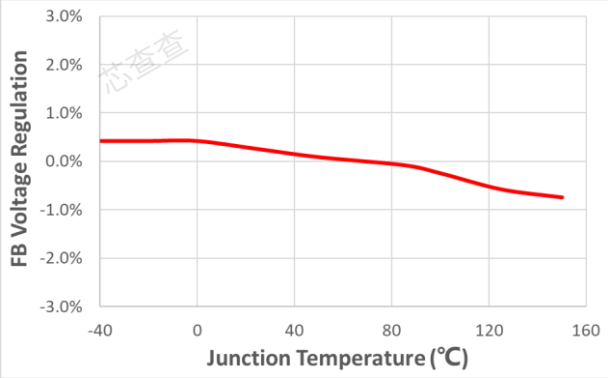


Figure 7. FB Voltage Regulaion vs. Junction Temperature

FUNCTIONAL DESCRIPTION

The JWH5046 is a synchronous, current-mode, step-down regulator. It regulates input voltages from 4.5V to 17V down to an output voltage as low as 0.6V, and is capable of supplying up to 6A of load current.

Power Switch

N-Channel MOSFET switches are integrated in the JWH5046 to down convert the input voltage to the regulated output voltage. Since the top MOSFET needs a gate voltage greater than the input voltage, a boost capacitor connected between BST and SW pins is required to drive the gate of the top switch. The boost capacitor is charged by the internal 3.3V rail when SW is low.

Current-Mode Control

The JWH5046 utilizes fixed frequency, peak current-mode control to regulate the output voltage. The output voltage is measured at the FB pin through a resistive voltage divider and the error is amplified by the internal transconductance error amplifier. The voltage feedback loop is compensated by an external RC network connected between the COMP pin and GND pin.

An internal oscillator initiates the turn on of the high side power switch, and the error amplifier output at the COMP pin controls the high side power switch current that When the high side MOSFET switch current reaches the threshold level set by the COMP voltage, the power switch is turned off.

The COMP pin voltage will increase and decrease as the output current increases and decreases. The device is implemented current limiting by clamping the COMP pin voltage to a maximum level.

Slope Compensation

The JWH5046 adds a compensating ramp to the COMP voltage to prevent sub-harmonic oscillations at duty cycles greater than 50%. The peak current limit of the high side switch is not affected by the slope compensation and remains constant over the full duty cycle range.

Shut-Down Mode

The JWH5046 shuts down when voltage at EN pin is below 1.17V. The entire regulator is off and the supply current consumed by the JWH5046 drops below 5uA.

Enable and Adjustable UVLO Protection

The JWH5046 is enabled when the VIN pin voltage rises above 4.2V and the EN pin voltage exceeds the enable threshold of 1.22V. The JWH5046 is disabled when the VIN pin voltage falls below 3.95V or when the EN pin voltage is below 1.17V. The EN pin has an internal pull-up current that enables operation of the JWH5046 when the EN pin floats.

If an application requires a higher VIN under-voltage lockout (UVLO) threshold, use a resistive divider connected between VIN and ground with the central tap connected to EN to adjust the input voltage UVLO. (Shown in Figure 8). So that when VIN rises to the pre-set value, EN rises above 1.22V to enable the device and when Vin drops below the pre-set value, EN drops below 1.17V to trigger input under voltage lockout protection.

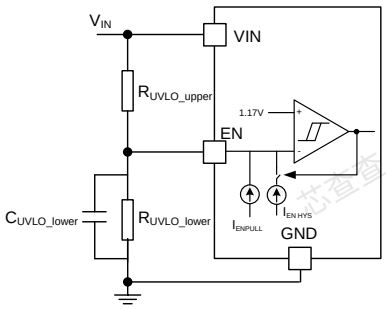


Figure 8 Adjustable UVLO

The input voltage UVLO threshold (V_{UVLO}) and hysteresis (V_{UVLO_HYS}) can be calculated by the following equation.

$$V_{UVLO} = \frac{R_{UVLO\_upper} + R_{UVLO\_lower}}{R_{UVLO\_lower}} \times (V_{EN\_TH} - I_{ENPULL} \times \frac{R_{UVLO\_upper} \times R_{UVLO\_lower}}{R_{UVLO\_upper} + R_{UVLO\_lower}})$$

$$V_{UVLO\_HYS} = \frac{R_{UVLO\_upper} + R_{UVLO\_lower}}{R_{UVLO\_lower}} \times (V_{EN\_HYS} + I_{ENHYS} \times \frac{R_{UVLO\_upper} \times R_{UVLO\_lower}}{R_{UVLO\_upper} + R_{UVLO\_lower}})$$

where

V_{EN_TH} is enable shutdown threshold (1.22V typ.);

V_{EN_HYS} is enable shutdown hysteresis (50mV typ.).

In order to ensure the proper V_{UVLO} and V_{UVLO_HYS}, 30kΩ is recommended for R_{UVLO_lower}. In addition, it is recommended to add pF level ceramic capacitor in parallel with R_{UVLO_LOWER} for low frequency. The following table lists the recommended values.

f_{SW} (kHz)	R_{UVLO_lower} (kΩ)	C_{UVLO_lower} (pF)
1000	30	NC
700	30	51
400	30	100

External Soft-start

Soft-start is designed in JWH5046 to prevent the converter output voltage from overshooting during startup and short-circuit recovery. An internal current source (I_{SS}) of 2.3uA is designed to charge the external soft-start capacitor (C_{SS}) and generates a soft-start (SS) voltage. When it is less than internal reference voltage (V_{REF}, typ. 0.6V), SS voltage overrides V_{REF} and the error amplifier uses SS voltage as the reference. When SS exceeds V_{REF}, V_{REF} regains control.

The soft start time (10% to 90%) T_{SS} can be calculated by the following equation.

$$T_{SS}(ms) = \frac{C_{SS}(nF) \cdot V_{REF}(V) \cdot 0.8}{I_{SS}(\mu A)}$$

Switching Frequency

The switching frequency of JWH5046 can be programmed by the resistor R_T from the RT pin and GND pin over a wide range from 210 kHz to 1770 kHz. The RT pin voltage is typically 1.2V and must have a resistor to ground to set the switching frequency. The R_T resistance can be calculated by the following equation for a given switching frequency f_{SW}.

$$R_T(k\Omega) = 48000 \times f_{SW}(kHz)^{-0.997} - 2$$

To reduce the solution size one would typically set the switching frequency as high as possible, but tradeoffs of the conversion efficiency, maximum input voltage and minimum controllable on time should be considered. The minimum controllable on time is typically 100 ns which limit the maximum operating frequency in applications with high input to output step down ratios.

Output Current Run-Away Protection

At start-up, due to the high voltage at input and low voltage at output, current inertia of the output inductance can be easily built up, resulting in a large start-up output current. A valley current limit is designed in the JWH5046 so that only when output current drops below the valley current limit can the top power switch be turned on. By such control mechanism, the output current at start-up is well controlled.

Over Current Protection and Hiccup

JWH5046 has a cycle-by-cycle current limit. When the inductor current triggers current limit and lasts for more than 512 switching cycles, JWH5046 enters hiccup mode and periodically restart the chip after 16384 cycles.

JWH5046 will exit hiccup mode while not triggering current limit.

Power Good

The JWH5046 has power-good (PG) output. The PG pin is the open drain of a MOSFET. Connect to a voltage source (such as V_{OUT}) through a resistor. When the output voltage becomes within +4% and -6% of the target value, internal comparators detect power good state and the power good signal becomes high. If the feedback voltage goes under -8% or higher 6% of the target value, the power good signal becomes low.

Overvoltage Protection

Output overvoltage protection (OVP) is designed in JWH5046 to minimize voltage overshoot when recovering from output fault conditions or strong unload transients in designs with low output capacitance and the power supply output voltage increase faster than the response of the error amplifier output resulting in an output overshoot.

The OVP feature minimizes output overshoot when using a low value output capacitor by comparing the FB pin voltage to the rising OVP threshold which is nominally 106% of the internal voltage reference. If the FB pin voltage is greater than the rising OVP threshold, the high side MOSFET is immediately disabled to minimize output overshoot. When the FB voltage drops below the falling OVP threshold which is nominally 104% of the internal voltage reference, the high side MOSFET resumes normal operation.

Thermal Protection

When the temperature of the JWH5046 rises above 175°C, it is forced into thermal shut-down. Only when core temperature drops below 165°C and after 16384 cycles can the regulator become active again.

APPLICATION INFORMATION

Output Voltage Set

The output voltage is determined by the resistor divider connected at the FB pin, and the voltage ratio is:

$$V_{FB} = V_{OUT} \times \frac{R_L}{R_H + R_L}$$

where V_{FB} is the feedback voltage and V_{OUT} is the output voltage.

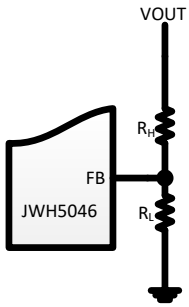


Figure 9. Output Voltage Set

To improve efficiency at very light loads consider using larger value resistors. However, using too high of resistance causes the circuit to be more susceptible to noise and voltage errors from the V_{FB} input current will be more noticeable.

Choose R_L around 15kΩ~30kΩ, and then R_H can be calculated by:

$$R_H = R_L \times \left(\frac{V_{out}}{0.6} - 1 \right)$$

The following table lists the recommended values.

VOUT (V)	R_L (kΩ)	R_H (kΩ)
5	15	110
3.3	15	68
0.8	30	10

Input Capacitor

The input capacitor is used to supply the AC input current to the step-down converter and maintaining the DC input voltage. Estimate the RMS current in the input capacitor with:

$$I_{C_{IN}} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

where I_{OUT} is the load current, V_{OUT} is the output voltage, V_{IN} is the input voltage.

Thus, the input capacitor can be calculated by the following equation when the input ripple voltage is determined.

$$C_{IN} = \frac{I_{OUT}}{f_{SW} \times \Delta V_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where C_{IN} is the input capacitance value, f_{SW} is the switching frequency, $\triangle V_{IN}$ is the input ripple voltage.

The input capacitor can be electrolytic, tantalum or ceramic. To minimizing the potential noise, a small X5R or X7R ceramic capacitor, i.e., 0.1uF, should be placed as close to the IC as possible when using electrolytic capacitors.

A 32uF ceramic capacitor (22uF+10uF) is recommended in typical application, and an extra 47uF electrolytic capacitor is needed if hot-plug is required.

Output Capacitor

The output capacitor is required to maintain the DC output voltage, and the capacitance value determines the output ripple voltage. The output voltage ripple can be calculated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right)$$

where COUT is the output capacitance value and RESR is the equivalent series resistance value of the output capacitor.

The output capacitor can be low ESR electrolytic, tantalum or ceramic, which lower ESR capacitors get lower output ripple voltage.

The output capacitors also affect the system stability and transient response, and a 94uF ceramic capacitor (47uF×2) is recommended in typical application.

Inductor

The inductor is used to supply constant current to the output load, and the value determines the ripple current which affect the efficiency and the output voltage ripple. The ripple current is typically allowed to be 30% of the maximum switch current limit, thus the inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where VIN is the input voltage, VOUT is the output voltage, f_{SW} is the switching frequency, and △IL is the peak-to-peak inductor ripple current.

Generally, when the duty is larger than 0.5, in order to avoid sub-harmonic oscillation, the inductance and switching frequency should preferably meet the following formula:

$$f_{SW} \cdot L \geq \frac{V_{OUT}}{8}$$

Meanwhile, if the off time of high side MOSFET is less than 350ns, the inductance and switching frequency should preferably meet the following formula:

$$f_{SW} \cdot L \geq \frac{V_{OUT}}{4}$$

External Bootstrap Capacitor

The bootstrap capacitor is required to supply voltage to the top switch driver. A 0.1μF~1μF low ESR ceramic capacitor is recommended to connected to the BST pin and SW pin.

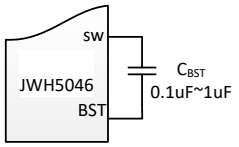


Figure 10. External Bootstrap Capacitor

Power Good

JoulWatt recommends using a 10kΩ to 100kΩ pull-up resistor (R_{PG}) to logic rail or other DC voltage (VCC) no higher than 5V.

Compensation Network Design

In order to ensure stable operation while maximizing the dynamic performance, the appropriate loop compensation is important. Generally, follow the steps below to calculate the compensation components:

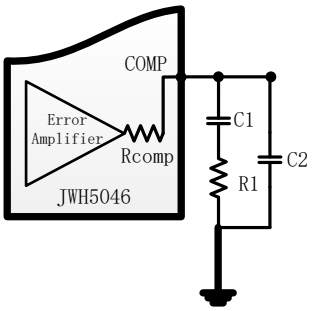


Figure 11. Compensation Network

1. Set up the crossover frequency, f_C. In general, one-twentieth to one-sixth of the switching frequency is recommended to be the crossover frequency.

2. R_1 can be determined by:

$$R_1 = \frac{2\pi \times f_C \times C_{OUT}}{g_M \times g_{CS}} \times \frac{R_L + R_H}{R_L} - R_{comp}$$

where g_M=1300uA/V, g_{CS}=16A/V，R_{comp}=500Ω.

3. A compensation zero can be placed at or before the dominant pole of buck which is provided by output capacitor and maximum output loading (R_{LOAD}). Calculate C_1:

$$C_1 = \frac{C_{OUT} \times R_{LOAD}}{R_1 + R_{comp}}$$

4. The compensation pole is set to the frequency at the ESR zero or 1/2 of the operating frequency. Output capacitor and its ESR provide a zero, and optional C_2 can be used to cancel this zero. Calculate C_2:

$$C_2 = \frac{C_{OUT} \times R_{ESR}}{R_1}$$

If 1/2 of the operating frequency is lower than the ESR zero, the compensation pole is set at 1/2 of the operating frequency. Calculate C_2:

$$C_2 = \frac{1}{2\pi \times \frac{f_{SW}}{2} \times R_1}$$

5. Generally, C_2 is an optional component used to enhance noise immunity.

PCB Layout Note

For minimum noise problem and best operating performance, the PCB is preferred to following the guidelines as reference.

1. Place the input decoupling capacitor as close to JWH5046 (VIN pin and GND) as possible to eliminate noise at the input pin. The loop area formed by input capacitor and GND must be minimized.
2. Put the feedback trace as short as possible, and far away from the inductor and noisy power traces like SW node.

3. Keep the switching node SW short to prevent excessive capacitive coupling

4. Make VIN, VOUT and ground bus connections as wide as possible. This reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.

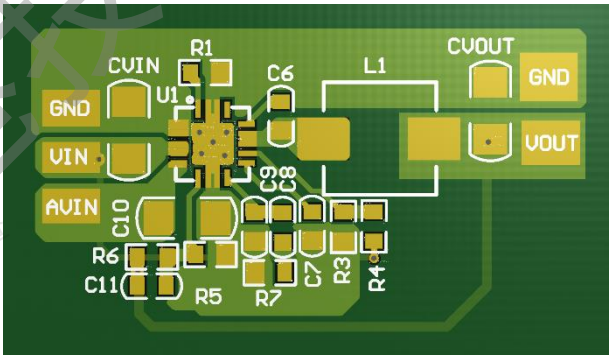
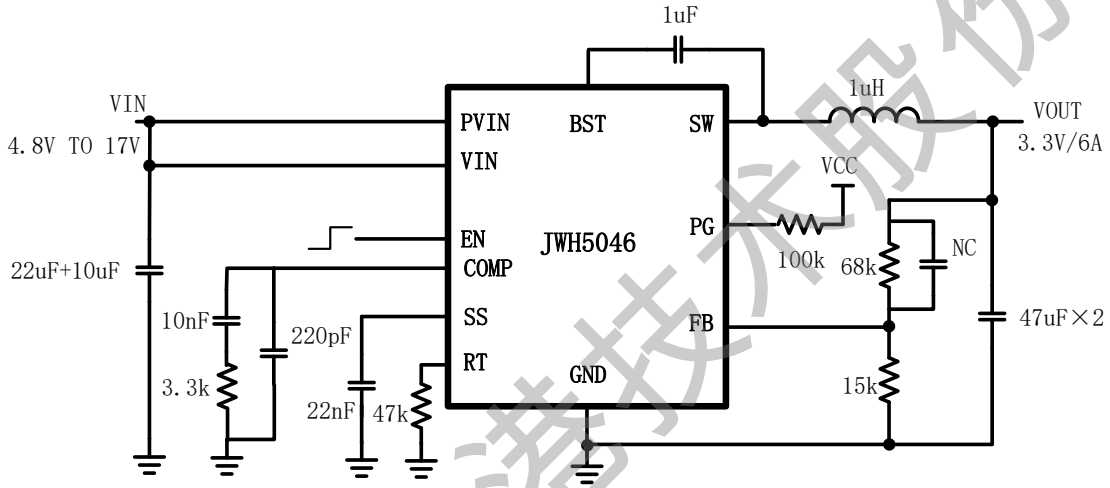


Figure 12. PCB Layout Recommendation

REFERENCE DESIGN

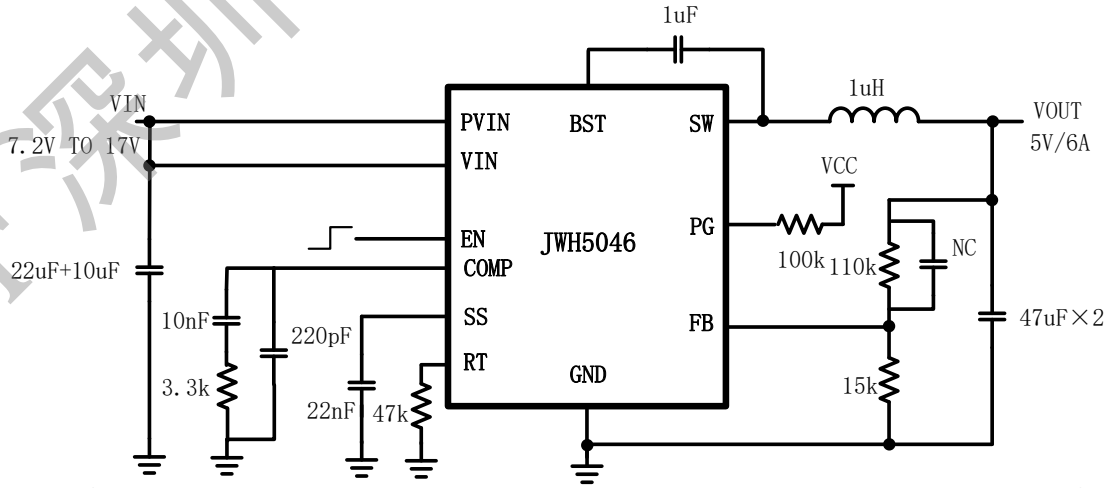
Reference 1：

VIN: 4.8V ~ 17V
VOUT: 3.3V
IOUT: 0 ~ 6A



Reference 2：

VIN: 7.2V ~ 17V
VOUT: 5V
IOUT: 0 ~ 6A

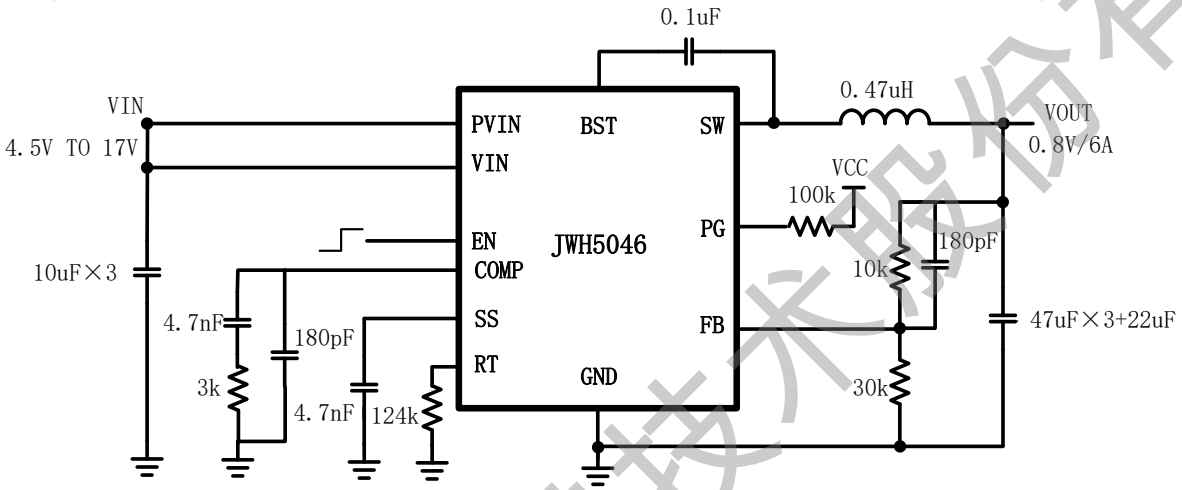


Reference 3：

VIN: 4.5V ~ 17V

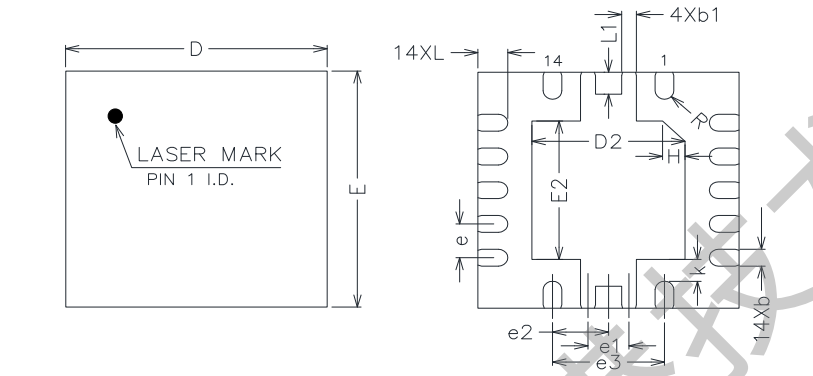
VOUT: 0.8V

IOUT: 0 ~ 6A

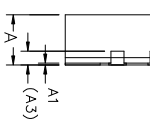


PACKAGE OUTLINE

QFN3.5x3.5-14 Unit: mm

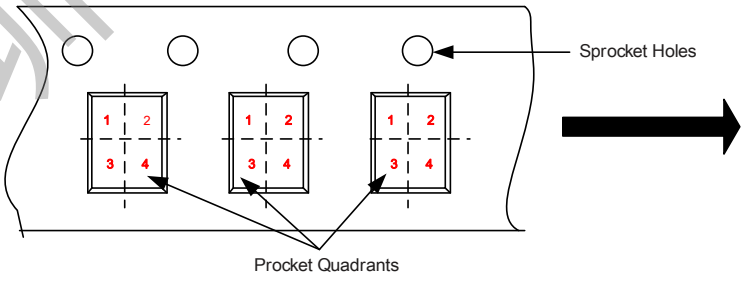


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05
A3		0.20REF	
b	0.20	0.25	0.30
b1	0.15	0.20	0.25
D	3.40	3.50	3.60
E	3.40	3.50	3.60
D2	1.95	2.05	2.15
E2	1.95	2.05	2.15
e		0.50BSC	
e1		0.55BSC	
e2		0.75BSC	
e3		1.50BSC	
H		0.30REF	
K	0.225	0.325	0.425
L	0.30	0.40	0.50
L1	0.225	0.325	0.425
R	0.09	–	–



SIDE VIEW

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPAE



Package Type	Pin1 Quadrant
QFN3.5x3.5-14	1

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