

SN74LVC1G86 单路 2 输入异或门

1 特性

- 静电放电 (ESD) 保护性能超过 JESD 22 规范的要求
 - 2000V 人体放电模型 (A114-A)
 - 1000V 组件充电模式 (C101)
- 适用于 -40°C 至 $+125^{\circ}\text{C}$
- 支持 5V V_{CC} 运行
- 输入为高达 5.5V 过压容差
- 支持下行转换到 V_{CC}
- 3.3V 和 15pF 负载条件下 t_{pd} 最大值为 4ns
- 低功耗, 85°C 条件下 I_{CC} 最大值为 10 μA
- 电压为 3.3V 时, 输出驱动为 $\pm 24\text{mA}$
- I_{off} 支持部分断电模式和后驱动保护
- 采用德州仪器 (TI) 的 NanoFree™ 封装
- 锁断性能超过 100mA, 符合 JESD 78 II 类规范的要求

2 应用

- 无线耳机
- 电机驱动与控制
- 电视
- 机顶盒
- 音频

3 说明

SN74LVC1G86 器件以正逻辑执行布尔函数 $Y = \overline{A}B + A\overline{B}$ 。该单路 2 输入异或门适用于 1.65V 至 5.5V V_{CC} 运行环境。

如果一个输入为低电平, 另一个输入则可在输出时重新生成真实形态。如果一个输入为高电平, 另一个输入的信号则可在输出时重新生成反向信号。该器件功耗低, 3.3V 和 15pF 电容性负载条件下 t_{pd} 最大值为 4ns。最大输出驱动为 $\pm 32\text{mA}/4.5\text{V}$ 和 $\pm 24\text{mA}/3.3\text{V}$ 。

该器件完全适用于使用 I_{off} 的局部掉电应用。 I_{off} 电路可禁用输出, 以防在器件断电时电流回流对器件造成损坏。

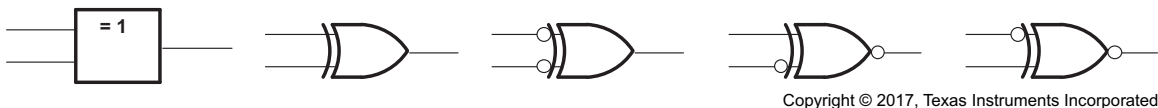
器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
SN74LVC1G86DBV	SOT-23 (5)	2.90mm × 1.60mm
SN74LVC1G86DCK	SC70 (5)	2.00mm × 1.25mm
SN74LVC1G86DRL	SOT (5)	1.60mm × 1.20mm
SN74LVC1G86YZP	DSBGA (5)	1.44mm × 0.94mm

(1) 要了解所有可用封装, 请参见数据表末尾的可订购产品附录。

功能框图

EXCLUSIVE OR



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异或门具有多种应用, 并可用其他逻辑符号更好地表示其中部分应用。

共有五种等效异或门符号适用于采用正逻辑的 SN74LVC1G86 门; 任意两个端口可能显示否定逻辑。



目录

1	特性	1	8.2	Functional Block Diagram	8
2	应用	1	8.3	Feature Description	8
3	说明	1	8.4	Function Table	9
4	修订历史记录	2	9	Application and Implementation	10
5	Pin Configuration and Functions	3	9.1	Application Information	10
6	Specifications	4	9.2	Typical Application	10
6.1	Absolute Maximum Ratings	4	10	Power Supply Recommendations	11
6.2	ESD Ratings	4	11	Layout	12
6.3	Recommended Operating Conditions	4	11.1	Layout Guidelines	12
6.4	Thermal Information	5	11.2	Layout Example	12
6.5	Electrical Characteristics	5	12	器件和文档支持	13
6.6	Switching Characteristics, $C_L = 15$ pF	6	12.1	接收文档更新通知	13
6.7	Switching Characteristics, $C_L = 30$ pF or 50 pF	6	12.2	社区资源	13
6.8	Operating Characteristics	6	12.3	商标	13
6.9	Typical Characteristics	6	12.4	静电放电警告	13
7	Parameter Measurement Information	7	12.5	Glossary	13
8	Detailed Description	8	13	机械、封装和可订购信息	13
8.1	Overview	8			

4 修订历史记录

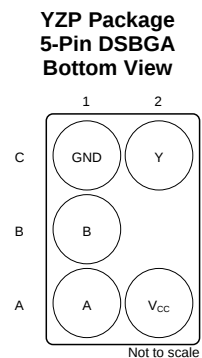
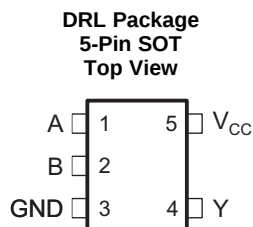
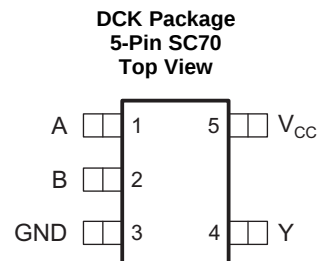
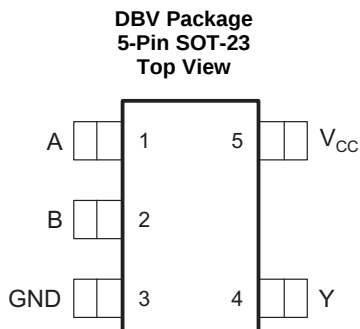
注：之前版本的页码可能与当前版本有所不同。

Changes from Revision P (September 2015) to Revision Q	Page
• Changed YZP (DSBGA) package pinout diagram and added DSBGA column	3
• Added <i>Balanced High-Drive CMOS Push-Pull Outputs</i> , <i>Standard CMOS Inputs</i> , <i>Clamp Diodes</i> , <i>Partial Power Down</i> (I_{off}), and <i>Over-voltage Tolerant Inputs</i> sections	8

Changes from Revision O (December 2013) to Revision P	Page
• 已添加应用 部分、器件信息 表、ESD 额定值 表、热性能信息 表、典型特性 部分、特性 说明 部分、器件功能模式、应用和实施 部分、电源相关建议 部分、布局 部分、器件和文档支持 部分以及机械、封装和可订购信息 部分	1

Changes from Revision N (January 2007) to Revision O	Page
• 将文档更新为了新的 TI 数据表格式。	1
• 删除了订购信息 表。	1
• 更新了 I_{off} (特性 部分)。	1
• Updated operating temperature range.	4

5 Pin Configuration and Functions



Pin Functions⁽¹⁾

NAME	PIN		I/O	DESCRIPTION
	DBV, DRL, DCK	DSBGA		
A	1	A1	I	Input A
B	2	B1	I	Input B
GND	3	C1	—	Ground
V _{CC}	5	A2	—	Positive Supply
Y	4	C2	O	Output Y

(1) See mechanical drawings for dimensions.

6 Specifications

6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		−0.5	6.5	V
V _I	Input voltage ⁽²⁾		−0.5	6.5	V
V _O	Voltage applied to any output in the high-impedance or power-off state ⁽²⁾		−0.5	6.5	V
V _O	Voltage applied to any output in the high or low state ⁽²⁾⁽³⁾		−0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0	−50		mA
I _{OK}	Output clamp current	V _O < 0	−50		mA
I _O	Continuous output current		±50		mA
	Continuous current through V _{CC} or GND		±100		mA
T _J	Junction temperature		150		°C
T _{std}	Storage temperature		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	1000

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	Operating	1.65	5.5
		Data retention only	1.5	
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	1.7	
		V _{CC} = 3 V to 3.6 V	2	
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}	
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	0.7	
		V _{CC} = 3 V to 3.6 V	0.8	
		V _{CC} = 4.5 V to 5.5 V	0.3 × V _{CC}	
V _I	Input voltage	0	5.5	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V	−4	mA
		V _{CC} = 2.3 V	−8	
		V _{CC} = 3 V	−16	
		V _{CC} = 4.5 V	−24	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#), SCBA004.

Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
I_{OL} Low-level output current	$V_{CC} = 1.65\text{ V}$		4	mA
	$V_{CC} = 2.3\text{ V}$		8	
	$V_{CC} = 3\text{ V}$		16	
			24	
	$V_{CC} = 4.5\text{ V}$		32	
$\Delta t/\Delta v$ Input transition rise or fall rate	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}, 2.5\text{ V} \pm 0.2\text{ V}$		20	ns/V
	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		10	
	$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		5	
T_A Operating free-air temperature	YZP package	–40	85	°C
	DCK, DBV, and DRL packages	–40	125	

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	SN74LVC1G86			UNIT
	DBV (SOT-23)	DCK (SC70)	YZP (DSBGA)	
	5 PINS	5 PINS	5 PINS	
$R_{\theta JA}$ Junction-to-ambient thermal resistance	206	252	132	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	I _{OH} = −100 μA			1.65 V to 5.5 V	V _{CC} − 0.1			V
	I _{OH} = −4 mA			1.65 V	1.2			
	I _{OH} = −8 mA			2.3 V	1.9			
	I _{OH} = −16 mA			3 V	2.4			
	I _{OH} = −24 mA				2.3			
	I _{OH} = −32 mA			4.5 V	3.8			
V _{OL}	I _{OL} = 100 μA			1.65 V to 5.5 V	0.1			V
	I _{OL} = 4 mA			1.65 V	0.45			
	I _{OL} = 8 mA			2.3 V	0.3			
	I _{OL} = 16 mA			3 V	0.4			
	I _{OL} = 24 mA				0.55			
	I _{OL} = 32 mA			4.5 V	0.55			
I _I A or B input	V _I = 5.5 V or GND			0 to 5.5 V	±5			μA
I _{off}	V _I or V _O = 5.5 V			0	±10			μA
I _{CC}	V _I = V _{CC} or GND,	I _O = 0	−40°C to 85°C	1.65 V to 5.5 V	10			μA
			−40°C to 125°C		15			
ΔI _{CC}	One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND			3 V to 5.5 V	500			μA
C _i	V _I = V _{CC} or GND			3.3 V	6			pF

(1) All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

SN74LVC1G86

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6.6 Switching Characteristics, $C_L = 15 \text{ pF}$

 over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	2.1	9.1	1	4.5	0.6	4	0.8	3.3	ns

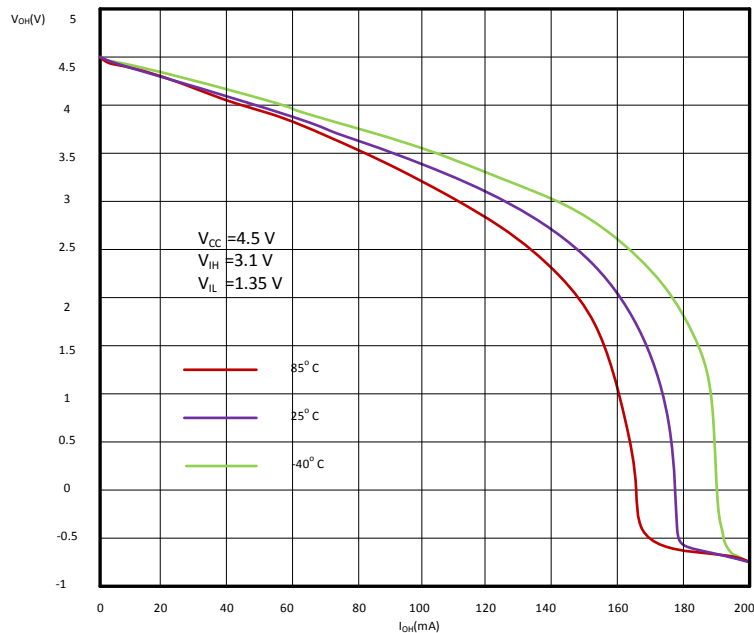
6.7 Switching Characteristics, $C_L = 30 \text{ pF}$ or 50 pF

over recommended operating free-air temperature range (unless otherwise noted)

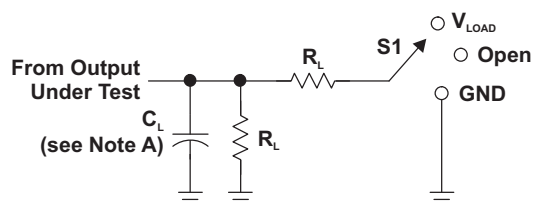
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	-40°C to $+85^\circ\text{C}$ temperature range, see Figure 2	3.5	9.9	1.8	5.5	1.3	5	1	4	ns
			-40°C to $+125^\circ\text{C}$ temperature range, see Figure 2	3.5	12	1.8	7	1.3	6	1	5	

6.8 Operating Characteristics
 $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	V _{CC} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance	f = 10 MHz	22	22	22	24	pF

6.9 Typical Characteristics

Figure 1. V_{OH} vs I_{OH} at 4.5 V

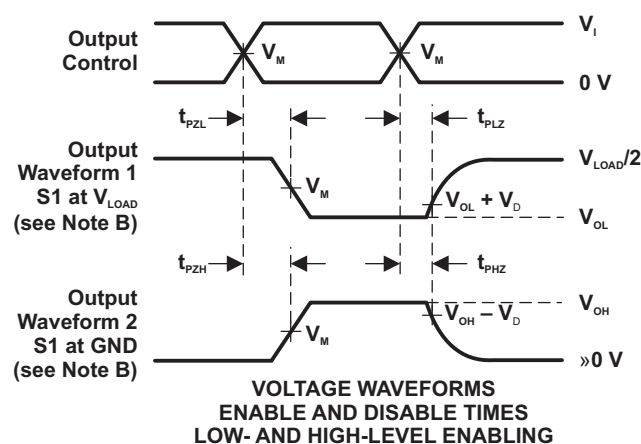
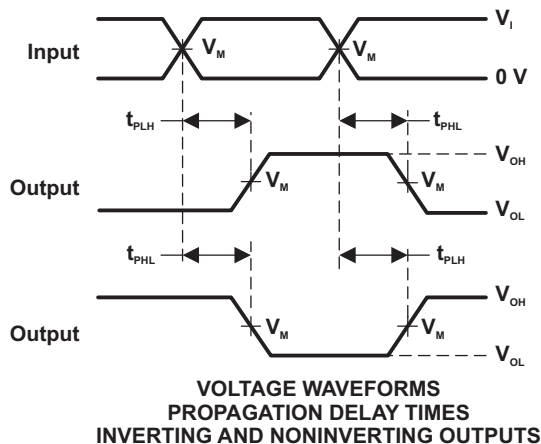
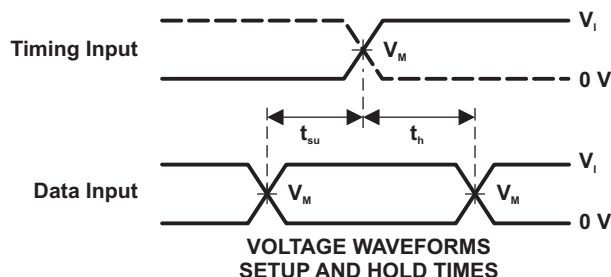
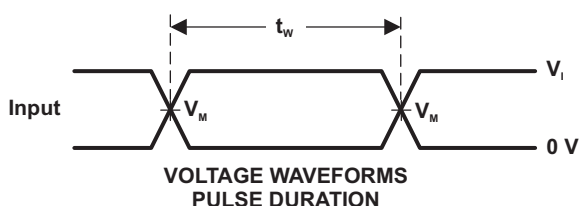
7 Parameter Measurement Information



LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_D
	V_I	t_f/t_r					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	15 pF	1 M Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.3 V



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_o = 50\ \Omega$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

8 Detailed Description

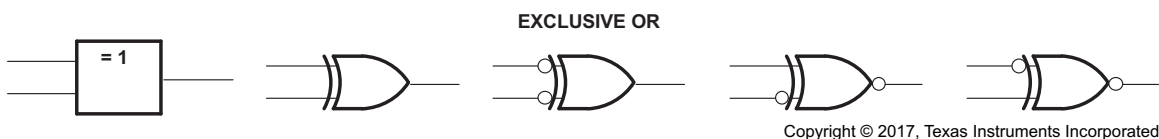
8.1 Overview

The SN74LVC1G86 device performs the Boolean function $Y = \overline{A}B + A\overline{B}$ in positive logic. This single 2-input exclusive-OR gate is designed for 1.65-V to 5.5-V V_{CC} operation.

A common application is as a true and complement element. If the input is low, the other input is reproduced in true form at the output. If the input is high, the signal on the other input is reproduced inverted at the output.

NanoFree package technology is a major breakthrough in IC packaging concepts, using the die as the package. This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

8.2 Functional Block Diagram



These are five equivalent exclusive-OR symbols valid for an SN74LVC1G86 gate in positive logic; negation may be shown at any two ports.

8.3 Feature Description

8.3.1 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the power output of the device to be limited to avoid thermal runaway and damage due to over-current. The electrical and thermal limits defined in the [Absolute Maximum Ratings](#) must be followed at all times.

8.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the [Electrical Characteristics](#). The worst case resistance is calculated with the maximum input voltage, given in the [Recommended Operating Conditions](#), and the maximum input leakage current, given in the [Electrical Characteristics](#), using ohm's law ($R = V \div I$).

Signals applied to the inputs need to have fast edge rates, as defined by $\Delta t/\Delta v$ in [Recommended Operating Conditions](#) to avoid excessive currents and oscillations. If tolerance to a slow or noisy input signal is required, a device with a Schmitt-trigger input should be utilized to condition the input signal prior to the standard CMOS input.

Feature Description (continued)

8.3.3 Clamp Diodes

The inputs and outputs to this device have negative clamping diodes.

CAUTION

Avoid any voltage below or above the input or output voltage specified in the [Absolute Maximum Ratings](#). In this event, the current must be limited to the maximum input or output clamp current value indicated in the [Absolute Maximum Ratings](#) to avoid damage to the device.

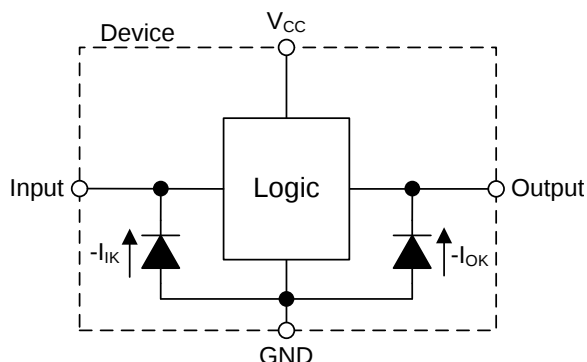


Figure 3. Electrical Placement of Clamping Diodes for Each Input and Output

8.3.4 Partial Power Down (I_{off})

The inputs and outputs for this device enter a high impedance state when the supply voltage is 0 V. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the [Electrical Characteristics](#).

8.3.5 Over-voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the [Recommended Operating Conditions](#).

8.4 Function Table

[Table 1](#) lists the functional modes of the SN74LVC1G86 device.

Table 1. Function Table

INPUTS		OUTPUT Y
A	B	
L	L	L
L	H	H
H	L	H
H	H	L

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LVC1G86 device can accept input voltages up to 5.5 V at any valid V_{CC} which makes the device suitable for down translation. This feature of the SN74LVC1G86 makes it ideal for various bus interface applications.

9.2 Typical Application

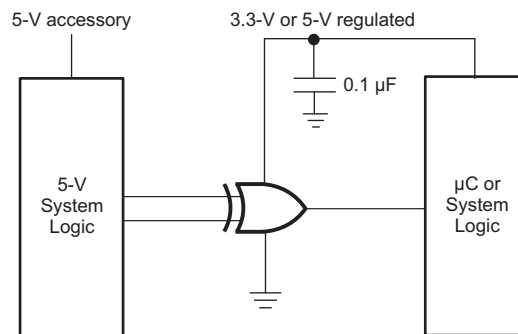


Figure 4. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
 - For rise time and fall time specifications, see $\Delta t/\Delta V$ in the [Recommended Operating Conditions](#) table.
 - For specified High and low levels, see V_{IH} and V_{IL} in the [Recommended Operating Conditions](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC} .
2. Recommended Output Conditions
 - Load currents should not exceed 32 mA per output and 50 mA total for the part.
 - Outputs should not be pulled above V_{CC} .

Typical Application (continued)

9.2.3 Application Curve

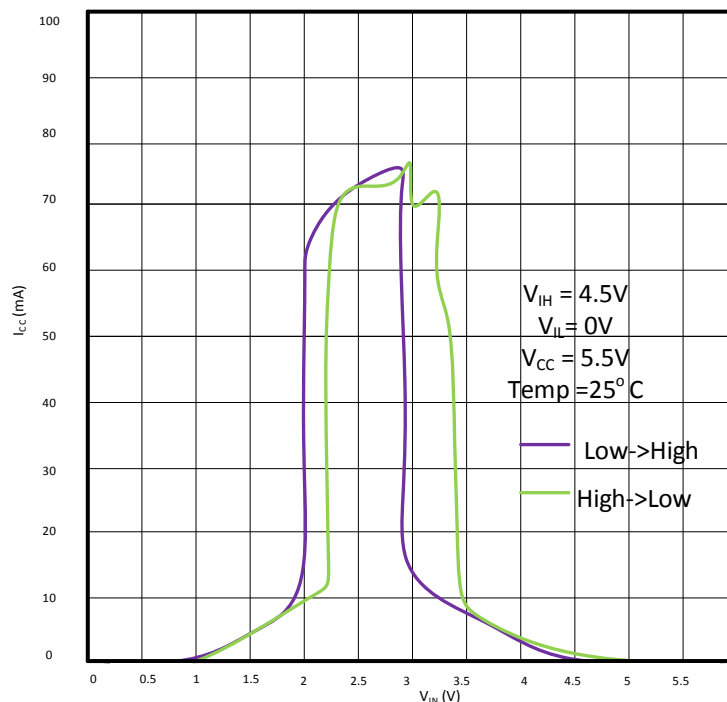


Figure 5. I_{CC} vs. V_{IN}

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended. If there are multiple V_{CC} pins, 0.01 μF or 0.022 μF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1- μF and 1- μF are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

Even low data rate digital signals can have high frequency signal components due to fast edge rates. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. [Figure 6](#) shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

11.2 Layout Example

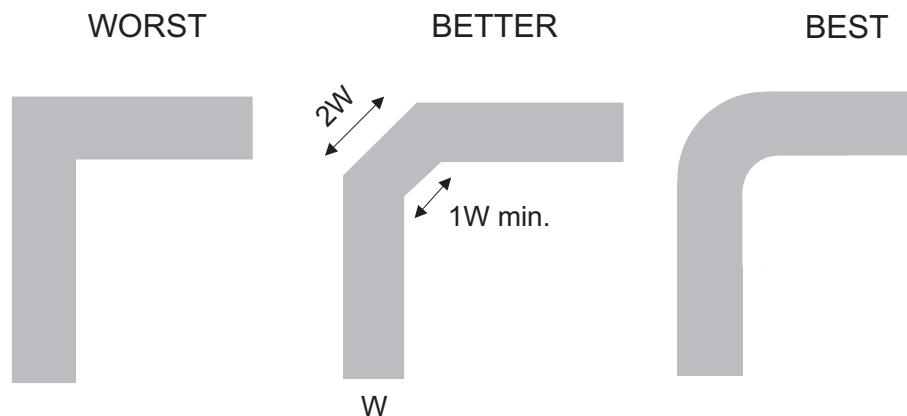


Figure 6. Trace Example

12 器件和文档支持

12.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。请单击右上角的通知我进行注册，即可收到任意产品信息更改每周摘要。有关更改的详细信息，请查看任意已修订文档中包含的修订历史记录。

12.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 商标

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12.4 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参见左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC1G86DBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C865, C86F, C86J, C86K, C86R)
SN74LVC1G86DBVRG4	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C86F
SN74LVC1G86DBVT	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU SN NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C865, C86F, C86J, C86K, C86R)
SN74LVC1G86DCKR	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU SN NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CH5, CHF, CHJ, CH K, CHR)
SN74LVC1G86DCKRE4	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CH5
SN74LVC1G86DCKRG4	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CH5
SN74LVC1G86DCKT	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU SN NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CH5, CHF, CHJ, CH K, CHR)
SN74LVC1G86DCKTG4	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CH5
SN74LVC1G86DRLR	Active	Production	SOT-5X3 (DRL) 5	4000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(CH7, CHR)
SN74LVC1G86YZPR	Active	Production	DSBGA (YZP) 5	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(CH7, CHN)

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74LVC1G86 :

- Automotive : [SN74LVC1G86-Q1](#)
- Enhanced Product : [SN74LVC1G86-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G86DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G86DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G86DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G86DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G86DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G86DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
SN74LVC1G86DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G86DCKRG4	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G86DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G86DCKT	SC70	DCK	5	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74LVC1G86DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G86DCKTG4	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G86DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74LVC1G86YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

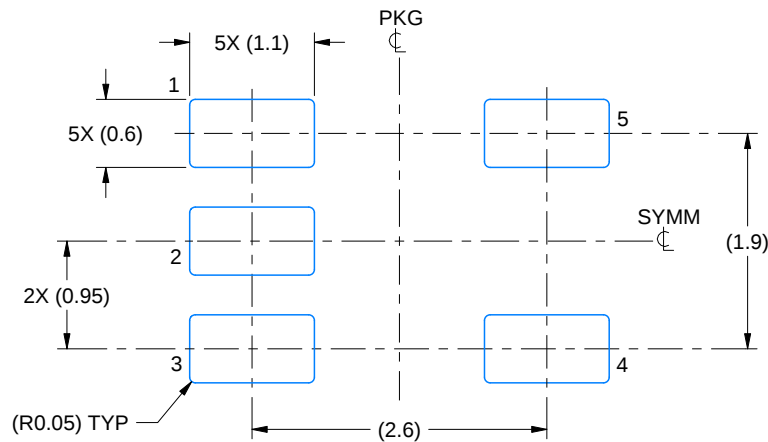
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G86DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74LVC1G86DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74LVC1G86DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G86DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
SN74LVC1G86DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
SN74LVC1G86DCKR	SC70	DCK	5	3000	210.0	185.0	35.0
SN74LVC1G86DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G86DCKRG4	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G86DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G86DCKT	SC70	DCK	5	250	202.0	201.0	28.0
SN74LVC1G86DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G86DCKTG4	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G86DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0
SN74LVC1G86YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0

EXAMPLE BOARD LAYOUT

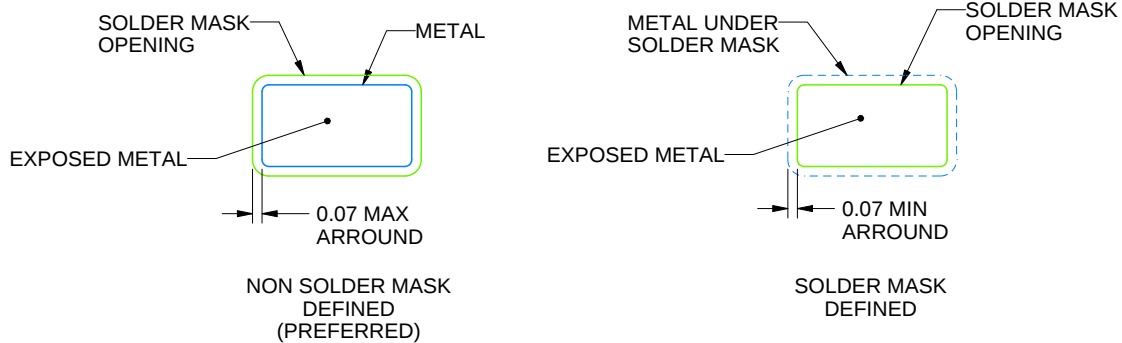
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



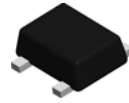
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

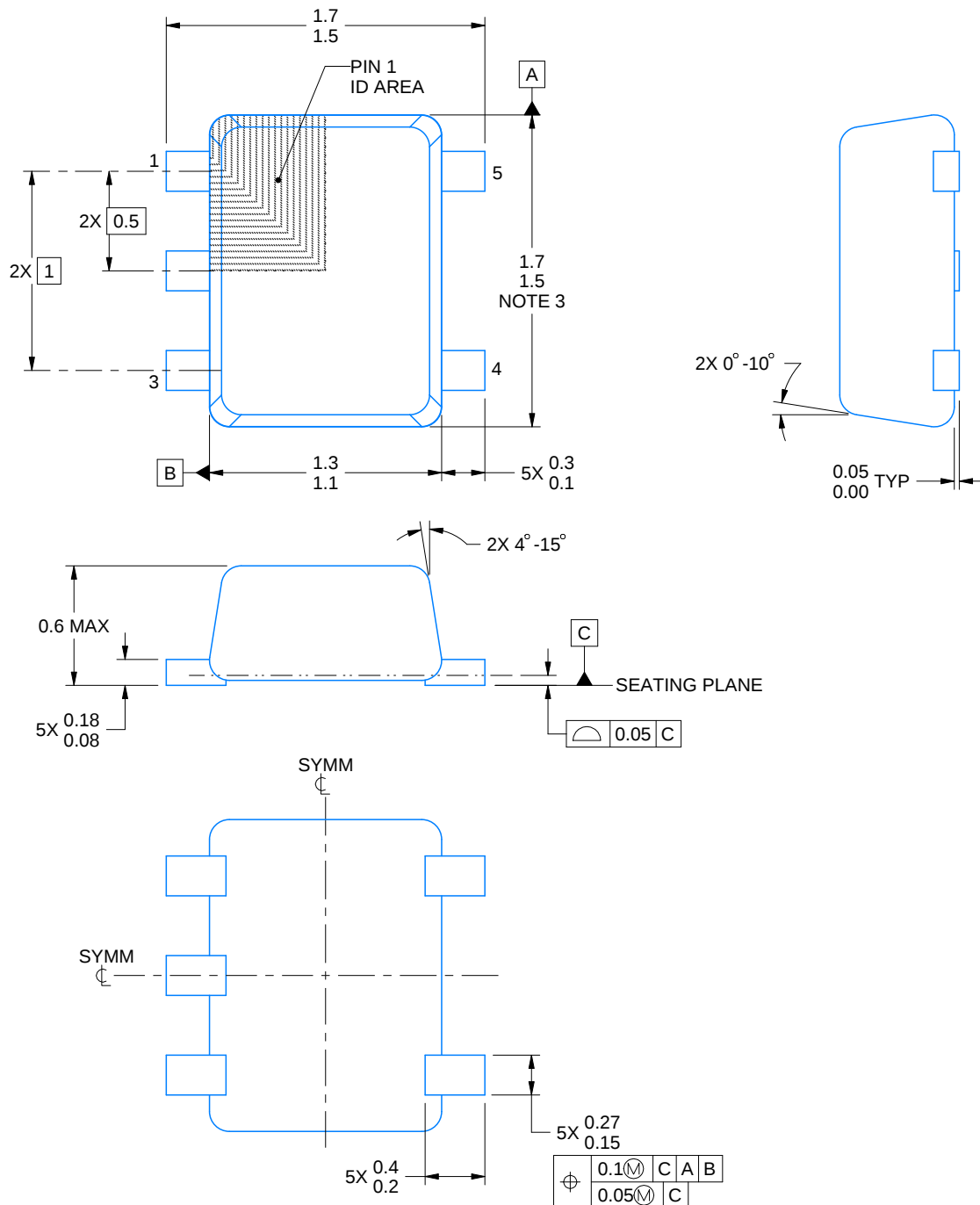
DRL0005A



PACKAGE OUTLINE

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



4220753/E 11/2024

NOTES:

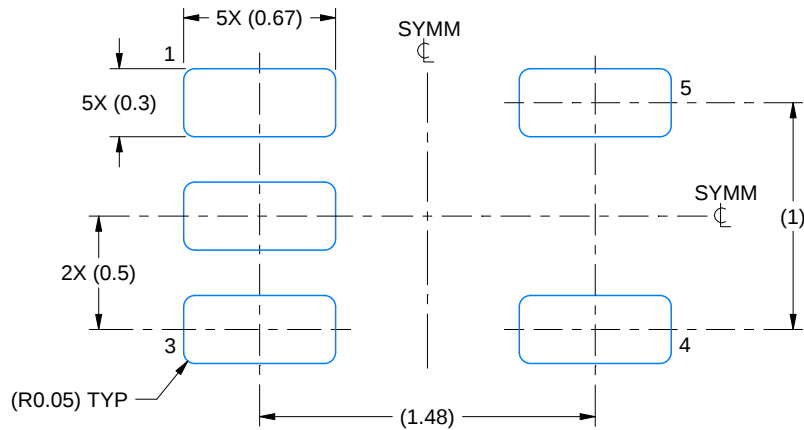
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1

EXAMPLE BOARD LAYOUT

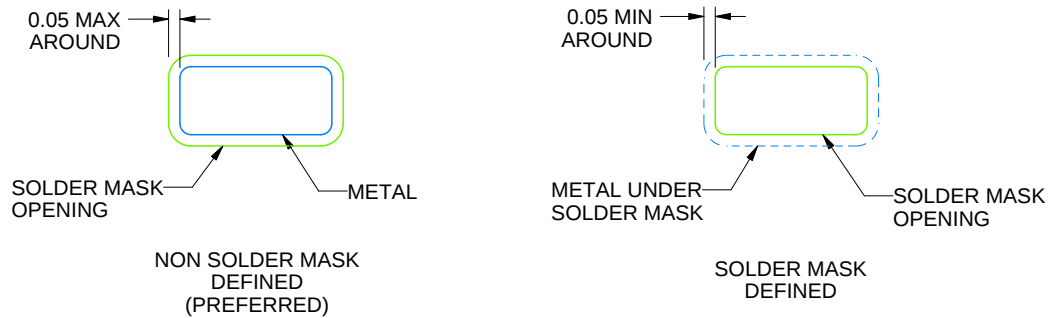
DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4220753/E 11/2024

NOTES: (continued)

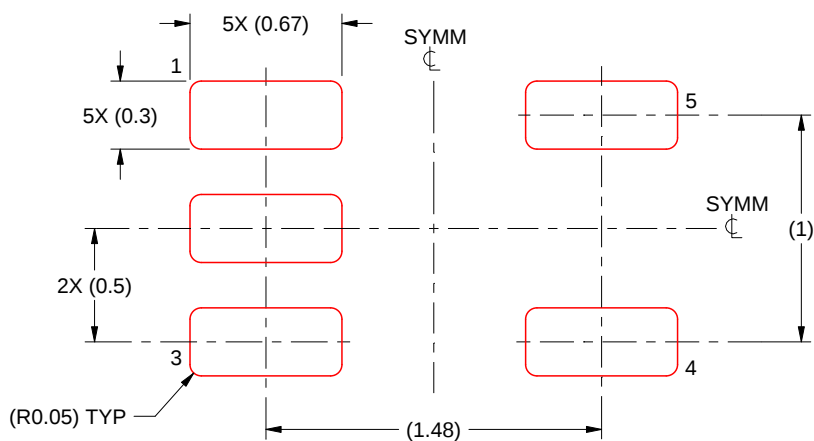
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/E 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

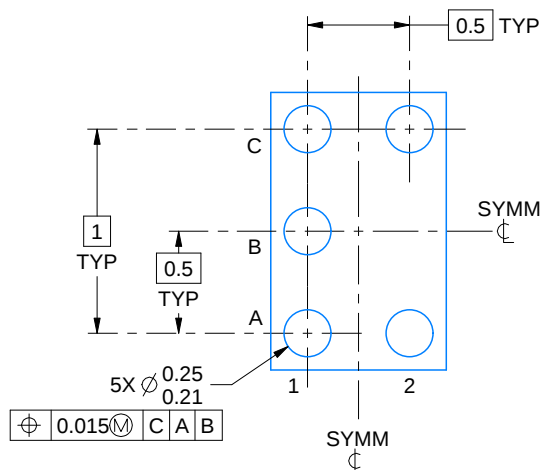
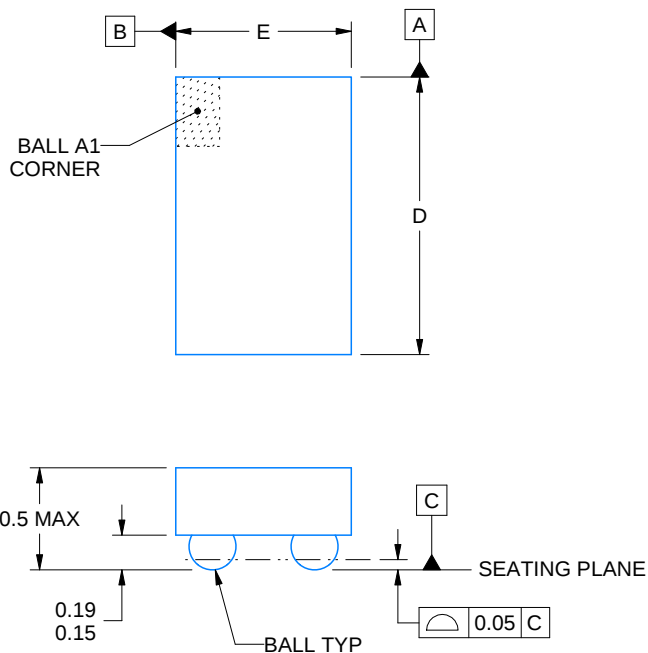
YZP0005



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.44 mm, Min = 1.38 mm
E: Max = 0.94 mm, Min = 0.88 mm

4219492/A 05/2017

NOTES:

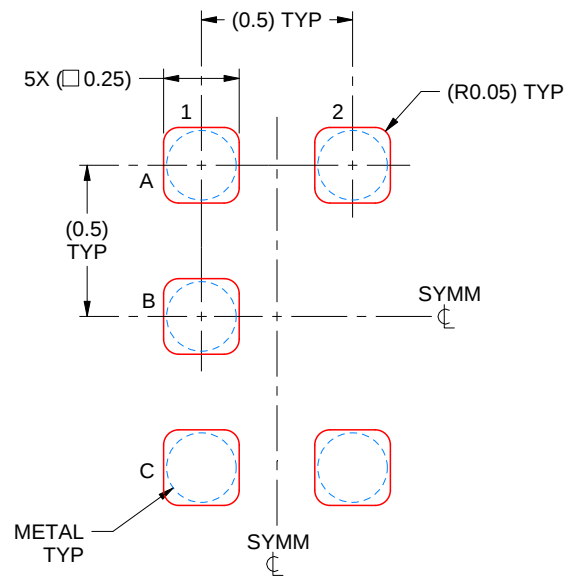
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE STENCIL DESIGN

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY

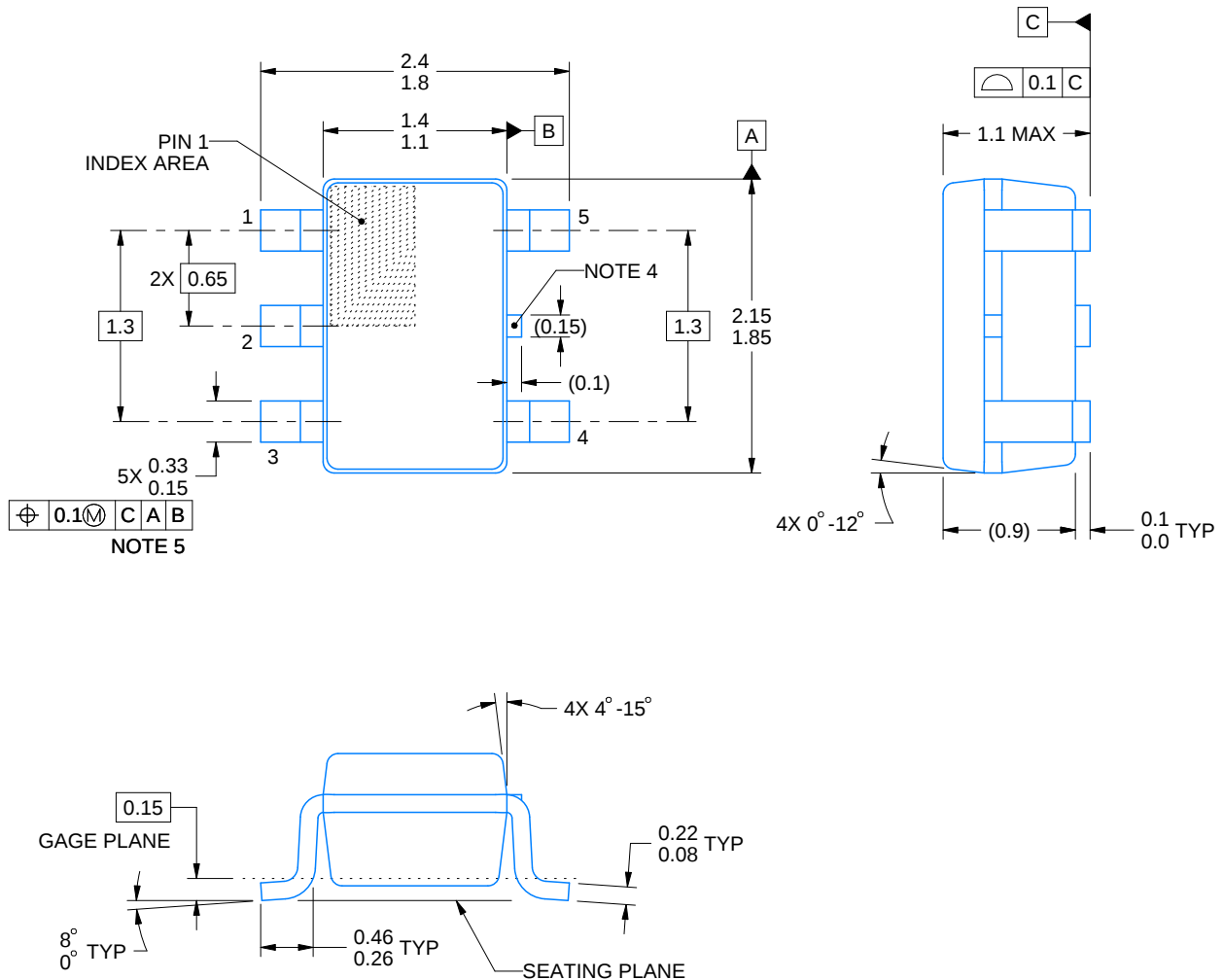


SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219492/A 05/2017

NOTES: (continued)

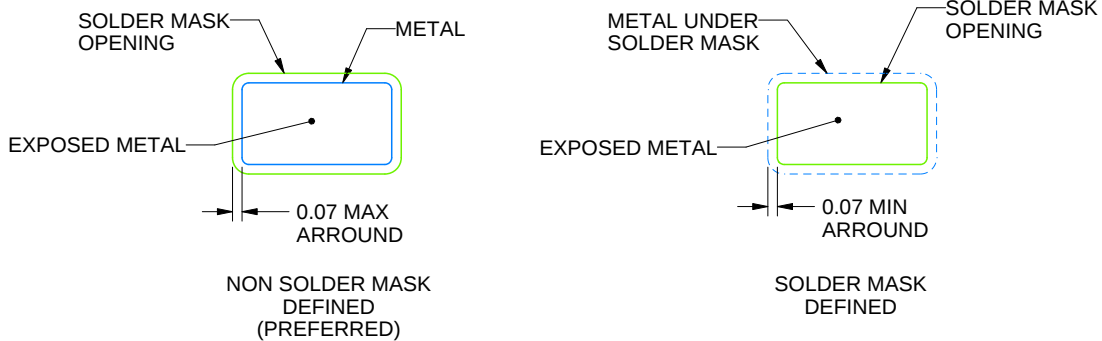
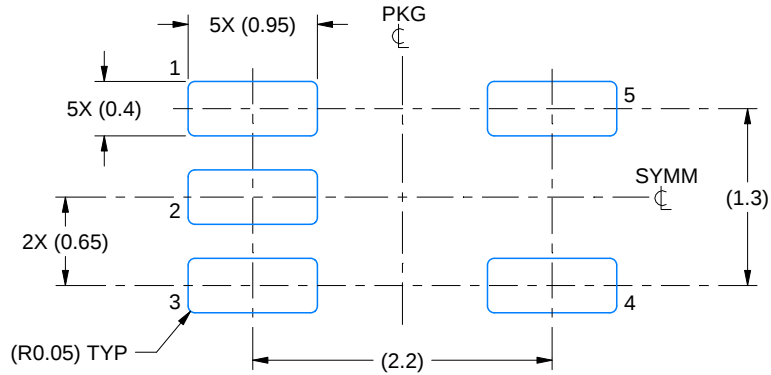
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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