

# 具有减少的接地 (GND) 开关 R<sub>导通</sub>和调频 (FM) 功能的自主音频头戴式耳机 开关

查询样品: TS3A226AE

### 特性

- 接地场效应晶体管 (FET) 开关(典型值 60mΩ)
- 耳机类型的自主检测:
   3 极或 4 极(SLEEVE 或 RING2 上有麦克风 (MIC))
- 麦克风线路开关
- 支持通过接地 FET 传输 FM 信号
- 减少卡嗒/爆裂噪音
- VDD 范围: 2.6V 4.7V
- 总谐波失真 (THD) (Mic): 典型值 0.002%
- 低流耗: 典型值 6.5µA
- ±8kV 接触放电 (IEC 61000-4-2) 静电放电 (ESD) SLEEVE 和 RING2 引脚的性能

### 应用范围

- 移动电话 / 平板个人电脑
- 笔记本计算机/超级本计算机

### 说明

TS3A226AE 是一款音频头戴式耳机开关,此开关可检测 3 极或 4 极 3.5mm 配件。对于带有麦克风的 4 极配件,TS3A226AE 还能够检测麦克风位置,并自动发送麦克风以及接地信号。此接地信号通过一对低阻抗接地 FET (典型值 60mΩ)发送,所以大大降低了对音频串扰性能的影响。自主检测特性使得最终用户能够将具有不同音频极配置的配件插入移动器件中,并使得它们运转正常,而无需增加软件控制,并且不会增加复杂度。器件的接地 FET 被设计成可让 FM 信号通过,这样的话,可将头戴式耳机的接地线用作移动音频应用中的 FM 天线。

TS3A226AE 采用 1.2mm x 1.2mm 晶圆级芯片 (WCSP) 封装,这使得它适合在移动应用中使用。

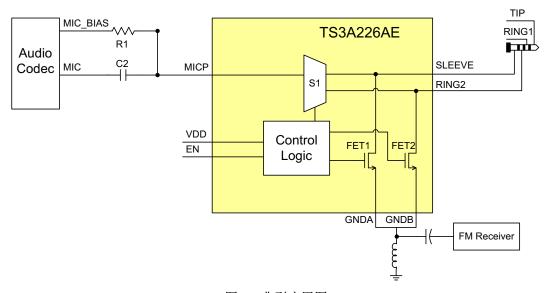


图 1. 典型应用图

### 订购信息

要获得最新的封装和订货信息,请参阅本文档末尾的封装选项附录,或者浏览 TI 网站 www.ti.com进行查询。



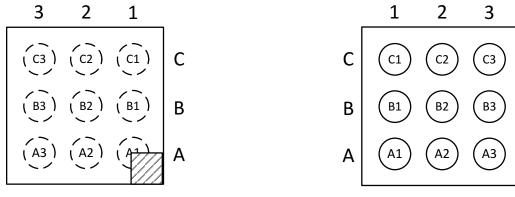
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### PACKAGE; YFF-WCSP



**Top View/Footprint** 

**Bump View** 

Die Size: 1.2mm ×1.2mm Bump Size: 0.25mm Bump Pitch: 0.4mm

### TS3A226AE Pin Mapping (Top View)

			,	
	3	2	1	
С	GND	TIP	EN	
В	SLEEVE	GNDA	MICp	
Α	RING2	GNDB	VDD	

### **PIN FUNCTIONS**

PIN			
NUMB ER	NAME IVE		DESCRIPTION
A1	VDD	Supply	Power supply for the chip.
A2	GNDB	Ground	FET2 ground reference.
А3	RING2	I/O	Connected to the RING2 segment of the jack. The pin will be routed automatically by TS3A226AE to either MICp or GNDB depending on the type of accessory.
B1	MICp	I/O	Microphone signal connection to codec. Microphone bias should be fed into this pin.
B2	GNDA	Ground	FET1 ground reference.
В3	SLEEVE	I/O	Connected to the SLEEVE segment of the jack. The pin will be routed automatically by TS3A226AE to either MICp or GNDA depending on the type of accessory.
C1	EN	Input	A rising edge triggers the detection sequence. This pin can be connected to the headset jack to allow automatic pull-up to supply after headset insertion.
C2	TIP	I/O	Connected to the TIP segment of the headphone jack.
C3	GND	Ground	Chip ground reference.



#### S1 MUX DETAIL

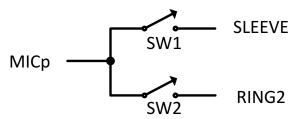


Figure 2. S1 Mux Detail

### **FUNCTIONAL TABLES: INTERNAL SWITCHES**

EN	Accessory Type	Accessory Configuration	SW1	SW2	FET1	FET2
0	N/A	_	High Z	High Z	High Z	High Z
1	TRS 3-pole Headphone or Speaker	TIP = Audio Left Ring = Audio Right Sleeve = <b>Ground</b>	On	On	On On	
1	TRRS 4-pole Headphone	TIP = Audio Left Ring1 = Audio Right Ring2 = <b>Ground</b> Sleeve = <b>Microphone</b>	On High Z		High Z	On
1	TRRS 4-pole Headphone	TIP = Audio Left Ring1 = Audio Right Ring2 = <b>Microphone</b> Sleeve = <b>Ground</b>	High Z	On	On	High Z
1	N/A	_	On	On	On	On

### **ABSOLUTE MAXIMUM RATINGS**

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE	UNIT
V	Voltage range on VDD <sup>(2)</sup>	-0.3 to 5	V
V <sub>I</sub>	Voltage range on EN, MICP, RING2, SLEEVE, TIP (2)	–0.3 to V <sub>DD</sub> +0.5	V
T <sub>A</sub>	Operating ambient temperature range <sup>(3)</sup>	-40 to 85	°C
T <sub>J (MAX)</sub>	Maximum operating junction temperature	125	°C
T <sub>stg</sub>	Storage temperature range	-65 to 150	°C
	Charge device model (JESD 22 C101)	500	V
ESD rating	Human body model(JESD 22 A114)	2	kV
	Contact discharge on RING2, SLEEVE, TIP (IEC 61000-4-2)	8	kV

<sup>(1)</sup> Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute—maximum—rated conditions for extended periods may affect device reliability.

<sup>(2)</sup> All voltage values are with respect to network ground terminal.

<sup>(3)</sup> In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature  $[T_{A(max)}]$ , is dependent on the maximum operating junction temperature  $[T_{J(max)}]$ , the maximum power dissipation of the device in the application  $[P_{D(max)}]$ , and the junction-to-ambient thermal resistance of the part/package in the application  $(\theta_{JA})$ , as given by the following equation:  $T_{A(max)} = T_{J(max)} - (\theta_{JA} \times P_{D(max)})$ 



### **RECOMMENDED OPERATING CONDITIONS**

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{DD}$	Supply voltage range		2.6	4.5	V
V <sub>IO</sub>	Input/Output voltage range (E	N, MICP, RING2, SLEEVE, TIP)	0	$V_{DD}$	V
V <sub>IO(TIP)</sub>	Input/Output voltage range for	TIP	-2.0	$V_{DD}$	V
		VDD = 2.6 V	1.16	$V_{DD}$	
V <sub>IH</sub>	Input Logic High for EN	VDD = 3.3 V	1.24	$V_{DD}$	V
		VDD = 4.5 V	1.48	$V_{DD}$	
		VDD = 2.6 V	0	0.19	
V <sub>IL</sub>	Input Logic Low for EN	VDD = 3.3 V	0	0.3	V
		VDD = 4.5 V	0	0.5	
T <sub>A</sub>	Operating temperature range		-40	85	°C

### **KEY ELECTRICAL CHARACTERISTICS**

Unless otherwise noted the specification applies over the  $V_{DD}$  range and operating junction temperature  $-40^{\circ}C \le T_{A} \le 70^{\circ}C$ . Typical values are for  $V_{DD} = 3.3V$  and  $T_{J} = 25^{\circ}C$ .

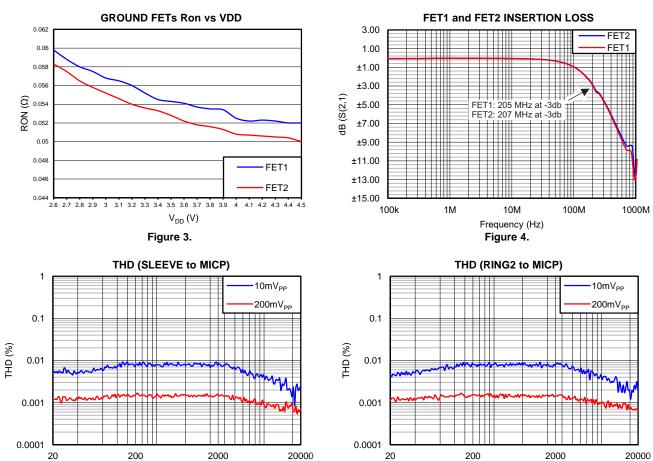
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$V_{DD}$	Input Voltage Range		2.6	3.3	4.5	V	
I <sub>DD</sub>	Quiescent Current	$V_{DD}$ = 4.5 V, $V_{MICp}$ = 1.8 V to $V_{DD}$ , EN=L or EN=H (after detection)		6.5	14	μA	
SWITCH	RESISTANCE						
R <sub>F1</sub>	FET1 On Resistance	V 26VV 0VI 10 mA		60	85	mΩ	
R <sub>F2</sub>	FET2 On Resistance	$V_{DD} = 2.6 \text{ V}, V_{GND} = 0 \text{ V}, I_{GND} = 10 \text{ mA}$		60	85	mt2	
R <sub>SW1</sub>	SW1 On Resistance	$V_{DD} = 2.6 \text{ V}, V_{SLEEVE/RING2} = 0 \text{ V to } 2.6 \text{ V},$	8.5		10.5	_	
R <sub>SW2</sub>	SW2 On Resistance	I <sub>MIC</sub> = ±10 mA		8.5	10.5	Ω	
	LEAKAGE CURRENT		•		•		
I <sub>OFF-0.1</sub>	FET1 and FET2 off leakage				1		
I <sub>OFF-10</sub>	SW1, SW2 off leakage	$V_{IN} = 0 \text{ V to } 2.6 \text{ V}, V_{OUT} = 0 \text{ V}, V_{DD} = 4.5 \text{ V}$			1	μΑ	
I <sub>ON-10</sub>	SW1, SW2 on leakage				1		
SWITCH	DYNAMIC CHARACTERISTICS		1				
BW <sub>F1</sub>	FET1 Bandwidth	V 00 mV 1 40 mA	160	200		N.41.1-	
BW <sub>F2</sub>	FET2 Bandwidth	$V = 60 \text{ mV}_{PP}, I_{\text{bias}} = 10 \text{ mA}$	160	200		MHz	
PSR <sub>217</sub>		V = 200 mV <sub>PP</sub> , f = 217 Hz		-110		dB	
PSR <sub>1k</sub>	Power Supply Rejection, $R_1 = 50 \Omega$	V = 200 mV <sub>PP</sub> , f = 1 kHz		-100		dB	
PSR <sub>20k</sub>	N <sub>L</sub> = 50 12	V = 200 mV <sub>PP</sub> , f = 20 kHz		-85		dB	
ISO <sub>S1</sub>	SLEEVE or RING2 to MICP Isolation	$V = 200 \text{ mV}_{PP}, f = 20 \text{ kHz}, R_{L} = 50 \Omega$		-80		dB	
SEP <sub>S1</sub>	SLEEVE to RING2 Separation	$V = 200 \text{ mV}_{PP}$ , $f = 20 \text{ kHz}$ , $R_L = 50 \Omega$ (see Figure 5)		-80		dB	
THD <sub>10</sub>	T	$V = 10 \text{ mV}_{PP}, f = 20-20 \text{ kHz}, R_S = 600 \Omega$		0.01%			
THD <sub>200</sub>	Total Harmonic Distortion	$V = 200 \text{ mV}_{PP}$ , $f = 20-20 \text{ kHz}$ , $R_S = 600 \Omega$		0.002%			
TIMING	CHARACTERISTICS	·	1				
t <sub>dect</sub>	Total detection time	From EN=H to S1 switch(es) closing		180		ms	

Frequency (Hz)

Figure 6.



### **TYPICAL CHARACTERISTICS**



Frequency (Hz)

Figure 5.



## **REVISION HISTORY**

CI	Changes from Original (June 2013) to Revision A						
•	Removed Machine Model ESD specification.	3					
•	Added EN=L or EN=H (after detection) to I <sub>DD</sub> TEST CONDITIONS.	4					
•	Added typical values to R <sub>SW1</sub> and R <sub>SW2</sub>	4					
•	Added t <sub>dect</sub> PARAMETER to KEY ELECTRICAL CHARACTERISTICS table.	4					

www.ti.com 2-May-2025

#### PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
TS3A226AEYFFR	Active	Production	DSBGA (YFF)   9	3000   LARGE T&R	Yes	SNAGCU	(5) Level-1-260C-UNLIM	-40 to 85	YP2 26AE

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

# **PACKAGE MATERIALS INFORMATION**

www.ti.com 19-Jun-2024

### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3A226AEYFFR	DSBGA	YFF	9	3000	180.0	8.4	1.46	1.36	0.7	4.0	8.0	Q1

**PACKAGE MATERIALS INFORMATION** 

www.ti.com 19-Jun-2024

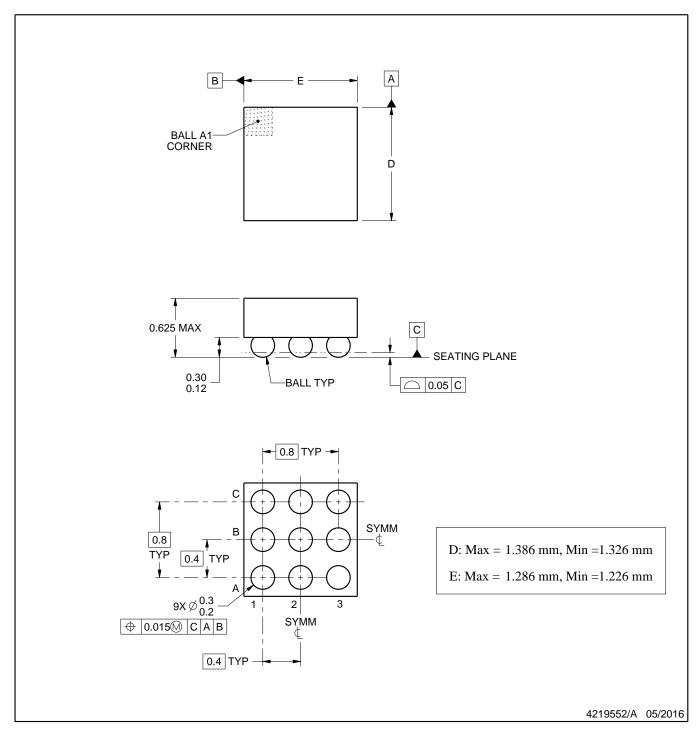


### \*All dimensions are nominal

	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ı	TS3A226AEYFFR	DSBGA	YFF	9	3000	182.0	182.0	20.0



DIE SIZE BALL GRID ARRAY



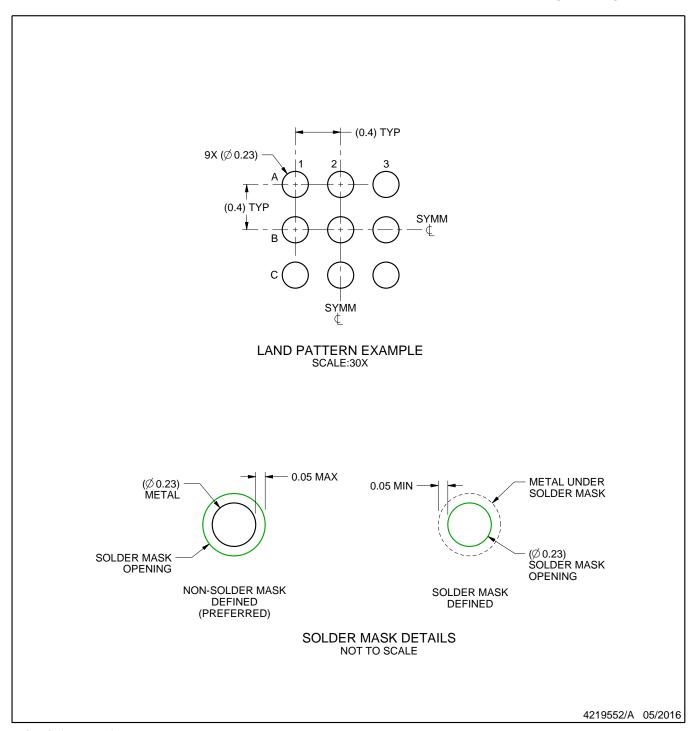
#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.



DIE SIZE BALL GRID ARRAY

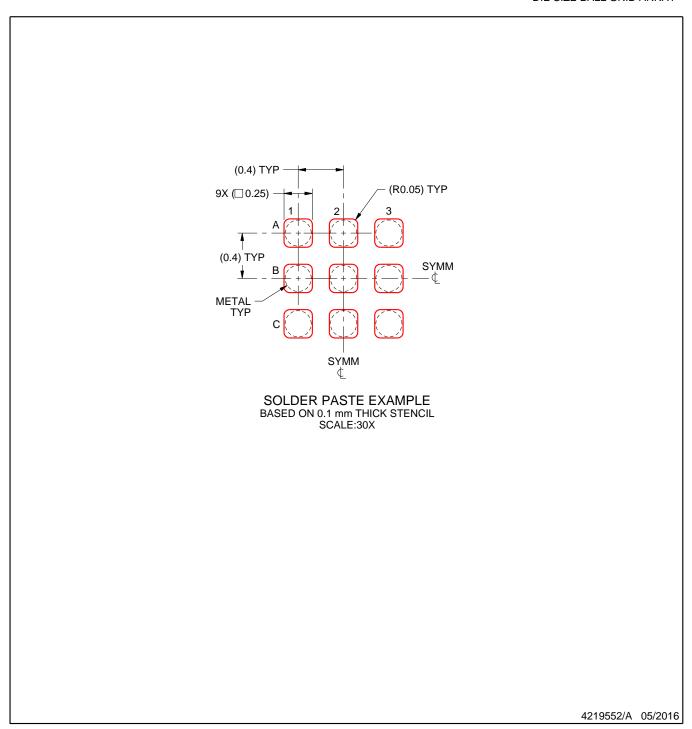


NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



### 重要通知和免责声明

TI"按原样"提供技术和可靠性数据(包括数据表)、设计资源(包括参考设计)、应用或其他设计建议、网络工具、安全信息和其他资源,不保证没有瑕疵且不做出任何明示或暗示的担保,包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任:(1) 针对您的应用选择合适的 TI 产品,(2) 设计、验证并测试您的应用,(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更,恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。 严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务,TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 版权所有 © 2025,德州仪器 (TI) 公司