CSD87588N 同步降压 NexFET™ 电源块 II

1 特性

- 半桥电源块
- 电流 20A 时，系统效率达到 90%
- 高达 25A 的工作电流
- 高密度 - 5mm × 2.5mm 接合栅格阵列 (LGA) 封装
- 双侧冷却能力
- 超薄 - 最大厚度为 0.48mm
- 针对 5V 栅极驱动进行了优化
- 低开关损耗
- 低电感封装
- 符合 RoHS 环保标准
- 无卤素
- 无铅

2 应用范围

- 同步降压转换器
  – 高电流、低占空比应用
- 多相位同步降压转换器
- 负载点 (POL) 直流 - 直流转换器

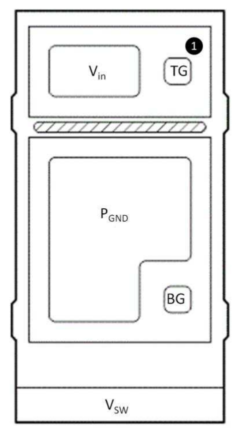
3 说明

此 CSD87588N NexFET™ 电源块 II 是针对同步降压应用的高度优化设计，能够在 5 mm × 2.5mm 的小外形尺寸封装内提供大电流和高效率。 针对 5V 栅极驱动进行了优化，这款产品可提供高效且灵活的解决方案，在与外部控制器/驱动器的任一 5V 栅极驱动器成对使用时，均可提一个供高密度电源。

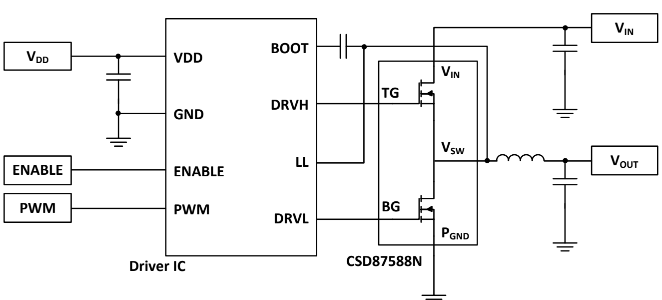
订购信息(1)

器件	介质	数量	封装	出货
CSD87588N	13 英寸卷带	2500	5 x 2.5 LGA	卷带封装
CSD87588NT	7 英寸卷带	250		

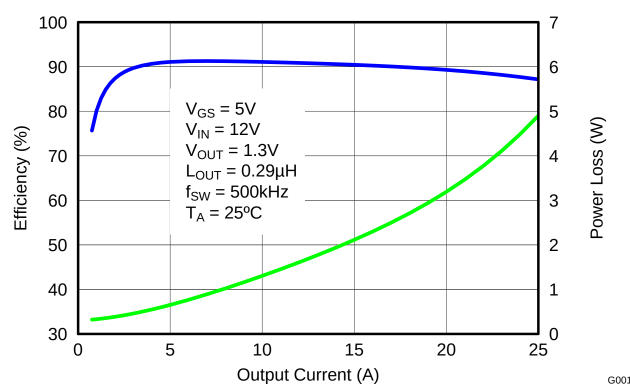
(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。



典型电路



典型电源块效率与功率损耗



目录

4 修订历史记录

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (June 2014) to Revision D	Page
• Changed capacitance units to read pF in Figure 15	8
• Changed capacitance units to read pF in Figure 16	8

Changes from Revision B (January 2014) to Revision C	Page
• 将“无铅引脚镀层”更改成了“无铅”	1

Changes from Revision A (May 2013) to Revision B	Page
• 已添加小卷带信息	1
• Updated Figure 5	5
• Updated Figure 6	5
• Updated Figure 7	5
• Updated Figure 8	5
• Changed figure reference to Figure 29 in electrical performance	13

Changes from Original (March 2013) to Revision A	Page
• Changed $R_{\theta JC\text{-}PCB}$To: $R_{\theta JC}$ in the *Thermal Information* table	3

5 Specifications

5.1 Absolute Maximum Ratings

T_A = 25°C (unless otherwise noted) (1)

			MIN	MAX	UNIT
	Voltage	V_{IN} to P_{GND}	–0.8	30	V
		V_{SW} to P_{GND}		30	
		V_{SW} to P_{GND} (10 ns)		32	
		T_G to V_{SW}	–20	20	
		B_G to P_{GND}	–20	20	
I_{DM}	Pulsed Current Rating (2)			50	A
P_D	Power Dissipation (3)			6	W
E_{AS}	Avalanche Energy	Sync FET, I_D = 45, L = 0.1 mH		101	mJ
		Control FET, I_D = 26, L = 0.1 mH		34	
T_J	Operating Junction		–55	150	°C
T_{stg}	Storage Temperature Range		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Pulse Duration ≤50 µs, duty cycle ≤0.01
(3) Device mounted on FR4 material with 1 inch^2 (6.45 cm^2) Cu

5.2 Recommended Operating Conditions

T_A = 25°C (unless otherwise noted)

			MIN	MAX	UNIT
V_{GS}	Gate Drive Voltage		4.5	16	V
V_{IN}	Input Supply Voltage			24	V
f_{SW}	Switching Frequency	C_{BST} = 0.1 µF (min)	200	1500	kHz
	Operating Current	No Airflow		25	A
		With Airflow (200 LFM)		30	A
		With Airflow + Heat Sink		35	A
T_J	Operating Temperature			125	°C

5.3 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance (Min Cu) (1)			170	°C/W
	Junction-to-ambient thermal resistance (Max Cu) (2) (1)			70	
$R_{θJC}$	Junction-to-case thermal resistance (Top of package) (1)			3.7	
	Junction-to-case thermal resistance (P_{GND} Pin) (1)			1.25	

(1) $R_{θJC}$ is determined with the device mounted on a 1 inch^2 (6.45 cm^2), 2 oz. (0.071 mm thick) Cu pad on a 1.5 inches × 1.5 inches (3.81 cm × 3.81 cm), 0.06 inch (1.52 mm) thick FR4 board. $R_{θJC}$ is specified by design while $R_{θJA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1 inch^2 (6.45 cm^2) Cu.

5.4 Power Block Performance

T_A = 25°C (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
P_{LOSS}	Power Loss(1)	V_{IN} = 12 V, V_{GS} = 5 V V_{OUT} = 1.3 V, I_{OUT} = 15 A f_{SW} = 500 kHz L_{OUT} = 0.29 µH, T_J = 25ºC		2.1		W
I_{QVIN}	V_{IN} Quiescent Current	T_G to T_{GR} = 0 V B_G to P_{GND} = 0 V		10		µA

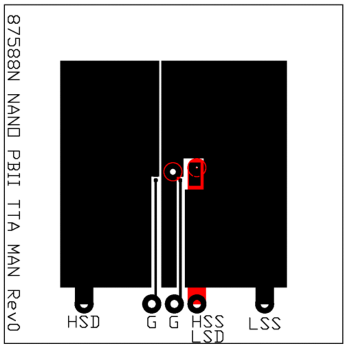
(1) Measurement made with six 10 µF (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across V_{IN} to P_{GND} pins and using a high current 5 V driver IC.

5.5 Electrical Characteristics

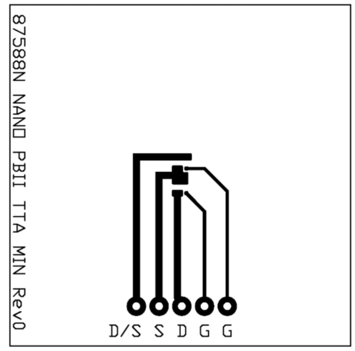
T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	Q1 FET			Q2 FET			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
STATIC CHARACTERISTICS									
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_{DS} = 250 µA	30			30			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = 24 V			1			1	µA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = 20			100			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = 250 µA	1.1		1.9	1.1		1.9	V
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = 4.5 V, I_{DS} = 15 A		10.4	12.5		3.5	4.2	mΩ
		V_{GS} = 10 V, I_{DS} = 15 A		8	9.6		2.9	3.5	
g_{fs}	Transconductance	V_{DS} = 10 V, I_{DS} = 15 A		43			93		S
DYNAMIC CHARACTERISTICS									
C_{ISS}	Input Capacitance (1)	V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz		566	736		2310	3000	pF
C_{OSS}	Output Capacitance (1)			341	444		682	887	pF
C_{RSS}	Reverse Transfer Capacitance (1)			10.3	13.4		62	80.4	pF
R_G	Series Gate Resistance (1)			1.2	2.4		1.1	2.2	Ω
Q_g	Gate Charge Total (4.5 V) (1)	V_{DS} = 15 V, I_{DS} = 15 A		3.2	4.1		13.7	17.9	nC
Q_{gd}	Gate Charge - Gate-to-Drain			0.7			4.3		nC
Q_{gs}	Gate Charge - Gate-to-Source			1.4			4.3		nC
$Q_{g(th)}$	Gate Charge at V_{th}			0.8			2.8		nC
Q_{OSS}	Output Charge	V_{DD} = 12 V, V_{GS} = 0 V		7			18.6		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 15 V, V_{GS} = 4.5 V, I_{DS} = 15 A, R_G = 2 Ω		7.3			12.1		ns
t_r	Rise Time			31.6			36.7		ns
$t_{d(off)}$	Turn Off Delay Time			10.2			20.1		ns
t_f	Fall Time			5.0			6.3		ns
DIODE CHARACTERISTICS									
V_{SD}	Diode Forward Voltage	I_{DS} = 15 A, V_{GS} = 0 V		0.85			0.78		V
Q_{rr}	Reverse Recovery Charge	V_{dd} = 15 V, I_F = 15 A, di/dt = 300 A/µs		12.5			26.7		nC
t_{rr}	Reverse Recovery Time			16			23		ns

(1) Specified by design



Max $R_{\theta JA}$ = 70°C/W when mounted on 1 inch^2 (6.45 cm^2) of 2 oz. (0.071 mm thick) Cu.



Max $R_{\theta JA}$ = 170°C/W when mounted on minimum pad area of 2 oz. (0.071 mm thick) Cu.

5.6 Typical Power Block Device Characteristics

T_J = 125°C, unless stated otherwise.The Typical Power Block System Characteristic curves Figure 3 and Figure 4 are based on measurements made on a PCB design with dimensions of 4.0 inches (W) × 3.5 inches (L) × 0.062 inch (H) and 6 copper layers of 1 oz. copper thickness. See *Application and Implementation* for detailed explanation.

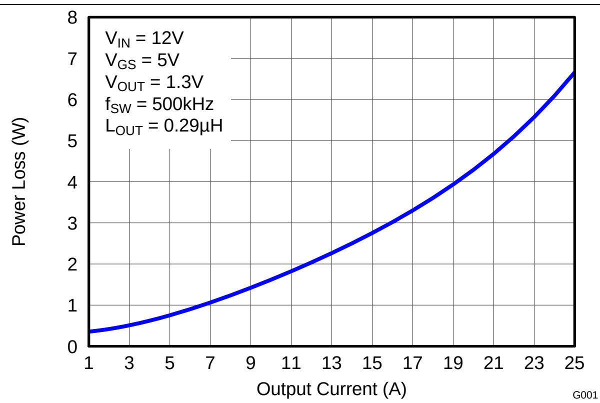


Figure 1. Power Loss vs Output Current

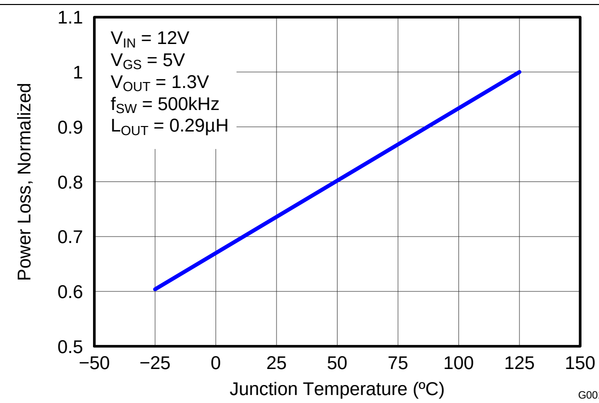


Figure 2. Normalized Power Loss vs Temperature

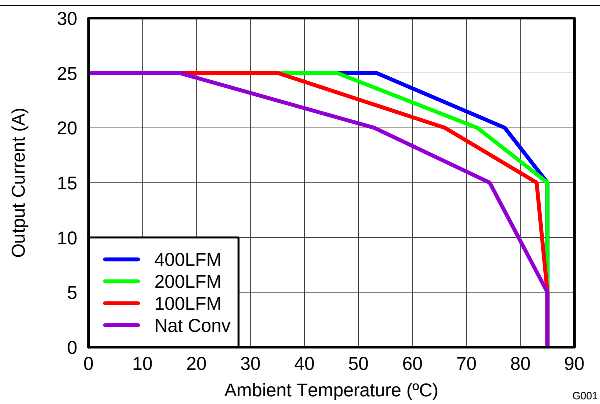


Figure 3. Safe Operating Area – PCB Horizontal Mount

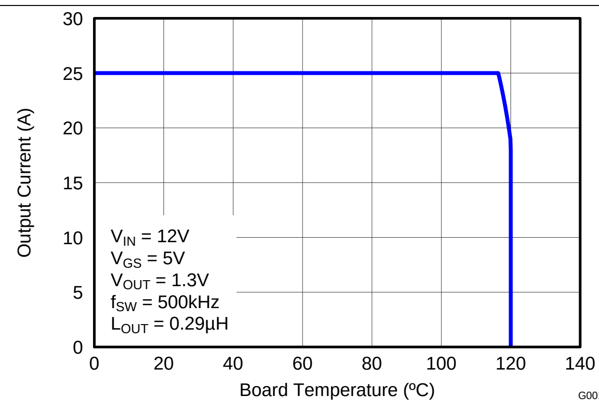


Figure 4. Typical Safe Operating Area

Typical Power Block Device Characteristics (continued)

T_J = 125°C, unless stated otherwise.The Typical Power Block System Characteristic curves Figure 3 and Figure 4 are based on measurements made on a PCB design with dimensions of 4.0 inches (W) × 3.5 inches (L) × 0.062 inch (H) and 6 copper layers of 1 oz. copper thickness. See *Application and Implementation* for detailed explanation.

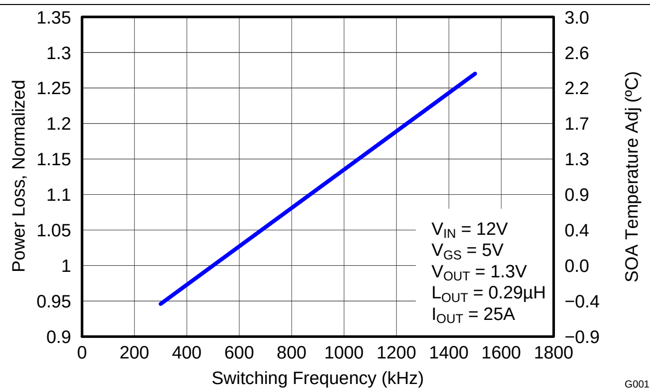


Figure 5. Normalized Power Loss vs Switching Frequency

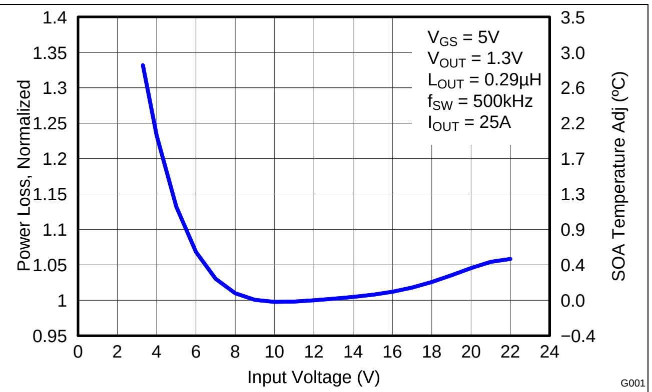


Figure 6. Normalized Power Loss vs Input Voltage

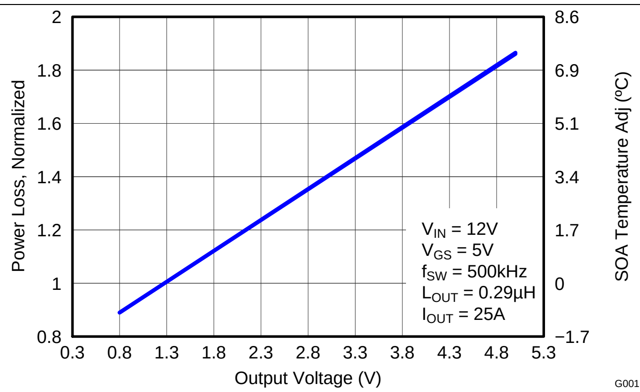


Figure 7. Normalized Power Loss vs Output Voltage

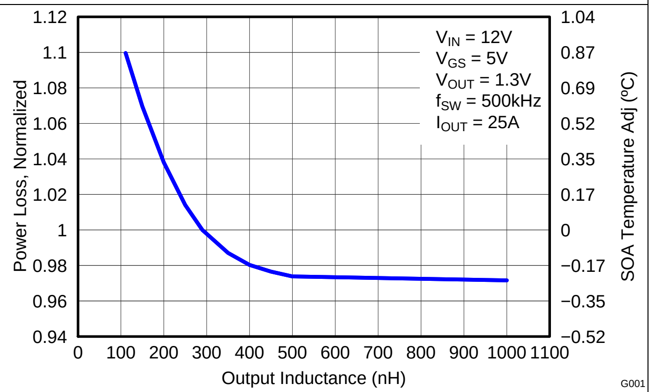


Figure 8. Normalized Power Loss vs Output Inductance

5.7 Typical Power Block MOSFET Characteristics

T_A = 25°C, unless stated otherwise.

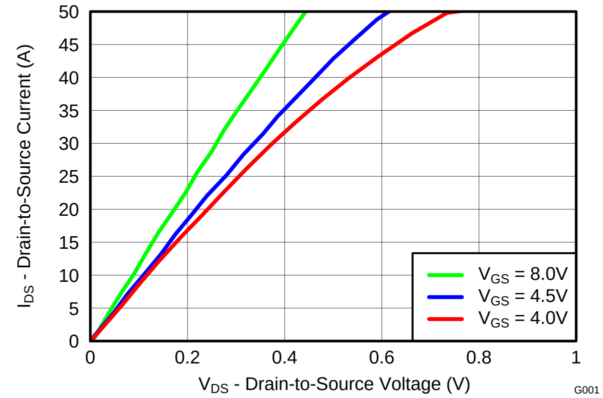


Figure 9. Control MOSFET Saturation

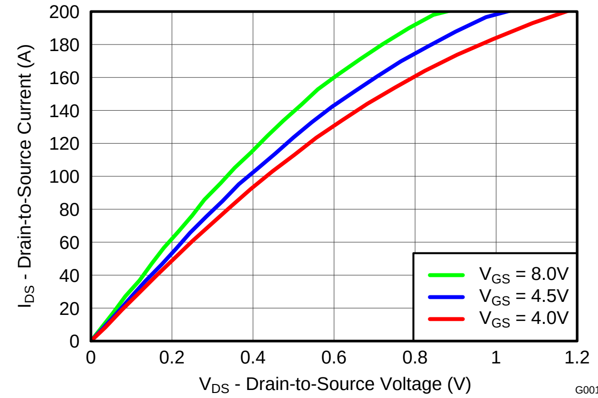


Figure 10. Sync MOSFET Saturation

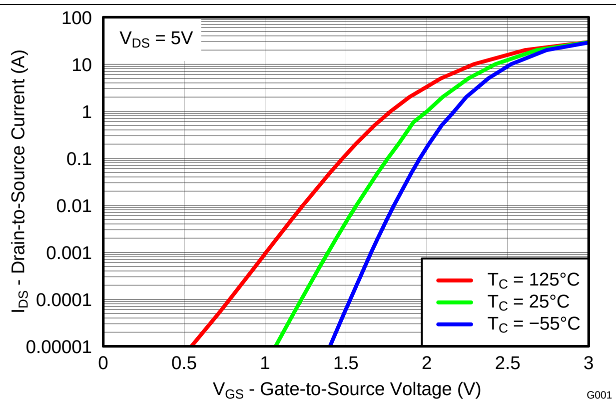


Figure 11. Control MOSFET Transfer

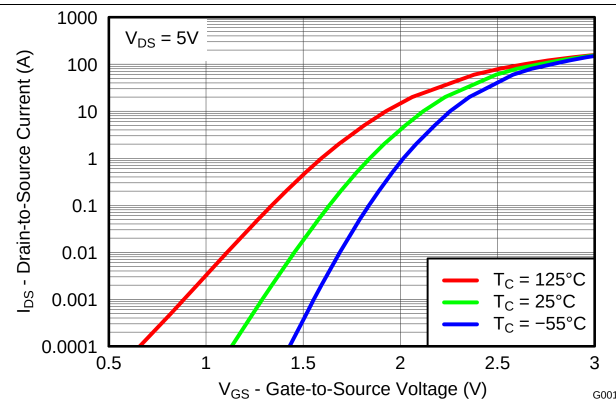


Figure 12. Sync MOSFET Transfer

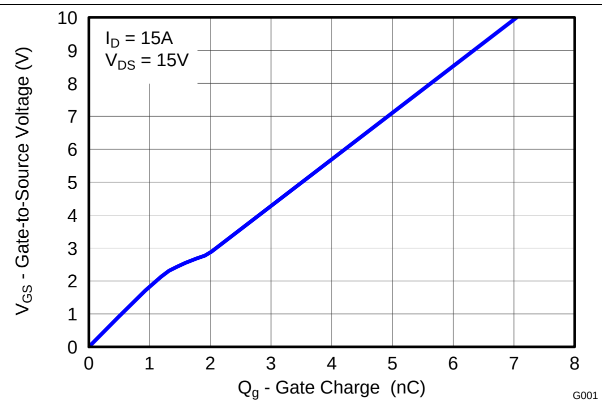


Figure 13. Control MOSFET Gate Charge

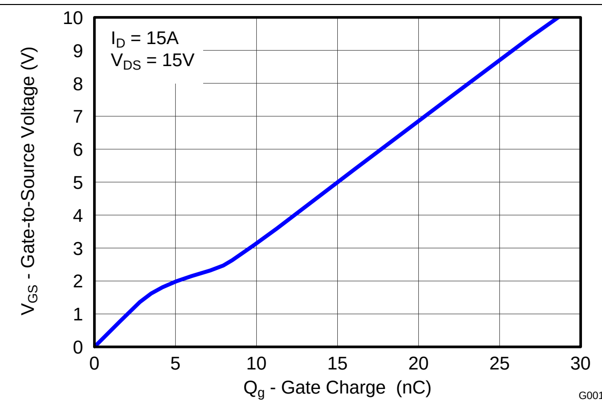


Figure 14. Sync MOSFET Gate Charge

Typical Power Block MOSFET Characteristics (continued)

T_A = 25°C, unless stated otherwise.

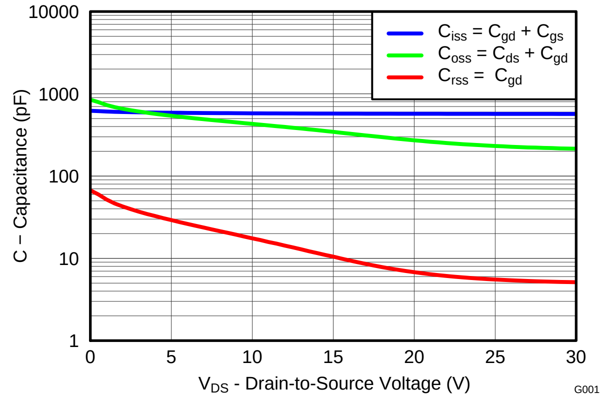


Figure 15. Control MOSFET Capacitance

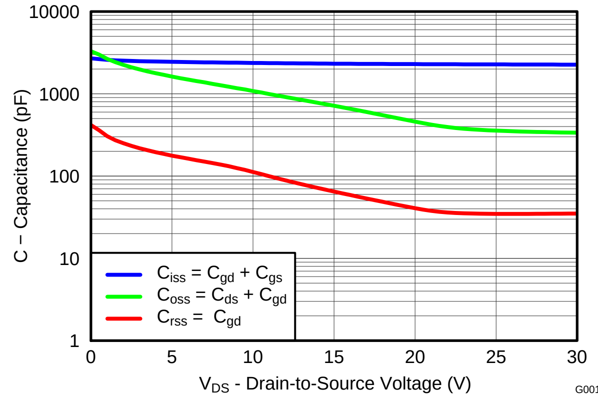


Figure 16. Sync MOSFET Capacitance

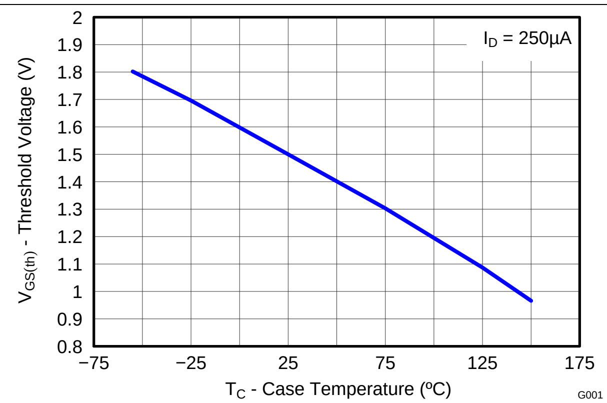


Figure 17. Control MOSFET $V_{GS(th)}$

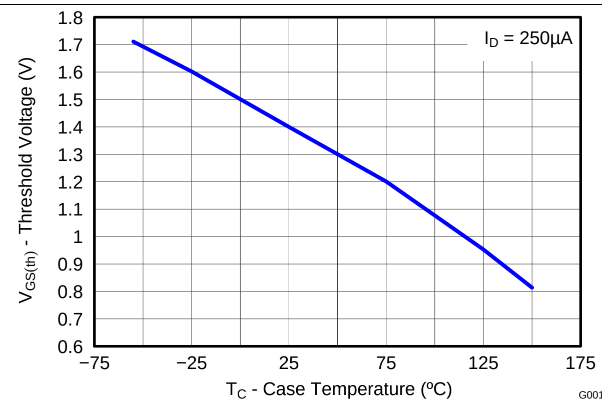


Figure 18. Sync MOSFET $V_{GS(th)}$

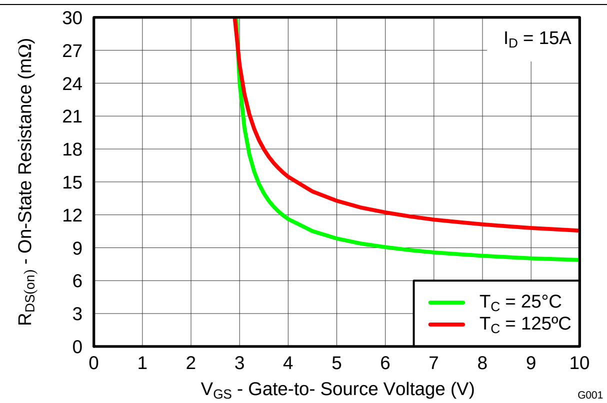


Figure 19. Control MOSFET $R_{DS(on)}$ vs V_{GS}

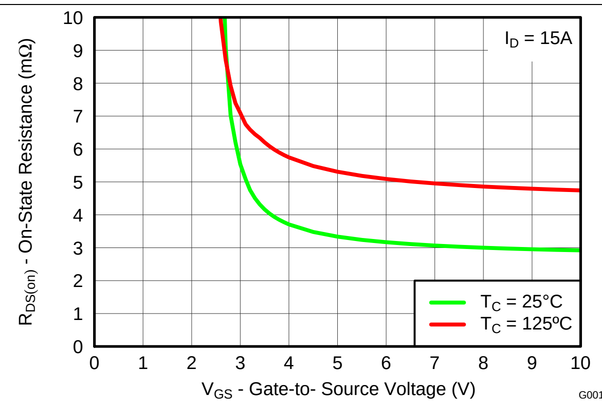


Figure 20. Sync MOSFET $R_{DS(on)}$ vs V_{GS}

Typical Power Block MOSFET Characteristics (continued)

T_A = 25°C, unless stated otherwise.

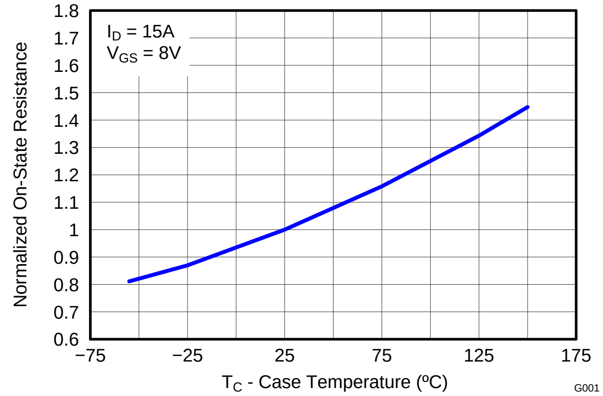


Figure 21. Control MOSFET Normalized $R_{DS(on)}$

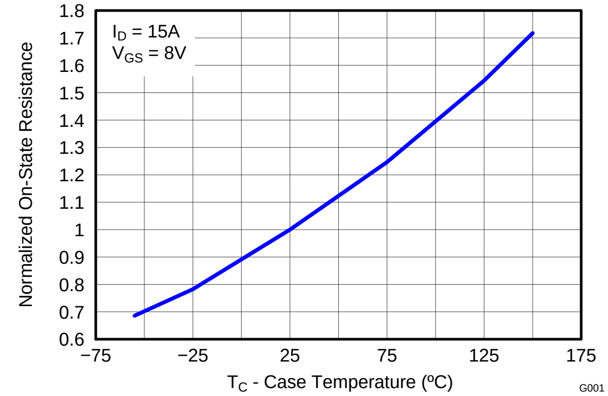


Figure 22. Sync MOSFET Normalized $R_{DS(on)}$

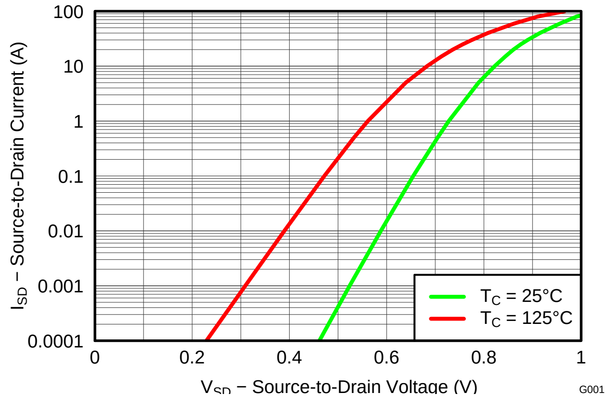


Figure 23. Control MOSFET Body Diode

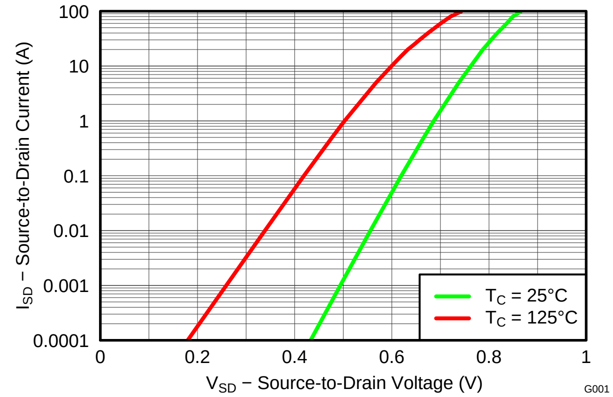


Figure 24. Sync MOSFET Body Diode

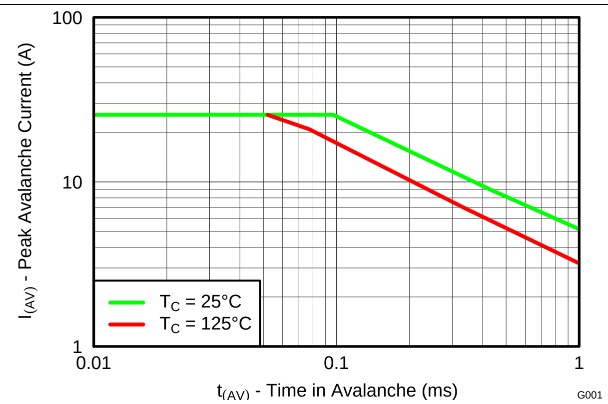


Figure 25. Control MOSFET Unclamped Inductive Switching

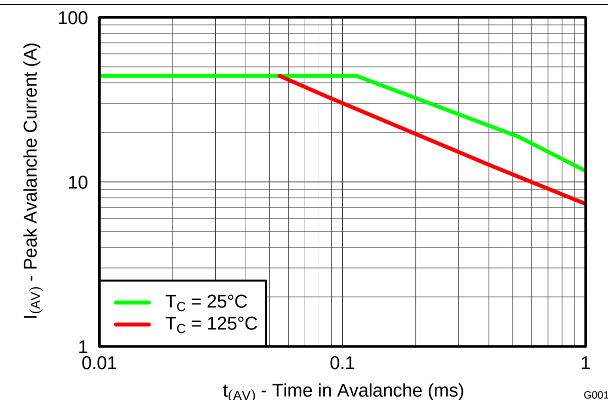


Figure 26. Sync MOSFET Unclamped Inductive Switching

6 Application and Implementation

6.1 Application Information

The CSD87588N NexFET power block is an optimized design for synchronous buck applications using 5 V gate drive. The Control FET and Sync FET silicon are parametrically tuned to yield the lowest power loss and highest system efficiency. As a result, a new rating method is needed which is tailored toward a more systems-centric environment. System-level performance curves such as Power Loss, Safe Operating Area, and normalized graphs allow engineers to predict the product performance in the actual application.

6.1.1 Power Loss Curves

MOSFET-centric parameters such as $R_{DS(ON)}$ and Q_{gd} are needed to estimate the loss generated by the devices. To simplify the design process for engineers, TI has provided measured power loss performance curves. Figure 1 plots the power loss of the CSD87588N as a function of load current. This curve is measured by configuring and running the CSD87588N as it would be in the final application (see Figure 27). The measured power loss is the CSD87588N loss and consists of both input conversion loss and gate drive loss. Equation 1 is used to generate the power loss curve.

$$(V_{IN} \times I_{IN}) + (V_{DD} \times I_{DD}) - (V_{SW\_AVG} \times I_{OUT}) = \text{Power Loss} \quad (1)$$

The power loss curve in Figure 1 is measured at the maximum recommended junction temperatures of 125°C under isothermal test conditions.

6.1.2 Safe Operating Curves (SOA)

The SOA curves in the CSD87588N data sheet provide guidance on the temperature boundaries within an operating system by incorporating the thermal resistance and system power loss. Figure 3 to Figure 4 outline the temperature and airflow conditions required for a given load current. The area under the curve dictates the safe operating area. All the curves are based on measurements made on a PCB design with dimensions of 4 inches (W) × 3.5 inches (L) × 0.062 inch (T) and 6 copper layers of 1 oz. copper thickness.

6.1.3 Normalized Curves

The normalized curves in the CSD87588N data sheet provides guidance on the Power Loss and SOA adjustments based on their application-specific needs. These curves show how the power loss and SOA boundaries adjust for a given set of systems conditions. The primary y-axis is the normalized change in power loss and the secondary y-axis is the change in system temperature required in order to comply with the SOA curve. The change in power loss is a multiplier for the Power Loss curve and the change in temperature is subtracted from the SOA curve.

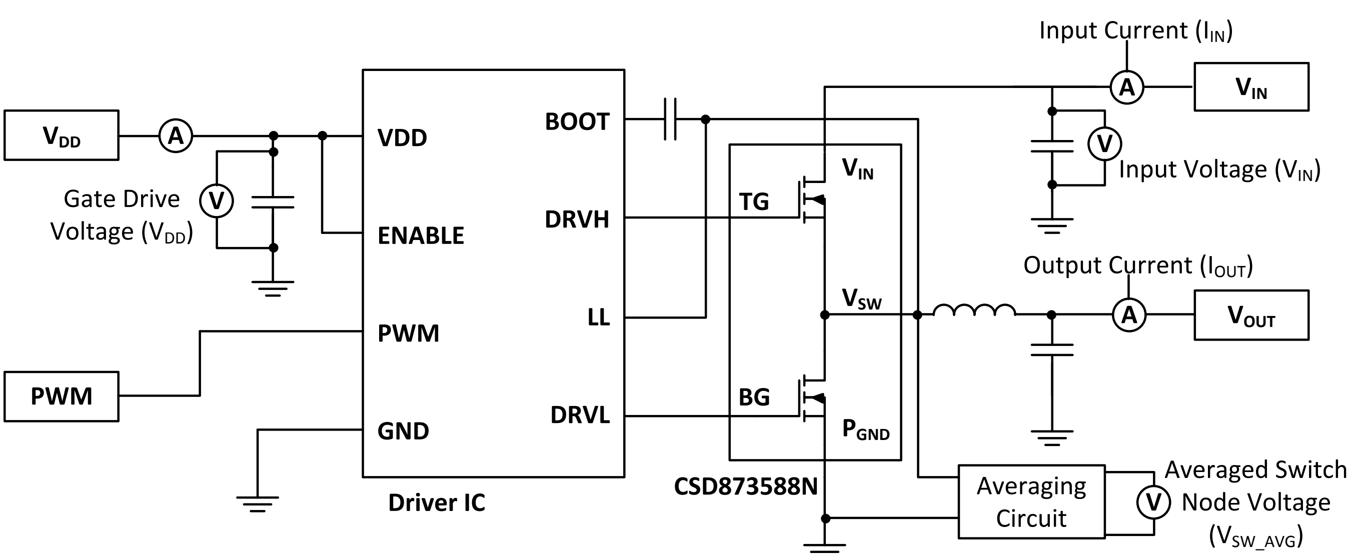


Figure 27. Typical Application

Application Information (continued)

6.1.4 Calculating Power Loss and SOA

The user can estimate product loss and SOA boundaries by arithmetic means (see *Design Example*). Though the Power Loss and SOA curves in this data sheet are taken for a specific set of test conditions, the following procedure outlines the steps the user should take to predict product performance for any set of system conditions.

6.1.4.1 Design Example

Operating Conditions:

- Output Current = 15 A
- Input Voltage = 7 V
- Output Voltage = 1 V
- Switching Frequency = 800 kHz
- Inductor = 0.2 µH

6.1.4.2 Calculating Power Loss

- Power Loss at 15 A = 2.75 W (Figure 1)
- Normalized Power Loss for input voltage ≈ 1.03 (Figure 6)
- Normalized Power Loss for output voltage ≈ 0.94 (Figure 7)
- Normalized Power Loss for switching frequency ≈ 1.08 (Figure 5)
- Normalized Power Loss for output inductor ≈ 1.03 (Figure 8)
- **Final calculated Power Loss = 2.75 W × 1.05 × 0.95 × 1.05 × 1.05 ≈ 3.02 W**

6.1.4.3 Calculating SOA Adjustments

- SOA adjustment for input voltage ≈ 0.3ºC (Figure 6)
- SOA adjustment for output voltage ≈ –0.5ºC (Figure 7)
- SOA adjustment for switching frequency ≈ 0.7ºC (Figure 5)
- SOA adjustment for output inductor ≈ 0.3ºC (Figure 8)
- **Final calculated SOA adjustment = 0.3 + (–0.5) + 0.7 + 0.3 ≈ 0.8ºC**

In the previous design example, the estimated power loss of the CSD87588N would increase to 3.02 W. In addition, the maximum allowable board and/or ambient temperature would have to decrease by 0.8ºC. Figure 28 graphically shows how the SOA curve would be adjusted accordingly.

1. Start by drawing a horizontal line from the application current to the SOA curve.
2. Draw a vertical line from the SOA curve intercept down to the board/ambient temperature.
3. Adjust the SOA board/ambient temperature by subtracting the temperature adjustment value.

Application Information (continued)

In the design example, the SOA temperature adjustment yields a reduction in allowable board/ambient temperature of 0.8ºC. In the event the adjustment value is a negative number, subtracting the negative number would yield an increase in allowable board/ambient temperature.

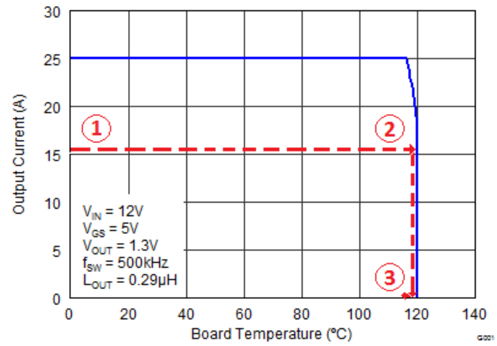


Figure 28. Power Block SOA

7 Layout

7.1 Layout Guidelines

There are two key system-level parameters that can be addressed with a proper PCB design: electrical and thermal performance. Properly optimizing the PCB layout yields maximum performance in both areas. The following sections provide a brief description on how to address each parameter.

7.1.1 Electrical Performance

The CSD87588N has the ability to switch voltages at rates greater than 10 kV/µs. Take special care with the PCB layout design and placement of the input capacitors, inductor, and output capacitors.

- The placement of the input capacitors relative to VIN and PGND pins of CSD87588N device should have the highest priority during the component placement routine. It is critical to minimize these node lengths. As such, ceramic input capacitors need to be placed as close as possible to the VIN and PGND pins (see Figure 29). The example in Figure 29 uses 1 x 10 nF 0402 25 V and 4 x 10 µF 1206 25 V ceramic capacitors (TDK part number C3216X5R1C106KT or equivalent). Notice there are ceramic capacitors on both sides of the board with an appropriate amount of vias interconnecting both layers. In terms of priority of placement next to the Power Stage C21, C5, C8, C19, and C18 should follow in order.
- The switching node of the output inductor should be placed relatively close to the Power Block II CSD87588N VSW pins. Minimizing the VSW node length between these two components will reduce the PCB conduction losses and actually reduce the switching noise level. See Figure 29. (1)

7.1.2 Thermal Performance

The CSD87588N has the ability to utilize the PGND planes as the primary thermal path. As such, the use of thermal vias is an effective way to pull away heat from the device and into the system board. Concerns of solder voids and manufacturability problems can be addressed by the use of three basic tactics to minimize the amount of solder attach that wicks down the via barrel:

- Intentionally space out the vias from each other to avoid a cluster of holes in a given area.
- Use the smallest drill size allowed in your design. The example in Figure 29 uses vias with a 10 mil drill hole and a 16 mil capture pad.
- Tent the opposite side of the via with solder-mask.

The number and drill size of the thermal vias should align with the end user's PCB design rules and manufacturing capabilities.

7.2 Layout Example

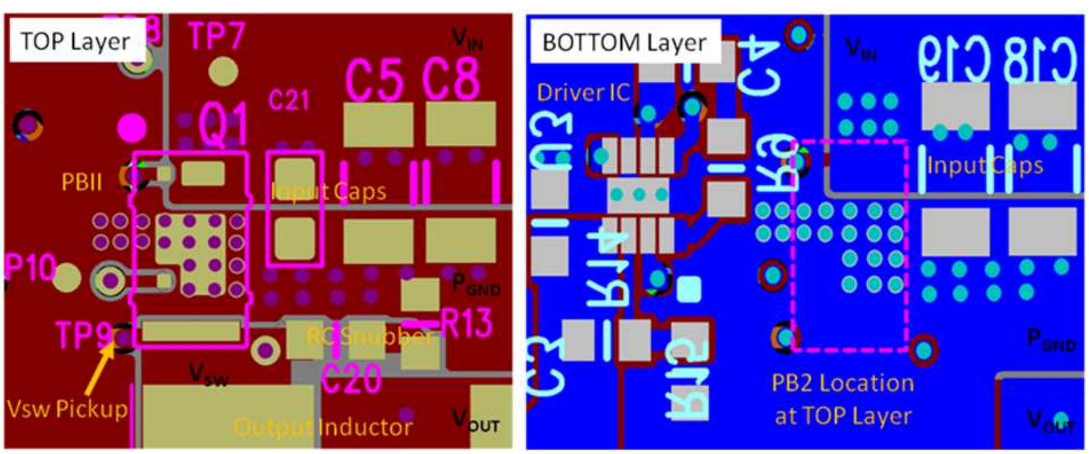


Figure 29. Recommended PCB Layout (Top Down View)

(1) Keong W. Kam, David Pommerenke, "EMI Analysis Methods for Synchronous Buck Converter EMI Root Cause Analysis", University of Missouri – Rolla

8 器件和文档支持

8.1 商标

NexFET is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

8.2 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

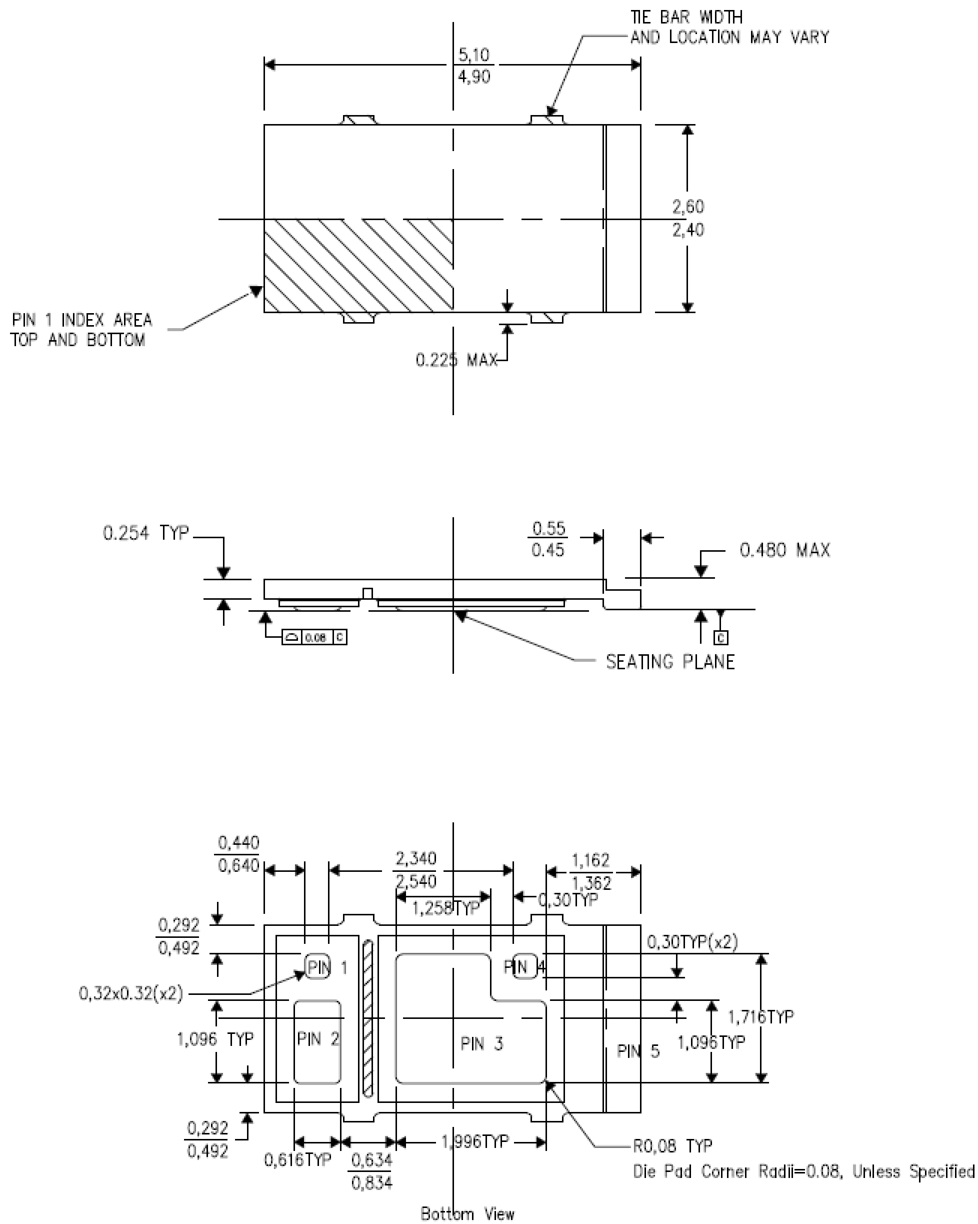
8.3 术语表

SLYZ022 — *TI 术语表*。
这份术语表列出并解释术语、首字母缩略词和定义。

9 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

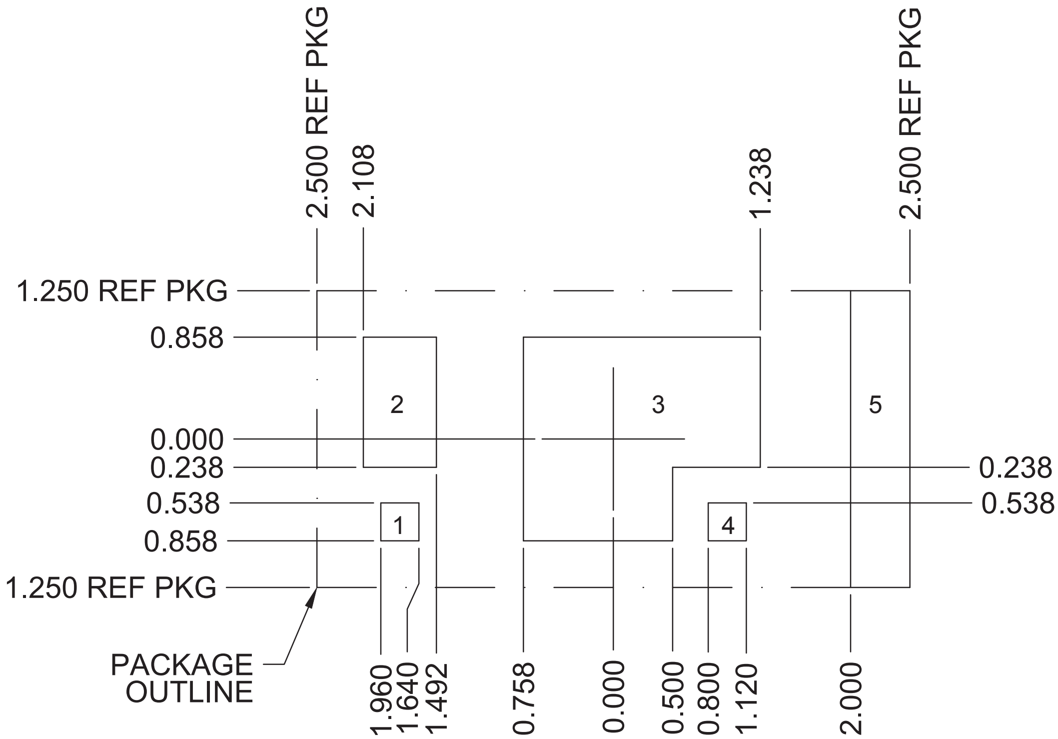
9.1 CSD87588N 封装尺寸



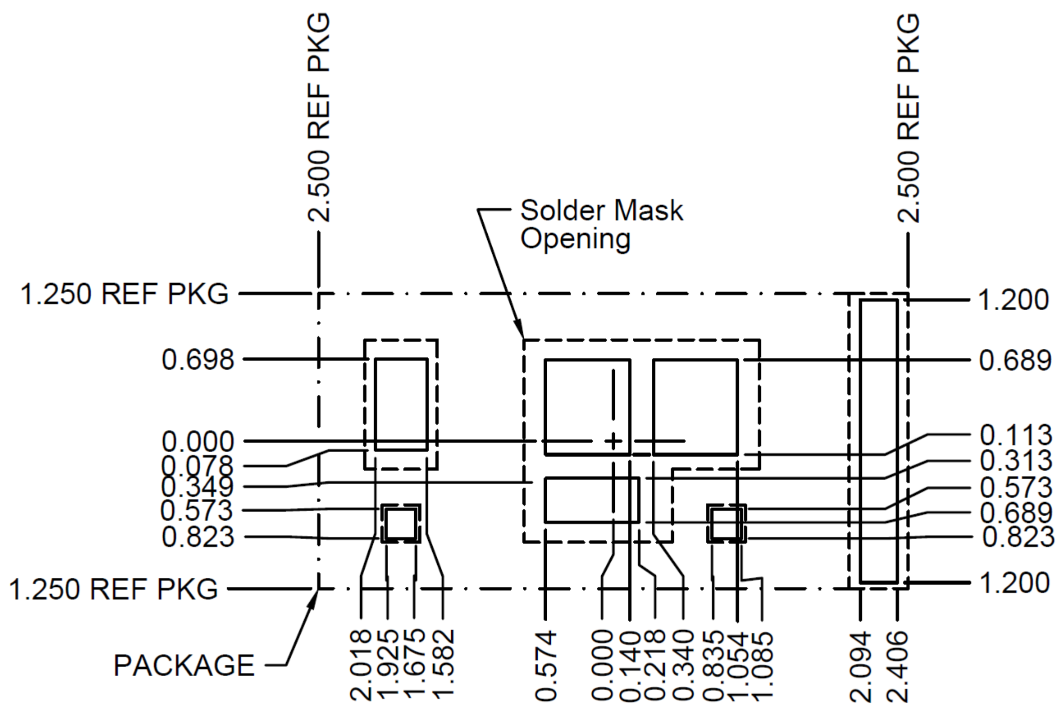
引脚配置

位置	名称
引脚 1	TG
引脚 2	V_{IN}
引脚 3	P_{GND}
引脚 4	BG
引脚 5	V_{SW}

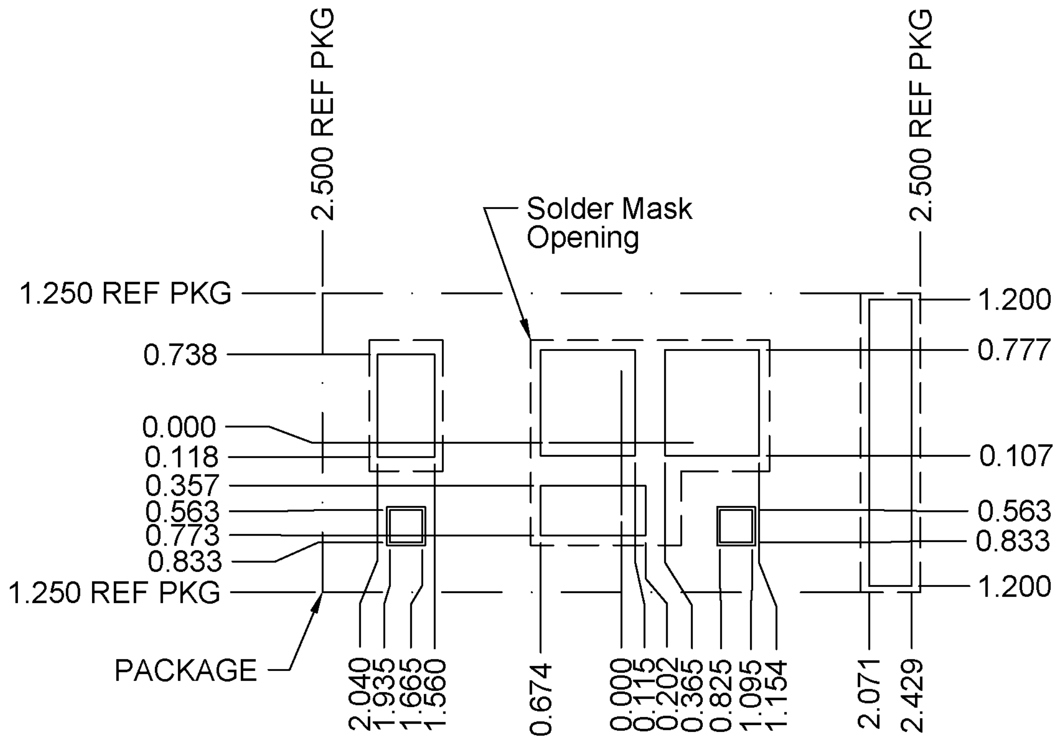
9.2 焊盘布局建议



9.3 模板建议 (100μm)

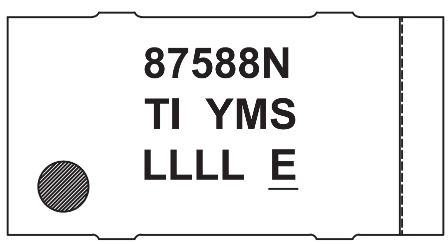


9.4 模板建议 (125μm)

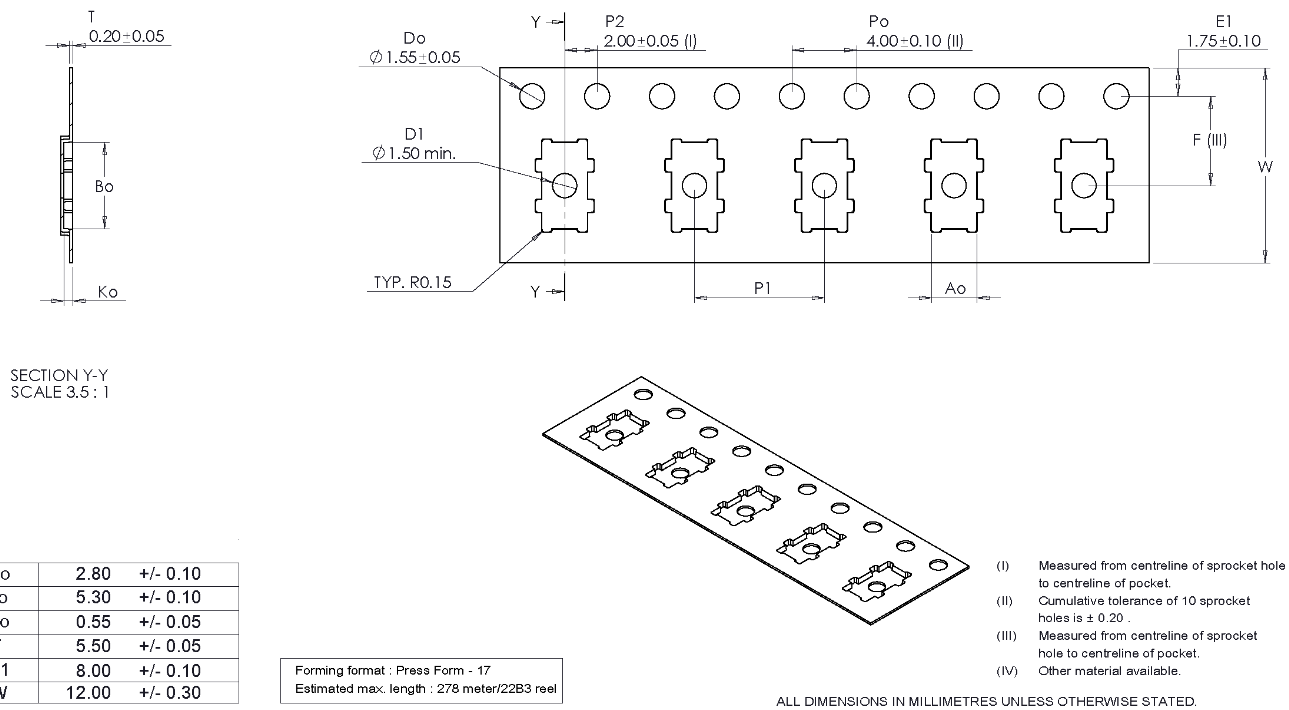


要获得与印刷电路板 (PCB) 设计相关的建议电路布局布线，请参见《应用说明》SLPA005 - *通过 PCB 布局布线技巧来减少振铃*。

9.5 引脚图



9.6 CSD87588N 压纹载带尺寸



Ao	2.80	+/- 0.10
Bo	5.30	+/- 0.10
Ko	0.55	+/- 0.05
F	5.50	+/- 0.05
P1	8.00	+/- 0.10
W	12.00	+/- 0.30

Forming format : Press Form - 17
Estimated max. length : 278 meter/22B3 reel

(1) 引脚 1 位于载带封装左上象限内（最靠近载带齿孔的位置）

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD87588N	Active	Production	PTAB (MPA) | 5	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87588N
CSD87588NT	Active	Production	PTAB (MPA) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87588N

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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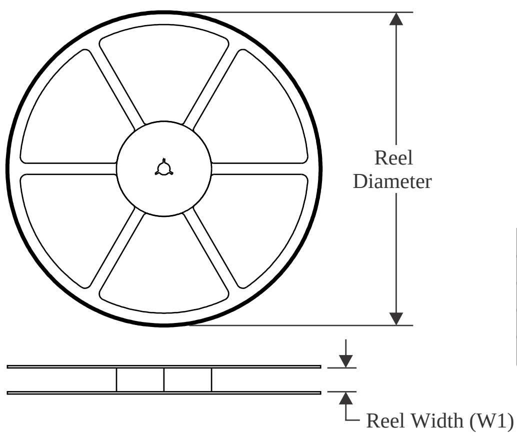
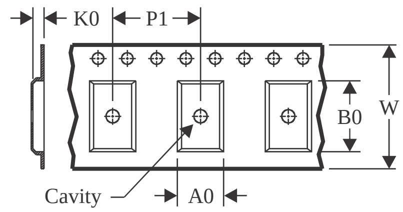
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

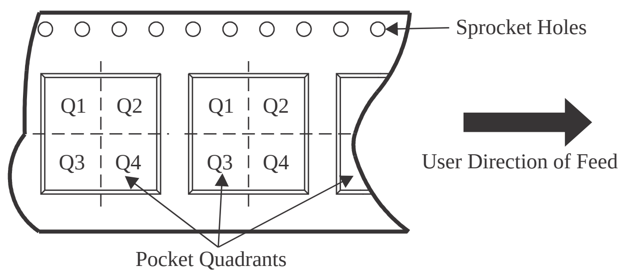


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

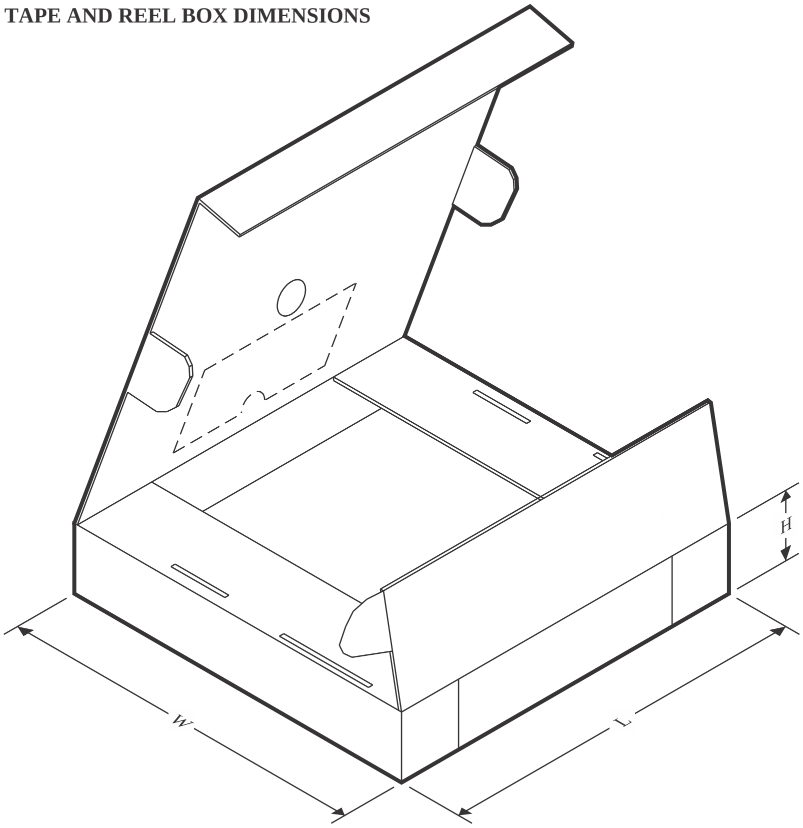
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD87588N	PTAB	MPA	5	2500	330.0	12.4	2.8	5.3	0.55	8.0	12.0	Q1
CSD87588NT	PTAB	MPA	5	250	180.0	12.4	2.8	5.3	0.55	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD87588N	PTAB	MPA	5	2500	346.0	346.0	33.0
CSD87588NT	PTAB	MPA	5	250	182.0	182.0	20.0

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