BQ25302 独立型 1 节 2.0A 降压电池充电器

1 特性

- 独立充电器且易于配置
- 高效 1.2MHz 同步开关模式降压充电器
  - 在 1A 电流（5V 输入）下具有 94.3% 的充电效率
- 单个输入，支持 USB 输入
  - 支持 4.1V 至 6.2V 输入电压范围，绝对最大输入电压额定值为 28V
  - 输入电压动态电源管理 (VINDPM) 跟踪电池电压
- 高度集成
  - 集成反向阻断和同步开关 MOSFET
  - 内部输入和充电电流检测
  - 内部环路补偿
  - 集成式自举二极管
- 4.1V/4.2V/4.35V/4.4V 充电电压
- 2.0A 最大快速充电电流
- 4.5V V_{BAT} 下的 200nA 低电池漏电流
- IC 禁用模式下的 4μA VBUS 电源电流
- 120°C 时充电电流热调节
- 预充电电流：快速充电电流的 10%
- 终止电流：快速充电电流的 10%
- 充电精度
  - 充电电压调节范围为 ±0.5%
  - 充电电流调节范围为 ±10%
- 安全
  - 热调节和热关断
  - 输入欠压锁定 (UVLO) 和过压保护 (OVP)
  - 电池过充保护
  - 预充电和快速充电安全计时器
  - 如果电流设置引脚 ICHG 开路或短路，则充电被禁用
  - 冷/热电池温度保护
  - 关于 STAT 引脚的故障报告
- 采用 WQFN 3x3-16 封装

2 应用

- 无线扬声器
- 条形码扫描仪
- 游戏
- 底座充电器
- 无线电动工具
- 楼宇自动化
- 医疗

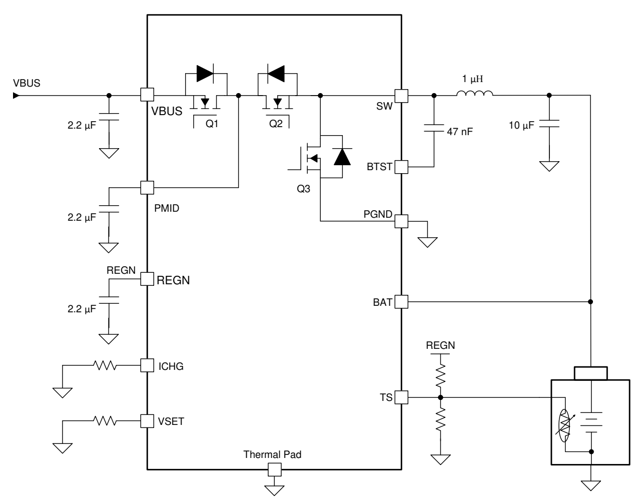
3 说明

BQ25302 是一款高度集成的独立型开关模式电池充电器，适用于单节锂离子和锂聚合物电池。BQ25302 支持 4.1V 至 6.2V 输入电压和 2A 快速充电电流。该器件的集成式电流检测拓扑可实现高充电效率和低 BOM 成本。此器件具有出色的 200nA 低静态电流，可节省电池电量并更大限度地延长便携式设备的存放时间。BQ25302 采用 3x3 WQFN 封装，适用于 2 层布局和空间有限的应用。

器件信息

器件型号(1)	封装	封装尺寸（标称值）
BQ25302	RTE	3.00mm x 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化版应用

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4 Revision History

DATE	REVISION	NOTES
October 2020	*	Initial release.

5 说明（续）

BQ25302 支持 4.1V 至 6.2V 输入电压，可为单节电池充电。 BQ25302 为单节电池提供高达 2A 的连续快速充电电流。该器件可为便携式设备进行快速充电。其输入电压调节功能可从输入源向电池提供最大充电功率。该解决方案与输入反向阻断 FET（RBFET，Q1）、高侧开关 FET（HSFET，Q2）和低侧开关 FET（LSFET，Q3）高度集成。

BQ25302 具有无损集成式电流检测功能，可通过尽可能地减少元件数量来降低功率损耗和 BOM 成本。它还集成了自举二极管以进行高侧栅极驱动和电池温度监控，从而简化系统设计。此器件无需主机控制即可启动并完成一个充电周期。BQ25302 充电电压和充电电流可通过外部电阻设定。BQ25302 在启动时检测充电电压设置，并分四个阶段为电池充电：电池短路、预调节、恒定电流和恒定电压。在充电周期结束时，如果充电电流低于终止电流阈值并且电池电压高于再充电阈值，则充电器自动终止。当电池电压下降到低于再充电阈值时，充电器将自动启动另一个充电周期。充电器为电池充电和系统操作提供各种安全特性，包括基于负温度系数 (NTC) 热敏电阻的电池温度监控、充电安全计时器、输入过压和过流保护，以及电池过压保护。还内置了引脚开路和短路保护功能，可防止充电电流设置引脚 ICHG 意外开路或对地短路。热调节功能可调节充电电流，从而在高功率运行或高环境温度条件下限制内核温度。

STAT 引脚输出报告充电状态和故障状况。当移除输入电压时，此器件以极低的电池到充电器器件漏电流自动进入高阻态模式。BQ25302 采用 3mm x 3mm 薄型 WQFN 封装。

6 Pin Configuration and Functions

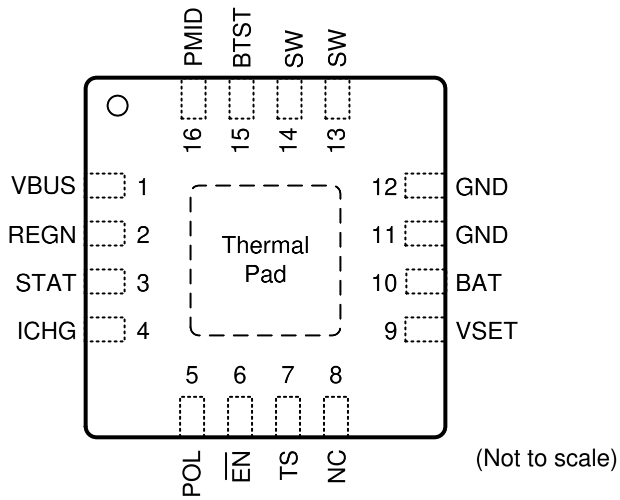


图 6-1. RTE Package 16-Pin WQFN Top View

表 6-1. Pin Functions

PIN		I/O[(1)]	DESCRIPTION
NAME	NO.		
VBUS	1	P	Charger Input Voltage. The internal n-channel reverse block MOSFET (RBFET) is connected between VBUS and PMID with VBUS on source. Place a 2.2uF ceramic capacitor from VBUS to GND and place it as close as possible to IC.
PMID	16	P	Connected to the drain of the reverse blocking MOSFET (RBFET) and the drain of high-side MOSFET (HSFET). Place ceramic 10 µF on PMID to GND and place it as close as possible to IC.
SW	13,14	P	Switching node. Connected to output inductor. Internally SW is connected to the source of the n-channel HSFET and the drain of the n-channel LSFET. Connect the 0.047 µF bootstrap capacitor from SW to BTST.
BTST	15	P	High-Side FET Driver Supply. Internally, the BTST is connected to the cathode of the internal boost-strap diode. Connect the 0.047 µF bootstrap capacitor from SW to BTST.
GND	11,12	P	Ground. Connected directly to thermal pad on the top layer. A single point connection is recommended between power ground and analog ground near the IC GND pins.
REGN	2	P	Low-Side FET driver positive supply output. Connect a 2.2 µF ceramic capacitor from REGN to GND. The capacitor should be placed close to the IC.
BAT	10	AI	Battery Voltage Sensing Input. Connect this pin to the positive terminal of the battery pack and the node of inductor output terminal. 10-µF capacitor is recommended to connect to this pin.
TS	7	AI	Battery Temperature Protection Voltage Input. Connect a negative temperature coefficient thermistor (NTC). Program temperature window with a resistor divider from REGN to TS and TS to GND. Charge suspends when TS pin voltage is out of range. When TS pin is not used, connect a 10-kΩ resistor from REGN to TS and a 10-kΩ resistor from TS to GND. It is recommended to use a 103AT-2 thermistor.
ICHG	4	AI	Charge current program input. Connect a 1% resistor RICHG from this pin to ground to program the charge current as ICHG = K_{ICHG} / R_{ICHG} (K_{ICHG} = 40,000). No capacitor is allowed to connect at this pin. When ICHG pin is pulled to ground or left open, the charger stop switching and STAT pin starts blinking.
STAT	3	AO	Charge Status Indication Output. This pin is open drain output. Connect this pin to REGN via a current limiting resistor and LED. The STAT pin indicates charger status as: • Charge in progress: STAT pin is pulled LOW • Charge completed, charge disabled by $\overline{EN}$: STAT pin is OPEN • Fault conditions: STAT pin blinks.

表 6-1. Pin Functions (continued)

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
VSET	9	AI	Charge Voltage Setting Input. VSET pin sets battery charge voltage. Program battery regulation voltage with a resistor pull-down from VSET to GND: • Floating (R > 200kΩ±10%): 4.1V • Shorted to GND (R < 510Ω): 4.2V • R = 51kΩ ± 10%: 4.35V • R = 10kΩ ± 10%: 4.4V The maximum allowed capacitance on this pin is 50pF.
POL	5	AI	This pin must be floating.
$\overline{EN}$	6	AI	Device Disable Input. The device is enabled with $\overline{EN}$ pin floating or pulled low. The device is disabled if $\overline{EN}$ pin is pulled high.
NC	8	-	No connection. Keep this pin floating or grounded.
Thermal Pad	17	-	Ground reference for the device that is also the thermal pad used to conduct heat from the device. This connection serves two purposes. The first purpose is to provide an electrical ground connection for the device. The second purpose is to provide a low thermal-impedance path from the device die to the PCB. This pad should be tied externally to a ground plane. Ground layer(s) are connected to thermal pad through vias under thermal pad.

(1) AI = Analog input, AO = Analog Output, AIO = Analog input Output, DI = Digital input, DO = Digital Output, DIO = Digital input Output, P = Power

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[(1)]

PARAMETER		MIN	MAX	UNIT
Voltage Range (with respect to GND)	VBUS (converter not switching)	–2	28	V
	PMID(converter not switching)	–0.3V	28	V
	SW	–2V[(3)]	20	V
	BTST	–0.3V	25.5	V
	STAT	–0.3V	5.5	V
	BAT	–0.3V	11	V
	BTST to SW	–0.3V	5.5	V
	ICHG	–0.3V	5.5	V
	REGN	–0.3V	5.5	V
	POL	–0.3V	5.5	V
	/EN	–0.3V	5.5	V
	TS	–0.3V	5.5	V
Voltage Range (with respect to GND)	VSET	–0.3V	11[(2)]	V
Output Sink Current	STAT		6	mA
	REGN		20	mA
Junction temperature	T_J	–40C	150	ºC
Storage temperature	T_{stg}	–65C	150	ºC

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The absolute maximum rating is specified at 11V DC voltage and up to 13V for a maximum 100us
(3) -3V for 10ns transient

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[(2)]	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
V_{VBUS}	Input voltage	4.1		6.2	V
V_{BAT}	Battery voltage			4.4	V
I_{VBUS}	Input current			2	A
I_{SW}	Output current (SW)			2	A
T_A	Ambient temperature	–40		85	°C
L	Effective inductance	0.7	1		µH
C_{VBUS}	Effective VBUS capacitance	1.1	2.2		µF

7.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
C_{PMID}	Effective PMID capacitance	5	10		µF
C_{BAT}	Effective BAT capacitance	5	10		µF

7.4 Thermal Information

THERMAL METRIC		DEVICE	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (JEDEC[1])	45.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	19.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OVP}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENT						
I_{VBUS_REVS}	VBUS reverse current from BAT/SW to VBUS, T_J = -40°C - 85°C	$V_{BAT} = V_{SW}$ = 4.5V, V_{BUS} is shorted to GND, measure V_{BUS} reverse current		0.07	3	µA
$I_{Q\_VBUS\_DIS}$	VBUS leakage current in disable mode, T_J = -40°C - 85°C	V_{BUS} = 5V, V_{BAT} = 4V, charger is disabled, /EN is pulled high			4.1	µA
$I_{Q\_BAT\_DIS}$	Leakage current from battery in disable mode, T_J = -40°C - 65°C	V_{BUS} = 5V, V_{BAT} = 4V, charger is disabled, POL is grounded /EN is floating			1.0	µA
$I_{Q\_BAT\_HIZ}$	BAT and SW pin leakage current in HiZ mode, T_J = -40°C - 65°C	$V_{BAT} = V_{SW}$ = 4.5V, V_{BUS} floating		0.17	1.0	µA
VBUS POWER UP						
V_{VBUS_OP}	V_{BUS} operating range		4.1		6.2	V
V_{VBUS_UVLOZ}	V_{BUS} power on reset	V_{BUS} rising	3.0		3.80	V
$V_{VBUS\_UVLOZ\_HYS}$	V_{BUS} power on reset hysteresis	V_{BUS} falling		250		mV
V_{VBUS_LOWV}	A condition to turnon REGN	V_{BUS} rising, REGN turns on, V_{BAT} = 3.2V	3.8	3.90	4.00	V
$V_{VBUS\_LOWV\_HYS}$	A condition to turnon REGN, hysteresis	V_{BUS} falling, REGN turns off, V_{BAT} = 3.2V		300		mV
V_{SLEEP}	Enter sleep mode threshold	V_{BUS} falling, V_{BUS} - VBAT, $V_{VBUS\_LOWV} < V_{BAT} < V_{BATREG}$	30	60	100	mV
V_{SLEEPZ}	Exit sleep mode threshold	V_{BUS} rising, $V_{BUS} - V_{BAT}$, $V_{VBUS\_LOWV} < V_{BAT} < V_{BATREG}$	110	157	250	mV
$V_{VBUS\_OVP\_RISE}$	V_{BUS} overvoltage rising threshold	V_{BUS} rising, converter stops switching	6.20	6.40	6.60	V
$V_{VBUS\_OVP\_HYS}$	V_{BUS} overvoltage falling hysteresis	V_{BUS} falling, converter stops switching		500		mV
MOSFETS						
R_{DSON_Q1}	Top reverse blocking MOSFET on-resistance between VBUS and PMID (Q1)	V_{REGN} = 5V		40	65	mΩ
R_{DSON_Q2}	High-side switching MOSFET on-resistance between PMID and SW (Q2)	V_{REGN} = 5V		50	82	mΩ

7.5 Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OVP}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{DSON_Q3}	Low-side switching MOSFET on-resistance between SW and GND (Q3)	V_{REGN} = 5V		45	72	mΩ
BATTERY CHARGER						
V_{BATREG}	Charge voltage regulation	VSET pin floating, T_J = -40°C to +85°C	4.078	4.100	4.118	V
		VSET pin is grounded, T_J = -40°C to +85°C	4.178	4.200	4.218	V
		Connect VSET pin to 51kΩ resistor, T_J = -40°C to +85°C	4.328	4.350	4.371	V
		Connect VSET pin to 10kΩ resistor, T_J = -40°C to +85°C	4.376	4.400	4.418	V
I_{CHG}	Charge current regulation	ICHG set at 1.72A with R_{ICHG}=23.2kΩ, V_{BAT} = 3.8V, VBUS = 5V	1.55	1.72	1.89	A
		ICHG set at 1.0A with RICHG=40.2kΩ, V_{BAT} = 3.8V, V_{BUS} = 5V	0.90	1.00	1.10	A
		ICHG set at 0.5A with R_{ICHG}=78.7kΩ, V_{BAT} = 3.8V, V_{BUS} = 5V	0.40	0.517	0.60	A
I_{TERM}	Termination current	ICHG = 1.72A, 10% of ICHG, RICHG=23.2kΩ, BATREG = 4.2V, VBUS = 5V	138	172	206	mA
I_{TERM}	Termination current	ICHG = 1.0A, 10% of ICHG, RICHG=40.2kΩ, BATREG = 4.2V, VBUS = 5V	70	100	130	mA
I_{TERM}	Termination current	ICHG=500mA, ITERM =63mA RICHG=78.7kΩ, BATREG = 4.2V, VBUS = 5V	33	63	93	mA
I_{PRECHG}	Precharge current	ICHG = 1.72A, 10% of ICHG, R_{ICHG}=23.2kΩ, V_{BATREG} = 4.2V, V_{BAT} = 2.5V, V_{BUS} = 5V	115	172	225	mA
		ICHG = 1.72A, 10% of ICHG, R_{ICHG}=40.2kΩ, V_{BATREG} = 4.2V, V_{BAT} = 2.5V, V_{BUS} = 5V	50	100	150	mA
		ICHG = 1.72A, 10% of ICHG, R_{ICHG}=78.7kΩ, V_{BATREG} = 4.2V, V_{BAT} = 2.5V, V_{BUS} = 5V	28	63	98	mA
$V_{BAT\_SHORT\_RISE}$	VBAT short rising threshold	Short to precharge	2.05	2.20	2.35	V
$V_{BAT\_SHORT\_FALL}$	VBAT short falling threshold	Precharge to battery short	1.85	2.00	2.15	V
I_{BAT_SHORT}	Battery short current	$V_{BAT} < V_{BAT\_SHORT\_FALL}$, V_{BUS} = 5V	24	30	36	mA
$V_{BAT\_LOWV\_RISE}$	Rising threshold	Precharge to fast charge	2.90	3.00	3.10	V
$V_{BAT\_LOWV\_FALL}$	Falling threshold	Fast charge to precharge	2.60	2.70	2.80	V
V_{RECHG_HYS}	Recharge hysteresis below V_{BATREG}	V_{BAT} falling	110	160	216	mV
INPUT VOLTAGE / CURRENT REGULATION						
V_{INDPM_MIN}	Minimum input voltage regulation	V_{BAT} = 3.5V, measured at PMID pin	4.0	4.07	4.2	V
V_{INDPM}	Input voltage regulation	V_{BAT} = 4V, measured at PMID pin, V_{INDPM} = 1.044*V_{BAT} + 0.125V	4.15	4.28	4.41	V
$I_{INDPM\_2A\_5V}$	Input current regulation	V_{VBUS} = 5V	2.1	2.25	2.4	A
BATTERY OVER-VOLTAGE PROTECTION						
$V_{BAT\_OVP\_RISE}$	Battery overvoltage rising threshold	V_{BAT} rising, as percentage of VBATREG	101.9	103.5	105	%
$V_{BAT\_OVP\_FALL}$	Battery overvoltage falling threshold	V_{BAT} falling, as percentage of VBATREG	100.0	101.6	103.1	%
CONVERTER PROTECTION						

7.5 Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OVP}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{BTST\_REFRESH}$	Bootstrap refresh comparator threshold	(V_{BTST} - V_{SW}) when LSFET refresh pulse is requested, V_{BUS} = 5V	2.7	3	3.3	V
I_{HSFET_OCP}	HSFET cycle by cycle over current limit threshold		5.2	6.2	6.7	A
STAT INDICATION						
I_{STAT_SINK}	STAT pin sink current		6			mA
F_{BLINK}	STAT pin blink frequency			1		Hz
F_{BLINK_DUTY}	STAT pin blink duty cycle			50		%
THERMAL REGULATION AND THERMAL SHUTDOWN						
T_{REG}	Junction temperature regulation accuracy		111	120	133	°C
T_{SHUT}	Thermal shutdown rising threshold	Temperature increasing		150		°C
	Thermal shutdown falling threshold	Temperature decreasing		125		°C
BUCK MODE OPERATION						
F_{SW}	PWM switching frequency	SW node frequency	1.02	1.20	1.38	MHz
D_{MAX}	Maximum PWM Duty Cycle			97.0		%
REGN LDO						
V_{REGN_UVLO}	REGN UVLO	V_{VBUS} rising			3.85	V
V_{REGN}	REGN LDO output voltage	V_{VBUS} = 5V, I_{REGN} = 0 to 16mA	4.2		5.0	V
ICHG SETTING						
V_{ICHG}	ICHG pin regulated voltage		993	998	1003	mV
$R_{ICHG\_SHORT\_FALL}$	Maximum resistance to disable charge	V_{BUS}=5V			1.00	kΩ
$R_{ICHG\_OPEN\_RISE}$	Minimum resistance to disable charge	V_{BUS}=5V,	565			kΩ
R_{ICHG_MAX}	Maximum programmable resistance at ICHG	V_{BUS}=5V			250.00	kΩ
$R_{ICHG\_MIN\_SLE0}$	Minimum programmable resistance at ICHG	V_{BUS}=5V	17.40			kΩ
R_{ICHG_HIGH}	ICHG setting resistor threshold to clamp precharge and termination current to 63mA	$R_{ICHG} > R_{ICHG\_HIGH}$	60.0	65.0	70.0	kΩ
K_{ICHG}	Charge current ratio	ICHG set at 1.72A with R_{ICHG} = 23.2kΩ, V_{BAT}=3.8V, V_{BUS}=5V, $I_{CHG} = K_{ICHG} / R_{ICHG}$	36000	40000	44000	AxΩ
K_{ICHG}	Charge current ratio	ICHG set at 1.0A with R_{ICHG} = 40.2kΩ, V_{BAT} = 3.8V, V_{BUS} = 5V, $I_{CHG} = K_{ICHG} / R_{ICHG}$	36000	40280	44000	AxΩ
K_{ICHG}	Charge current ratio	ICHG set at 0.5A with R_{ICHG} = 78.7kΩ, V_{BAT} = 3.8V, V_{BUS} = 5V, $I_{CHG} = K_{ICHG} / R_{ICHG}$	32000	40700	48000	AxΩ
COLD/HOT THERMISTOR COMPARATOR						
V_{T1}%	TCOLD (0°C) threshold, charge suspended if thermistor temperature is below T1	V_{TS} rising, as percentage to V_{REGN}	72.68	73.5	74.35	%
V_{T1}%	V_{TS} falling	As Percentage to V_{REGN}	70.68	71.5	72.33	%
V_{T3}%	THOT (45°C) threshold, charge suspended if thermistor temperature is above T_HOT	V_{TS} falling, as percentage to V_{REGN}	46.35	47.25	48.15	%

7.5 Electrical Characteristics (continued)

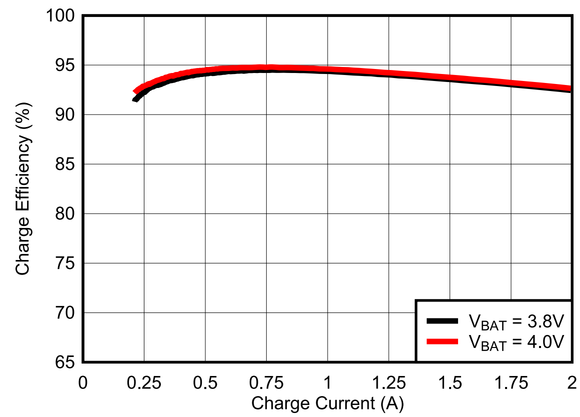
V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{T3}%	V_{TS} rising	As percentage to VREGN	47.35	48.25	49.15	%
LOGIC I/O PIN CHARACTERESTICS (POL, EN)						
V_{ILO}	Input low threshold	Falling			0.40	V
V_{IH}	Input high threshold	Rising	1.3			V
I_{BIAS}	High-level leakage current at /EN pin	/EN pin is pulled up to 1.8 V		1.0		µA

7.6 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
VBUS/BAT POWER UP						
t_{VBUS_OV}	VBUS OVP reaction-time	VBUS rising above V_{BUS_OV} threshold to converter turnoff		200		ns
$t_{CHG\_ON\_EN}$	Delay from enable at /EN pin to charger power on	/EN pin voltage rising		245		ms
$t_{CHG\_ON\_VBUS}$	Delay from VBUS to charge start	/EN pin is grounded, batttery present		275		ms
BATTERY CHARGER						
t_{SAFETY_FAST}	Charge safety timer	Fast charge safety timer 20 hours	15.0	20.0	24.0	hr
t_{SAFETY_PRE}	Charge safety timer	Precharge safety timer	1.5	2.0	2.5	hr

7.7 Typical Characteristics



f_{SW} = 1.2 MHz   Inductance 1 uH

V_{BUS} = 5 V   Inductor DCR = 14.6 mΩ

图 7-1. Battery Charge Efficiency vs. Charge Current

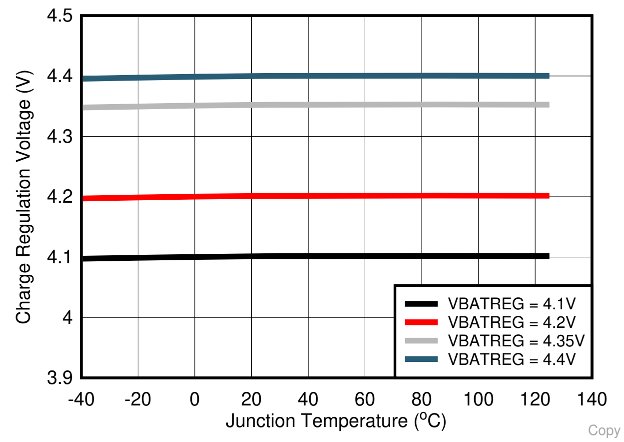


图 7-2. Battery Charge Regulation Voltage vs. Junction Temperature

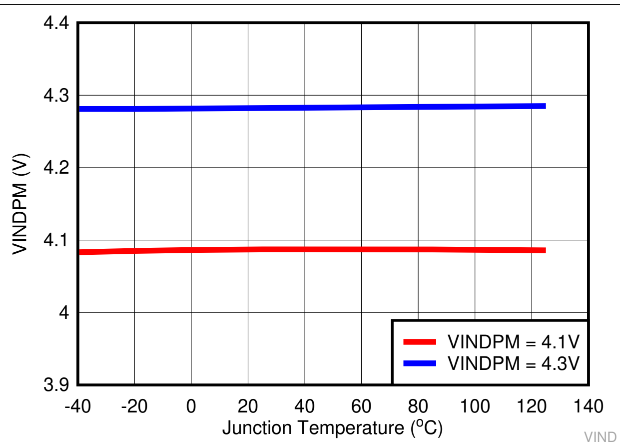


图 7-3. VINDPM vs. Junction Temperature

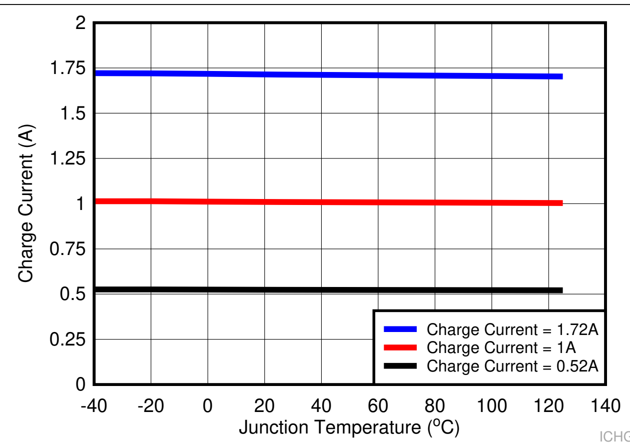


图 7-4. Charge Current vs. Junction Temperature

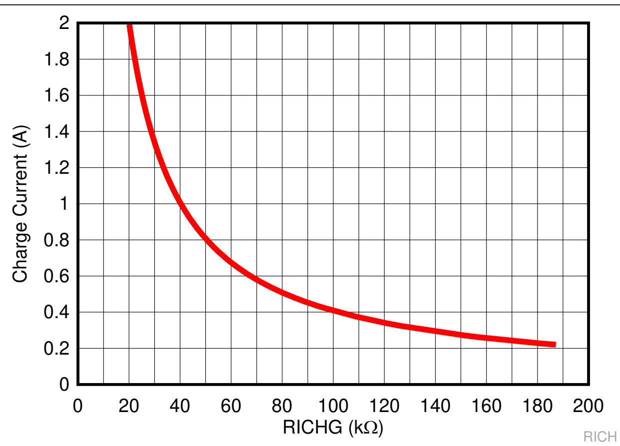


图 7-5. Charge Current vs. Charge Current Setting Resistance RICHG

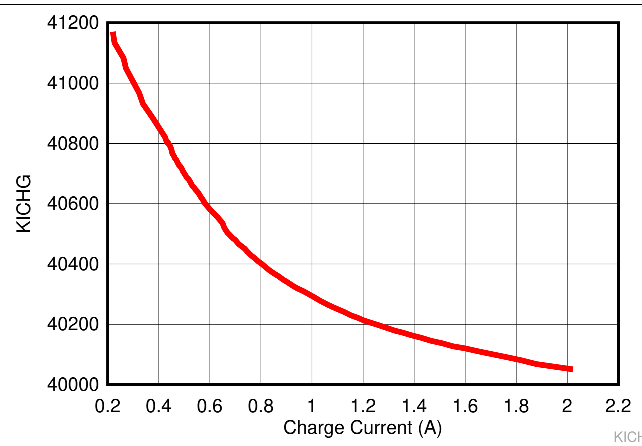


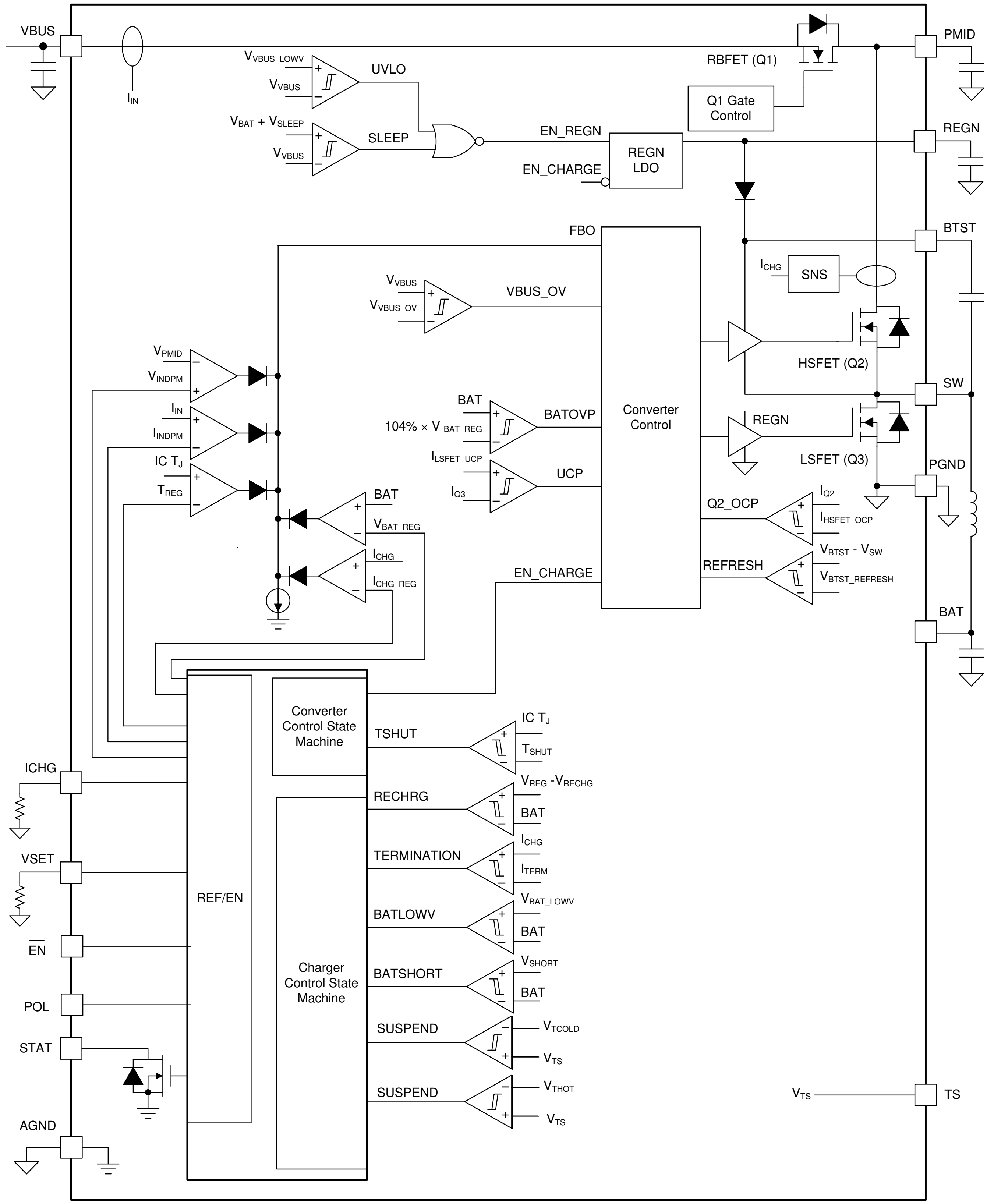
图 7-6. KICHG vs. Charge Current

8 Detailed Description

8.1 Overview

The BQ25302 is a highly integrated standalone switch-mode battery charger for single cell Li-Ion and Li-polymer batteries with charge voltage and charge current programmable by an external resistor. It includes an input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and bootstrap diode for the high-side gate drive as well as current sensing circuitry.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Device Power Up

The $\overline{EN}$ pin enable or disable the device. When the device is disabled, the device draws minimum current from VBUS pin. POL grouding or floating determines the polority of the $\overline{EN}$ pin. The device can be powered up from either VBUS or by enabling the device from $\overline{EN}$ pin.

8.3.1.1 Power-On-Reset (POR)

The $\overline{EN}$ pin can enable or disable the device. When the device is disabled, the device is in disable mode and it draws minimum current at VBUS. When the device is enabled, if VBUS rises above V_{VBUS_UVLOZ}, the device powers part of internal bias and comparators and starts Power on Reset (POR).

8.3.1.2 REGN Regulator Power Up

The internal bias circuits are powered from the input source. The REGN supplies internal bias circuits as well as the HSFET and LSFET gate drive. The REGN also provides voltage rail to STAT LED indication. The REGN is enabled when all the below conditions are valid:

- Chip is enabled by $\overline{EN}$ pin
- V_{VBUS} above V_{VBUS_UVLOZ}
- V_{VBUS} above V_{BAT} + V_{SLEEPZ}
- After sleep comparator deglitch time, VSET detection time, and REGN delay time

REGN remains on at fault conditions. REGN is powered by VBUS only and REGN is off when VBUS power is removed.

8.3.1.3 Charger Power Up

Following REGN power-up, if there is no fault conditions, the charger powers up with soft start. If there is any fault, the charger will remain off until fault is clear. Any of the fault conditions below gates charger power-up:

- $V_{VBUS} > V_{VBUS\_OVP}$
- Thermistor cold/hot fault on TS pin
- $V_{BAT} > V_{BAT\_OVP}$
- Safety timer fault
- ICHG pin is open or short to GND
- Die temperature is above TSHUT

8.3.1.4 Charger Enable and Disable by $\overline{EN}$ Pin

The charger can be enabled or disabled by $\overline{EN}$ pin pulled high or low. The charger is in disable mode when disabled.

8.3.1.5 Device Unplugged from Input Source

When V_{BUS} is removed from an adaptor, the device stays in HiZ mode and the leakage current from the battery to BAT pin and SW pin is less than $I_{Q\_BAT\_HIZ}$.

8.3.2 Battery Charging Management

The BQ25302 charges 1-cell Li-Ion battery with up to 2.0-A charge current from 4.1-V to 6.2-V input voltage. A new charge cycle starts when the charger power-up conditions are met. The charge voltage is set by external resistor connected at VSET pin and charge current are set by external resistors at ICHG pin. The charger terminates the charging cycle when the charging current is below termination threshold I_{TERM} and charge voltage is above recharge threshold (V_{BATREG} - V_{RECHG_HYS}), and device is not in IINDPM or thermal regulation. When a fully charged battery's voltage is discharged below recharge threshold, the device automatically starts a new charging cycle with safety timer reset. To initiate a recharge cycle, the conditions of charger power-up must be met. The STAT pin output indicates the charging status of charging (LOW), charging complete or charge disabled (HIGH) or charging faults (BLINKING).

8.3.2.1 Battery Charging Profile

The device charges the battery in four phases: battery short, preconditioning, constant current, constant voltage. The device charges battery based on charge voltage set by VSET pin and charge current set by ICHG pin as well as actual battery voltage. The battery charging profile is shown in 图 8-1. The battery short current is provided by internal linear regulator.

表 8-1. Charging Current Setting

MODE	BATTERY VOLTAGE V_{BAT}	CHARGE CURRENT	TYPICAL VALUE
Battery Short	$V_{BAT} < V_{BAT\_SHORT}$	I_{BAT_SHORT}	30 mA
Precharge	$V_{BAT\_SHORT} < V_{BAT} < V_{BAT\_LOWV}$	I_{PRECHG}	10% of I_{CHG}
Fast Charge	$V_{BAT\_LOWV} < V_{BAT}$	I_{CHG}	Set by ICHG resistor

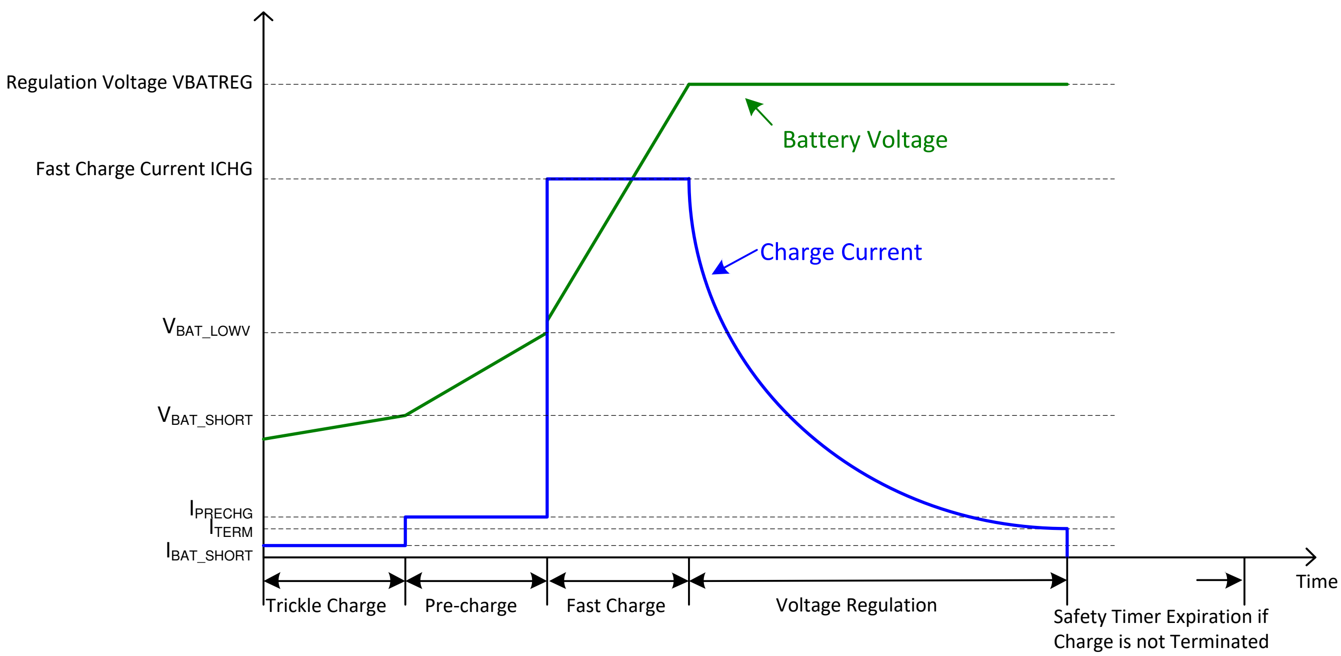


图 8-1. Battery Charging Profile

8.3.2.2 Precharge

The device charges the battery at 10% of set fast charge current in precharge mode. When $R_{ICHG} > R_{ICHG\_HIGH}$, the precharge current is clamped at 63mA.

8.3.2.3 Charging Termination

The device terminates a charge cycle when the battery voltage is above recharge threshold and the charge current is below termination current. After a charging cycle is completed, the charger is terminated and the system load is powered from battery. Termination is temporarily disabled when the charger device is in input current regulation or thermal regulation mode and the charging safety timer is counted at half the clock rate. The charge termination current is 10% of set fast charge current if $R_{ICHG} < R_{ICHG\_HIGH}$. The termination current is clamped at 63mA if $R_{ICHG} > R_{ICHG\_HIGH}$.

8.3.2.4 Battery Recharge

A charge cycle is completed when battery is fully charged with charge terminated. If the battery voltage decreases below the recharge threshold (V_{BATREG} - V_{RECHG_HYS}), the charger is enabled with safety timer reset and enabled.

8.3.2.5 Charging Safety Timer

The device has built-in safety timer to prevent extended charging cycle due to abnormal battery conditions. The safety timer is 20 hours when the battery voltage is above V_{BAT_LOWV} threshold and 2 hours below V_{BAT_LOWV} threshold. When the safety timer expires, charge is suspended until the safety timer is reset. Safety timer is reset and charge starts under one of the following conditions:

- Battery voltage falls below recharge threshold
- VBUS voltage is recycled
- $\overline{EN}$ pin is toggled
- Battery voltage transits across V_{BAT_SHORT} threshold
- Battery voltage transits across V_{BAT_LOWV} threshold

If the safety timer expires and the battery voltage is above recharge threshold, the charger is suspended and the STAT pin is open. If the safety timer expires and the battery voltage is below the recharge threshold, the charger is suspended and the STAT pin blinks to indicate a fault. The safety timer fault is cleared with safety timer reset.

During input current regulation, thermal regulation, the safety timer counts at half the original clock frequency and the safety timer is doubled. During TS fault, V_{BUS_OVP}, V_{BAT_OVP}, ICHG pin open and short, and IC thermal shutdown faults, the safety timer is suspended. Once the fault(s) is clear, the safety timer resumes to count.

8.3.2.6 Thermistor Temperature Monitoring

The charger device provides a single thermistor input TS pin for battery temperature monitor. RT1 and RT2 programs the cold temperature T1 and hot temperature T3. In the equations, $R_{NTC,T1}$ is NTC thermistor resistance value at temperature T1 and $R_{NTC,T3}$ is NTC thermistor resistance values at temperature T3. Assuming RHOT = 0, select 0°C to 45°C for battery charge temperature range, then NTC thermistor 103AT-2 resistance $R_{NTC,T1}$ = 27.28 kΩ (at 0°C) and $R_{NTC,T3}$ = 4.91 kΩ (at 45°C), from the 方程式 1 and 方程式 2, RT1 and RT2 are derived as:

- RT1 = 4.527 kΩ
- RT2 = 23.26 kΩ

On top of the calculation results, adding RHOT resisitor can shift HOT temperature T3 up and only slightly shift up COLD temperature T1. The actual temperature T3 can be looked up in a NTC resistance table based on ($R_{NTC,T3}$ - RHOT) and T1 can be looked up in a NTC resistance table based on ($R_{NTC,T1}$ - RHOT). Because $R_{NTC,T1}$ is much higher than $R_{NTC,T3}$, RHOT can adjust HOT temperature significantly with mimimal affect on COLD temperature. RHOT is optional.

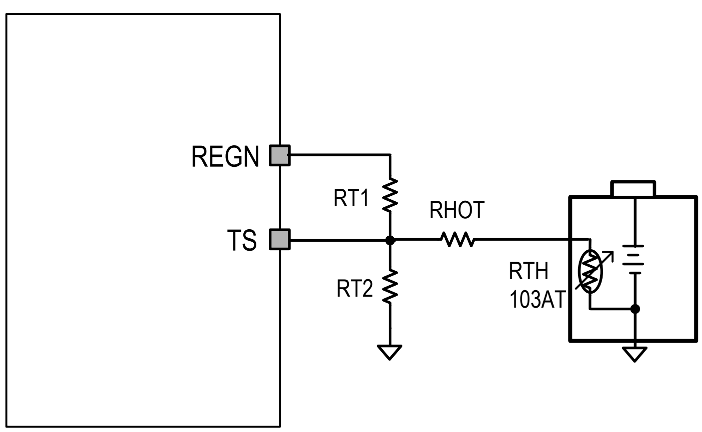


图 8-2. Battery Temperature Sensing Circuit

$$RT2 = \frac{R_{NTC,T1} \times R_{NTC,T3} \times \left(\frac{1}{V_{T3}\%} - \frac{1}{V_{T1}\%}\right)}{R_{NTC,T1} \times \left(\frac{1}{V_{T1}\%} - 1\right) - R_{NTC,T3} \times \left(\frac{1}{V_{T3}\%} - 1\right)} \tag{1}$$

$$RT1 = \frac{\frac{1}{V_{T1}\%} - 1}{\frac{1}{R_{T2}} + \frac{1}{R_{NTC,T1}}} \tag{2}$$

8.3.3 Charging Status Indicator (STAT)

The device indicates charging state on the open drain STAT pin. The STAT pin can drive a LED that is pulled up to REGN rail through a current limit resistor.

表 8-2. STAT Pin State

CHARGING STATE	STAT INDICATOR
Charging in progress (including recharge)	LOW
Charging complete	HIGH
HiZ mode, sleep mode, charge disable	HIGH
Safety timer expiration with battery voltage above recharge threshold	HIGH
Charge faults: 1. VBUS input over voltage 2. TS cold/hot faults 3. Battery over voltage 4. IC thermal shutdown 5. Safety timer expiration with battery voltage below recharge threshold 6. ICHG pin open or short	BLINKING at 1 Hz with 50% duty cycle

8.3.4 Protections

8.3.4.1 Voltage and Current Monitoring

The device closely monitors the input voltage and input current for safe operation.

8.3.4.1.1 Input Over-Voltage Protection

This device integrates the functionality of an input over-voltage protection (OVP). The input OVP threshold is $V_{VBUS\_OVP\_RISE}$. During an input over-voltage event, the converter stops switching and safety timer stops counting as well. The converter resumes switching and the safety timer resumes counting once the VBUS voltage drops back below ($V_{VBUS\_OVP\_RISE}$ - $V_{VBUS\_OVP\_HYS}$). The REGN LDO remains on during an input over-voltage event. The STAT pin blinks during an input OVP event.

8.3.4.1.2 Input Voltage Dynamic Power Management (VINDPM)

When the input current of the device exceeds the current capability of the power supply, the charger device regulates PMID voltage by reducing charge current to avoid crashing the input power supply. VINDPM dynamically tracks the battery voltage. The actual VINDPM is the higher of V_{INDPM_MIN} and (1.044*VBAT + 125mV).

8.3.4.1.3 Input Current Limit

The device has built-in input current limit. When the input current is over the threshold I_{INDPM}, the converter duty cycle is reduced to reduce input current.

8.3.4.1.4 Cycle-by-Cycle Current Limit

High-side (HS) FET current is cycle-by-cycle limited. Once the HSFET peak current hits the limit I_{HSFET_OCP}, the HSFET shuts down until the current is reduced below a threshold.

8.3.4.2 Thermal Regulation and Thermal Shutdown

The device monitors the junction temperature T_J to avoid overheating the chip and limit the device surface temperature. When the internal junction temperature exceeds thermal regulation limit T_{REG}, the device lowers down the charge current. During thermal regulation, the average charging current is usually below the programmed battery charging current. Therefore, termination is disabled and the safety timer runs at half the clock rate.

Additionally, the device has thermal shutdown built in to turn off the charger when device junction temperature exceeds T_{SHUT}. The charger is reenabled when the junction temperature is 25°C below T_{SHUT}. During thermal shutdown, the safety timer stops counting and it resumes when the temperature drops below the threshold.

8.3.4.3 Battery Protection

8.3.4.3.1 Battery Over-Voltage Protection (V_{BAT_OVP})

The battery voltage is clamped at 3.5% above the battery regulation voltage. When the battery voltage is over $V_{BAT\_OVP\_RISE}$, the converter stops switching until the battery voltage is below the falling threshold. During a battery over-voltage event, the safety timer stops counting and STAT pin reports the fault and it resumes once the battery voltage falls below the falling threshold. A 7-mA pull-down current is on the BAT pin once BAT_OVP is triggered. BAT_OVP may be triggered in charging mode, termination mode, and fault mode.

8.3.4.3.2 Battery Short Circuit Protection

When the battery voltage falls below the V_{BAT_SHORT} threshold, the charge current is reduced to I_{BAT_SHORT}.

8.3.4.4 ICHG Pin Open and Short Protection

To protect against ICHG pin is short or open, the charger immediately shuts off once ICHG pin is open or short to GND and STAT pin blinks to report the fault. At powerup, if ICHG pin is detected open or short to GND, the charge will not power up until the fault is clear.

8.4 Device Functional Modes

8.4.1 Disable Mode, HiZ Mode, Sleep Mode, Charge Mode, Termination Mode, and Fault Mode

The device operates in different modes depending on VBUS voltage, battery voltage, and $\overline{EN}$ pin, POL pin, and ICHG pin connection. The functional modes are listed in the following table.

表 8-3. Device Functional Modes

MODE	CONDITIONS	REGN LDO	CHARGE ENABLED	STAT PIN
Disable Mode	Device is disable	OFF	NO	OPEN
HiZ Mode	$V_{VBUS} < V_{VBUS\_UVLOZ}$ and device is enabled	OFF	NO	OPEN
Sleep Mode	$V_{VBUS} > V_{VBUS\_UVLOZ}$ and $V_{VBUS} < V_{BAT} + V_{SLEEPZ}$ and device is enabled	OFF	NO	OPEN
Charge Mode	$V_{VBUS} > V_{VBUS\_LOWV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEPZ}$ and device is enabled, no faults, charge is not terminated	ON	YES	SHORT to GND
Charge Termination Mode	$V_{VBUS} > V_{VBUS\_LOWV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEPZ}$ and device is enabled, no faults, charge is terminated	ON	NO	OPEN
Fault Mode	V_{BUS_OVP}, TS cold/hot, V_{BAT_OVP}, IC thermal shutdown, safety timer fault, ICHG pin open or short	ON	NO	BLINKING

9 Application and Implementation

备注

以下应用部分的信息不属于 TI 组件规范，TI 不担保其准确性和完整性。客户应负责确定 TI 组件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

A typical application consists of a single cell battery charger for Li-Ion, Li-polymer batteries used in a wide range of portable devices and accessories. It integrates an input reverse-block FET (RBFET, Q1), high-side switching FET (HSFET, Q2), and low-side switching FET (LSFET, Q3). The Buck converter output is connected to the battery directly to charge the battery and power system loads. The device also integrates a bootstrap diode for high-side gate drive.

9.2 Typical Applications

The typical applications in this section include a standalone charger without power path, a standalone charger with external power path, and a typical application with MCU programmed charge current.

9.2.1 Typical Application

The typical application in this section includes a standalone charger without power path.

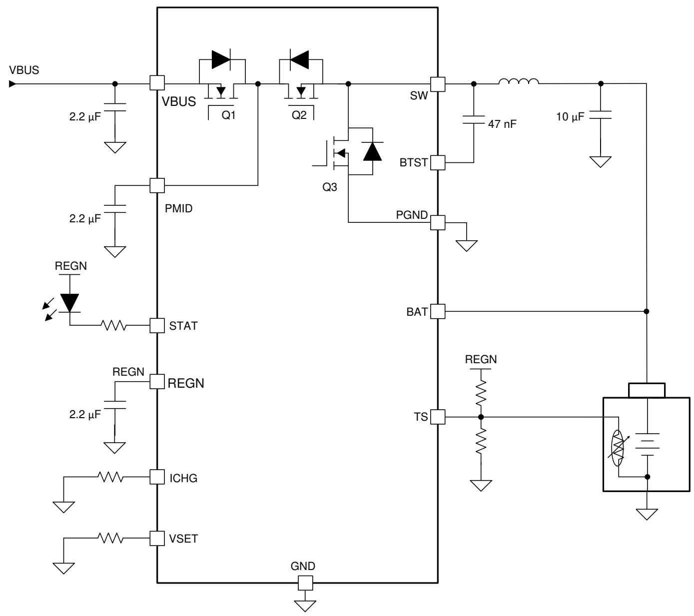


图 9-1. Typical Application Diagram (1-µH inductor is recommended)

9.2.1.1 Design Requirements

表 9-1. Design Requirements

PARAMETER	VALUE
Input Voltage	4.1V to 6.2V
Input Current	2.0A
Fast Charge Current	2.0A
Battery Regulation Voltage	4.1V/4.2V/4.35V/4.4V

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Charge Voltage Settings

Battery charge voltage is set by a resistor connected at the VSET pin. When the REGN LDO startup conditions are met, and before the REGN LDO powers up, the internal VSET detection circuit is enabled to detect VSET pin resistance and set battery charge voltage accordingly. The VSET detection circuit is disabled after detection is complete and changing resistance values on the fly does not change the battery charge voltage. VSET detection is reenabled once the REGN LDO is recycled.

9.2.1.2.2 Charge Current Setting

The charger current is set by the resistor value at the ICHG pin according to the equation below:

I_{CHG} (A) = K_{ICHG} (A·Ω) / R_{ICHG}(Ω)

K_{ICHG} is a coefficient that is listed in Electrical Characteristics table and R_{ICHG} is the resistor value from ICHG pin to GND. K_{ICHG} is typically 40,000 (A·Ω) and it is slightly shifted up at lower charge current setting. The K_{ICHG} vs. ICHG typical characteresitc curve is shown in 图 7-6.

9.2.1.2.3 Inductor Selection

The 1.2-MHz switching frequency allows the use of small inductor and capacitor values to maintain an inductor saturation current higher than the charging current (I_{CHG}) plus half the ripple current (I_{RIPPLE}):

$$I_{SAT} \geqslant I_{CHG} + (1/2)\, I_{RIPPLE} \tag{3}$$

The inductor ripple current depends on the input voltage (V_{VBUS}), the duty cycle ($D = V_{BAT}/V_{VBUS}$), the switching frequency (f_S) and the inductance (L).

$$I_{RIPPLE} = \frac{V_{IN} \times D \times (1 - D)}{fs \times L} \tag{4}$$

The maximum inductor ripple current occurs when the duty cycle (D) is 0.5 or approximately 0.5. Usually inductor ripple is designed in the range between 20% and 40% maximum charging current as a trade-off between inductor size and efficiency for a practical design.

9.2.1.2.4 Input Capacitor

Design input capacitance to provide enough ripple current rating to absorb the input switching ripple current. Worst case RMS ripple current is half of the charging current when the duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current I_{Cin} occurs where the duty cycle is closest to 50% and can be estimated using 方程式 5.

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1 - D)} \tag{5}$$

A low ESR ceramic capacitor such as X7R or X5R is preferred for the input decoupling capacitor and should be placed as close as possible to the drain of the high-side MOSFET and source of the low-side MOSFET. The voltage rating of the capacitor must be higher than the normal input voltage level. A rating of 16-V or higher capacitor is preferred for 5-V input voltage.

9.2.1.2.5 Output Capacitor

Ensure that the output capacitance has enough ripple current rating to absorb the output switching ripple current. The equation below shows the output capacitor RMS current I_{COUT} calculation.

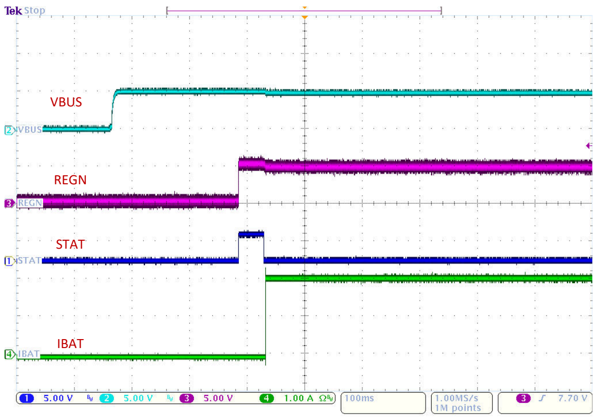
$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \tag{6}$$

The output capacitor voltage ripple can be calculated as follows:

$$\Delta V_O = \frac{V_{OUT}}{8LCfs^2}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \tag{7}$$

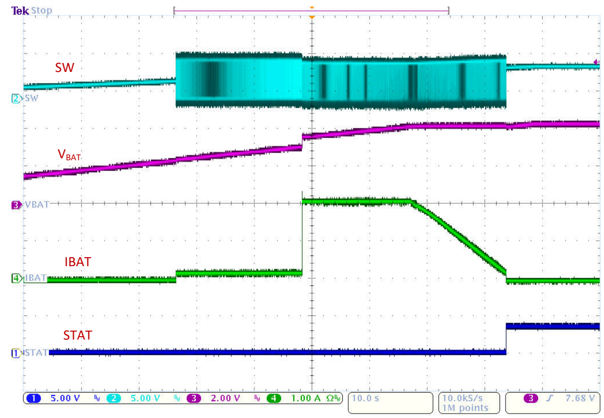
At certain input and output voltage and switching frequency, the voltage ripple can be reduced by increasing the output filter LC.

9.2.1.3 Application Curves



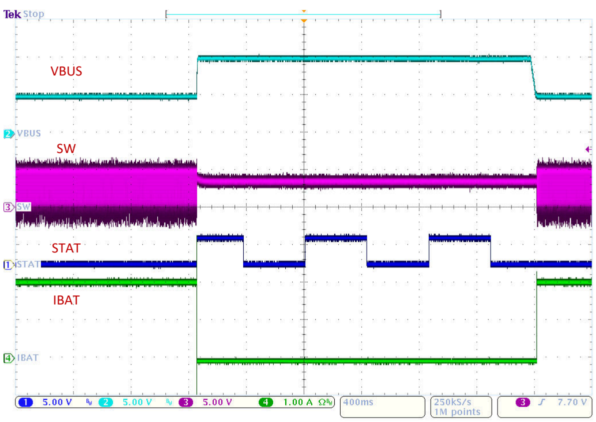
VBUS = 5 V
ICHG = 2A
Device Enabled

图 9-2. Power Up from VBUS



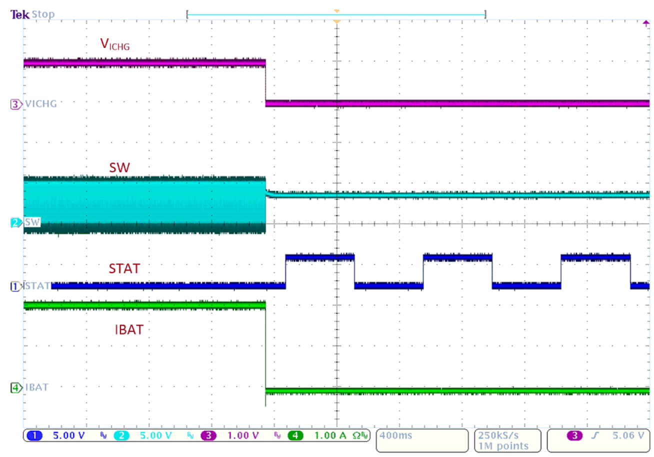
VBUS = 5 V
ICHG = 2 A
VBAT = 1.5V - 4.2V
VBATREG = 4.2V

图 9-3. Charge Cycle with Battery Simulator



VBUS = 5 V - 10V - 5V
ICHG = 2A
Adaptor Currrent Limit: 1A
VBAT =3.5V

图 9-4. VBUS into and out of Over Voltage Protection (OVP)



VBUS = 5 V
From ICHG = 2A to ICHG pin short

图 9-5. ICHG Pin Short Circuit Protection

9.2.2 Typical Application with External Power Path

In the case where a system needs to be immediately powered up from VBUS when the battery is overdischarged or dead, the application circuit shown in 图 9-6 can be used to provide a power path from VBUS/PMID to VSYS. PFET Q4 is an external PFET that turns on to supply VSYS from the battery when VBUS is removed; PFET Q4 turns off when VBUS is plugged in and VSYS is supplied from VBUS/PMID.

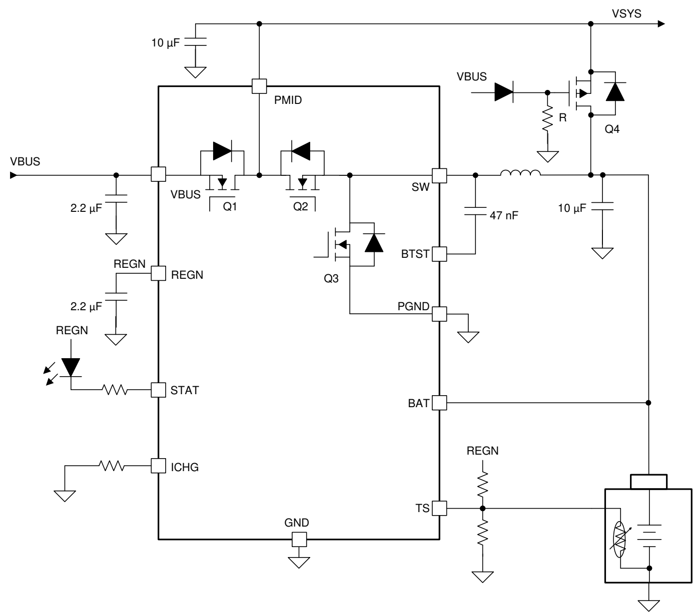


图 9-6. Typical Application Diagram with Power Path

9.2.2.1 Design Requirements

For design requirements, see 节 9.2.1.1.

9.2.3 Typical Application with MCU Programmable Charge Current

In some application cases, the charge current needs to be controlled by a MCU. In those cases, the GPIOs of the MCU can be used for on/off control of the charge current setting resistors R_{ICHG1} and R_{ICHG2} as shown in 图 9-7. With GPIO1 and GPIO2 on/off control, three levels of charge current can be programmed. If the charge current needs to be controlled smoothly in a wide range, a PWM output of the MCU can be used to generate an average DC voltage output to program the charge current as shown in the 图 9-7. The charge current can be calculated as: $(1V - V_{PWM}) / (R_{ICHG1} + R_{ICHG2})$. V_{PWM} is the averaged DC voltage of the PWM output and it must be lower than 1 V. The regulated voltage at the ICHG pin is 1 V.

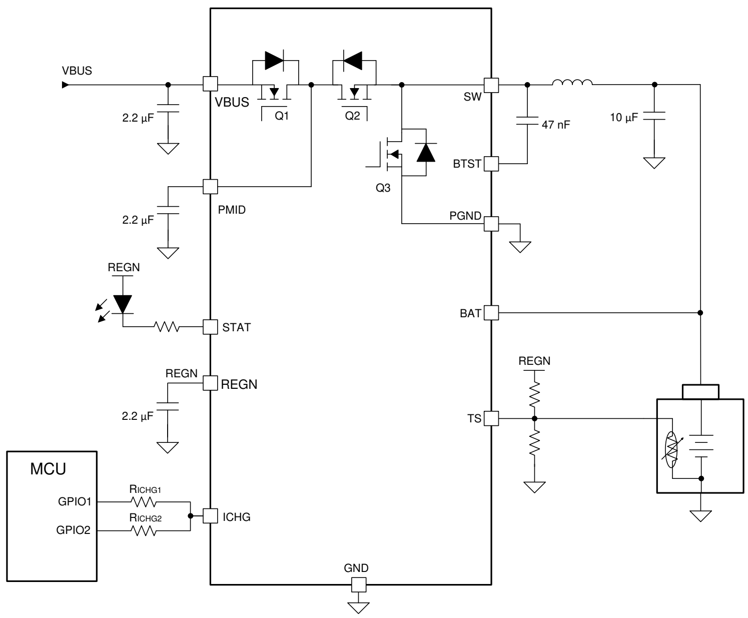


图 9-7. Typical Application with MCU Programmed Charge Current

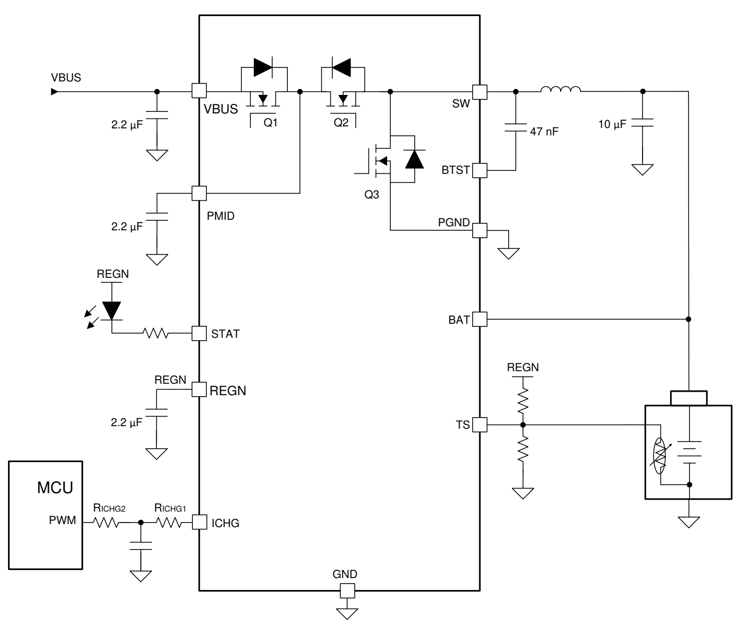


图 9-8. Typical Application with MCU Programmed Charge Current

9.2.3.1 Design Requirements

For design requirements, see 节 9.2.1.1.

10 Power Supply Recommendations

In order to provide an output voltage on the BAT pin, the device requires a power supply between 4.1 V and 6.2 V Li-Ion battery with positive terminal connected to BAT. The source current rating needs to be at least 2 A in order for the buck converter to provide maximum output power to BAT or the system connected to BAT pin.

11 Layout

11.1 Layout Guidelines

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop (see 图 11-1) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Follow this specific order carefully to achieve the proper layout.

- Place input capacitor as close as possible to PMID pin and GND pin and use shortest copper trace connection or GND plane.
- Put output capacitor near to the inductor output terminal and the charger device. Ground connections need to be tied to the IC ground with a short copper trace or GND plane
- Place inductor input terminal to SW pin as close as possible and limit SW node copper area to lower electrical and magnetic field radiation. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
- Route analog ground separately from power ground if possible. Connect analog ground and power ground together using thermal pad as the single ground connection point under the charger device. It is acceptable to connect all grounds to a single ground plane if multiple ground planes are not available.
- Decoupling capacitors should be placed next to the device pins and make trace connection as short as possible.
- It is critical that the exposed thermal pad on the backside of the device be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers
- Ensure that the number and sizes of vias allow enough copper for a given current path
- Try to avoid ground planes in parallel with high frequency traces in other layers.
- See the EVM design for the recommended component placement with trace and via locations.

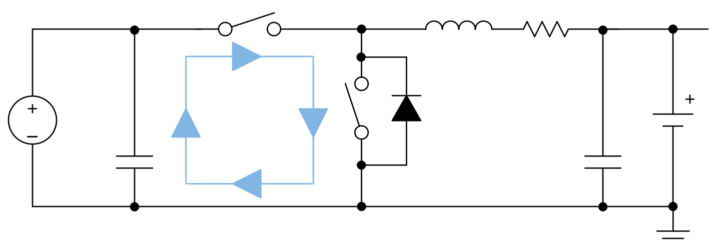


图 11-1. High Frequency Current Path

11.2 Layout Example

The device pinout and component count are optimized for a 2 layer PCB design. The 2-layer PCB layout example is shown in 图 11-2.

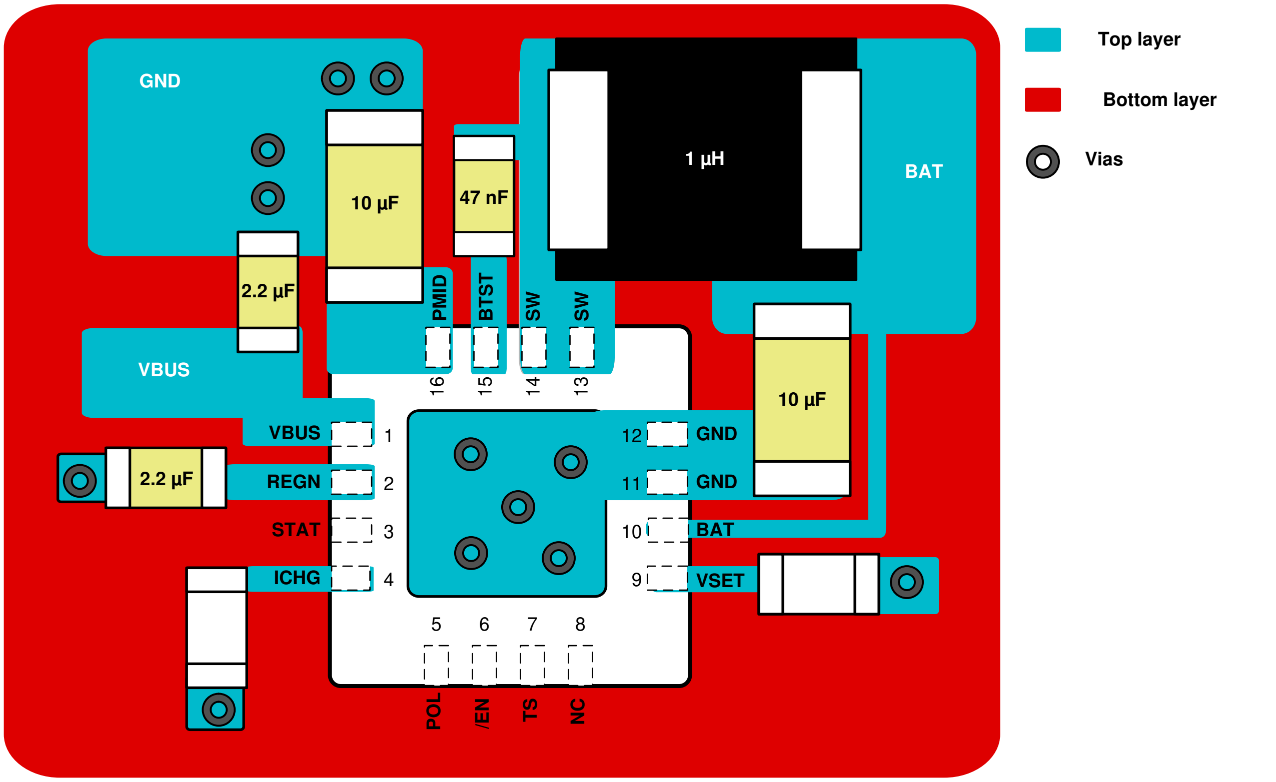


图 11-2. Layout Example

12 器件和文档支持

12.1 器件支持

12.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

12.2 文档支持

12.2.1 相关文档

如需相关文档，请参阅以下内容：*BQ25300、BQ25301、BQ25302、BQ25320 评估模块用户指南*

12.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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12.6 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.7 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ25302RTER	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	B25302

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

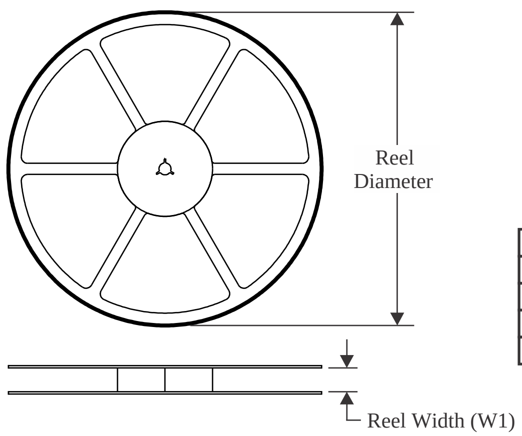
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

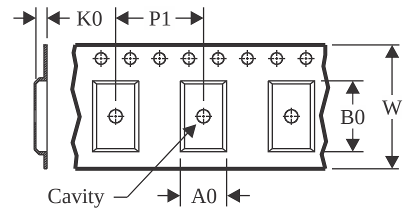
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

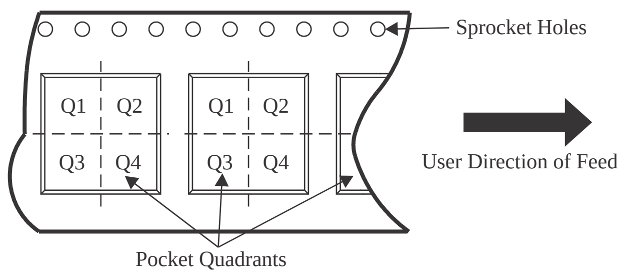


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

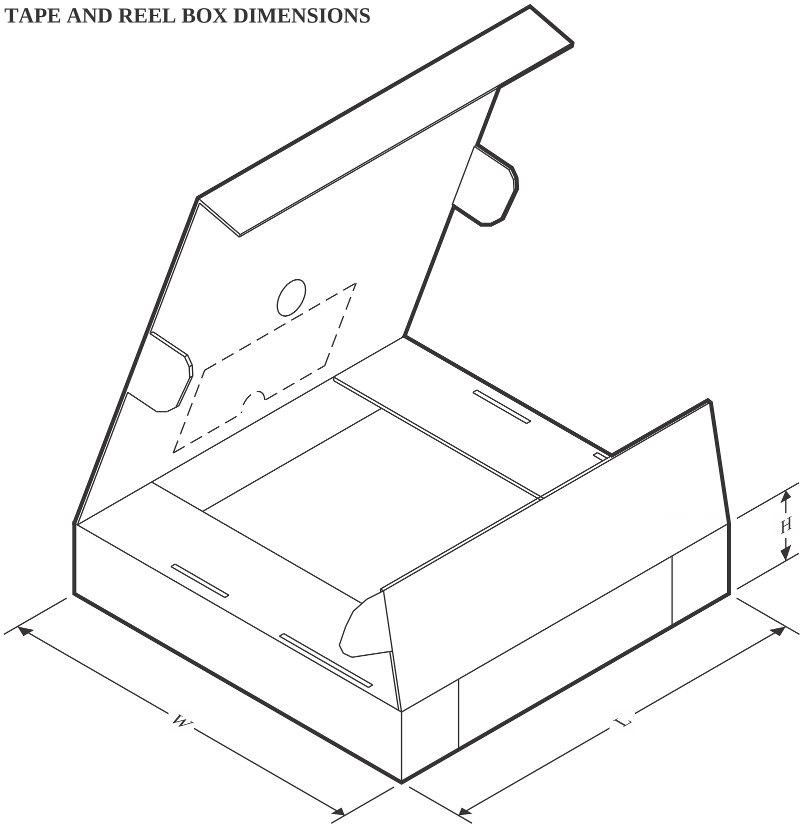
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25302RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ25302RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25302RTER	WQFN	RTE	16	3000	367.0	367.0	35.0
BQ25302RTER	WQFN	RTE	16	3000	367.0	367.0	35.0

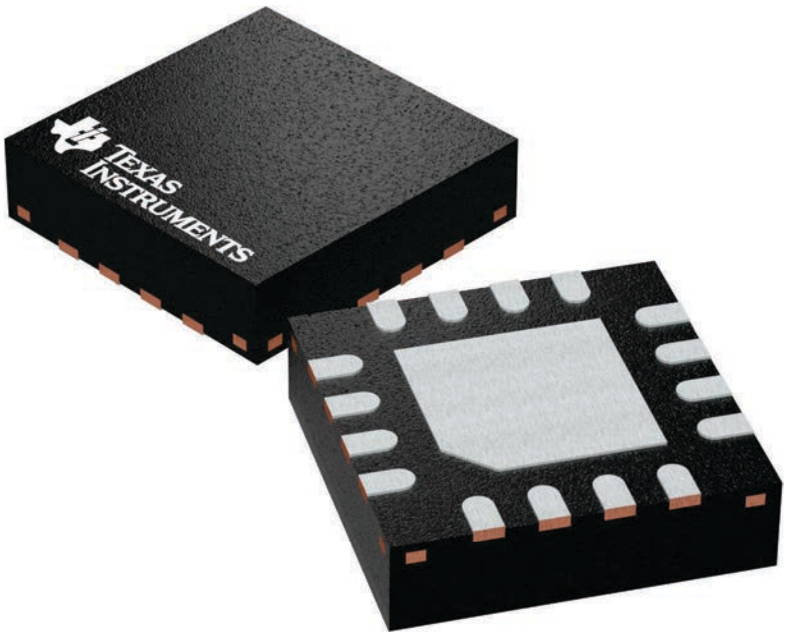
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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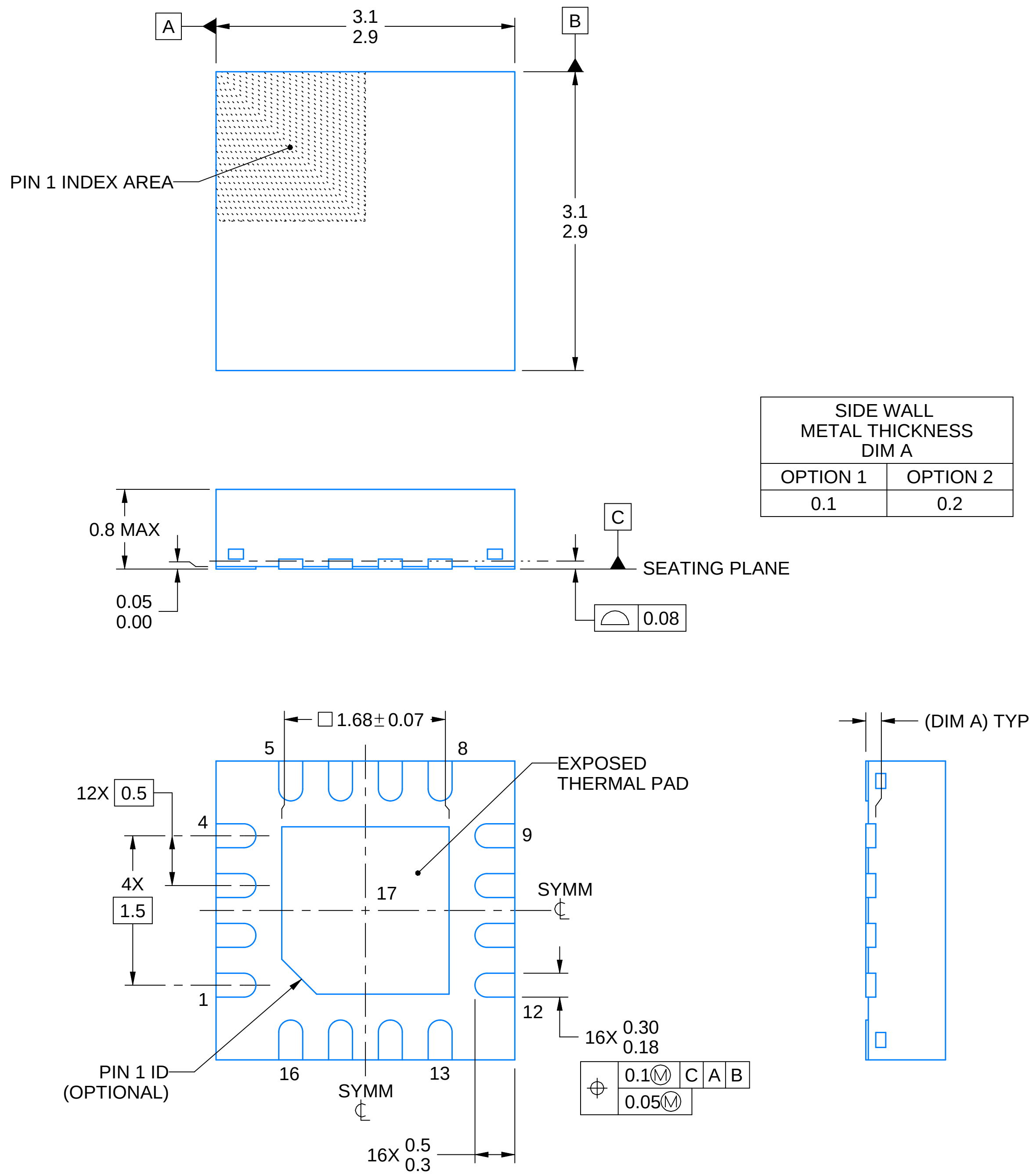

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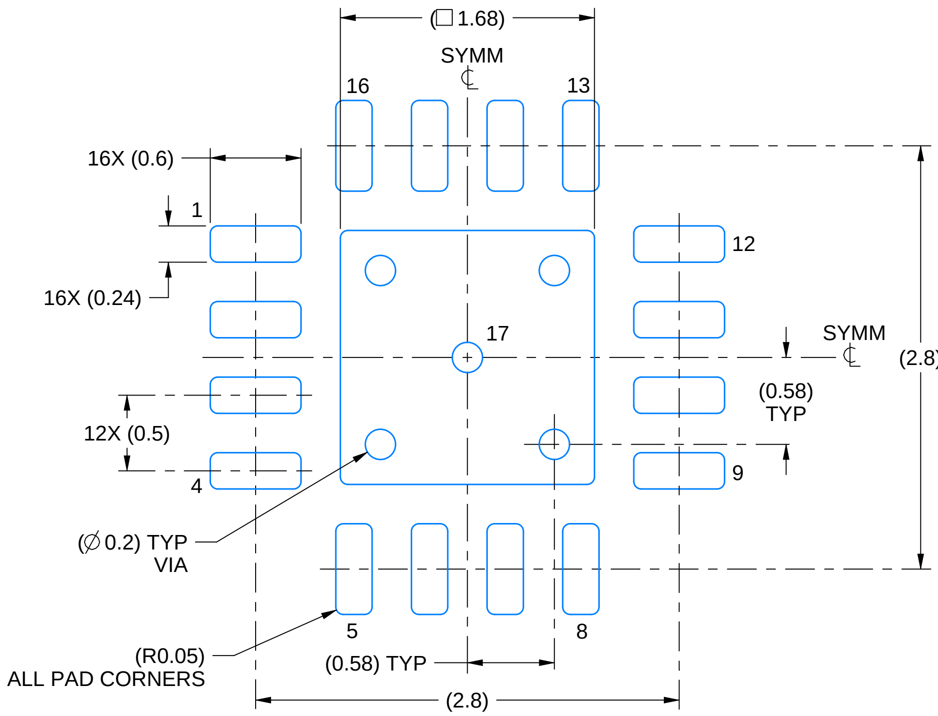
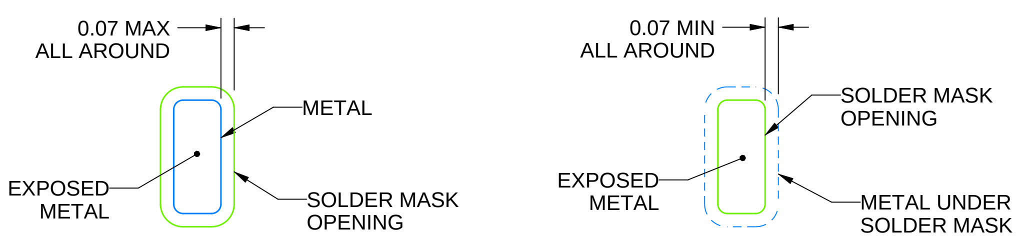
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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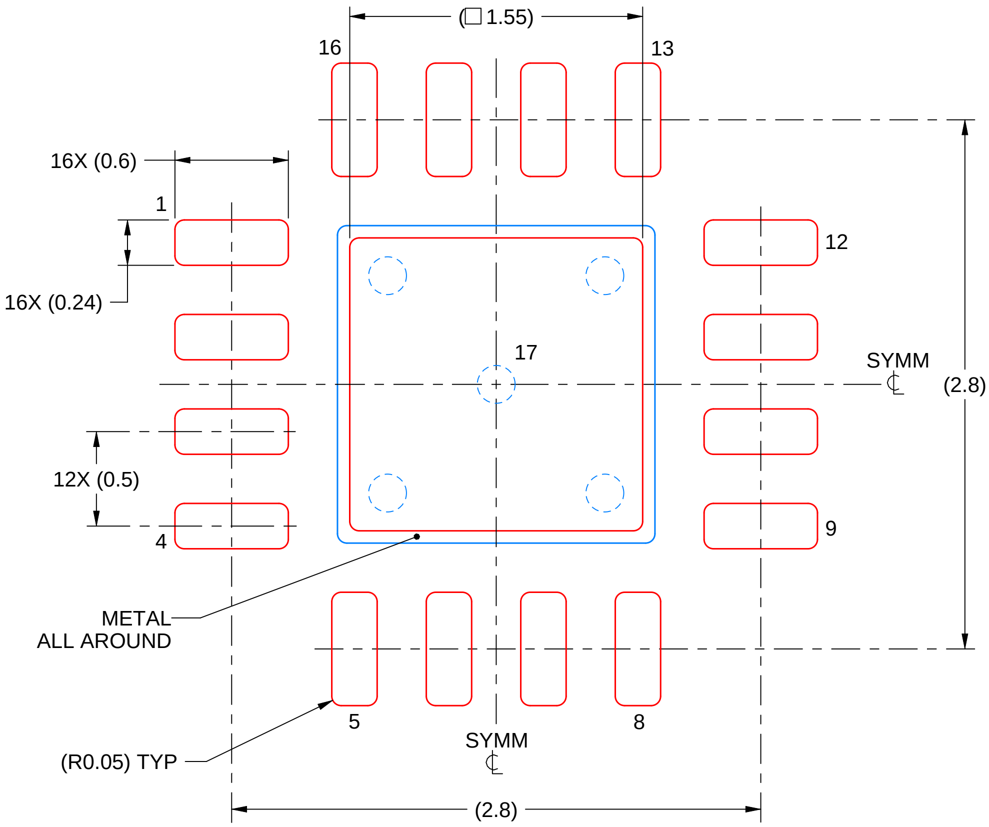
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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