



SN74AUP1G74 Low-Power Single Positive-Edge-Triggered D-Type Flip-Flop With Clear and Preset

1 Features

- Available in the Texas Instruments NanoStar™ Package
- Low Static-Power Consumption:
 $I_{CC} = 0.9 \mu\text{A}$ Maximum
- Low Dynamic-Power Consumption:
 $C_{pd} = 5.5 \text{ pF}$ Typical at 3.3 V
- Low Input Capacitance: $C_i = 1.5 \text{ pF}$ Typical
- Low Noise – Overshoot and Undershoot
< 10% of V_{CC}
- I_{off} Supports Partial-Power-Down Mode Operation
- Schmitt-Trigger Action Allows Slow Input Transition and Better Switching Noise Immunity at the Input
($V_{hys} = 250 \text{ mV}$ Typical at 3.3 V)
- Wide Operating V_{CC} Range of 0.8 V to 3.6 V
- Optimized for 3.3-V Operation
- 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- $t_{pd} = 5 \text{ ns}$ Maximum at 3.3 V
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)

2 Applications

- Servers
- LED Displays
- Network Switches
- Telecom Infrastructure
- Motor Drivers
- I/O Expanders

3 Description

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static- and dynamic-power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in increased battery life. This product also maintains excellent signal integrity (see the very low undershoot and overshoot characteristics shown in [Figure 6](#)).

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AUP1G74YFP	DSBGA (8)	1.56 mm × 0.76 mm
SN74AUP1G74YZP	DSBGA (8)	1.86 mm × 0.89 mm
SN74AUP1G74DCU	VSSOP (8)	2.30 mm × 2.00 mm
SN74AUP1G74DQE	X2SON (8)	1.40 mm × 1.00 mm
SN74AUP1G74RSE	UQFN (8)	1.50 mm × 1.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

AUP – The Lowest-Power Family

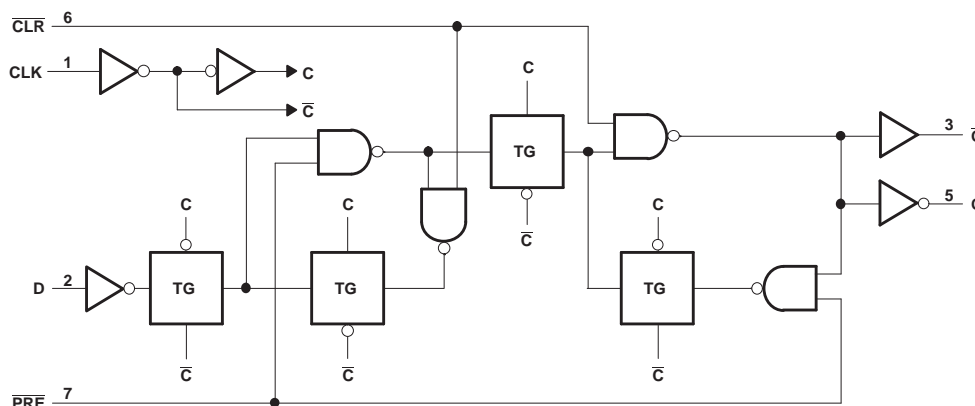


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4 Revision History

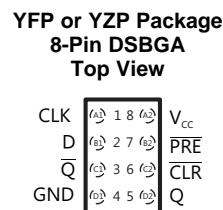
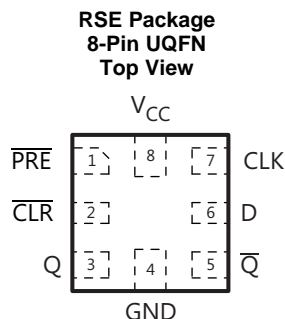
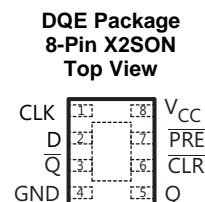
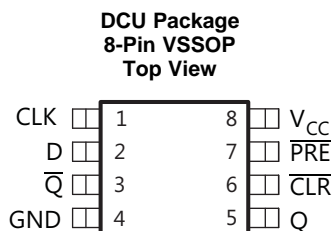
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (March 2010) to Revision D

Page

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section **1**

5 Pin Configuration and Functions



Pin Functions⁽¹⁾

NAME	PIN			I/O	DESCRIPTION
	VSSOP, X2SON	UQFN	DSBGA		
CLK	1	7	A1	I	Rising edge triggered clock signal input
CLR-bar	6	2	C2	I	Clear, Active low
D	2	6	B1	I	Data input
GND	4	4	D1	—	Ground
PRE-bar	7	1	B2	I	Preset, Active low
Q	5	3	D2	O	Output
Q-bar	3	5	C1	O	Inverted output
V _{CC}	8	8	A2	—	Power supply

(1) See [Mechanical, Packaging, and Orderable Information](#) for dimensions.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	–0.5	4.6	V
V _I	Input voltage ⁽²⁾	–0.5	4.6	V
V _O	Voltage applied to any output in the high-impedance or power-off state ⁽²⁾	–0.5	4.6	V
V _O	Output voltage in the high or low state ⁽²⁾	–0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		–50 mA
I _{OK}	Output clamp current	V _O < 0		–50 mA
I _O	Continuous output current		±20	mA
	Continuous current through V _{CC} or GND		±50	mA
T _J	Junction temperature		150	°C
T _{stg}	Storage temperature	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	0.8	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 0.8 V	V _{CC}	V
		V _{CC} = 1.1 V to 1.95 V	0.7 × V _{CC}	
		V _{CC} = 2.3 V to 2.7 V	1.6	
		V _{CC} = 3 V to 3.6 V	2	
V _{IL}	Low-level input voltage	V _{CC} = 0.8 V	0	V
		V _{CC} = 1.1 V to 1.95 V	0.3 × V _{CC}	
		V _{CC} = 2.3 V to 2.7 V	0.7	
		V _{CC} = 3 V to 3.6 V	0.9	
V _I	Input voltage	0	3.6	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 0.8 V	–20	mA
		V _{CC} = 1.1 V	–1.1	
		V _{CC} = 1.4 V	–1.7	
		V _{CC} = 1.65	–1.9	
		V _{CC} = 2.3 V	–3.1	
		V _{CC} = 3 V	–4	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

Recommended Operating Conditions⁽¹⁾ (continued)

		MIN	MAX	UNIT
I_{OL}	Low-level output current	$V_{CC} = 0.8\text{ V}$	20	μA
		$V_{CC} = 1.1\text{ V}$	1.1	mA
		$V_{CC} = 1.4\text{ V}$	1.7	
		$V_{CC} = 1.65\text{ V}$	1.9	
		$V_{CC} = 2.3\text{ V}$	3.1	
		$V_{CC} = 3\text{ V}$	4	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 0.8\text{ V to }3.6\text{ V}$	200	ns/V
T_A	Operating free-air temperature	–40	85	$^{\circ}\text{C}$

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	SN74AUP1G74				UNIT
	DCU (VSSOP)	DQE (X2SON)	RSE (UQFN)	YFP/YZP (DSBGA)	
	8 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance				$^{\circ}\text{C/W}$
	227	261	253	102	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics, $T_A = 25^{\circ}\text{C}$

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	$I_{OH} = -20\text{ }\mu\text{A}$	0.8 V to 3.6 V	$V_{CC} - 0.1$			V
	$I_{OH} = -1.1\text{ mA}$	1.1 V	$0.7 \times V_{CC}$			
	$I_{OH} = -1.7\text{ mA}$	1.4 V	1.11			
	$I_{OH} = -1.9\text{ mA}$	1.65 V	1.32			
	$I_{OH} = -2.3\text{ mA}$	2.3 V	2.05			
	$I_{OH} = -3.1\text{ mA}$		1.9			
	$I_{OH} = -2.7\text{ mA}$	3 V	2.72			
	$I_{OH} = -4\text{ mA}$		2.6			
V_{OL}	$I_{OL} = 20\text{ }\mu\text{A}$	0.8 V to 3.6 V			0.1	V
	$I_{OL} = 1.1\text{ mA}$	1.1 V			$0.3 \times V_{CC}$	
	$I_{OL} = 1.7\text{ mA}$	1.4 V			0.31	
	$I_{OL} = 1.9\text{ mA}$	1.65 V			0.31	
	$I_{OL} = 2.3\text{ mA}$	2.3 V			0.31	
	$I_{OL} = 3.1\text{ mA}$				0.44	
	$I_{OL} = 2.7\text{ mA}$	3 V			0.31	
	$I_{OL} = 4\text{ mA}$				0.44	
I_I	A or B input	$V_I = \text{GND to }3.6\text{ V}$	0 V to 3.6 V		0.1	μA
I_{off}	V_I or $V_O = 0\text{ V to }3.6\text{ V}$	0 V			0.2	μA
ΔI_{off}	V_I or $V_O = 0\text{ V to }3.6\text{ V}$	0 V to 0.2 V			0.2	μA
I_{CC}	$V_I = \text{GND or } (V_{CC} \text{ to } 3.6\text{ V}),$ $I_O = 0$	0.8 V to 3.6 V			0.5	μA
ΔI_{CC}	$V_I = V_{CC} - 0.6\text{ V}^{(1)}, I_O = 0$	3.3 V			40	μA
C_i	$V_I = V_{CC} \text{ or GND}$	0 V		1.5		pF
		3.6 V		1.5		
C_o	$V_O = \text{GND}$	0 V		3		pF

(1) One input at $V_{CC} - 0.6\text{ V}$, other input at V_{CC} or GND

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6.6 Electrical Characteristics, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}		$I_{OH} = -20\ \mu\text{A}$	0.8 V to 3.6 V	$V_{CC} - 0.1$			V
		$I_{OH} = -1.1\ \text{mA}$	1.1 V	$0.7 \times V_{CC}$			
		$I_{OH} = -1.7\ \text{mA}$	1.4 V	1.03			
		$I_{OH} = -1.9\ \text{mA}$	1.65 V	1.3			
		$I_{OH} = -2.3\ \text{mA}$	2.3 V	1.97			
		$I_{OH} = -3.1\ \text{mA}$		1.85			
		$I_{OH} = -2.7\ \text{mA}$	3 V	2.67			
		$I_{OH} = -4\ \text{mA}$		2.55			
V_{OL}		$I_{OL} = 20\ \mu\text{A}$	0.8 V to 3.6 V			0.1	V
		$I_{OL} = 1.1\ \text{mA}$	1.1 V			$0.3 \times V_{CC}$	
		$I_{OL} = 1.7\ \text{mA}$	1.4 V			0.37	
		$I_{OL} = 1.9\ \text{mA}$	1.65 V			0.35	
		$I_{OL} = 2.3\ \text{mA}$	2.3 V			0.33	
		$I_{OL} = 3.1\ \text{mA}$				0.45	
		$I_{OL} = 2.7\ \text{mA}$	3 V			0.33	
		$I_{OL} = 4\ \text{mA}$				0.45	
I_I	A or B input	$V_I = \text{GND to } 3.6\ \text{V}$	0 V to 3.6 V			0.5	μA
I_{off}		$V_I \text{ or } V_O = 0\ \text{V to } 3.6\ \text{V}$	0 V			0.6	μA
ΔI_{off}		$V_I \text{ or } V_O = 0\ \text{V to } 3.6\ \text{V}$	0 V to 0.2 V			0.6	μA
I_{CC}		$V_I = \text{GND or } (V_{CC} \text{ to } 3.6\ \text{V}),$ $I_O = 0$	0.8 V to 3.6 V			0.9	μA
ΔI_{CC}		$V_I = V_{CC} - 0.6\ \text{V}^{(1)}, I_O = 0$	3.3 V			50	μA
C_i		$V_I = V_{CC} \text{ or GND}$	0 V				pF
			3.6 V				
C_O		$V_O = \text{GND}$	0 V				pF

 (1) One input at $V_{CC} - 0.6\ \text{V}$, other input at V_{CC} or GND

6.7 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

		V _{CC}	MIN ⁽¹⁾	TYP ⁽²⁾	MAX ⁽¹⁾	UNIT
f _{clock}	Clock frequency	0.8 V	21			MHz
		1.2 V ± 0.1 V	40			
		1.5 V ± 0.1 V	50			
		1.8 V ± 0.15 V	60			
		2.5 V ± 0.2 V	90			
		3.3 V ± 0.3 V	90			
t _w	CLK high or low	0.8 V	3.5			ns
		1.2 V ± 0.1 V	2			
		1.5 V ± 0.1 V	2			
		1.8 V ± 0.15 V	2			
		2.5 V ± 0.2 V	2			
		3.3 V ± 0.3 V	2			
	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	0.8 V	4.5			
		1.2 V ± 0.1 V	2			
		1.5 V ± 0.1 V	2			
		1.8 V ± 0.15 V	2			
		2.5 V ± 0.2 V	2			
		3.3 V ± 0.3 V	2			
t _{su}	Data high	0.8 V	3			ns
		1.2 V ± 0.1 V	1.3			
		1.5 V ± 0.1 V	1			
		1.8 V ± 0.15 V	1			
		2.5 V ± 0.2 V	0.5			
		3.3 V ± 0.3 V	0.5			
	Data low	0.8 V	1			
		1.2 V ± 0.1 V	1.2			
		1.5 V ± 0.1 V	1			
		1.8 V ± 0.15 V	1			
		2.5 V ± 0.2 V	1			
		3.3 V ± 0.3 V	1			
	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	0.8 V	1			
		1.2 V ± 0.1 V	0.5			
		1.5 V ± 0.1 V	0.5			
		1.8 V ± 0.15 V	0.5			
		2.5 V ± 0.2 V	0.5			
		3.3 V ± 0.3 V	0.5			
t _h	Hold time, data after CLK↑	0.8 V	0			ns
		1.2 V ± 0.1 V	0			
		1.5 V ± 0.1 V	0			
		1.8 V ± 0.15 V	0			
		2.5 V ± 0.2 V	0			
		3.3 V ± 0.3 V	0			

(1) Minimum and maximum values are for T_A = –40°C to +85°C

(2) Typicals are for T_A = 25°C

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6.8 Switching Characteristics, $C_L = 5\text{ pF}$

over recommended operating free-air temperature range, $C_L = 5\text{ pF}$ (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A	MIN	TYP	MAX	UNIT
f _{max}			0.8 V	T _A = 25°C	60			MHz
			1.2 V ± 0.1 V	T _A = 25°C	80			
				T _A = −40°C to 85°C	60			
			1.5 V ± 0.1 V	T _A = 25°C	125			
				T _A = −40°C to 85°C	90			
			1.8 V ± 0.15 V	T _A = 25°C	150			
				T _A = −40°C to 85°C	120			
			2.5 V ± 0.2 V	T _A = 25°C	180			
T _A = −40°C to 85°C	160							
3.3 V ± 0.3 V	T _A = 25°C	190						
	T _A = −40°C to 85°C	180						
t _{pd}	CLK	Q	0.8 V	T _A = 25°C	31			ns
			1.2 V ± 0.1 V	T _A = 25°C	2	10	20	
				T _A = −40°C to 85°C	2.7	20.4		
			1.5 V ± 0.1 V	T _A = 25°C	2	6	12	
				T _A = −40°C to 85°C	1.9	12.4		
			1.8 V ± 0.15 V	T _A = 25°C	2	5	9	
				T _A = −40°C to 85°C	1.4	9.5		
		2.5 V ± 0.2 V	T _A = 25°C	2	3	6		
			T _A = −40°C to 85°C	1.1	6.2			
		3.3 V ± 0.3 V	T _A = 25°C	2	3	4		
			T _A = −40°C to 85°C	1	4.7			
		Q̄	0.8 V	T _A = 25°C	28			
			1.2 V ± 0.1 V	T _A = 25°C	2	9	19	
				T _A = −40°C to 85°C	2.4	19		
			1.5 V ± 0.1 V	T _A = 25°C	2	6	11	
	T _A = −40°C to 85°C			1.6	11.8			
	1.8 V ± 0.15 V		T _A = 25°C	2	5	9		
			T _A = −40°C to 85°C	1.3	9			
	2.5 V ± 0.2 V		T _A = 25°C	2	3	6		
		T _A = −40°C to 85°C	1.1	6				
	3.3 V ± 0.3 V	T _A = 25°C	2	3	4			
		T _A = −40°C to 85°C	1	4.6				
	PRE or CLR	Q or Q̄	0.8 V	T _A = 25°C	26			
			1.2 V ± 0.1 V	T _A = 25°C	2	9	20	
				T _A = −40°C to 85°C	2	20		
			1.5 V ± 0.1 V	T _A = 25°C	2	6	12	
				T _A = −40°C to 85°C	1.5	13		
			1.8 V ± 0.15 V	T _A = 25°C	2	5	9	
				T _A = −40°C to 85°C	1.3	10		
			2.5 V ± 0.2 V	T _A = 25°C	2	3	6	
				T _A = −40°C to 85°C	1	7		
			3.3 V ± 0.3 V	T _A = 25°C	2	3	5	
				T _A = −40°C to 85°C	1	5		

6.9 Switching Characteristics, $C_L = 10$ pF

over recommended operating free-air temperature range, $C_L = 10$ pF (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A	MIN	TYP	MAX	UNIT
f_{max}			0.8 V	$T_A = 25^\circ\text{C}$		46		MHz
			$1.2\text{ V} \pm 0.1\text{ V}$	$T_A = 25^\circ\text{C}$		65		
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	50			
			$1.5\text{ V} \pm 0.1\text{ V}$	$T_A = 25^\circ\text{C}$		95		
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	55			
			$1.8\text{ V} \pm 0.15\text{ V}$	$T_A = 25^\circ\text{C}$		110		
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	60			
			$2.5\text{ V} \pm 0.2\text{ V}$	$T_A = 25^\circ\text{C}$		170		
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	130			
			$3.3\text{ V} \pm 0.3\text{ V}$	$T_A = 25^\circ\text{C}$		180		
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	160			
t_{pd}	CLK	Q	0.8 V	$T_A = 25^\circ\text{C}$		33		ns
			$1.2\text{ V} \pm 0.1\text{ V}$	$T_A = 25^\circ\text{C}$	2	10	22	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	3.4		21.8	
			$1.5\text{ V} \pm 0.1\text{ V}$	$T_A = 25^\circ\text{C}$	2	7	13	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	2.4		13.5	
			$1.8\text{ V} \pm 0.15\text{ V}$	$T_A = 25^\circ\text{C}$	2	6	10	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	1.9		10.4	
			$2.5\text{ V} \pm 0.2\text{ V}$	$T_A = 25^\circ\text{C}$	2	4	6	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	1.5		7	
			$3.3\text{ V} \pm 0.3\text{ V}$	$T_A = 25^\circ\text{C}$	2	3	5	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	1.2		5.3	
		\overline{Q}	0.8 V	$T_A = 25^\circ\text{C}$		30		
			$1.2\text{ V} \pm 0.1\text{ V}$	$T_A = 25^\circ\text{C}$	2	10	20	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	3		20.3	
			$1.5\text{ V} \pm 0.1\text{ V}$	$T_A = 25^\circ\text{C}$	2	7	12	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	2.2		12.8	
			$1.8\text{ V} \pm 0.15\text{ V}$	$T_A = 25^\circ\text{C}$	2	5	9	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	1.8		9.9	
			$2.5\text{ V} \pm 0.2\text{ V}$	$T_A = 25^\circ\text{C}$	2	4	6	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	1.3		6.7	
			$3.3\text{ V} \pm 0.3\text{ V}$	$T_A = 25^\circ\text{C}$	2	3	5	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	1.1		5.2	
		Q or \overline{Q}	0.8 V	$T_A = 25^\circ\text{C}$		29		
			$1.2\text{ V} \pm 0.1\text{ V}$	$T_A = 25^\circ\text{C}$	2	10	21	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	2		21.4	
			$1.5\text{ V} \pm 0.1\text{ V}$	$T_A = 25^\circ\text{C}$	2	7	13	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	2		13.8	
			$1.8\text{ V} \pm 0.15\text{ V}$	$T_A = 25^\circ\text{C}$	2	5	10	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	2		10.8	
			$2.5\text{ V} \pm 0.2\text{ V}$	$T_A = 25^\circ\text{C}$	2	4	7	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	1.5		7.4	
			$3.3\text{ V} \pm 0.3\text{ V}$	$T_A = 25^\circ\text{C}$	2	3	5	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	1.5		5.8	

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6.10 Switching Characteristics, $C_L = 15$ pF

over recommended operating free-air temperature range, $C_L = 15$ pF (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A	MIN	TYP	MAX	UNIT
f_{max}			0.8 V	$T_A = 25^\circ\text{C}$		41		MHz
			$1.2\text{ V} \pm 0.1\text{ V}$	$T_A = 25^\circ\text{C}$		75		
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	50			
			$1.5\text{ V} \pm 0.1\text{ V}$	$T_A = 25^\circ\text{C}$		95		
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	55			
			$1.8\text{ V} \pm 0.15\text{ V}$	$T_A = 25^\circ\text{C}$		100		
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	60			
			$2.5\text{ V} \pm 0.2\text{ V}$	$T_A = 25^\circ\text{C}$		150		
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	130			
			$3.3\text{ V} \pm 0.3\text{ V}$	$T_A = 25^\circ\text{C}$		200		
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	160			
t_{pd}	CLK	Q	0.8 V	$T_A = 25^\circ\text{C}$		35		ns
			$1.2\text{ V} \pm 0.1\text{ V}$	$T_A = 25^\circ\text{C}$	2	12	23.1	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	4.1		23.2	
			$1.5\text{ V} \pm 0.1\text{ V}$	$T_A = 25^\circ\text{C}$	2	8	14.1	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	2.9		14.6	
			$1.8\text{ V} \pm 0.15\text{ V}$	$T_A = 25^\circ\text{C}$	2	6	10.7	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	2.4		11.3	
			$2.5\text{ V} \pm 0.2\text{ V}$	$T_A = 25^\circ\text{C}$	2	4	7	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	1.9		7.6	
			$3.3\text{ V} \pm 0.3\text{ V}$	$T_A = 25^\circ\text{C}$	2	4	5.4	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	1.6		5.9	
		\overline{Q}	0.8 V	$T_A = 25^\circ\text{C}$		32		
			$1.2\text{ V} \pm 0.1\text{ V}$	$T_A = 25^\circ\text{C}$	2	11	21.8	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	3.7		21.8	
			$1.5\text{ V} \pm 0.1\text{ V}$	$T_A = 25^\circ\text{C}$	2	7	13.5	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	2.6		14	
			$1.8\text{ V} \pm 0.15\text{ V}$	$T_A = 25^\circ\text{C}$	2	6	10.4	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	2.2		10.9	
			$2.5\text{ V} \pm 0.2\text{ V}$	$T_A = 25^\circ\text{C}$	2	4	7.1	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	1.7		7.5	
			$3.3\text{ V} \pm 0.3\text{ V}$	$T_A = 25^\circ\text{C}$	2	3	5.4	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	1.4		5.8	
	\overline{PRE} or \overline{CLR}	Q or \overline{Q}	0.8 V	$T_A = 25^\circ\text{C}$		31		
			$1.2\text{ V} \pm 0.1\text{ V}$	$T_A = 25^\circ\text{C}$	2	11	23	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	2		22.9	
			$1.5\text{ V} \pm 0.1\text{ V}$	$T_A = 25^\circ\text{C}$	2	7	14	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	2		14.9	
			$1.8\text{ V} \pm 0.15\text{ V}$	$T_A = 25^\circ\text{C}$	2	6	11	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	2		11.7	
			$2.5\text{ V} \pm 0.2\text{ V}$	$T_A = 25^\circ\text{C}$	2	4	7	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	2		8.1	
			$3.3\text{ V} \pm 0.3\text{ V}$	$T_A = 25^\circ\text{C}$	2	4	6	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	1.5		6.4	

6.11 Switching Characteristics, $C_L = 30$ pF

over recommended operating free-air temperature range, $C_L = 30$ pF (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A	MIN	TYP	MAX	UNIT
f_{max}			0.8 V	$T_A = 25^\circ\text{C}$		21		MHz
			$1.2\text{ V} \pm 0.1\text{ V}$	$T_A = 25^\circ\text{C}$		50		
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	40			
			$1.5\text{ V} \pm 0.1\text{ V}$	$T_A = 25^\circ\text{C}$		60		
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	50			
			$1.8\text{ V} \pm 0.15\text{ V}$	$T_A = 25^\circ\text{C}$		75		
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	70			
			$2.5\text{ V} \pm 0.2\text{ V}$	$T_A = 25^\circ\text{C}$		100		
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	90			
t_{pd}	CLK	Q	0.8 V	$T_A = 25^\circ\text{C}$		32		ns
			$1.2\text{ V} \pm 0.1\text{ V}$	$T_A = 25^\circ\text{C}$	3	14	27	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	5.9		27	
			$1.5\text{ V} \pm 0.1\text{ V}$	$T_A = 25^\circ\text{C}$	3	10	17	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	4.4		17.2	
			$1.8\text{ V} \pm 0.15\text{ V}$	$T_A = 25^\circ\text{C}$	3	8	13	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	3.6		13.4	
			$2.5\text{ V} \pm 0.2\text{ V}$	$T_A = 25^\circ\text{C}$	3	6	9	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	3		9.2	
		\bar{Q}	$3.3\text{ V} \pm 0.3\text{ V}$	$T_A = 25^\circ\text{C}$	3	5	7	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	2.6		7.2	
			0.8 V	$T_A = 25^\circ\text{C}$		40		
			$1.2\text{ V} \pm 0.1\text{ V}$	$T_A = 25^\circ\text{C}$	3	13	26	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	5.5		25.9	
			$1.5\text{ V} \pm 0.1\text{ V}$	$T_A = 25^\circ\text{C}$	3	9	16	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	4.1		16.8	
			$1.8\text{ V} \pm 0.15\text{ V}$	$T_A = 25^\circ\text{C}$	3	7	13	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	3.5		13.2	
			$2.5\text{ V} \pm 0.2\text{ V}$	$T_A = 25^\circ\text{C}$	3	5	9	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	2.7		9.2	
		Q or \bar{Q}	$3.3\text{ V} \pm 0.3\text{ V}$	$T_A = 25^\circ\text{C}$	3	5	7	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	2.4		7.2	
			0.8 V	$T_A = 25^\circ\text{C}$		38		
			$1.2\text{ V} \pm 0.1\text{ V}$	$T_A = 25^\circ\text{C}$	3	13	26	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	3		27	
			$1.5\text{ V} \pm 0.1\text{ V}$	$T_A = 25^\circ\text{C}$	3	9	17	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	3		17.4	
			$1.8\text{ V} \pm 0.15\text{ V}$	$T_A = 25^\circ\text{C}$	3	8	13	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	3		14	
	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or \bar{Q}	$2.5\text{ V} \pm 0.2\text{ V}$	$T_A = 25^\circ\text{C}$	3	6	9	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	3		10	
			$3.3\text{ V} \pm 0.3\text{ V}$	$T_A = 25^\circ\text{C}$	3	5	7	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	2.5		8	

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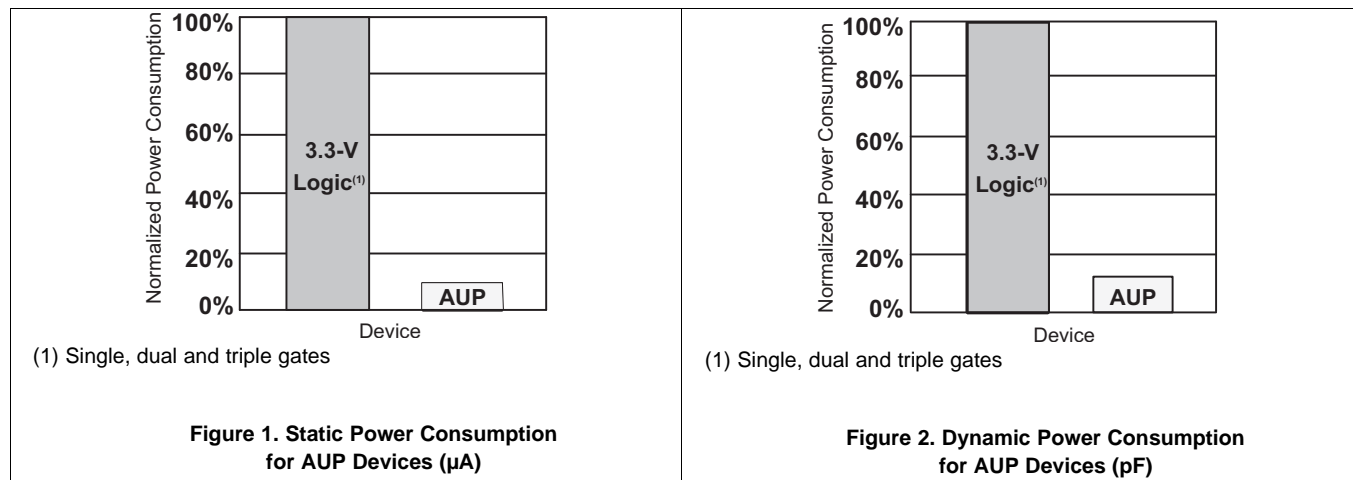
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6.12 Operating Characteristics

$T_A = 25^\circ\text{C}$

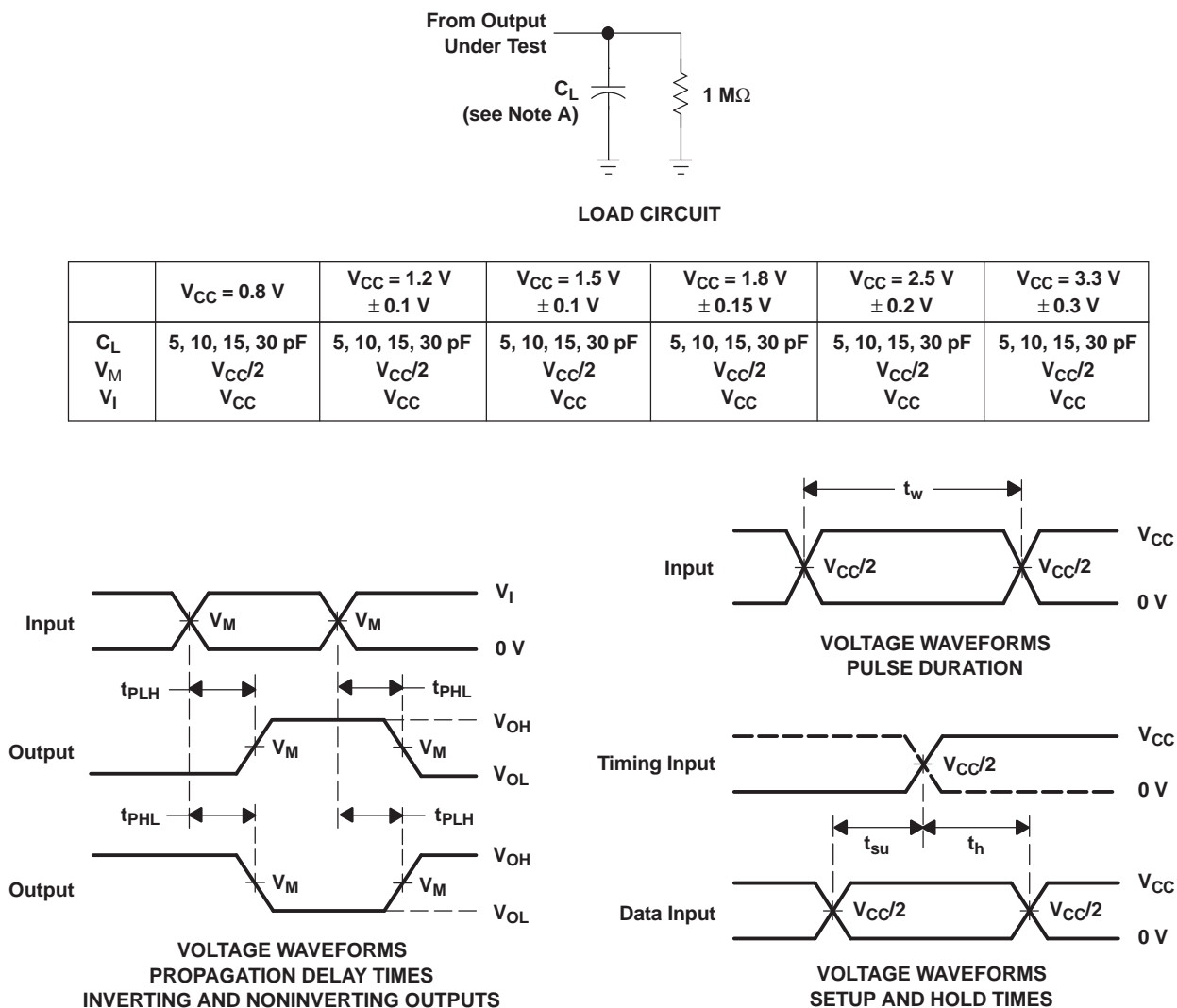
PARAMETER	TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd} Power dissipation capacitance	$f = 10\text{ MHz}$	0.8 V	5.5	pF
		1.2 V \pm 0.1 V	5.5	
		1.5 V \pm 0.1 V	5.5	
		1.8 V \pm 0.15 V	5.5	
		2.5 V \pm 0.2 V	5.5	
		3.3 V \pm 0.3 V	5.5	

6.13 Typical Characteristics



7 Parameter Measurement Information

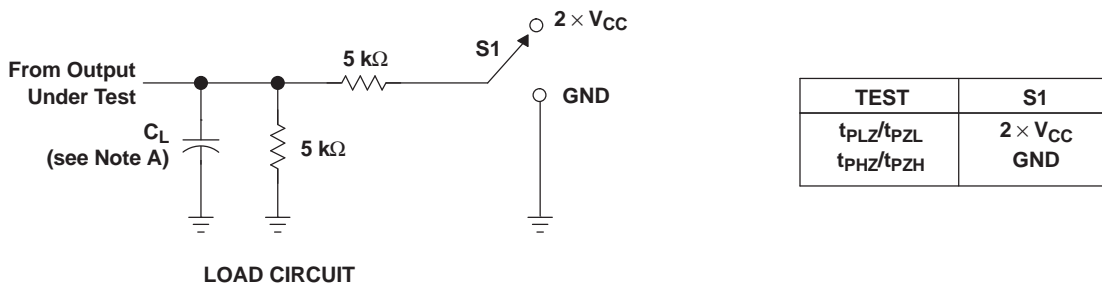
7.1 Propagation Delays, Setup and Hold Times, and Pulse Width



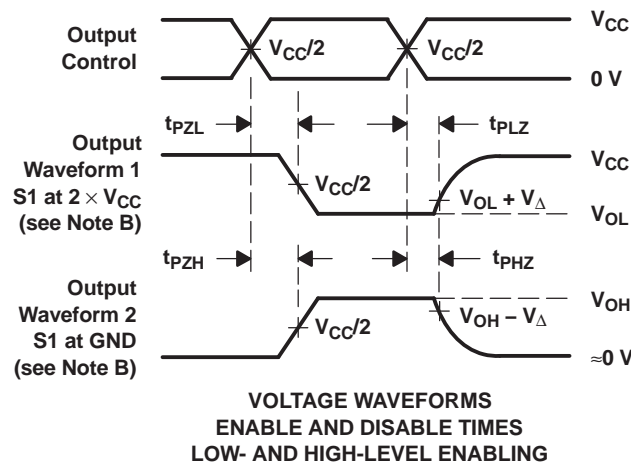
- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r/t_f = 3 \text{ ns}$.
 C. The outputs are measured one at a time, with one transition per measurement.
 D. t_{PLH} and t_{PHL} are the same as t_{pd} .
 E. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

7.2 Enable and Disable Times



	$V_{CC} = 0.8\text{ V}$	$V_{CC} = 1.2\text{ V}$ $\pm 0.1\text{ V}$	$V_{CC} = 1.5\text{ V}$ $\pm 0.1\text{ V}$	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_{Δ}	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r/t_f = 3\text{ ns}$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

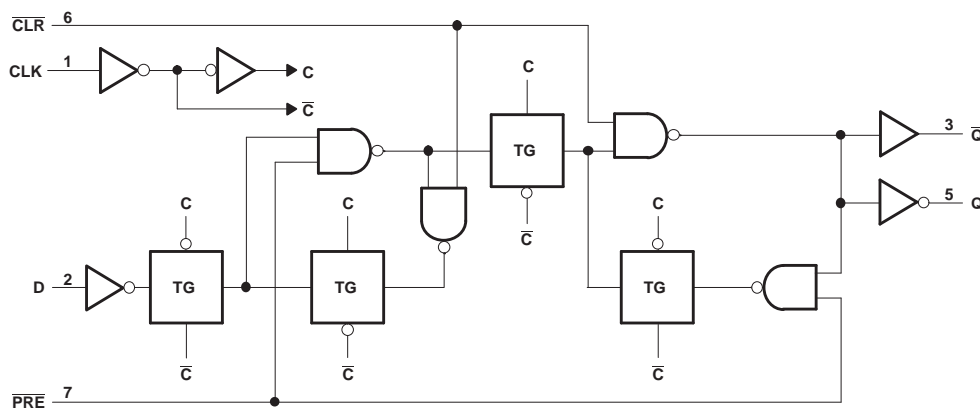
This single positive-edge-triggered D-type flip-flop is designed for 0.8-V to 3.6-V V_{CC} operation.

A low level at the preset (\overline{PRE}) or clear (\overline{CLR}) input sets or resets the outputs, regardless of the levels of the other inputs. When \overline{PRE} and \overline{CLR} are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs. When both the \overline{CLR} and \overline{PRE} inputs are set low, the \overline{CLR} input will override the \overline{PRE} input.

NanoStar package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

8.2 Functional Block Diagram



Pin numbers shown are for the DCU and DQE packages

8.3 Feature Description

This device is available in the Texas Instrument's NanoStar package. It has low static-power consumption of 0.9 μ A maximum. It has low noise with overshoot and undershoot at less than ten percent of V_{CC} . It supports partial-power-down mode operation, which is specified by I_{off} . The Schmitt-trigger inputs allow for slow or noisy input signals. The device has a wide operating voltage range of 0.8 V to 3.6 V, and is optimized for 3.3 V. It has low propagation delay of 5 ns maximum at 3.3 V.

8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74AUP1G74.

Table 1. Function Table

INPUTS				OUTPUTS	
\overline{PRE}	\overline{CLR}	CLK	D	Q	\overline{Q}
L	H	X	X	H	L
X	L	X	X	L	H
H	H	\uparrow	H	H	L
H	H	\uparrow	L	L	H
H	H	L	X	Q_0	\overline{Q}_0

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74AUP1G74 can be used to control a power button input. Tying \overline{Q} to D will switch the output between high and low each time that a high signal is sent to CLK from the push button.

A low level at the preset (\overline{PRE}) or clear (\overline{CLR}) input sets or resets the outputs, regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

The resistor and capacitor at the \overline{CLR} pin are optional. If they are not used, the \overline{CLR} pin must be connected directly to V_{CC} to be inactive.

9.2 Typical Power Button Circuit

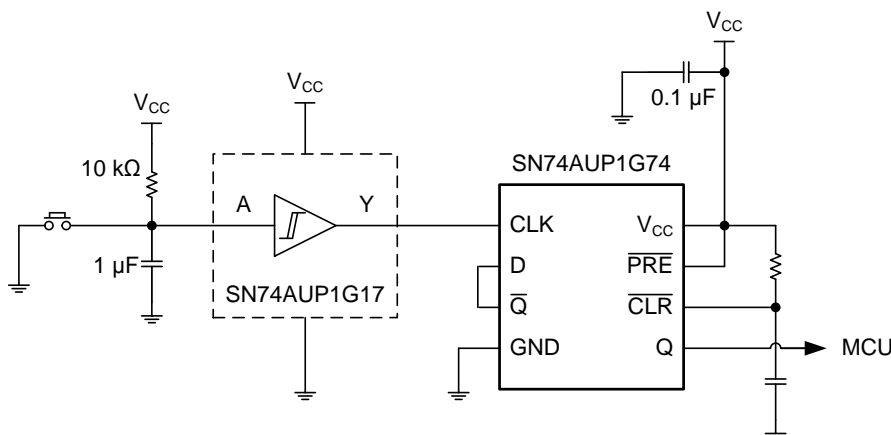


Figure 5. Device Power Button Circuit

9.2.1 Design Requirements

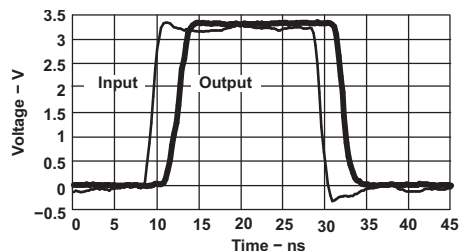
This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. Outputs can be combined to produce higher drive but the high drive will also create faster edges into light loads so routing and load conditions must be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
 - For rise time and fall time specifications, see $(\Delta t/\Delta V)$ in [Recommended Operating Conditions](#).
 - For specified high and low levels, see $(V_{IH}$ and $V_{IL})$ in [Recommended Operating Conditions](#).
 - Inputs are overvoltage tolerant allowing them to go as high as 4.6 V at any valid V_{CC} .
2. Recommend Output Conditions:
 - Series resistors on the output may be used if the user desires to slow the output edge signal or limit the output current.

Typical Power Button Circuit (continued)

9.2.3 Application Curve



AUP1G08 data at $C_L = 15$ pF

Figure 6. Switching Characteristics at 25 MHz

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in [Recommended Operating Conditions](#).

Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1- μ F capacitor, and if there are multiple V_{CC} pins, then TI recommends a 0.01- μ F or 0.022- μ F capacitor for each power pin. It is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs must not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient.

11.2 Layout Example

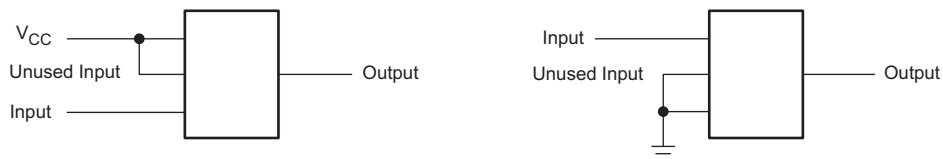


Figure 7. Layout Diagram

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

Implications of Slow or Floating CMOS Inputs, [SCBA004](#)

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

NanoStar, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AUP1G74DCUR	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H74R
SN74AUP1G74DQER	Active	Production	X2SON (DQE) 8	5000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	HS
SN74AUP1G74RSER	Active	Production	UQFN (RSE) 8	5000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	HS
SN74AUP1G74YFPR	Active	Production	DSBGA (YFP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HSN
SN74AUP1G74YZPR	Active	Production	DSBGA (YZP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HSN

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

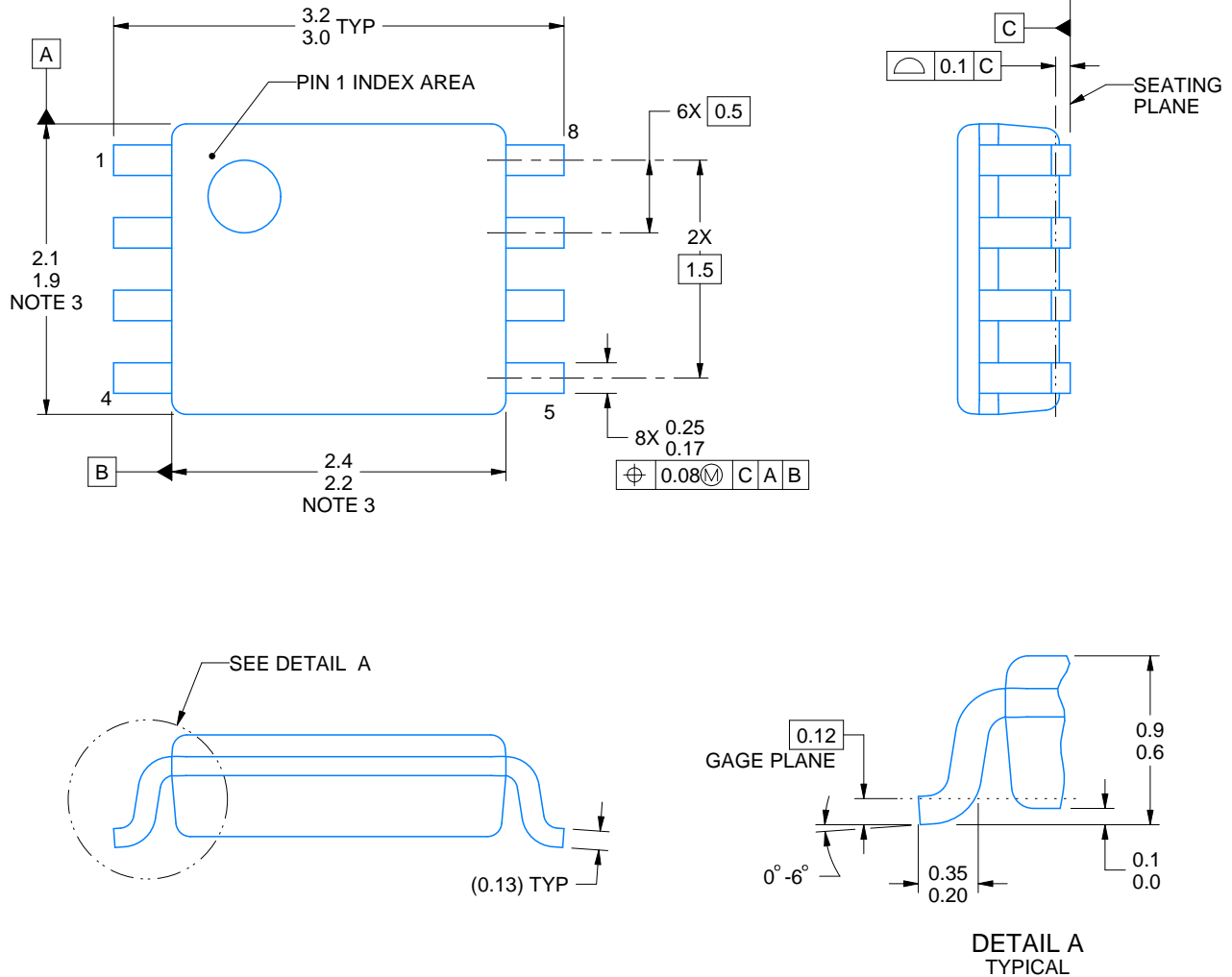
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1G74DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUP1G74DQER	X2SON	DQE	8	5000	180.0	8.4	1.2	1.6	0.55	4.0	8.0	Q1
SN74AUP1G74RSER	UQFN	RSE	8	5000	180.0	8.4	1.7	1.7	0.7	4.0	8.0	Q2
SN74AUP1G74YFPR	DSBGA	YFP	8	3000	178.0	9.2	0.9	1.75	0.6	4.0	8.0	Q1
SN74AUP1G74YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1G74DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AUP1G74DQER	X2SON	DQE	8	5000	202.0	201.0	28.0
SN74AUP1G74RSER	UQFN	RSE	8	5000	202.0	201.0	28.0
SN74AUP1G74YFPR	DSBGA	YFP	8	3000	220.0	220.0	35.0
SN74AUP1G74YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0



4225266/A 09/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.

EXAMPLE BOARD LAYOUT

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



4225266/A 09/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

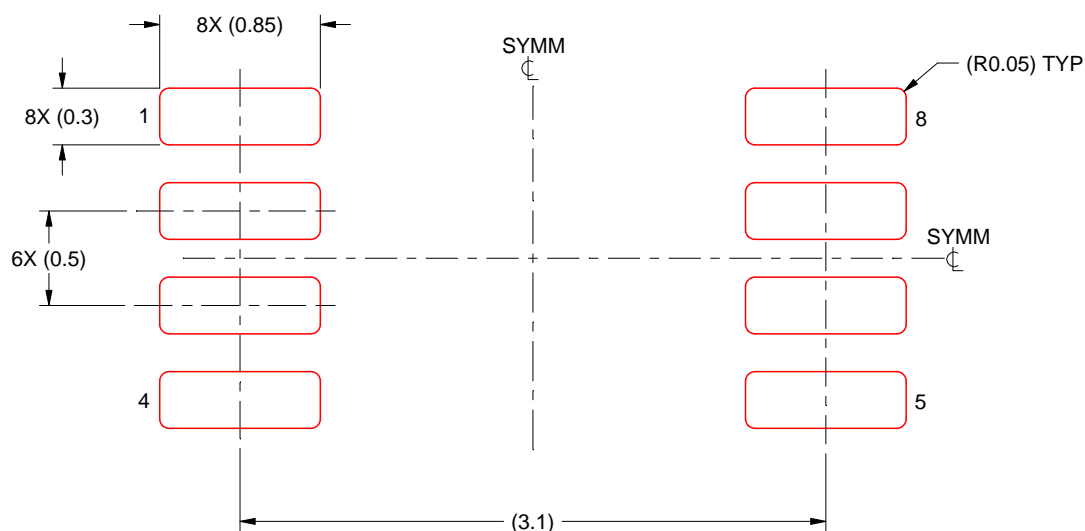
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE

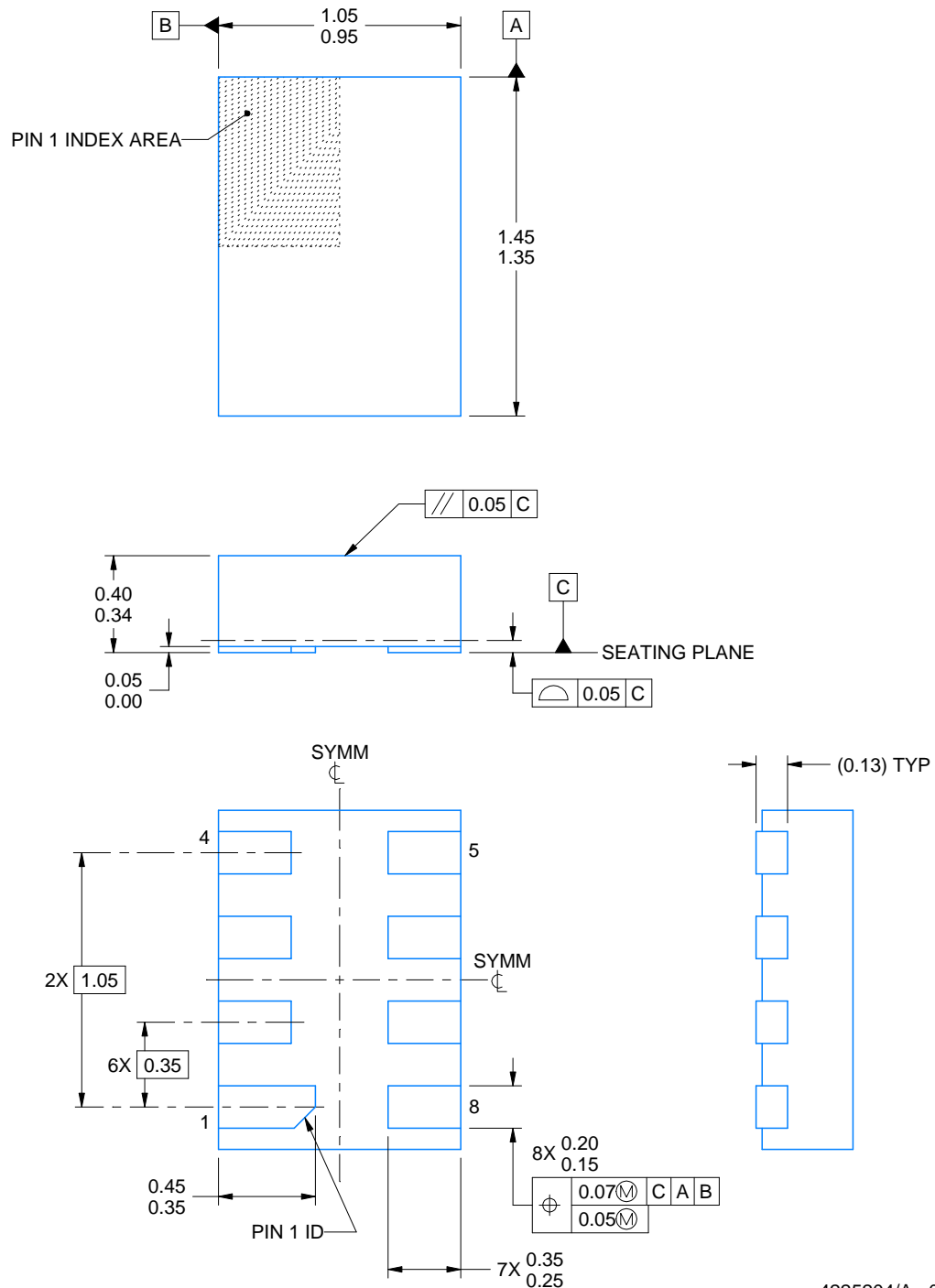
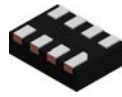


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



4225204/A 08/2019

NOTES:

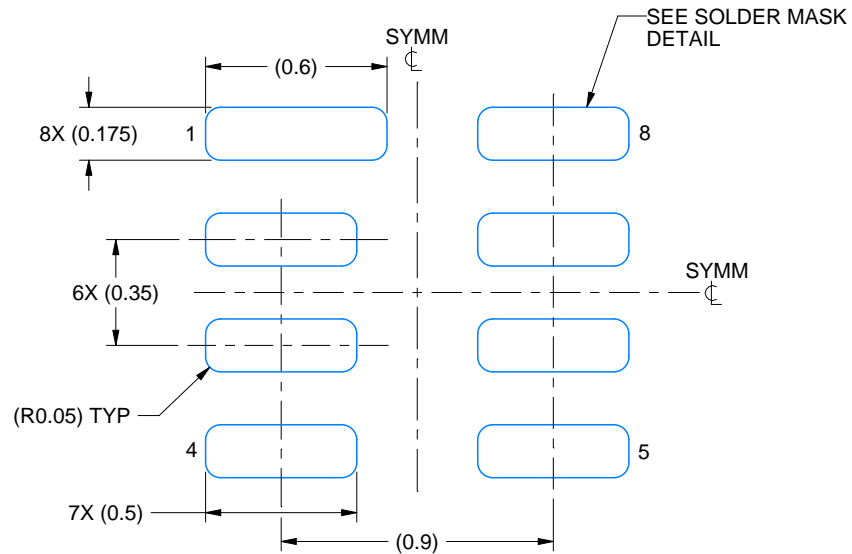
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package complies to JEDEC MO-287 variation X2EAF.

EXAMPLE BOARD LAYOUT

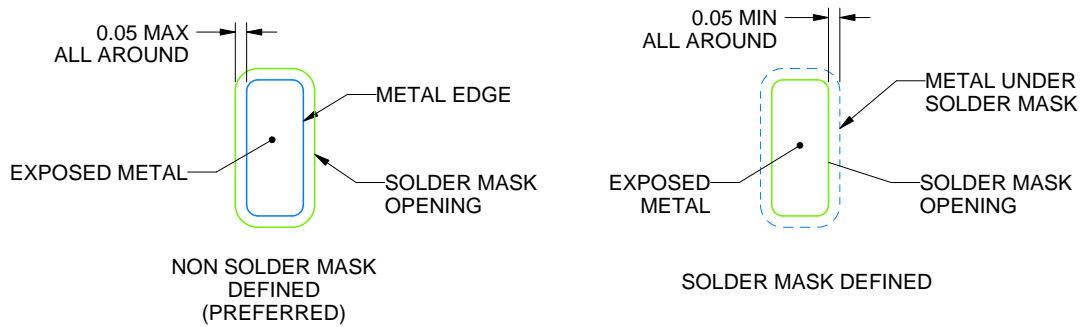
DQE0008A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X



SOLDER MASK DETAILS

4225204/A 08/2019

NOTES: (continued)

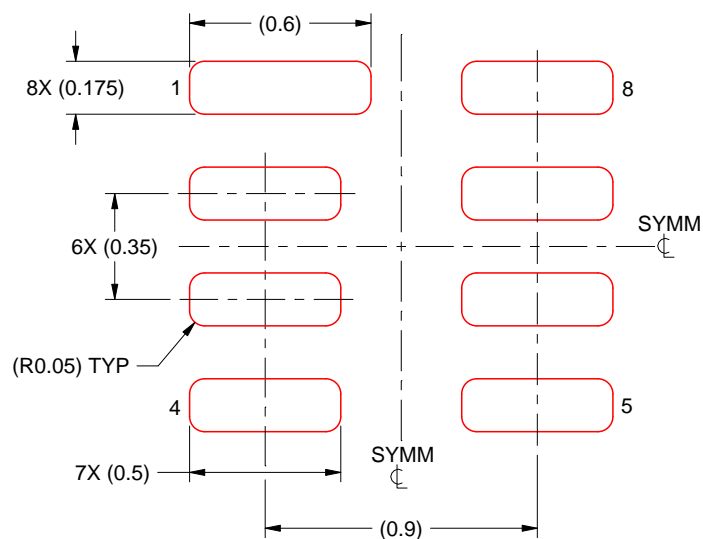
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).

EXAMPLE STENCIL DESIGN

DQE0008A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



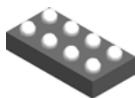
SOLDER PASTE EXAMPLE
BASED ON 0.075 MM THICK STENCIL
SCALE: 40X

4225204/A 08/2019

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

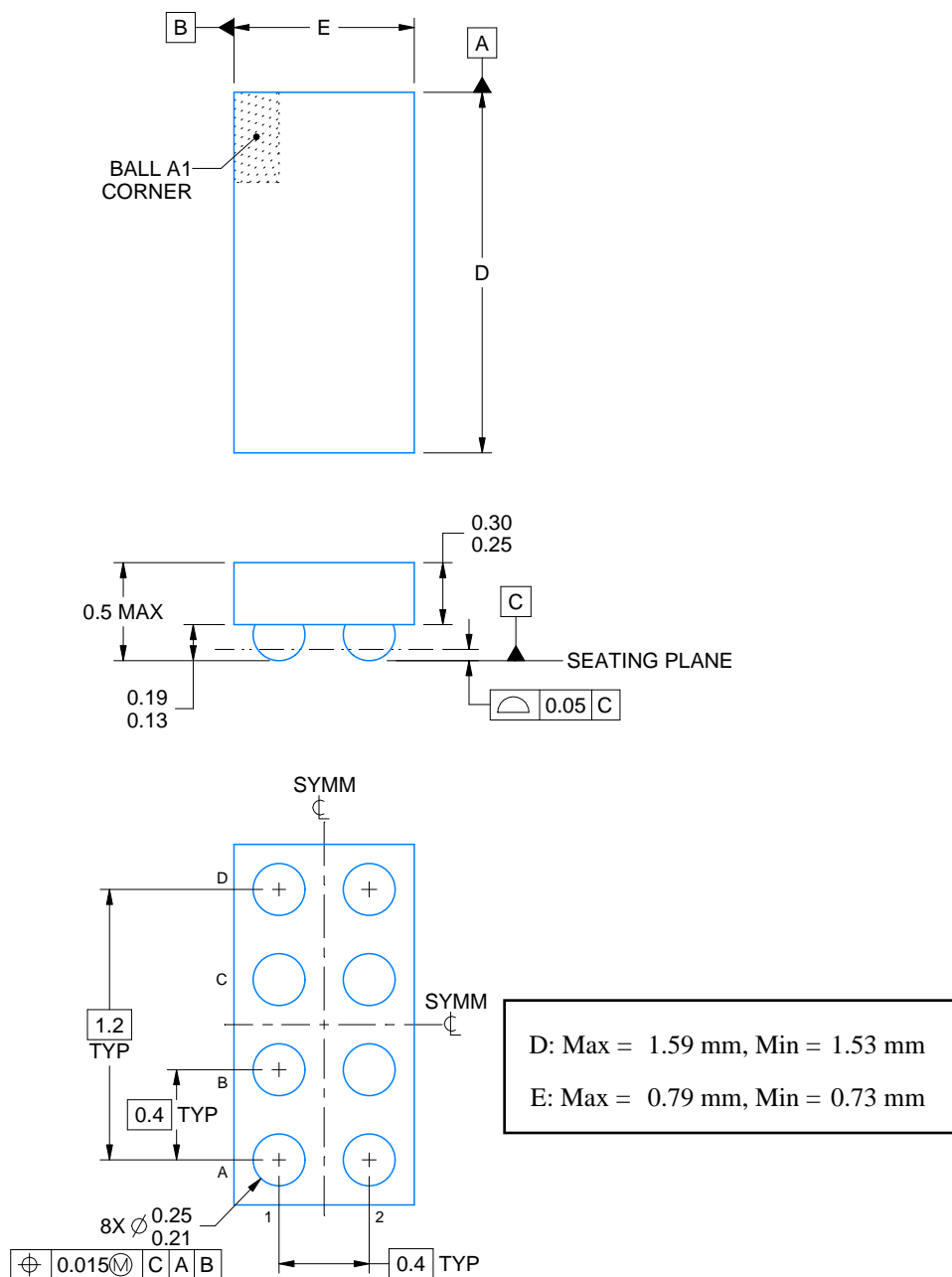
YFP0008



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4225242/A 08/2019

NOTES:

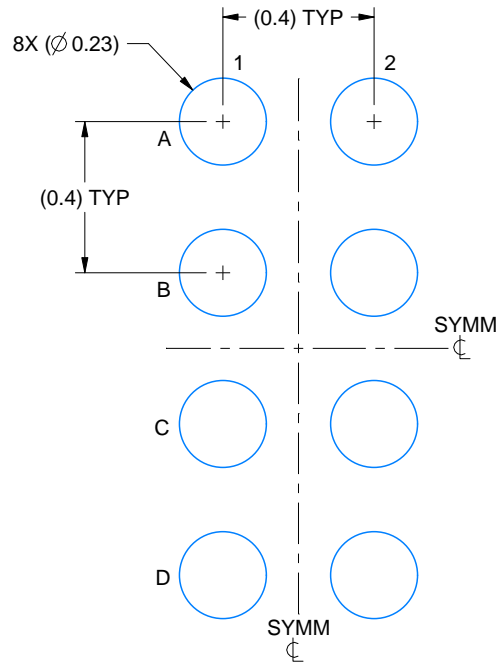
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

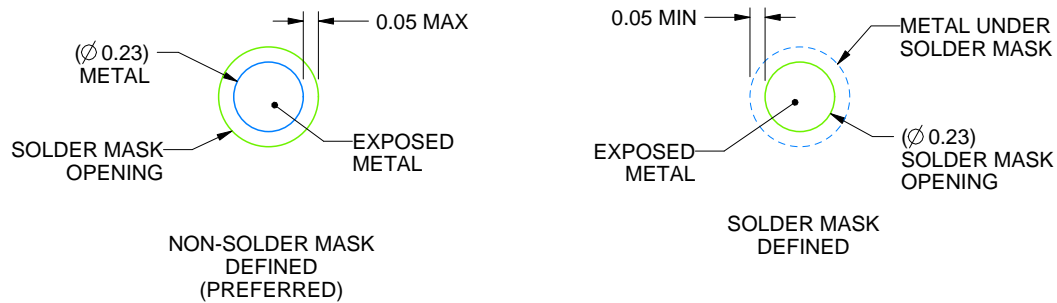
YFP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X

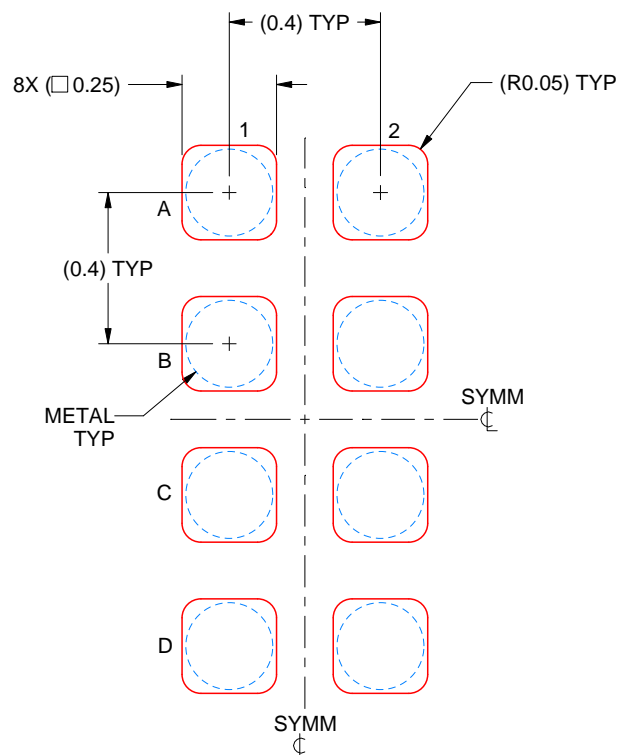


SOLDER MASK DETAILS
NOT TO SCALE

4225242/A 08/2019

NOTES: (continued)

- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

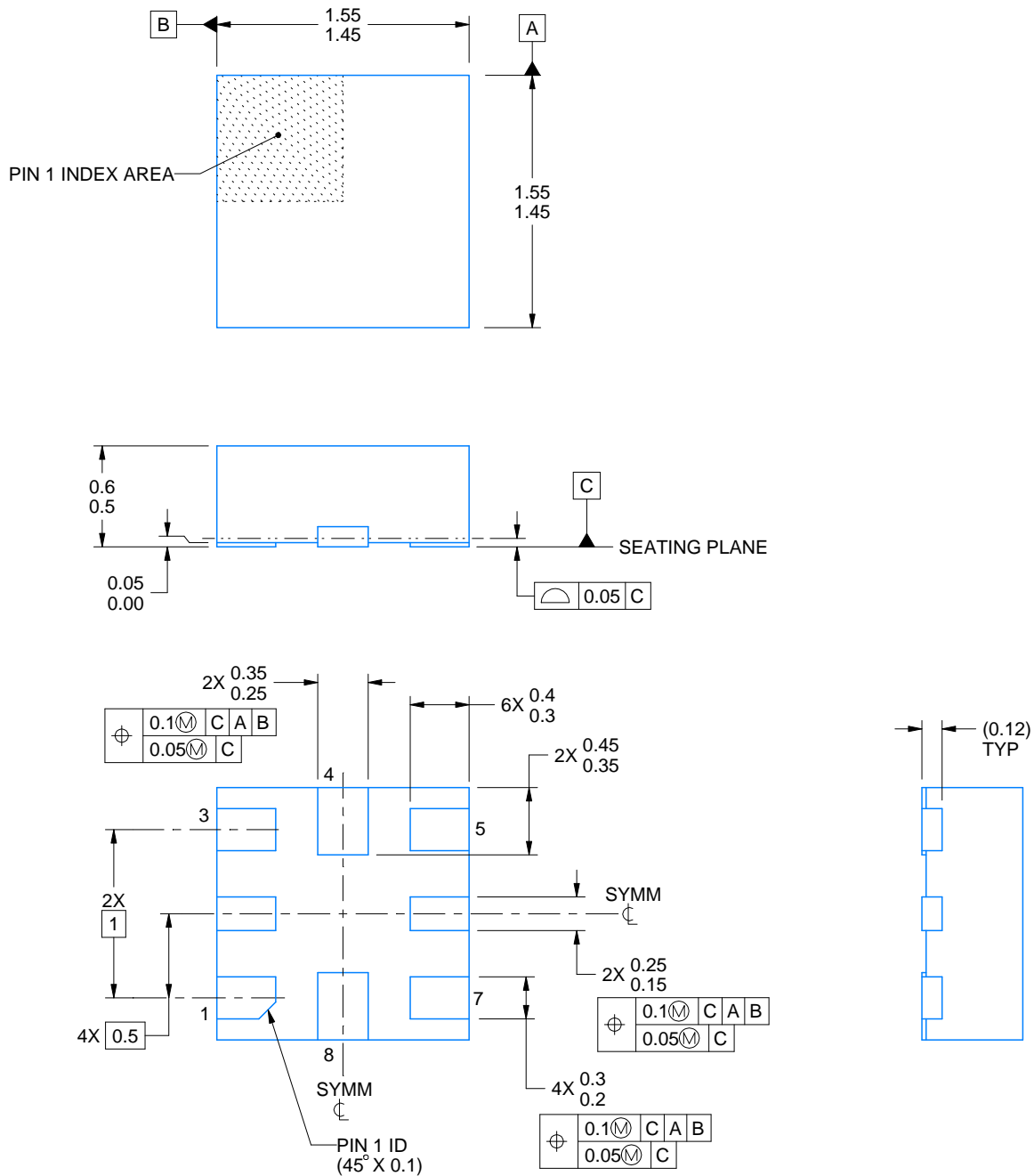


SOLDER PASTE EXAMPLE
 BASED ON 0.1 mm THICK STENCIL
 SCALE: 50X

4225242/A 08/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



4220323/B 03/2018

NOTES:

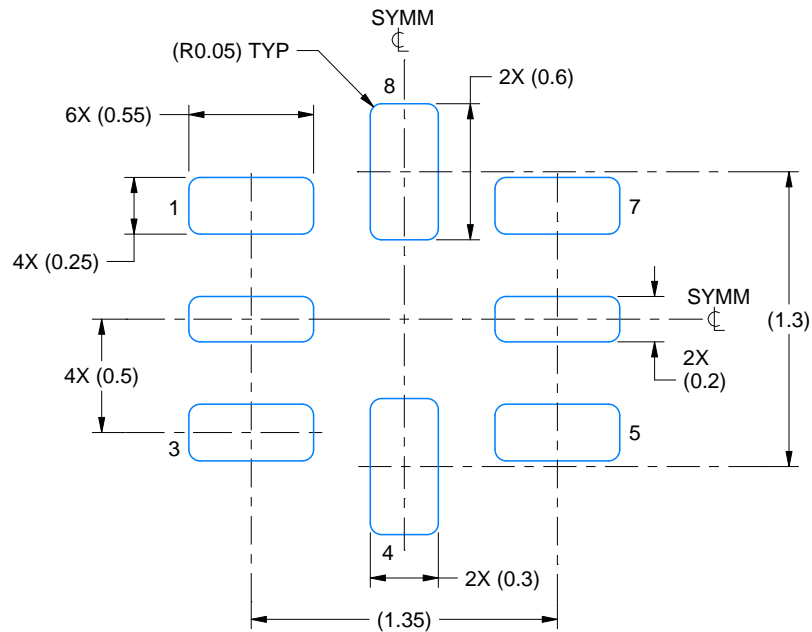
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

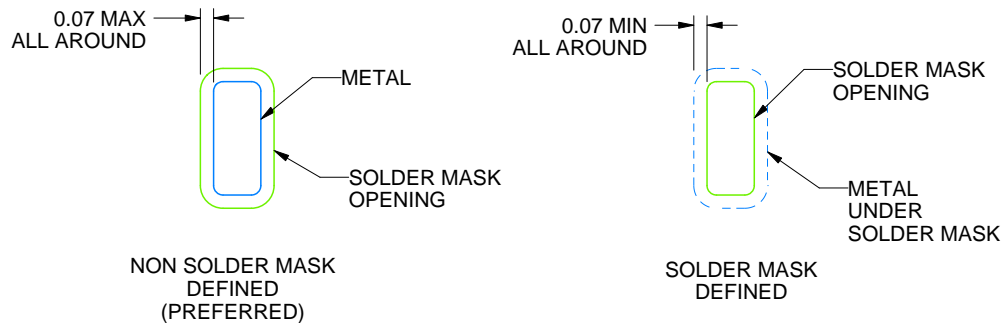
RSE0008A

UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

4220323/B 03/2018

NOTES: (continued)

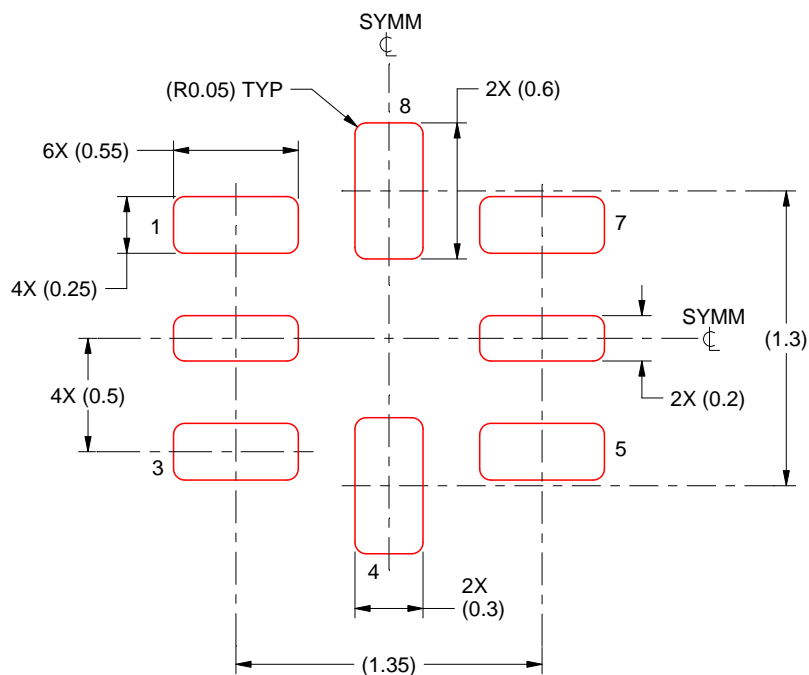
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RSE0008A

UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICKNESS
SCALE: 30X

4220323/B 03/2018

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

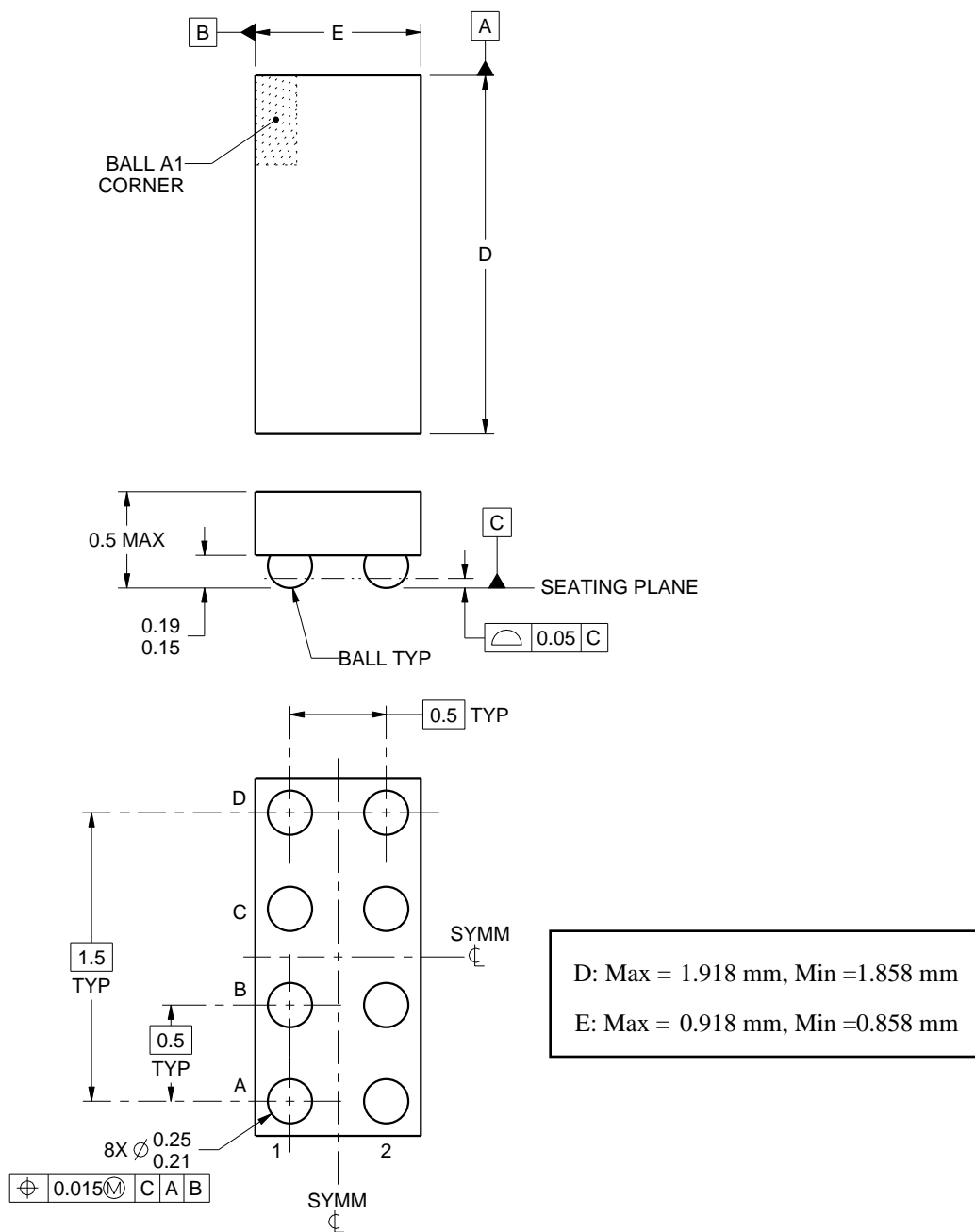
YZP0008



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4223082/A 07/2016

NOTES:

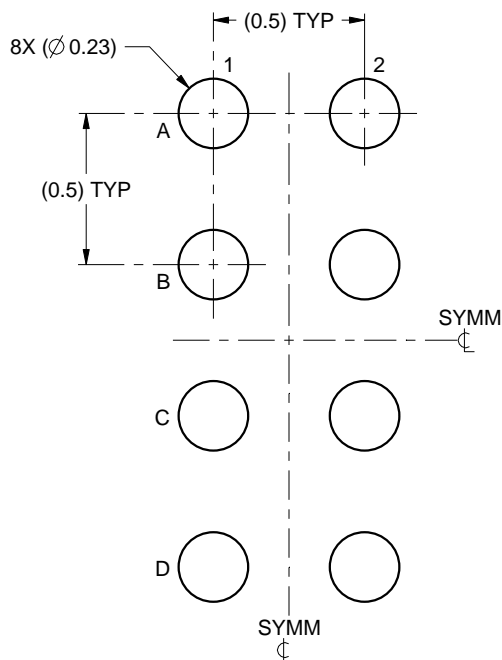
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

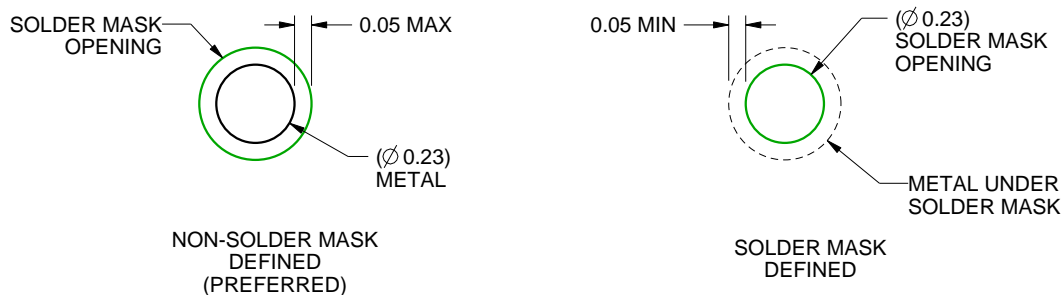
YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4223082/A 07/2016

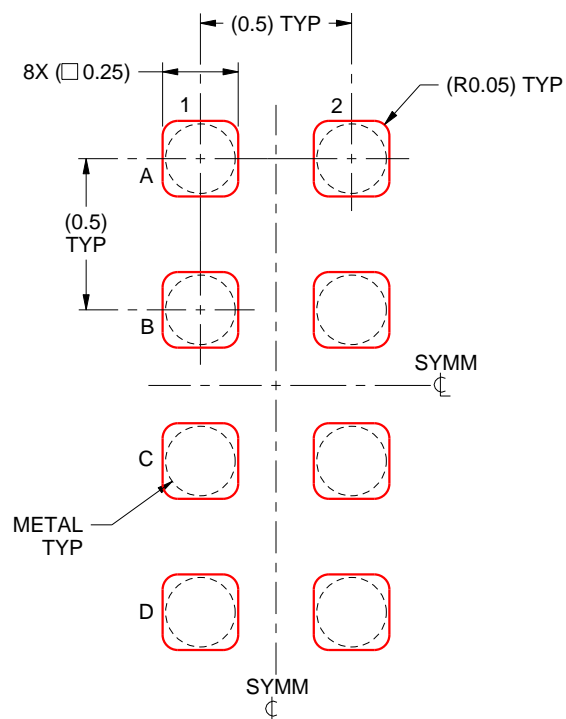
NOTES: (continued)

- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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