AM26LV32 低压高速四路差分线路接收器

1 特性

- 开关频率高达 32MHz
- 由 3.3V 单电源供电
- 超低功耗：27mW（典型值）
- 开路、短路及终止
  失效防护
- 具有 ±200mV 灵敏度的
  −0.3V 至 5.5V 共模范围
- 接受具有 3.3V V_{CC} 的 5V 逻辑输入
- 输入迟滞：50mV（典型值）
- 32MHz 具有四个接收器时为 235mW
- 与 AM26C32 和 AM26LS32 引脚对引脚兼容

2 应用

- 高可靠性汽车应用
- 工厂自动化
- ATM 和点钞机
- 智能电网
- 交流和伺服电机驱动器

3 说明

AM26LV32 器件是一款具有三态输出的 BiCMOS 四路差分线路接收器，其设计类似于 TIA/EIA-422-B 和 ITU Recommendation V.11 接收器，但由于电源电压降低，共模电压范围减小。

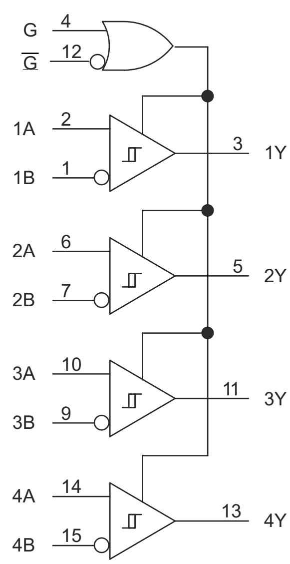
这款器件经过优化，可在高达 32MHz 的开关速率下实现平衡总线传输。四个接收器均具有使能功能，该功能提供了两种可选输入：高电平有效输入和低电平有效输入。通过三态输出，该器件可直接连接至总线组织式系统。每个器件都具有高输入阻抗、用于提高抗噪能力的输入滞后，以及在 −0.3V 至 5.5V 的共模输入电压范围内 ±200mV 的输入灵敏度。当输入开路时，输出处于逻辑高电平状态。

AM26LV32C 的特点是可在 0°C 至 70°C 的温度范围内工作。AM26LV32I 的特点是可在 -40°C 至 85°C 的温度范围内工作。

封装信息

器件型号	封装(1)	封装尺寸(2)
AM26LV32	SOIC (16)	9.9mm × 6mm
	SO (16)	10.2mm × 7.8mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 封装尺寸（长 x 宽）为标称值，并包括引脚（如适用）。



逻辑图（正逻辑）

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision G (October 2017) to Revision H (August 2023) — **Page**

- 将“器件信息”表更改为*封装信息* 表........ 1
- 将“描述”中的 AM26LV32I 温度从−45°C 至 85°C 更改为−40°C 至 85°C........ 1
- Changed the *Thermal Information* table........ 5
- Changed the *Typical Characteristics*........ 7

Changes from Revision F (November 2016) to Revision G (October 2017) — **Page**

- Changed the MAX value of $t_{sk(p)}$ From: 6 ns To: 14 ns in the *Switching Characteristics* table........ 6
- Changed the MAX value of $t_{sk(o)}$ From: 6 ns To: 14 ns in the *Switching Characteristics* table........ 6

Changes from Revision E (June 2005) to Revision F (November 2016) — **Page**

- 添加了 *ESD 等级* 表、*热性能信息* 表、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械*、*封装和可订购信息* 部分........ 1
- 从*特性* 列表中删除了 MB570........ 1
- 删除了*订购信息* 表；请参阅数据表末尾的*机械*、*封装和可订购信息*........ 1
- Deleted Lead temperature (260°C maximum) from *Absolute Maximum Ratings* table........ 4
- Changed Package thermal impedance, $R_{\theta JA}$, values in *Thermal Information* table From: 73°C To: 72.9°C (D) and From: 64°C To: 74°C (NS)........ 5

5 Pin Configuration and Functions

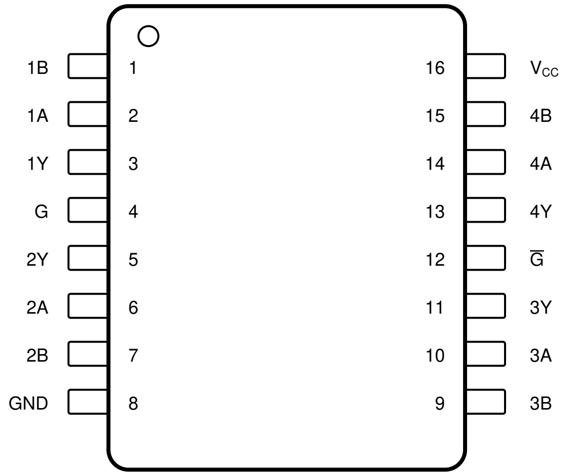


图 5-1. D and NS Package, 16-Pin SOIC and SO (Top View)

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1A	2	I	RS422, RS485 differential input (noninverting)
1B	1	I	RS422, RS485 differential input (inverting)
1Y	3	O	Logic level output
2A	6	I	RS422, RS485 differential input (noninverting)
2B	7	I	RS422, RS485 differential input (inverting)
2Y	5	O	Logic level output
3A	10	I	RS422, RS485 differential input (noninverting)
3B	9	I	RS422, RS485 differential input (inverting)
3Y	11	O	Logic level output
4A	14	I	RS422, RS485 differential input (noninverting)
4B	15	I	RS422, RS485 differential input (inverting)
4Y	13	O	Logic level output
$\overline{G}$	12	I	Active-low select
G	4	I	Active-high select
GND	8	—	Ground
V_{CC}	16	—	Power supply

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[1]

	MIN	MAX	UNIT
Supply voltage, V_{CC} [2]	–0.3	6	V
Input voltage, V_I	–4	8	V
Differential input voltage, V_{ID} [3]		±12	V
Enable input voltage	–0.3	6	V
Output voltage, V_O	–0.3	6	V
Maximum output current, I_O		±25	mA
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the GND terminal.
(3) Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3	3.3	3.6	V
High-level input voltage, $V_{IH(EN)}$		2			V
Low-level input voltage, $V_{IL(EN)}$				0.8	V
Common-mode input voltage, V_{IC}		–0.3		5.5	V
Differential input voltage, V_{ID}				±5.8	V
High-level output current, I_{OH}				–5	mA
Low-level output current, I_{OL}				5	mA
Operating free-air temperature, T_A	AM26LV32C	0		70	°C
	AM26LV32I	–40		85	

6.4 Thermal Information

THERMAL METRIC[(1)] [(2)]		AM26LV32				UNIT
		D (SOIC)	DR (SOIC-Reel)	NS (SO)	NSR (SO-Reel)	
		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	72.9	84.6	74	88.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.4	43.5	31.1	46.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30.4	43.2	34.8	50.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.4	10.4	5.1	13.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	30.1	42.8	34.5	50.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The package thermal impedance is calculated in accordance with JESD 51.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[(1)]	MAX	UNIT
V_{IT+}	Differential input high-threshold voltage				0.2	V
V_{IT-}	Differential input low-threshold voltage		–0.2			V
V_{IK}	Enable input clamp voltage	I_I = − 18 mA		–0.8	–1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = −5 mA	2.4	3.2		V
V_{OL}	Low-level output voltage	V_{ID} = 200 mV, I_{OH} = 5 mA		0.17	0.5	V
I_{OZ}	High-impedance-state output current	V_O = 0 to V_{CC}			±50	µA
$I_{IH(E)}$	High-level enable input current	V_{CC} = 0 or 3 V, V_I = 5.5 V			10	µA
$I_{IL(E)}$	Low-level enable input current	V_{CC} = 3.6 V, V_I = 0 V			–10	µA
r_I	Input resistance		7	12		kΩ
I_I	Input current	V_I = 5.5 V or − 0.3 V, all other inputs GND			±700	µA
I_{CC}	Supply current	$V_{I(E)}$ = V_{CC} or GND, no load, line inputs open		8	17	mA
C_{pd}	Power dissipation capacitance[(2)]	One channel		150		pF

(1) All typical values are at V_{CC} = 3.3 V and T_A = 25°C.
(2) C_{pd} determines the no-load dynamic current: $I_S = C_{pd} \times V_{CC} \times f + I_{CC}$.

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	See 图 7-1	8	16	20	ns
t_{PHL}	Propagation delay time, high- to low-level output	See 图 7-1	8	16	20	ns
t_t	Transition time (t_r or t_f)	See 图 7-1		5		ns
t_{PZH}	Output-enable time to high level	See 图 7-2		17	40	ns
t_{PZL}	Output-enable time to low level	See 图 7-3		10	40	ns
t_{PHZ}	Output-disable time from high level	See 图 7-2		20	40	ns
t_{PLZ}	Output-disable time from low level	See 图 7-3		16	40	ns
$t_{sk(p)}$ (1)	Pulse skew			4	14	ns
$t_{sk(o)}$ (2)	Pulse skew			4	14	ns
$t_{sk(pp)}$ (3)	Pulse skew (device to device)			6	9	ns

(1) $t_{sk(p)}$ is $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
(2) $t_{sk(o)}$ is the maximum difference in propagation delay times between any two channels of the same device switching in the same direction.
(3) $t_{sk(pp)}$ is the maximum difference in propagation delay times between any two channels of any two devices switching in the same direction.

6.7 Typical Characteristics

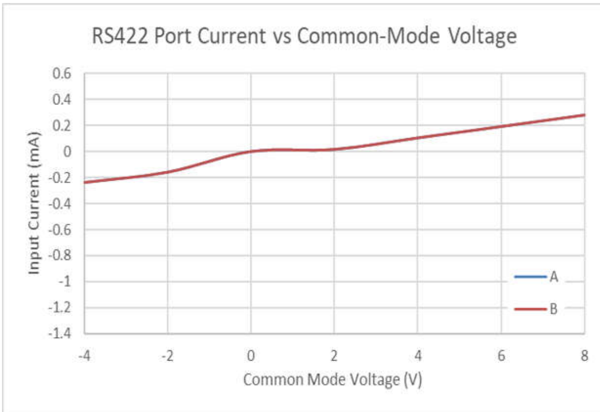


图 6-1. RS422 Port Current vs Common-Mode Voltage

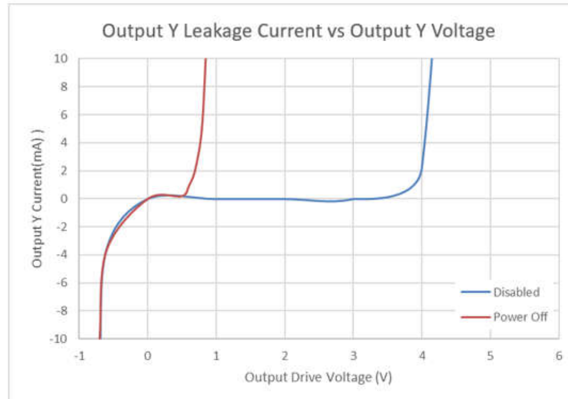


图 6-2. Output Y Leakage Current vs Output Y Voltage

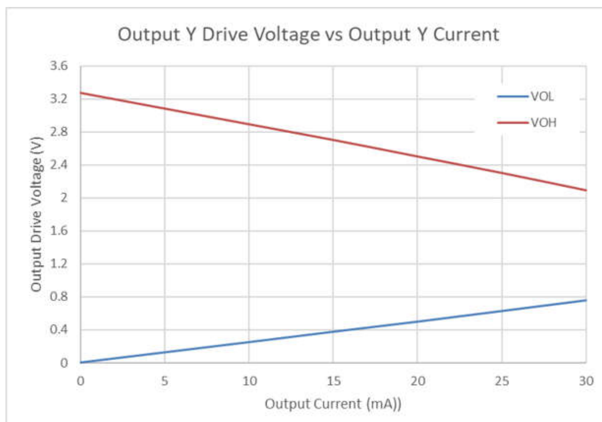
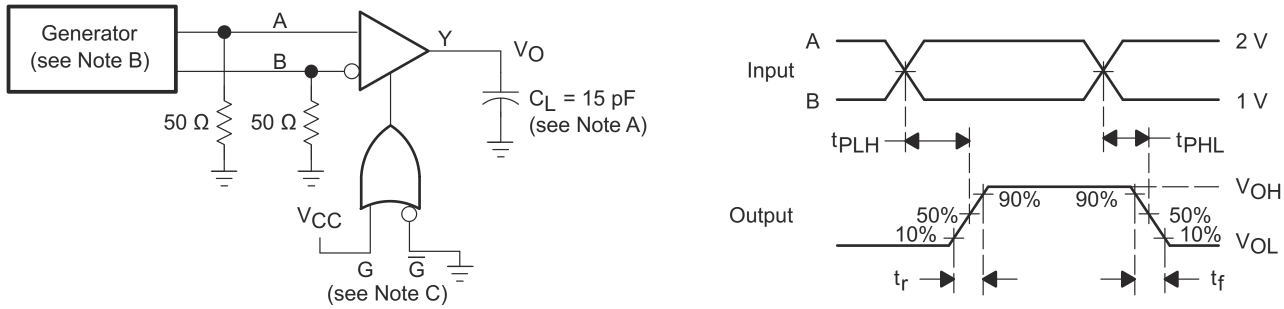


图 6-3. Output Y Drive Voltage vs Output Y Current

7 Parameter Measurement Information

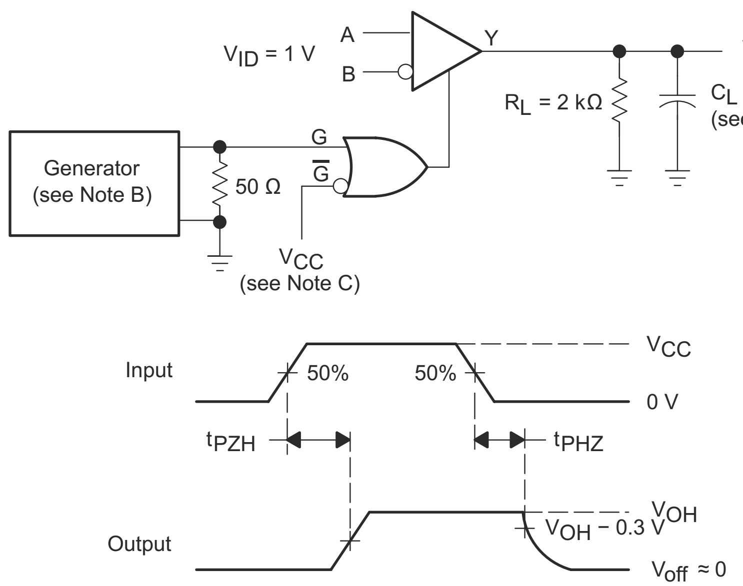


A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: Z_O = 50 Ω, PRR = 10 MHz, t_r and t_f (10% to 90%) ⩽ 2 ns, 50% duty cycle.

C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform $\overline{G}$.

图 7-1. t_{PLH} and t_{PHL} Test Circuit and Voltage Waveforms

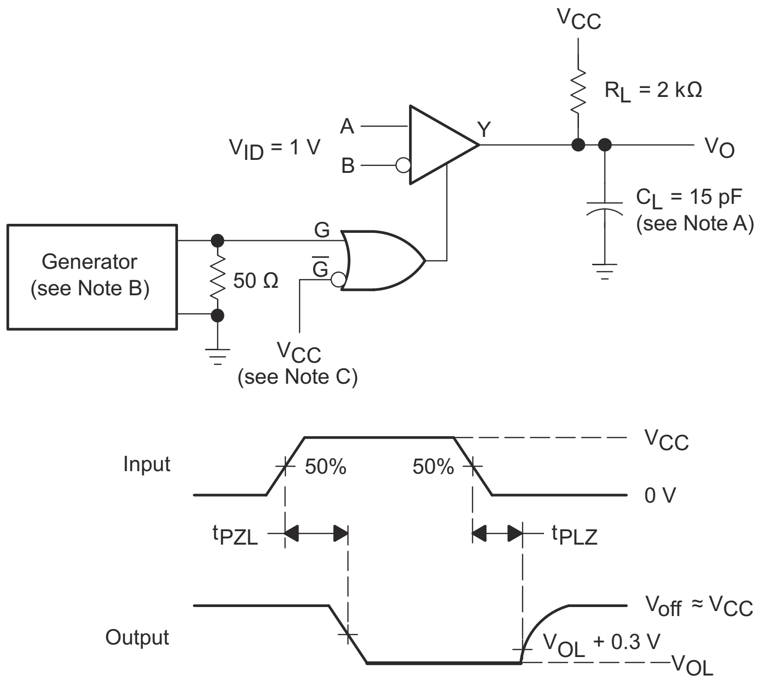


A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: Z_O = 50 Ω, PRR = 10 MHz, t_r and t_f (10% to 90%) ⩽ 2 ns, 50% duty cycle.

C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform $\overline{G}$.

图 7-2. t_{PZH} and t_{PHZ} Test Circuit and Voltage Waveforms



A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: Z_O = 50 Ω, PRR = 10 MHz, t_r and t_f (10% to 90%) ⩽ 2 ns, 50% duty cycle.

C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform $\overline{G}$.

图 7-3. t_{PZL} and t_{PLZ} Test Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The AM26LV32 device is a quadruple differential line receiver that meets the necessary requirements for NSI TIA/EIA-422-B, TIA/EIA-423-B, and ITU Recommendation V.10 and V.11. This device allows a low-power or low-voltage MCU to interface with heavy machinery, subsystems, and other devices through long wires of up to 1000 m, giving any design a reliable and easy-to-use connection. As with any RS422 interface, the AM26LV32 works in a differential voltage range, which enables very good signal integrity.

8.2 Functional Block Diagram

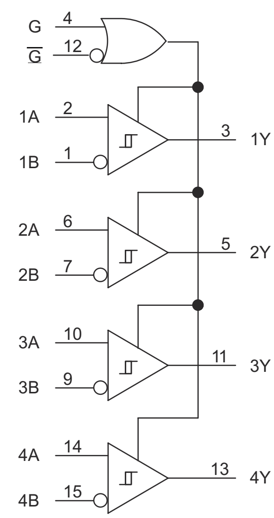


图 8-1. Logic Diagram (Positive Logic)

8.3 Feature Description

The device can be configured using the G and $\overline{G}$ logic inputs to select receiver output. The high voltage or logic 1 on the G pin allows the device to operate on an active-high, and having a low voltage or logic 0 on the $\overline{G}$ enables active-low operation. These are simple ways to configure the logic to match that of the receiving or transmitting controller or microprocessor.

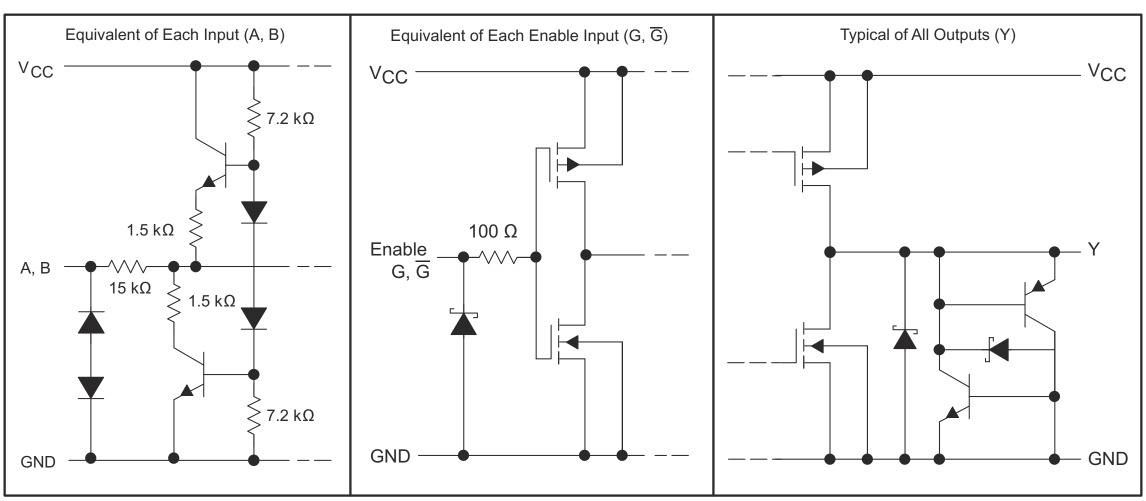


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图 8-2. Schematics of Equivalent Inputs and Outputs

8.4 Device Functional Modes

The receivers implemented in these RS422 devices can be configured using the G and $\overline{G}$ logic pins to be enabled or disabled. This allows the option to ignore or filter out transmissions as desired. 表 8-1 lists the function of each receiver.

表 8-1. Function Table (Each Receiver)

DIFFERENTIAL INPUT	ENABLES		OUTPUT(1)
	G	$\overline{G}$	
$V_{ID} \geqslant 0.2$ V	H	X	H
	X	L	H
-0.2 V < V_{ID} < 0.2 V	H	X	?
	X	L	?
$V_{ID} \leqslant -0.2$ V	H	X	L
	X	L	L
Open, shorted, or terminated(2)	H	X	H
	X	L	H
X	L	H	Z

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), ? = indeterminate
(2) See 节 9 section

8.4.1 Fail-Safe Conditions

The AM26LV32 is a quadruple differential line receiver that is designed to function properly when appropriately connected to active drivers. Applications do not always have ideal situations where all bits are being used, the receiver inputs are never left floating, and fault conditions do not exist. In actuality, most applications have the capability to either place the drivers in a high-impedance mode or power down the drivers altogether, and cables may be purposely (or inadvertently) disconnected, both of which lead to floating receiver inputs. Furthermore, even though measures are taken to avoid fault conditions like a short between the differential signals, this does occur. The AM26LV32 device has an internal fail-safe circuitry which prevents the device from putting an unknown voltage signal at the receiver outputs. In the following three cases, a high-state is produced at the respective output:

1. Open fail-safe: Unused input pins are left open. Do not tie unused pins to ground or any other voltage. Internal circuitry places the output in the high state.
2. 100-Ω terminated fail-safe: Disconnected cables, drivers in high-impedance state, or powered-down drivers does not cause the AM26LV32 to malfunction. The outputs remain in a high state under these conditions. When the drivers are either turned-off or placed into the high-impedance state, the receiver input may still be able to pick up noise due to the cable acting as an antenna. To avoid having a large differential voltage being generated, the use of twisted-pair cable induces the noise as a common-mode signal and is rejected.
3. Shorted fail-safe: Fault conditions that short the differential input pairs together does not cause incorrect data at the outputs. A differential voltage (V_{ID}) of 0 V forces a high state at the outputs. Shorted fail-safe, however, is not supported across the recommended common-mode input voltage (V_{IC}) range. An unwanted state can be induced to all outputs when an input is shorted and is biased with a voltage between −0.3 V and +5.5 V. The shorted fail-safe circuitry functions properly when an input is shorted, but with no external common-mode voltage applied.

8.4.2 Fail-Safe Precautions

The internal fail-safe circuitry was designed such that the input common-mode (V_{IC}) and differential (V_{ID}) voltages must be observed. To ensure the outputs of unused or inactive receivers remain in a high state when the inputs are open-circuited, shorted, or terminated, extra precaution must be taken on the active signal. In applications where the drivers are placed in a high-impedance mode or are powered-down, TI recommends that for 1, 2, or 3 active receiver inputs, the low-level input voltage (V_{IL}) must be greater than 0.4 V. As in all data transmission applications, it is necessary to provide a return ground path between the two remote grounds (driver and receiver ground references) to avoid ground differences. 表 8-2 and 图 8-3 through 图 8-5 are examples of active input voltages with their respective waveforms and the effect each have on unused or inactive outputs. Note that the active receivers behave as expected, regardless of the input levels.

表 8-2. Active Receiver Inputs vs Outputs

1, 2, OR 3 ACTIVE INPUTS			SEE FIGURE	1, 2, OR 3 ACTIVE OUTPUTS	3, 2, OR 1 UNUSED OR INACTIVE OUTPUTS
V_{IL}	V_{ID}	V_{IC}			
900 mV	200 mV	1 V	图 8-3	Known state	High state
– 100 mV	200 mV	0 V	图 8-4	Known state	?
600 mV	800 mV	1 V	图 8-5	Known state	High state
0 mV	800 mV	400 mV	图 8-6	Known state	?

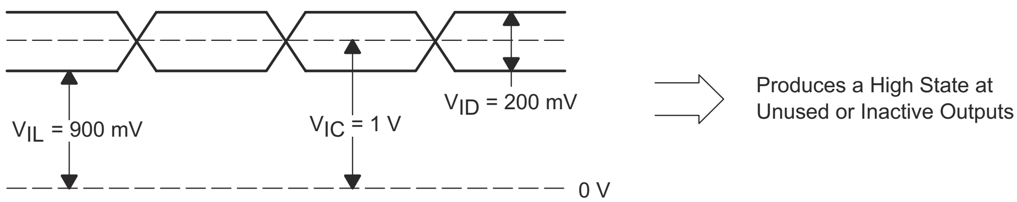

图 8-3. Waveform 1

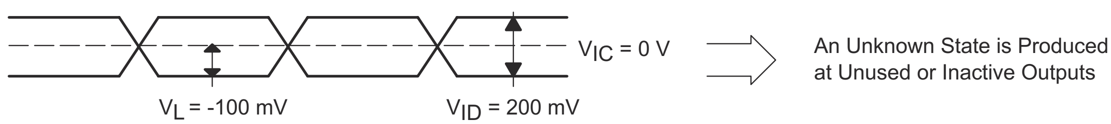

图 8-4. Waveform 2

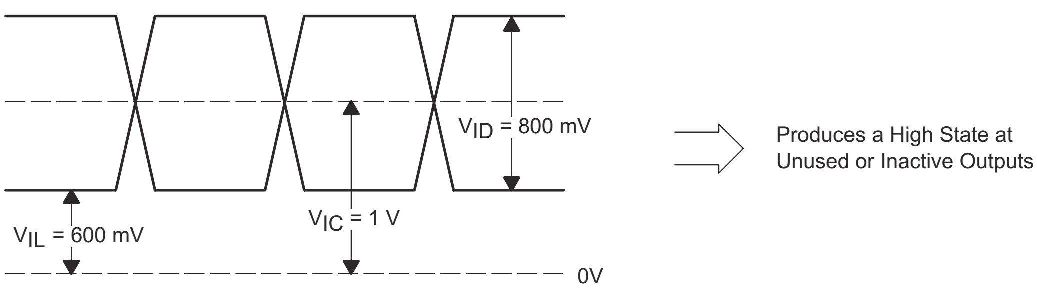

图 8-5. Waveform 3

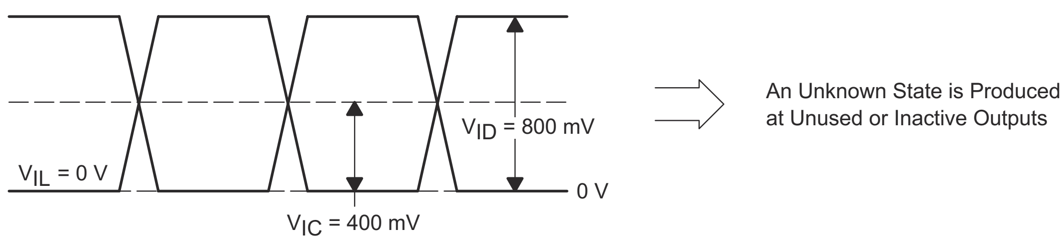

图 8-6. Waveform 4

In most applications, having a common-mode input close to ground and a differential voltage larger than 2 V is not customary. Because the common-mode input voltage is typically around 1.5 V, a 2-V V_{ID} would result in a V_{IL} of 0.5 V, thus satisfying the recommended V_{IL} level of greater than 0.4 V.

图 8-7 plots seven different input threshold curves from a variety of production lots and shows how the fail-safe circuitry behaves with the input common-mode voltage levels. These input threshold curves are representative samples of production devices. The curves specifically illustrate a typical range of input threshold variation. The

AM26LV32 is specified with ±200 mV of input sensitivity to account for the variance in input threshold. Each data point represents the input's ability to produce a known state at the output for a given V_{IC} and V_{ID}. Applying a differential voltage at or above a certain point on a curve would produce a known state at the output. Applying a differential voltage less than a certain point on a curve would activate the fail-safe circuit and the output would be in a high state. For example, inspecting the top input threshold curve reveals that for a V_{IC} that is approximately 1.6 V, V_{ID} yields around 87 mV. Applying 90 mV of differential voltage to this particular production lot generates a known receiver output voltage. Applying a V_{ID} of 80 mV activates the input fail-safe circuitry and the receiver output is placed in the high state. Texas Instruments specifies the input threshold at ±200 mV, because normal process variations affect this parameter. Note that at common-mode input voltages around 0.2 V, the input differential voltages are low compared to their respective data points. This phenomenon points to the fact that the inputs are very sensitive to small differential voltages around 0.2 V V_{IC}. TI recommends that V_{IC} levels be kept greater than 0.5 V to avoid this increased sensitivity at $V_{IC} \approx 0.2$ V. In most applications, because V_{IC} typically is 1.5 V, the fail-safe circuitry functions properly to provide a high state at the receiver output.

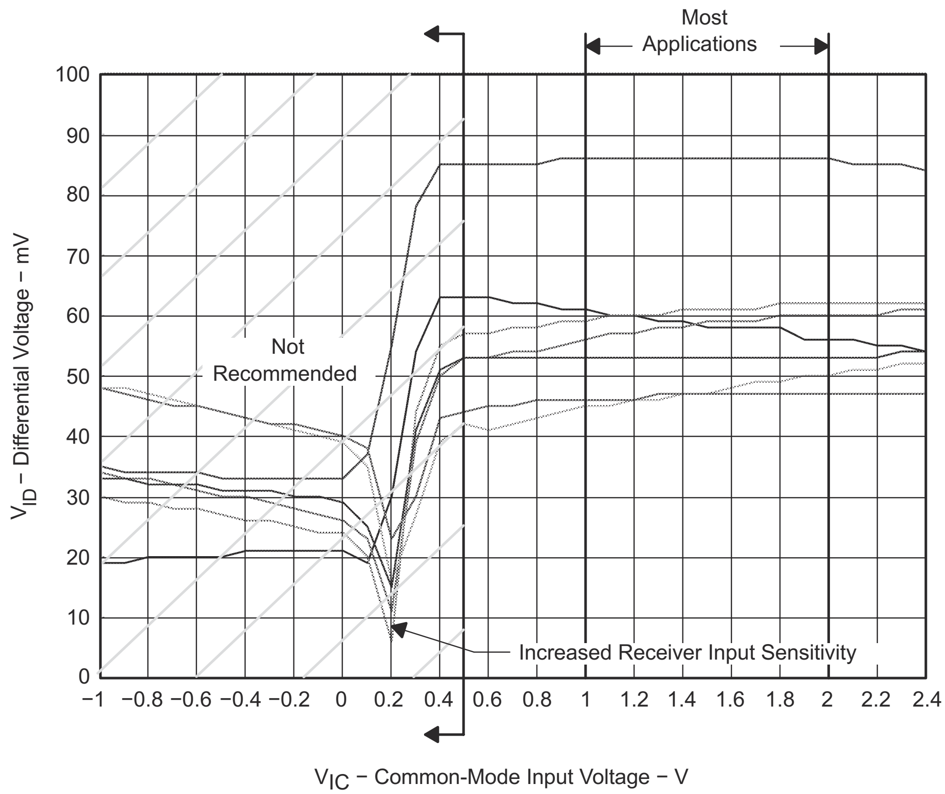

图 8-7. V_{IC} vs V_{ID} Receiver Sensitivity Levels

图 8-8 represents a typical application where two receivers are not used. In this case, there is no need to worry about the output voltages of the unused receivers because these are not connected in the system architecture.

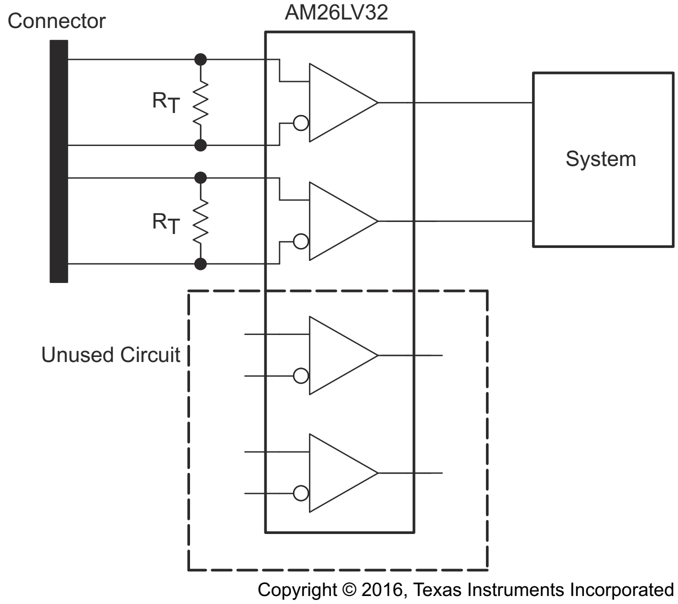

图 8-8. Typical Application With Unused Receivers

图 8-9 shows a common application where one or more drivers are either disabled or powered down. To ensure the inactive receiver outputs are in a high state, the active receiver inputs must have V_{IL} > 0.4 V and V_{IC} > 0.5 V.

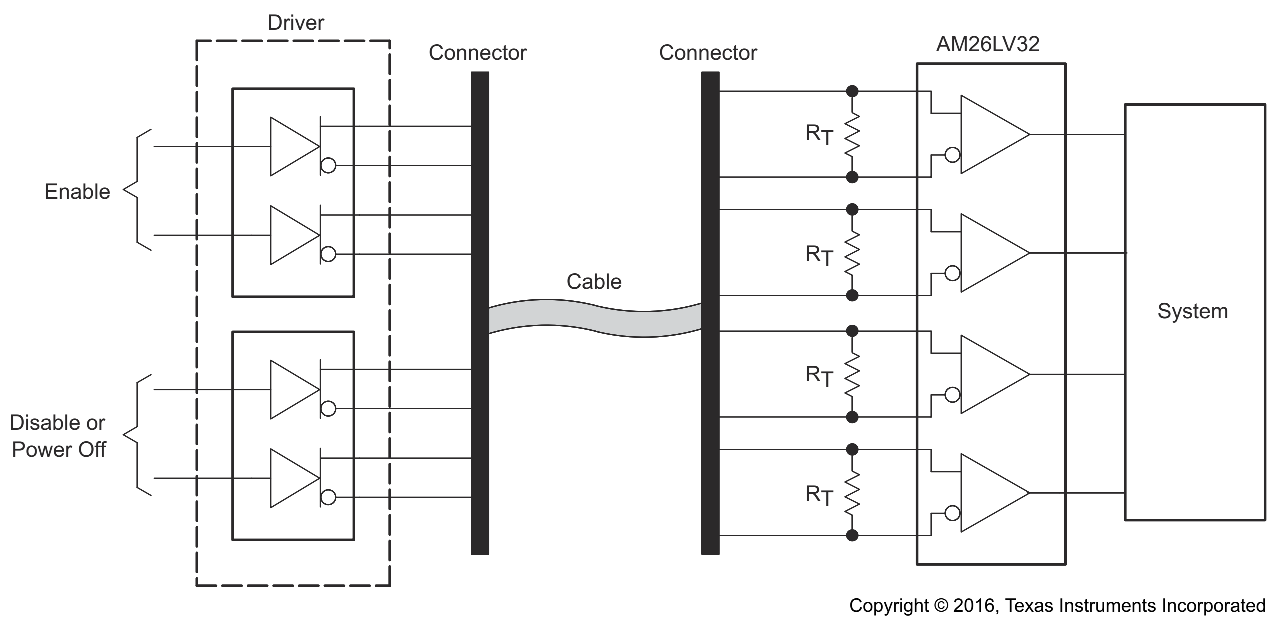

图 8-9. Typical Application Where Two or More Drivers Are Disabled

图 8-10 is an alternative application design to replace the application in 图 8-9. This design uses two AM26LV32 devices instead of one. However, this design does not require the input levels be monitored to ensure the outputs are in the correct state, only that they comply to the RS-232 standard.

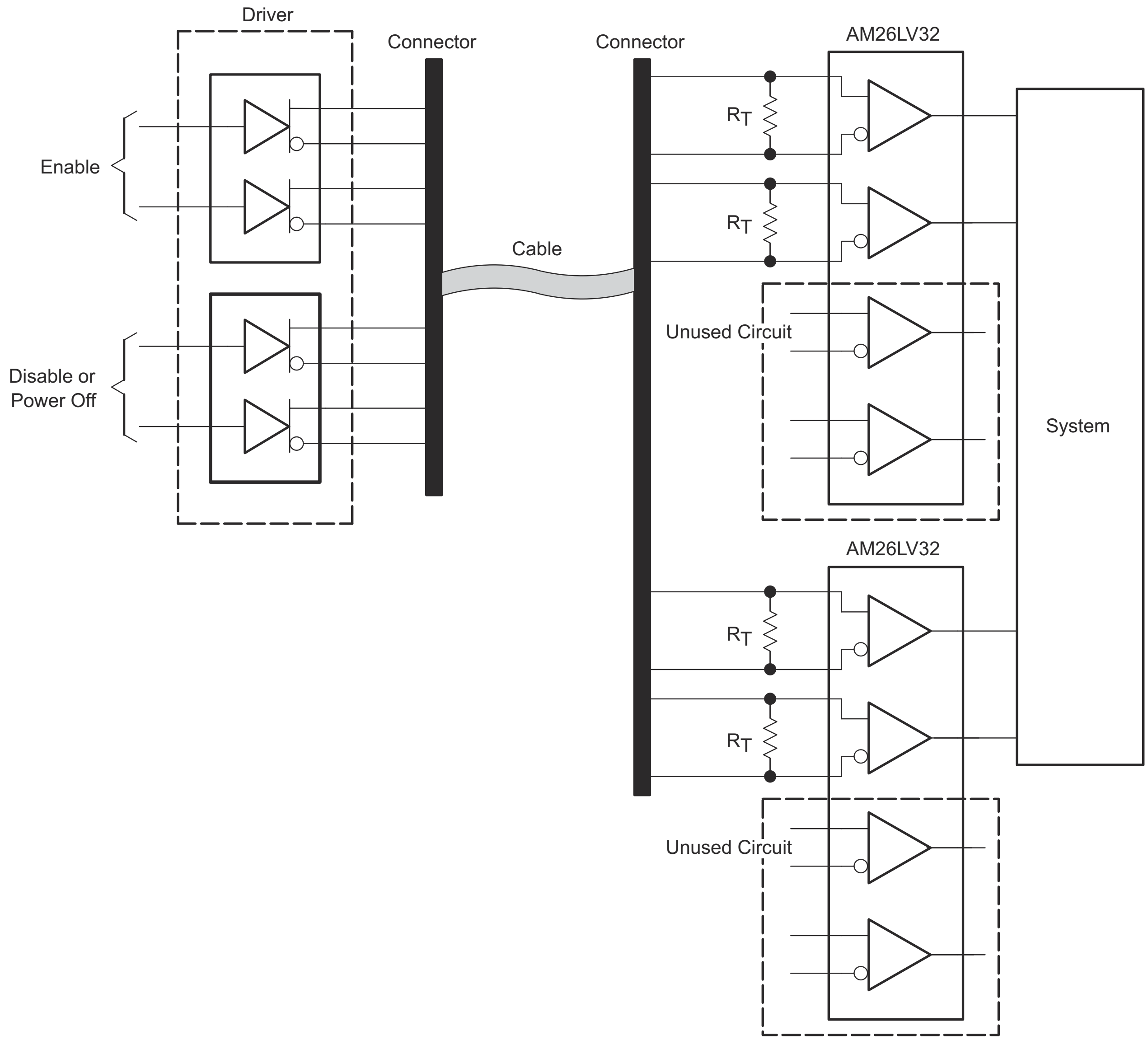

图 8-10. Alternative Solution for 图 8-9

图 8-11 and 图 8-12 show typical applications where a disconnected cable occurs. 图 8-11 illustrates a typical application where a cable is disconnected. Similar to 图 8-9, the active input levels must be monitored to make sure the inactive receiver outputs are in a high state. An alternative solution is shown in 图 8-12.

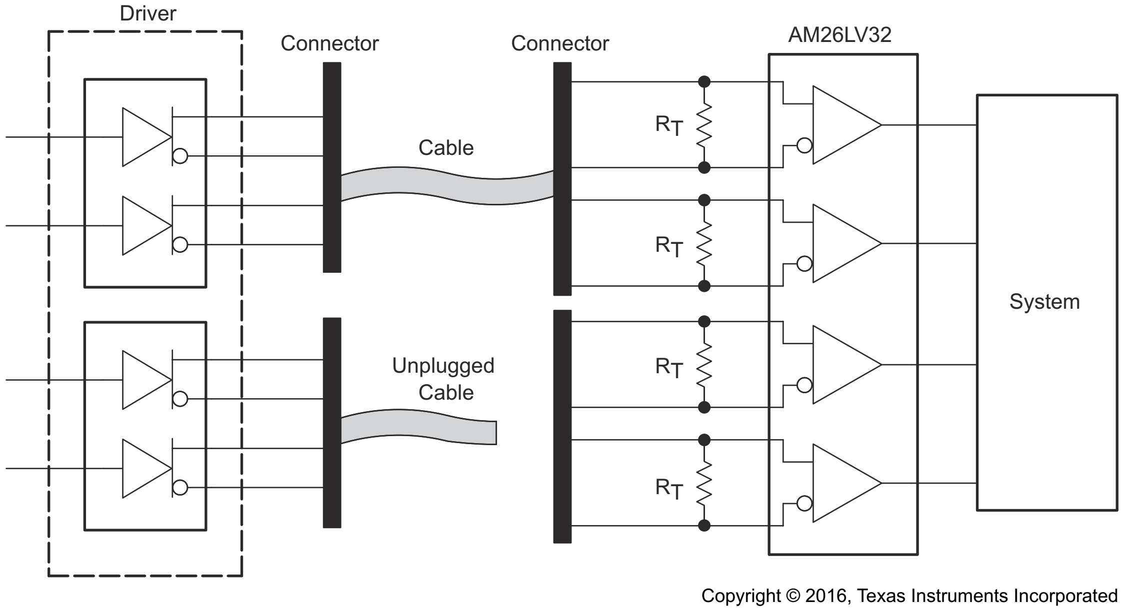

图 8-11. Typical Application Where Two or More Drivers Are Disconnected

图 8-12 is an alternative solution so the receiver inputs do not have to be monitored. This solution also requires the use of two AM26LV32 devices instead of one.

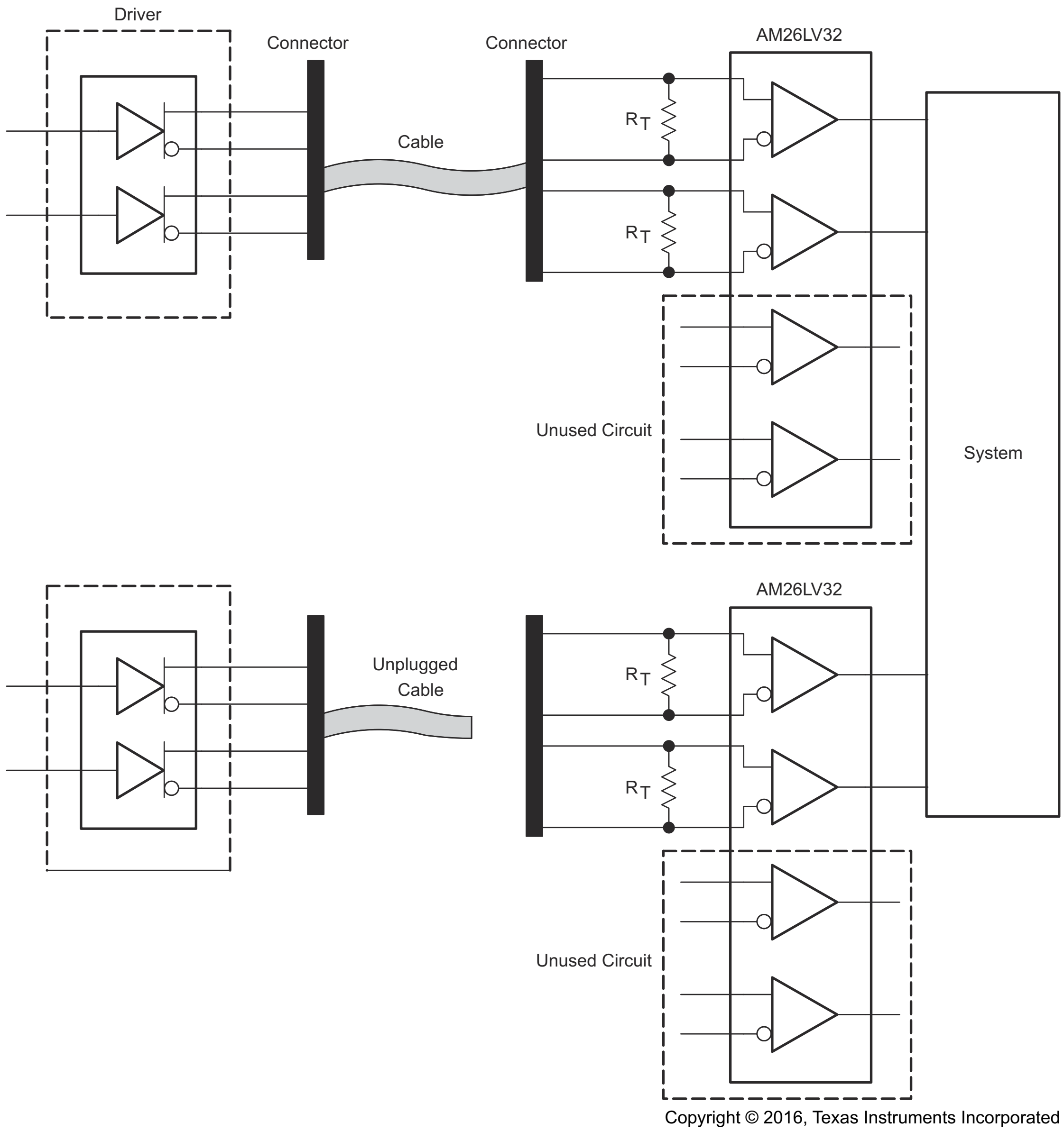

图 8-12. Alternative Solution to 图 8-11

When designing a system using the AM26LV32, the device provides a robust solution where fail-safe and fault conditions are of concern. The RS422-like inputs accept common-mode input levels from −0.3 V to 5.5 V with a specified sensitivity of ±200mV. As previously shown, take care with active input levels because this can affect the outputs of unused or inactive bits. However, most applications meet or exceed the requirements to allow the device to perform properly.

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

When designing a system that uses drivers, receivers, and transceivers that comply with RS422 or RS485, proper cable termination is essential for highly reliable applications with reduced reflections in the transmission line. Because RS422 allows only one driver on the bus, if termination is used, it is placed only at the end of the cable near the last receiver. In general, RS485 requires termination at both ends of the cable. Factors to consider when determining the type of termination usually are performance requirements of the application and the ever-present factor, cost. The different types of termination techniques include unterminated lines, parallel termination, ac termination, and multipoint termination.

9.2 Typical Application

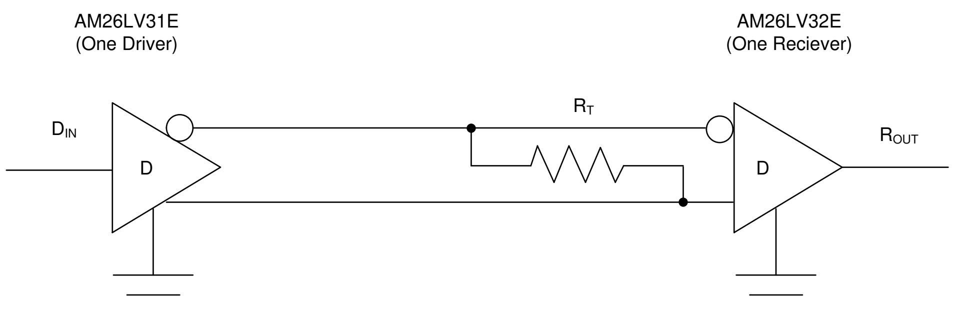

图 9-1. Differential Terminated Configuration

9.2.1 Design Requirements

Resistor and capacitor (if used) termination values vary from system to system. The termination resistor, R_T, must be within 20% of the characteristic impedance, R_{OUT}, of the cable and can vary from about 80 Ω to 120 Ω.

9.2.2 Detailed Design Procedure

图 9-1 shows a configuration with R_T as termination. Although reflections are present at the receiver inputs at a data signaling rate of 200 kbps with no termination, the RS422-compliant receiver reads only the input differential voltage and produces a clean signal at the output.

9.2.3 Application Curve

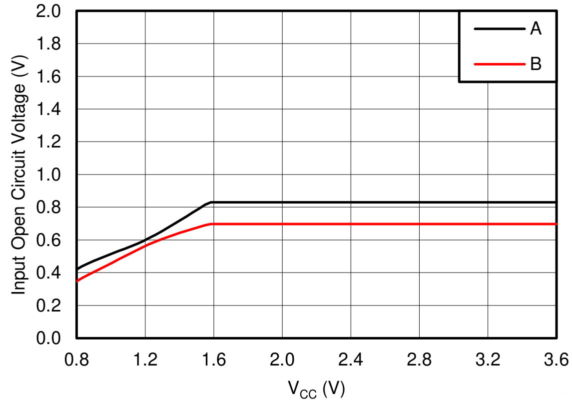

图 9-2. RS422 Port Open-Circuit Voltage vs V_{CC}

9.3 Power Supply Recommendations

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies.

9.4 Layout

9.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
- Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, and pay attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

9.4.2 Layout Example

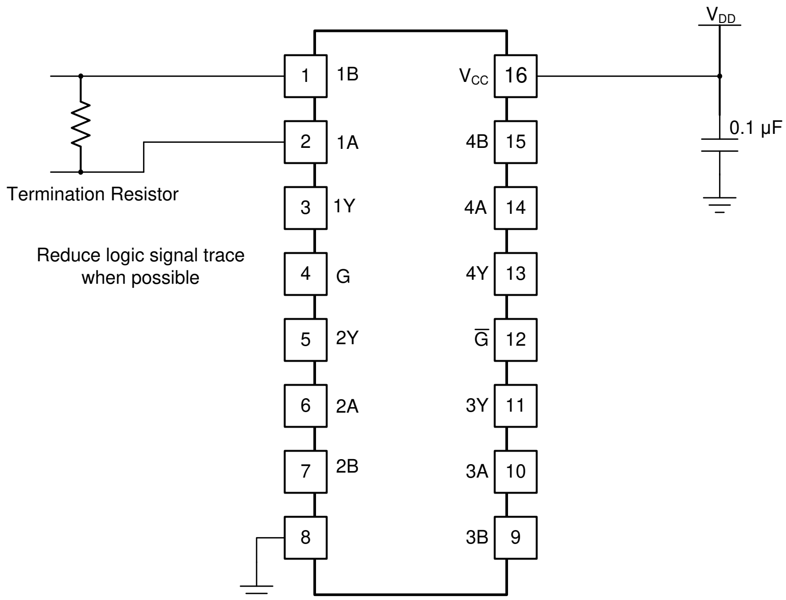

图 9-3. Layout With PCB Recommendations

10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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10.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AM26LV32CD	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	0 to 70	AM26LV32C
AM26LV32CDR	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	0 to 70	AM26LV32C
AM26LV32CDRG4	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	0 to 70	AM26LV32C
AM26LV32ID	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-40 to 85	AM26LV32I
AM26LV32IDR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26LV32I
AM26LV32INS	Obsolete	Production	SOP (NS) | 16	-	-	Call TI	Call TI	-40 to 85	26LV32I
AM26LV32INSR	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-1-260C-UNLIM	-40 to 85	26LV32I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

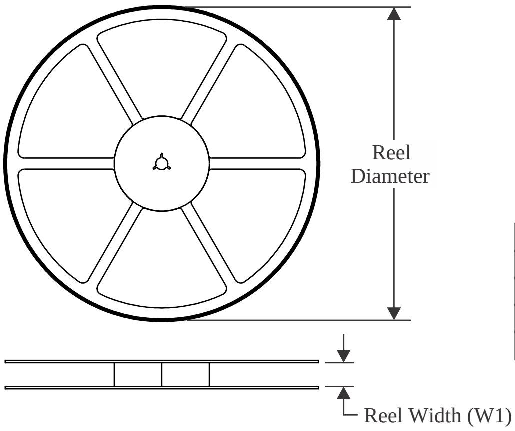
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

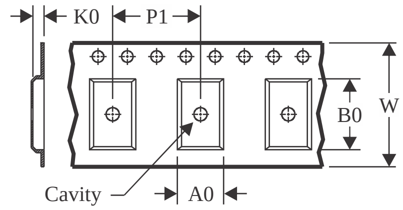
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

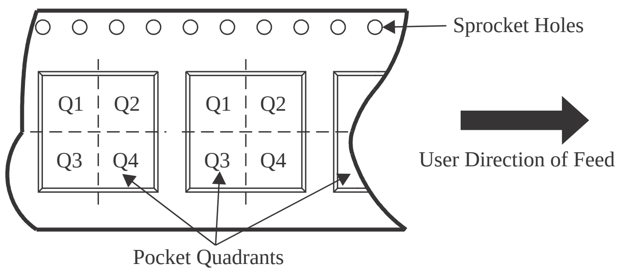


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

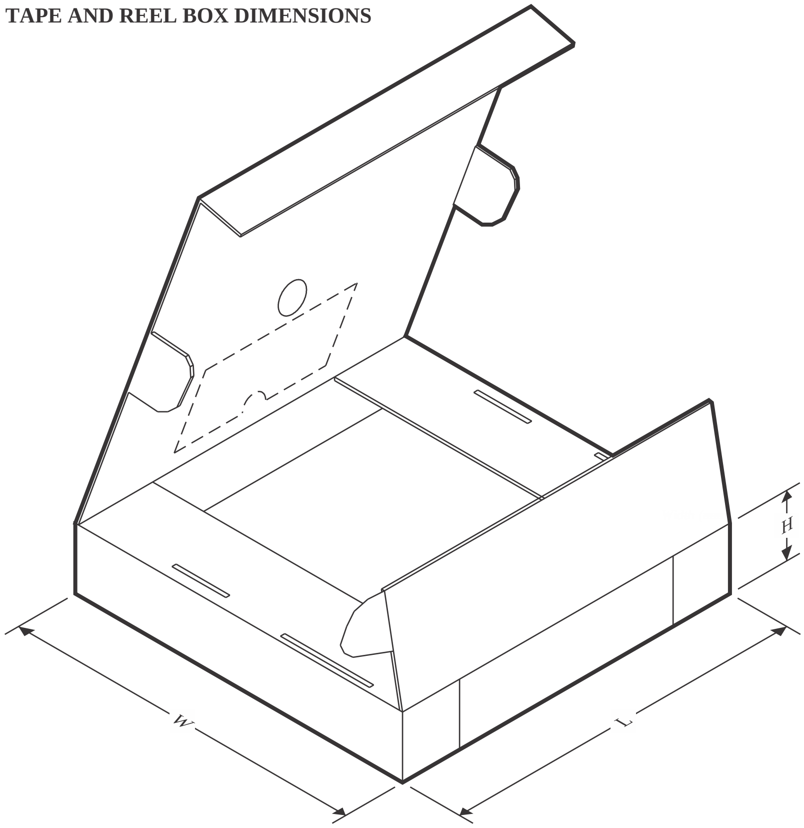
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

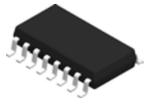
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AM26LV32IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26LV32INSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
AM26LV32INSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AM26LV32IDR	SOIC	D	16	2500	340.5	336.1	32.0
AM26LV32INSR	SOP	NS	16	2000	353.0	353.0	32.0
AM26LV32INSR	SOP	NS	16	2000	367.0	367.0	38.0

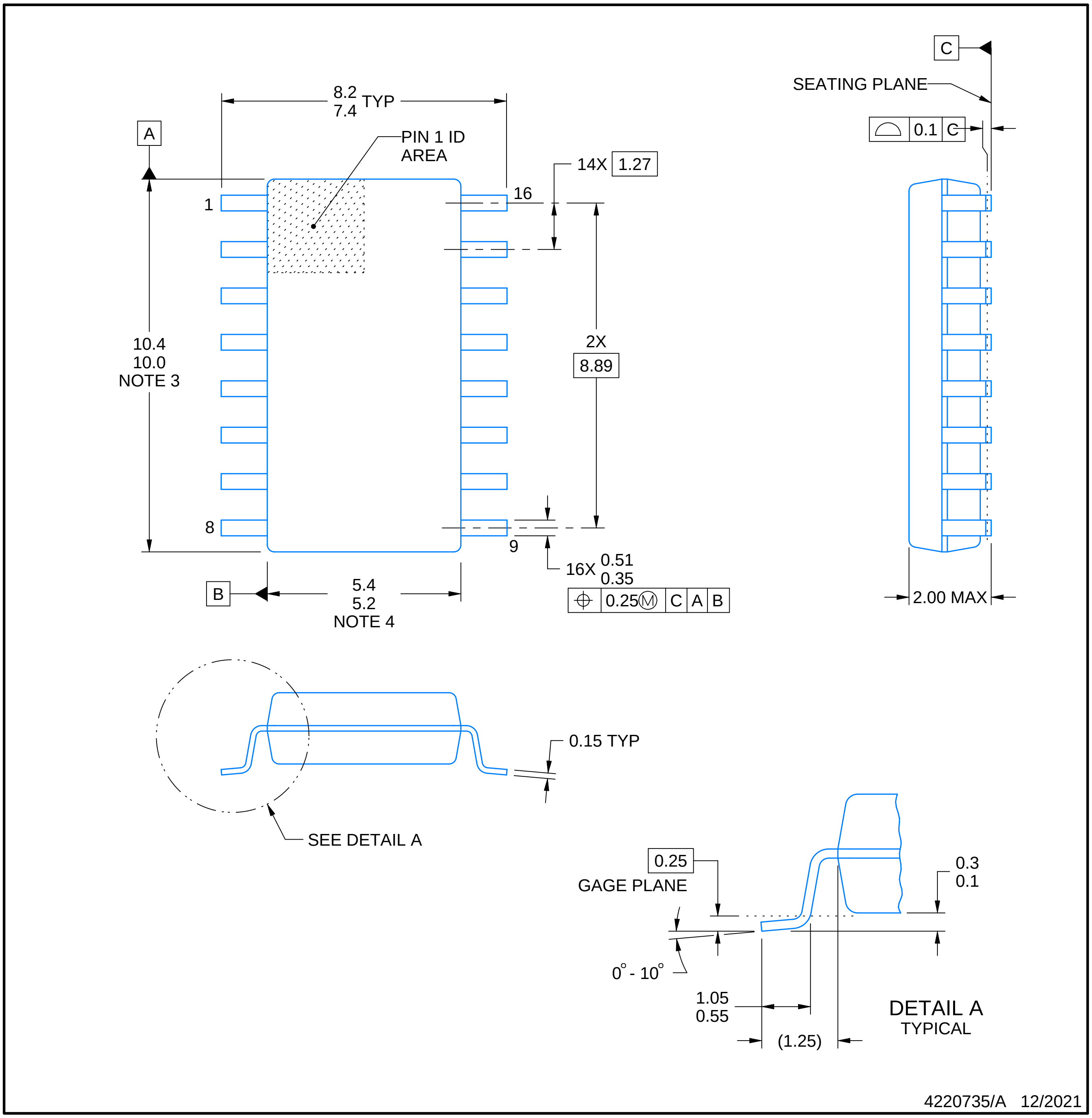


PACKAGE OUTLINE

NS0016A

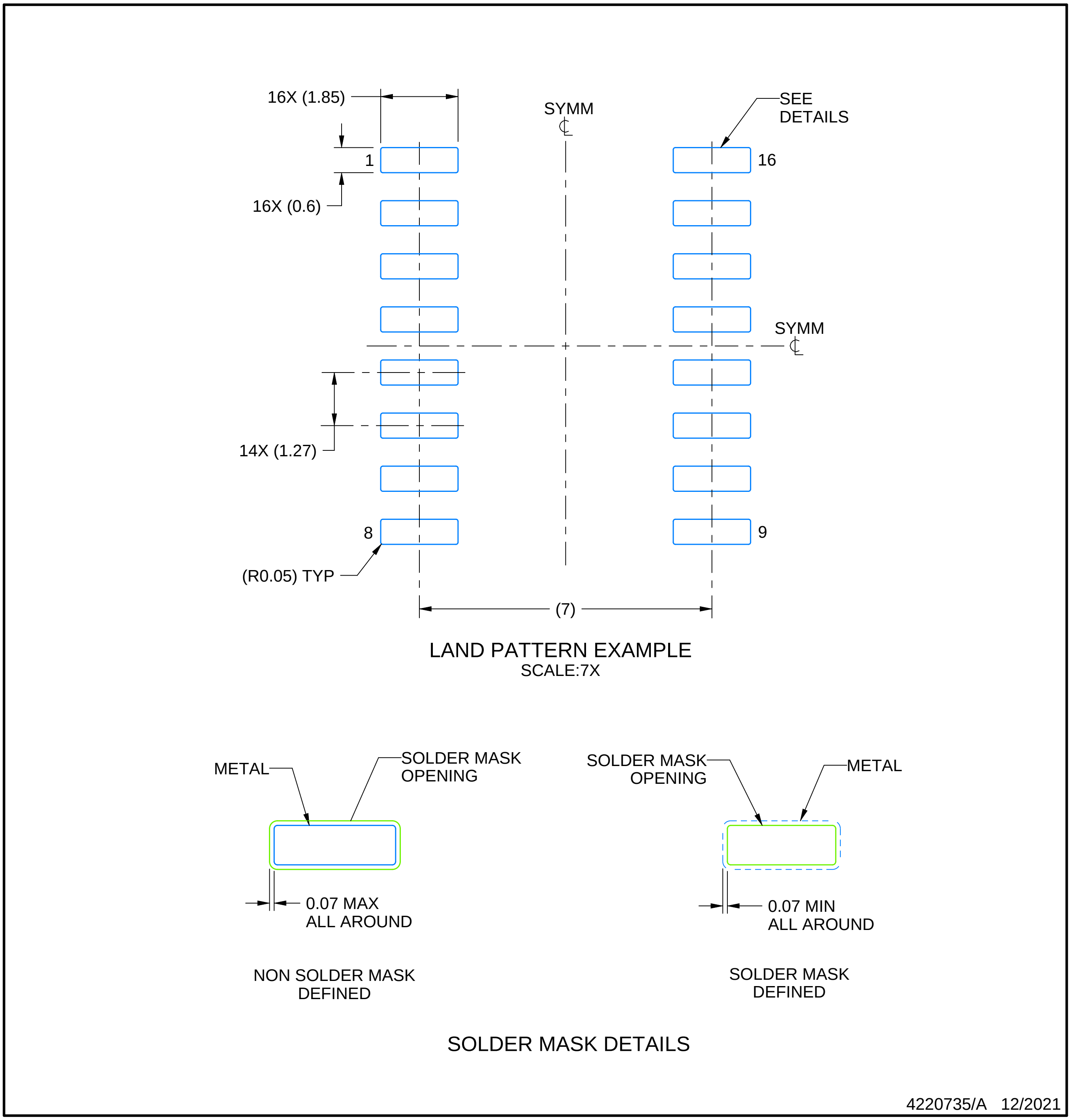
SOP - 2.00 mm max height

SOP



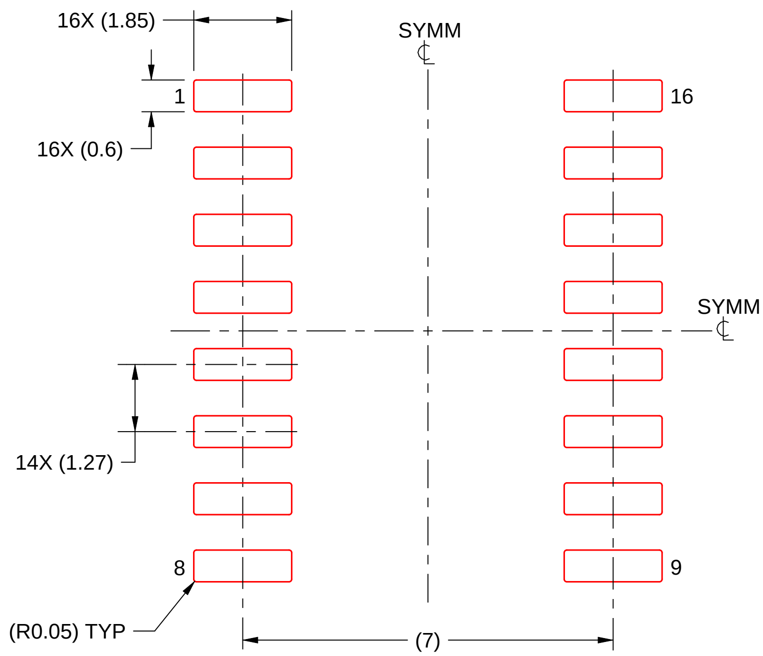
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



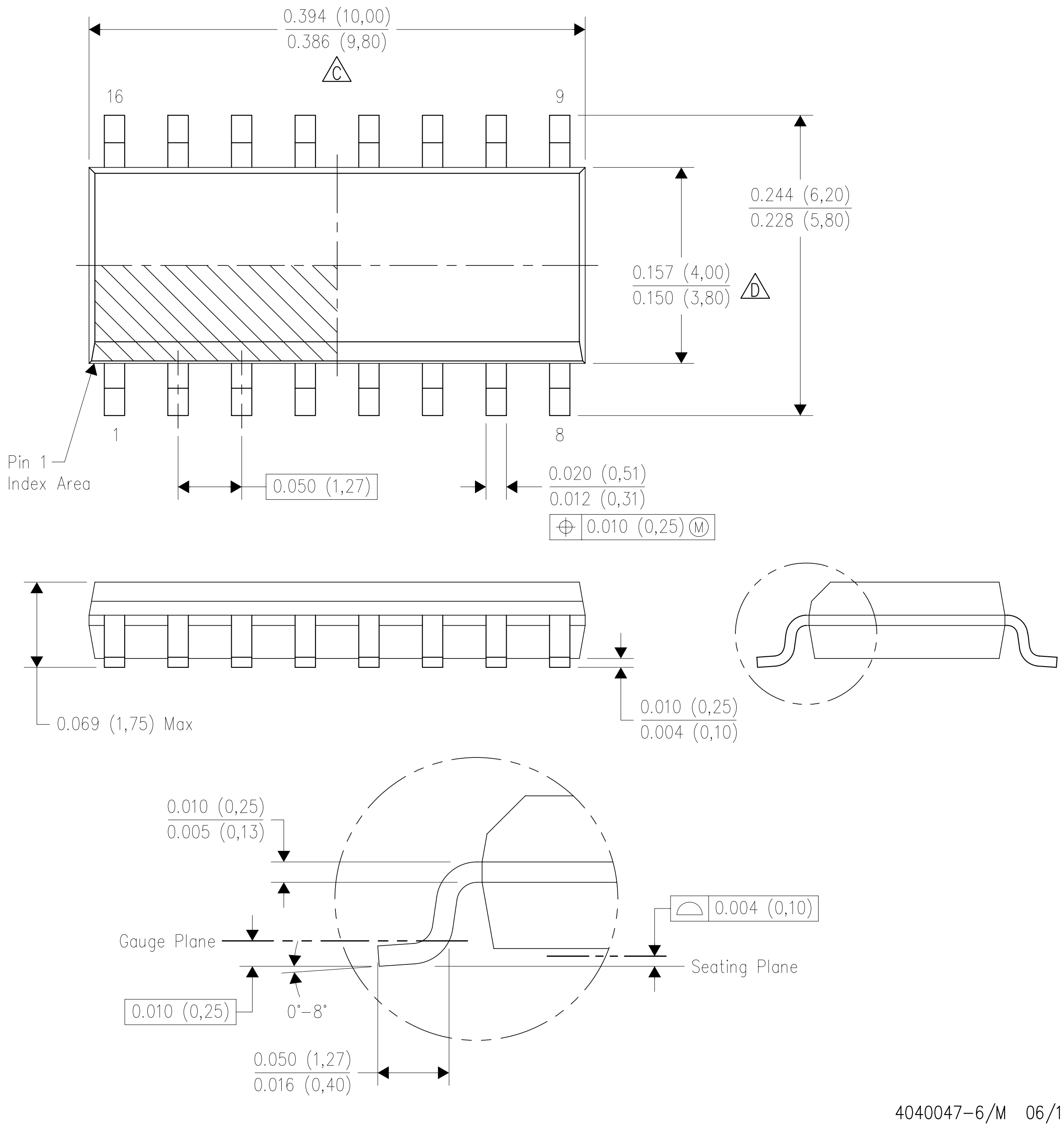
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

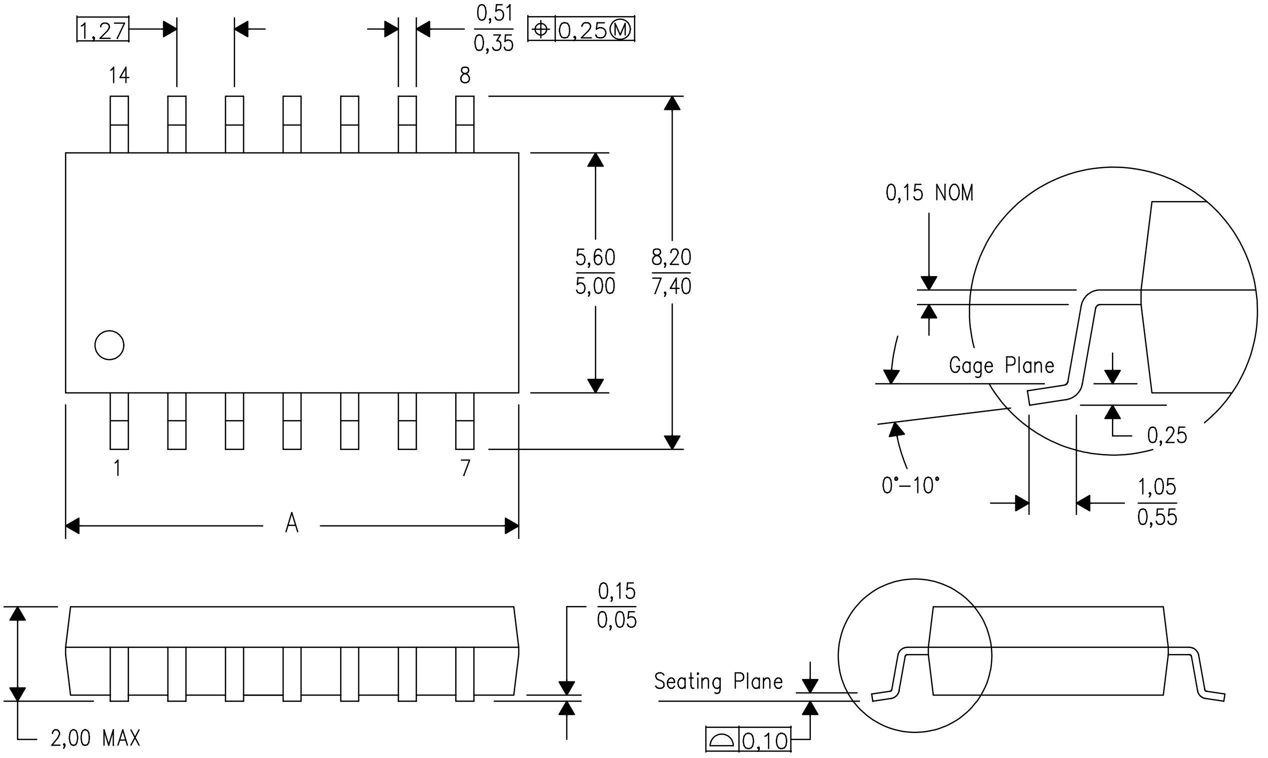
D (R-PDSO-G16) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



PINS ** / DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.