

- 150-mA Load Current Without External Power Transistor
- Adjustable Current-Limiting Capability
- Input Voltages up to 40 V
- Output Adjustable From 2 V to 37 V
- Direct Replacement for Fairchild μA723C

**description**

The μA723 is a precision integrated-circuit voltage regulator, featuring high ripple rejection, excellent input and load regulation, excellent temperature stability, and low standby current. The circuit consists of a temperature-compensated reference-voltage amplifier, an error amplifier, a 150-mA output transistor, and an adjustable-output current limiter.

The μA723 is designed for use in positive or negative power supplies as a series, shunt, switching, or floating regulator. For output currents exceeding 150 mA, additional pass elements can be connected as shown in Figures 4 and 5.

The μA723C is characterized for operation from 0°C to 70°C.

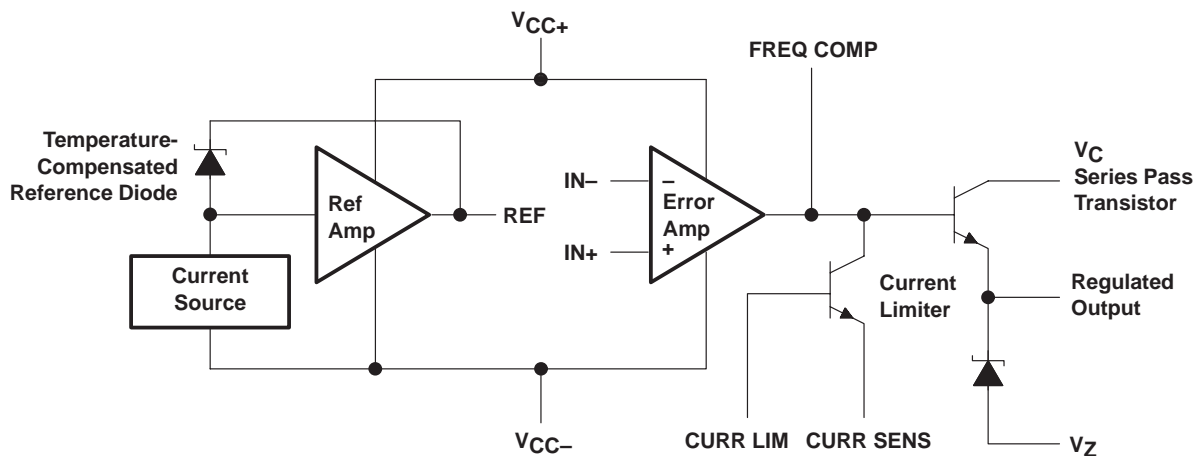


**AVAILABLE OPTIONS**

| T <sub>A</sub> | PACKAGED DEVICES |                   | CHIP FORM (Y) |
|----------------|------------------|-------------------|---------------|
|                | PLASTIC DIP (N)  | SMALL OUTLINE (D) |               |
| 0°C to 70°C    | μA723CN          | μA723CD           | μA723Y        |

The D package is available taped and reeled. Add the suffix R to the device type (e.g., μA723CDR). Chip forms are tested at 25°C.

**functional block diagram**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



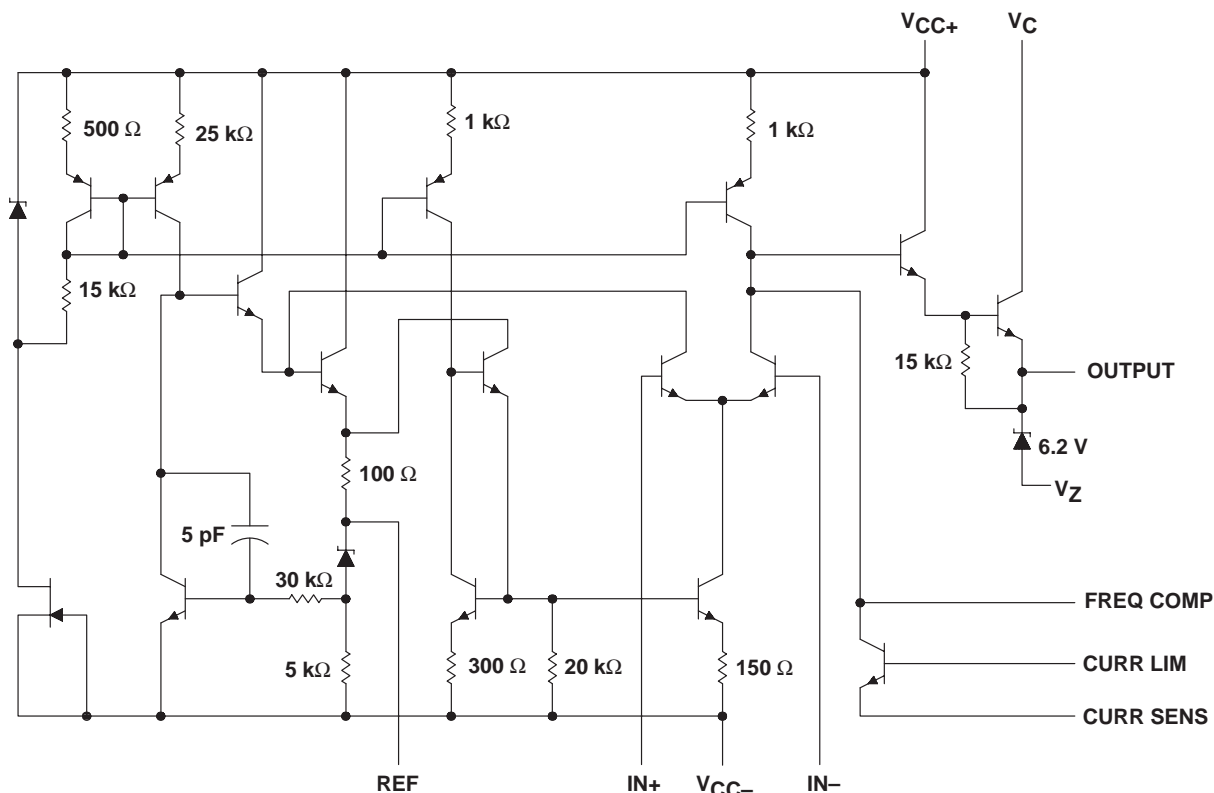
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# μA723 PRECISION VOLTAGE REGULATORS

SLVS057D – AUGUST 1972 – REVISED JULY 1999

## schematic



Resistor and capacitor values shown are nominal.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|  |                |
|--|----------------|
| Peak voltage from $V_{CC+}$ to $V_{CC-}$ ( $t_w \leq 50$ ms)                 | 50 V           |
| Continuous voltage from $V_{CC+}$ to $V_{CC-}$                               | 40 V           |
| Input-to-output voltage differential   | 40 V           |
| Differential input voltage to error amplifier                                | $\pm 5$ V      |
| Voltage between noninverting input and $V_{CC-}$                             | 8 V            |
| Current from $V_Z$   | 25 mA          |
| Current from REF   | 15 mA          |
| Package thermal impedance, $\theta_{JA}$ (see Notes 1 and 2): D package      | 86°C/W         |
| N package  | 101°C/W        |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package | 260°C          |
| Storage temperature range, $T_{stg}$   | -65°C to 150°C |

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Maximum power dissipation is a function of  $T_J(\max)$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(\max) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can impact reliability.  
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

**recommended operating conditions**

|   | MIN    | MAX | UNIT    |
|---|--------|-----|---------|
| Input voltage, $V_I$                              | 9.5    | 40  | V       |
| Output voltage, $V_O$                             | 2      | 37  | V       |
| Input-to-output voltage differential, $V_C - V_O$ | 3      | 38  | V       |
| Output current, $I_O$                             |        | 150 | mA      |
| Operating free-air temperature range, $T_A$       | μA723C |     | 0 70 °C |

**electrical characteristics at specified free-air temperature (see Notes 3 and 4)**

| PARAMETER                                 | TEST CONDITIONS   | $T_A$       | μA723C |       |       | UNIT |
|---|---|-------------|--------|-------|-------|------|
|   |   |             | MIN    | TYP   | MAX   |      |
| Input regulation                          | $V_I = 12\text{ V to }V_I = 15\text{ V}$                | 25°C        |        | 0.1   | 1     | mV/V |
|   | $V_I = 12\text{ V to }V_I = 40\text{ V}$                | 25°C        |        | 1     | 5     |      |
|   | $V_I = 12\text{ V to }V_I = 15\text{ V}$                | 0°C to 70°C |        |       | 3     |      |
| Ripple rejection                          | f = 50 Hz to 10 kHz, $C_{ref} = 0$                      | 25°C        |        | 74    |       | dB   |
|   | f = 50 Hz to 10 kHz, $C_{ref} = 5\text{ }\mu\text{F}$   | 25°C        |        | 86    |       |      |
| Output regulation                         |   | 25°C        |        | -0.3  | -2    | mV/V |
|   |   | 0°C to 70°C |        |       | -6    |      |
| Reference voltage, $V_{ref}$              |   | 25°C        | 6.8    | 7.15  | 7.5   | V    |
| Standby current                           | $V_I = 30\text{ V}, I_O = 0$                            | 25°C        |        | 2.3   | 4     | mA   |
| Temperature coefficient of output voltage |   | 0°C to 70°C |        | 0.003 | 0.015 | %/°C |
| Short-circuit output current              | $R_{SC} = 10\text{ }\Omega, V_O = 0$                    | 25°C        |        | 65    |       | mA   |
| Output noise voltage                      | BW = 100 Hz to 10 kHz, $C_{ref} = 0$                    | 25°C        |        | 20    |       | μV   |
|   | BW = 100 Hz to 10 kHz, $C_{ref} = 5\text{ }\mu\text{F}$ | 25°C        |        | 2.5   |       |      |

- NOTES: 3. For all values in this table, the device is connected as shown in Figure 1 with the divider resistance as seen by the error amplifier  $\leq 10\text{ k}\Omega$ . Unless otherwise specified,  $V_I = V_{CC+} = V_C = 12\text{ V}$ ,  $V_{CC-} = 0$ ,  $V_O = 5\text{ V}$ ,  $I_O = 1\text{ mA}$ ,  $R_{SC} = 0$ , and  $C_{ref} = 0$ .
4. Pulse-testing techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

**electrical characteristics,  $T_A = 25^\circ\text{C}$  (see Notes 3 and 4)**

| PARAMETER                    | TEST CONDITIONS   | μA723Y |      |     | UNIT |
|------------------------------|---|--------|------|-----|------|
|                              |   | MIN    | TYP  | MAX |      |
| Input regulation             | $V_I = 12\text{ V to }V_I = 15\text{ V}$                |        | 0.1  |     | mV/V |
|                              | $V_I = 12\text{ V to }V_I = 40\text{ V}$                |        | 1    |     |      |
| Ripple rejection             | f = 50 Hz to 10 kHz, $C_{ref} = 0$                      |        | 74   |     | dB   |
|                              | f = 50 Hz to 10 kHz, $C_{ref} = 5\text{ }\mu\text{F}$   |        | 86   |     |      |
| Output regulation            |   |        | -0.3 |     | mV/V |
| Reference voltage, $V_{ref}$ |   |        | 7.15 |     | V    |
| Standby current              | $V_I = 30\text{ V}, I_O = 0$                            |        | 2.3  |     | mA   |
| Short-circuit output current | $R_{SC} = 10\text{ }\Omega, V_O = 0$                    |        | 65   |     | mA   |
| Output noise voltage         | BW = 100 Hz to 10 kHz, $C_{ref} = 0$                    |        | 20   |     | μV   |
|                              | BW = 100 Hz to 10 kHz, $C_{ref} = 5\text{ }\mu\text{F}$ |        | 2.5  |     |      |

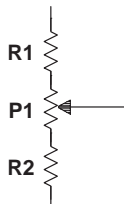
- NOTES: 3. For all values in this table, the device is connected as shown in Figure 1 with the divider resistance as seen by the error amplifier  $\leq 10\text{ k}\Omega$ . Unless otherwise specified,  $V_I = V_{CC+} = V_C = 12\text{ V}$ ,  $V_{CC-} = 0$ ,  $V_O = 5\text{ V}$ ,  $I_O = 1\text{ mA}$ ,  $R_{SC} = 0$ , and  $C_{ref} = 0$ .
4. Pulse-testing techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

**APPLICATION INFORMATION**

**Table 1. Resistor Values (kΩ) for Standard Output Voltages**

| OUTPUT VOLTAGE (V) | APPLICABLE FIGURES (SEE NOTE 5) | FIXED OUTPUT ±5% |         | OUTPUT ADJUSTABLE ±10% (SEE NOTE 6) |         |         |
|--------------------|---------------------------------|------------------|---------|-------------------------------------|---------|---------|
|                    |                                 | R1 (kΩ)          | R2 (kΩ) | R1 (kΩ)                             | P1 (kΩ) | P2 (kΩ) |
| 3.0                | 1, 5, 6, 9, 11, 12 (4)          | 4.12             | 3.01    | 1.8                                 | 0.5     | 1.2     |
| 3.6                | 1, 5, 6, 9, 11, 12 (4)          | 3.57             | 3.65    | 1.5                                 | 0.5     | 1.5     |
| 5.0                | 1, 5, 6, 9, 11, 12 (4)          | 2.15             | 4.99    | 0.75                                | 0.5     | 2.2     |
| 6.0                | 1, 5, 6, 9, 11, 12 (4)          | 1.15             | 6.04    | 0.5                                 | 0.5     | 2.7     |
| 9.0                | 2, 4, (5, 6, 9, 12)             | 1.87             | 7.15    | 0.75                                | 1.0     | 2.7     |
| 12                 | 2, 4, (5, 6, 9, 12)             | 4.87             | 7.15    | 2.0                                 | 1.0     | 3.0     |
| 15                 | 2, 4, (5, 6, 9, 12)             | 7.87             | 7.15    | 3.3                                 | 1.0     | 3.0     |
| 28                 | 2, 4, (5, 6, 9, 12)             | 21.0             | 7.15    | 5.6                                 | 1.0     | 2.0     |
| 45                 | 7                               | 3.57             | 48.7    | 2.2                                 | 10      | 39      |
| 75                 | 7                               | 3.57             | 78.7    | 2.2                                 | 10      | 68      |
| 100                | 7                               | 3.57             | 105     | 2.2                                 | 10      | 91      |
| 250                | 7                               | 3.57             | 255     | 2.2                                 | 10      | 240     |
| -6 (see Note 7)    | 3, 10                           | 3.57             | 2.43    | 1.2                                 | 0.5     | 0.75    |
| -9                 | 3, 10                           | 3.48             | 5.36    | 1.2                                 | 0.5     | 2.0     |
| -12                | 3, 10                           | 3.57             | 8.45    | 1.2                                 | 0.5     | 3.3     |
| -15                | 3, 10                           | 3.57             | 11.5    | 1.2                                 | 0.5     | 4.3     |
| -28                | 3, 10                           | 3.57             | 24.3    | 1.2                                 | 0.5     | 10      |
| -45                | 8                               | 3.57             | 41.2    | 2.2                                 | 10      | 33      |
| -100               | 8                               | 3.57             | 95.3    | 2.2                                 | 10      | 91      |
| -250               | 8                               | 3.57             | 249     | 2.2                                 | 10      | 240     |

- NOTES: 5. The R1/R2 divider can be across either  $V_O$  or  $V_{(ref)}$ . If the divider is across  $V_{(ref)}$ , use the figure numbers without parentheses. If the divider is across  $V_O$ , use the figure numbers in parentheses.  
 6. To make the voltage adjustable, the R1/R2 divider shown in the figures must be replaced by the divider shown below.



**Adjustable Output Circuit**

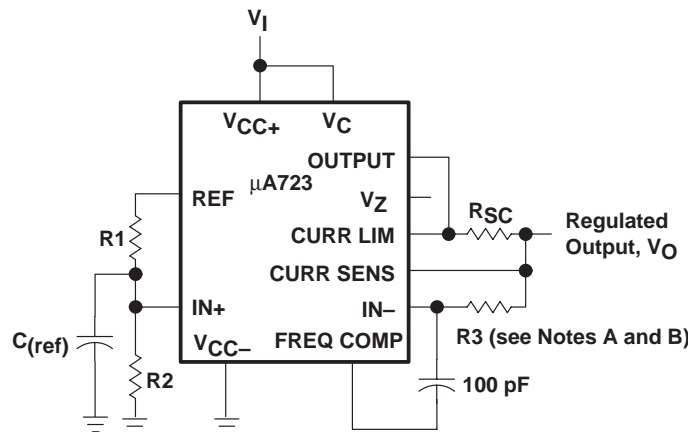
7. For Figures 3, 8, and 10, the device requires a minimum of 9V between  $V_{CC+}$  and  $V_{CC-}$  when  $V_O$  is equal to or more positive than -9 V.

**APPLICATION INFORMATION**

**Table 2. Formulas for Intermediate Output Voltages**

| OUTPUTS FROM 2 V TO 7 V<br>SEE FIGURES 1, 5, 6, 9, 11, 12 (4)<br>AND NOTE 5   | OUTPUTS FROM 4 V TO 250 V<br>SEE FIGURE 7 AND NOTE 5                     | CURRENT LIMITING  |
|---|--|---|
| $V_O = V_{(ref)} \times \frac{R_2}{R_1 + R_2}$                                | $V_O = \frac{V_{(ref)}}{2} \times \frac{R_2 - R_1}{R_1}$<br>$R_3 = R_4$  | $I_{(limit)} \approx \frac{0.65 \text{ V}}{R_{SC}}$   |
| OUTPUTS FROM 7 V TO 37 V<br>SEE FIGURES 2, 4, (5, 6, 9, 11, 12)<br>AND NOTE 5 | OUTPUTS FROM -6 V TO -250 V<br>SEE FIGURES 3, 8, 10<br>AND NOTES 5 AND 7 | FOLDBACK CURRENT LIMITING<br>SEE FIGURE 6   |
| $V_O = V_{(ref)} \times \frac{R_1 + R_2}{R_2}$                                | $V_O = -\frac{V_{(ref)}}{2} \times \frac{R_1 + R_2}{R_1}$<br>$R_3 = R_4$ | $I_{(knee)} \approx \frac{V_O R_3 + (R_3 + R_4) 0.65 \text{ V}}{R_{SC} R_4}$<br>$I_{OS} \approx \frac{0.65 \text{ V}}{R_{SC}} \times \frac{R_3 + R_4}{R_4}$ |

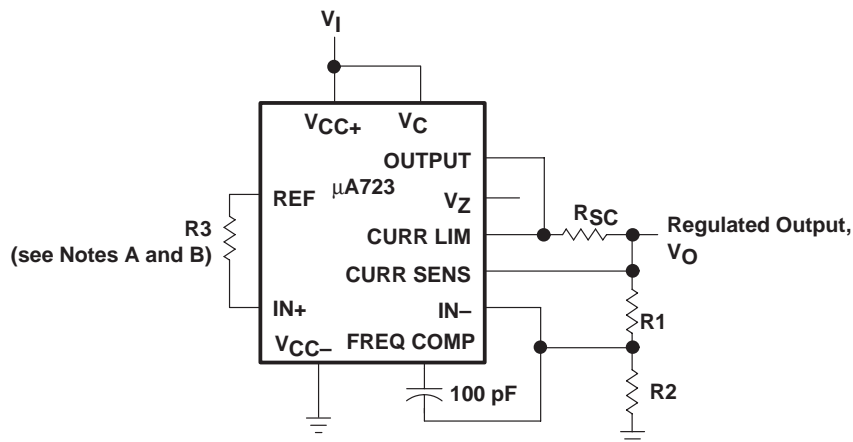
- NOTES: 5. The R1/R2 divider can be across either  $V_O$  or  $V_{(ref)}$ . If the divider is across  $V_{(ref)}$ , use figure numbers without parentheses. If the divider is across  $V_O$ , use the figure numbers in parentheses.
7. For Figures 3, 8, and 10, the device requires a minimum of 9 V between  $V_{CC+}$  and  $V_{CC-}$  when  $V_O$  is equal to or more positive than -9 V.



- NOTES: A.  $R_3 = \frac{R_1 \times R_2}{R_1 + R_2}$  for a minimum  $\alpha_{V_O}$
- B.  $R_3$  can be eliminated for minimum component count. Use direct connection (i.e.,  $R_3 = 0$ ).

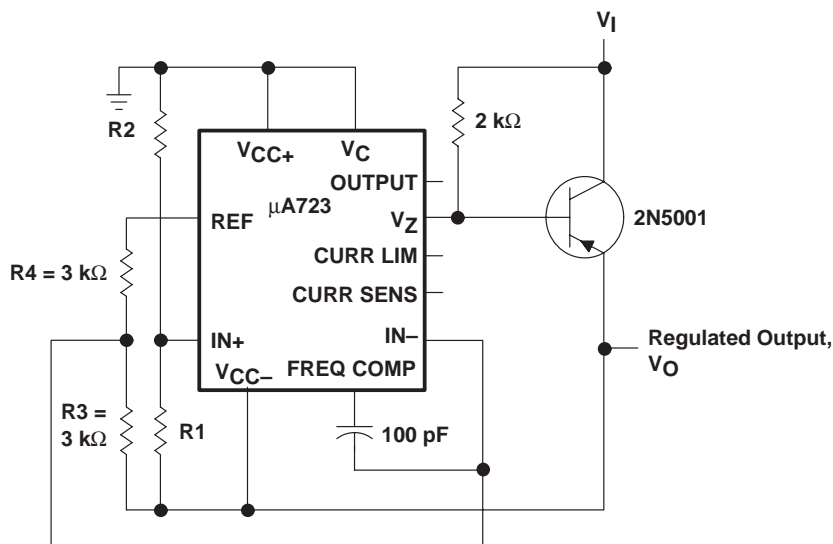
**Figure 1. Basic Low-Voltage Regulator ( $V_O = 2 \text{ V to } 7 \text{ V}$ )**

**APPLICATION INFORMATION**



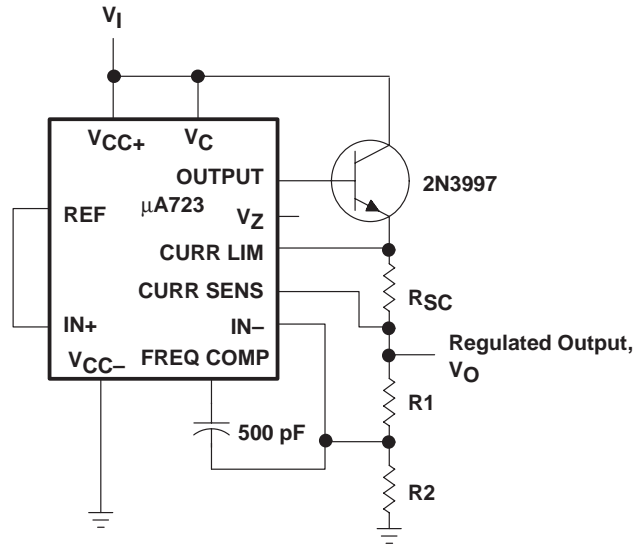
- NOTES: A.  $R_3 = \frac{R_1 \times R_2}{R_1 + R_2}$  for a minimum  $\alpha_{V_O}$   
 B.  $R_3$  can be eliminated for minimum component count. Use direct connection (i.e.,  $R_3 = 0$ ).

**Figure 2. Basic High-Voltage Regulator ( $V_O = 7\text{ V to }37\text{ V}$ )**



**Figure 3. Negative-Voltage Regulator**

**APPLICATION INFORMATION**

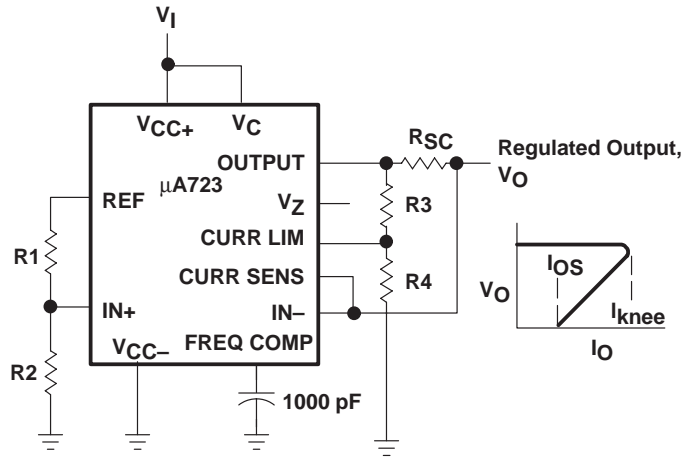


**Figure 4. Positive-Voltage Regulator (External npn Pass Transistor)**

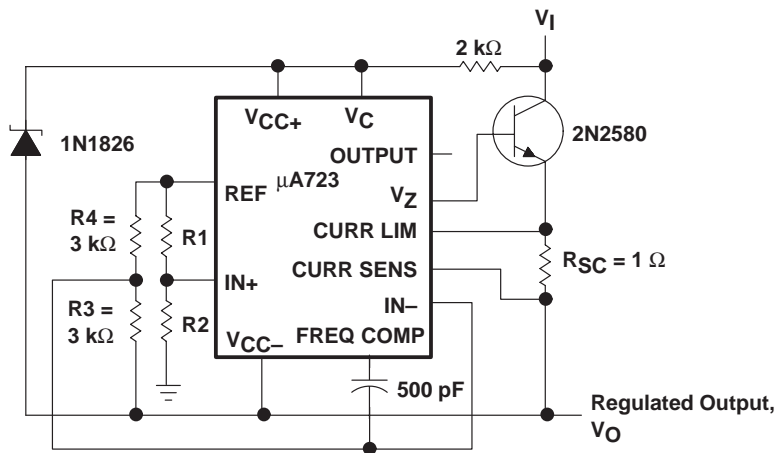


**Figure 5. Positive-Voltage Regulator (External pnp Pass Transistor)**

**APPLICATION INFORMATION**



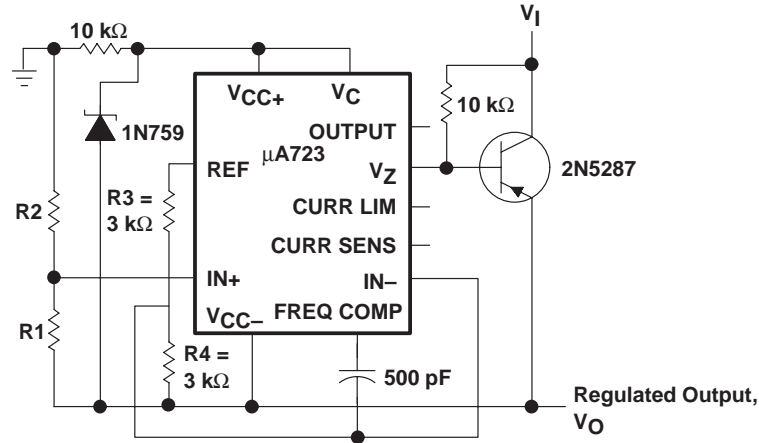
**Figure 6. Foldback Current Limiting**



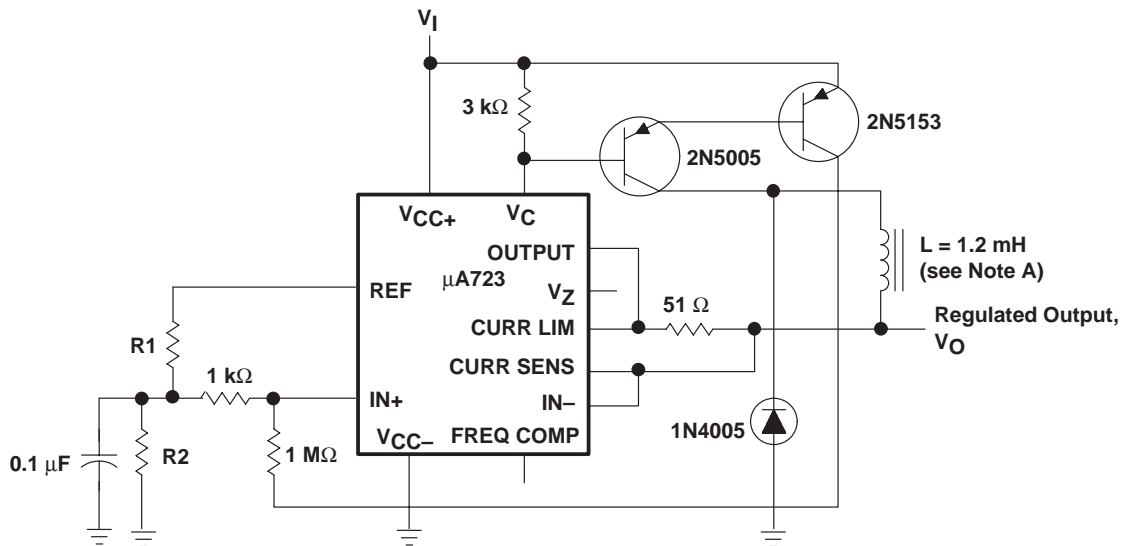
**Figure 7. Positive Floating Regulator**



**APPLICATION INFORMATION**



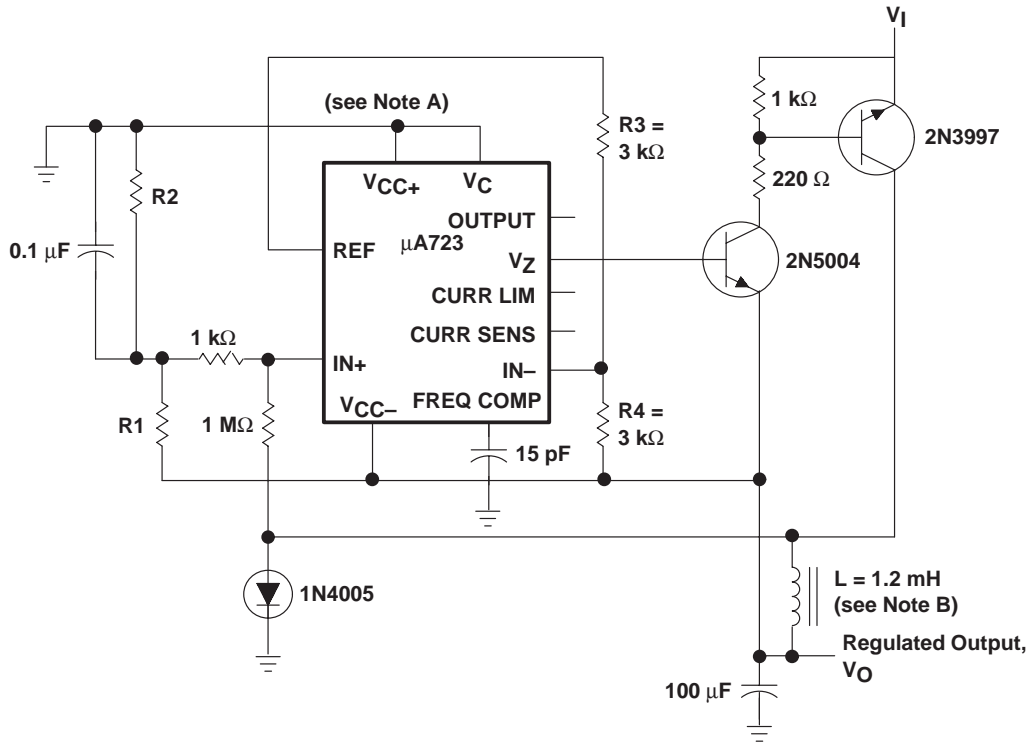
**Figure 8. Negative Floating Regulator**



NOTE A: L is 40 turns of No. 20 enameled copper wire wound on Ferroxcube P36/22-3B7 potted core, or equivalent, with a 0.009-inch air gap.

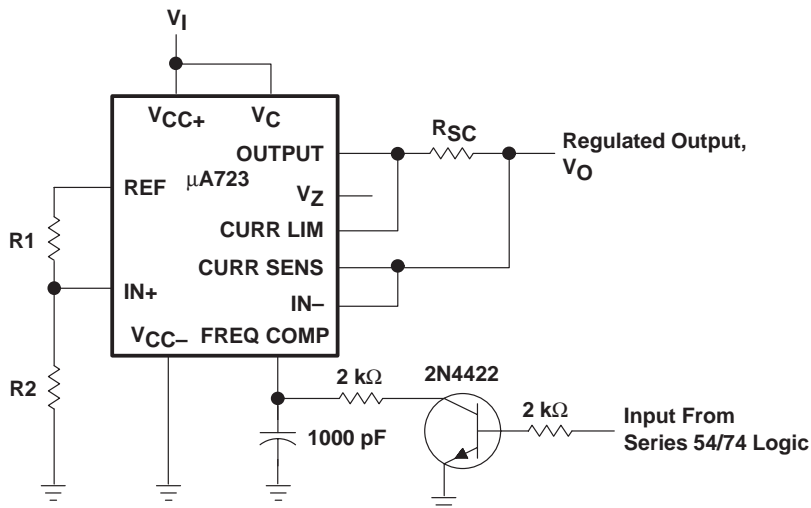
**Figure 9. Positive Switching Regulator**

**APPLICATION INFORMATION**



- NOTES: A. The device requires a minimum of 9 V between  $V_{CC+}$  and  $V_{CC-}$  when  $V_O$  is equal to or more positive than  $-9$  V.  
 B. L is 40 turns of No. 20 enameled copper wire wound on Ferroxcube P36/22-3B7 potted core, or equivalent, with a 0.009-inch air gap.

**Figure 10. Negative Switching Regulator**



NOTE A: A current-limiting transistor can be used for shutdown if current limiting is not required.

**Figure 11. Remote Shutdown Regulator With Current Limiting**

APPLICATION INFORMATION



Figure 12. Shunt Regulator

**PACKAGING INFORMATION**

| Orderable part number | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| UA723CD               | Active        | Production           | SOIC (D)   14  | 50   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | UA723C              |
| UA723CDR              | Active        | Production           | SOIC (D)   14  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | UA723C              |
| UA723CN               | Active        | Production           | PDIP (N)   14  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | UA723CN             |
| UA723CNSR             | Active        | Production           | SOP (NS)   14  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | UA723               |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device    | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| UA723CDR  | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| UA723CNSR | SOP          | NS              | 14   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device    | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------|--------------|-----------------|------|------|-------------|------------|-------------|
| UA723CDR  | SOIC         | D               | 14   | 2500 | 356.0       | 356.0      | 35.0        |
| UA723CNSR | SOP          | NS              | 14   | 2000 | 356.0       | 356.0      | 35.0        |

**TUBE**


\*All dimensions are nominal

| Device    | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------|--------------|--------------|------|-----|--------|--------|--------|--------|
| UA723CD   | D            | SOIC         | 14   | 50  | 506.6  | 8      | 3940   | 4.32   |
| UA723CDE4 | D            | SOIC         | 14   | 50  | 506.6  | 8      | 3940   | 4.32   |
| UA723CN   | N            | PDIP         | 14   | 25  | 506    | 13.97  | 11230  | 4.32   |
| UA723CNE4 | N            | PDIP         | 14   | 25  | 506    | 13.97  | 11230  | 4.32   |



# D0014A

# PACKAGE OUTLINE

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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