

LP3982 Micropower, Ultra-Low-Dropout, Low-Noise, 300-mA CMOS Regulator

1 Features

- 2.5-V to 6-V Input Range
- MAX8860 Pin, Package, and Specification Compatible
- 300-mA Output Current
- 120-mV Typical Dropout at 300 mA
- 90- μ A Typical Quiescent Current
- 1-nA Typical Shutdown Mode
- 60-dB Typical PSRR
- 120- μ s Typical Turnon Time
- Stable With Small Ceramic Output Capacitors
- 37- μ V_{RMS} Output Voltage Noise (10 Hz to 100 kHz)
- Overtemperature/Overcurrent Protection
- $\pm 2\%$ Output Voltage Tolerance
- Create a Custom Design Using the LP3982 With the [WEBENCH® Power Designer](#)

2 Applications

- Wireless Handsets
- DSP Core Power
- Battery Powered Electronics
- Portable Information Appliances

3 Description

The LP3982 low-dropout (LDO) CMOS linear regulator is available in 1.8-V, 2.5-V, 2.82-V, 3-V, 3.3-V, and adjustable versions. They deliver 300 mA of output current. Packaged in an 8-pin VSSOP, the LP3982 is pin- and package-compatible with Maxim's MAX8860. The LM3982 is also available in the small footprint WSON package.

The LP3982 suits battery-powered applications because of its shutdown mode (1 nA typical), low quiescent current (90 μ A typical), and LDO voltage (120 mV typical). The low dropout voltage allows for more utilization of a battery's available energy by operating closer to its end-of-life voltage. The LP3982 device's PMOS output transistor consumes relatively no drive current compared to PNP LDO regulators.

This PMOS regulator is stable with small ceramic capacitive loads (2.2 μ F typical).

These devices also include regulation fault detection, a bandgap voltage reference, constant current limiting, and thermal-overload protection.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP3982	WSON (8)	2.50 mm \times 3.00 mm
	VSSOP (8)	3.00 mm \times 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Application Circuit (Fixed V_{OUT} Version)

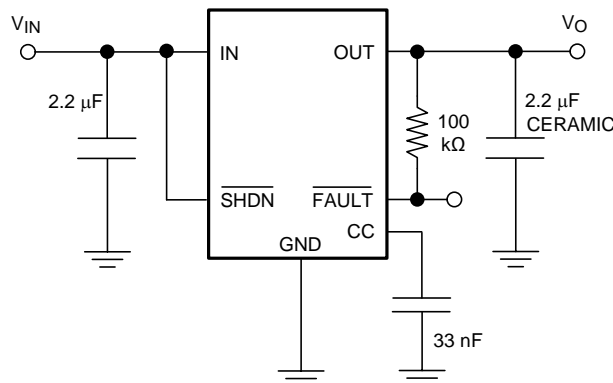


Table of Contents

1 Features	1	8 Application and Implementation	11
2 Applications	1	8.1 Application Information.....	11
3 Description	1	8.2 Typical Application	11
4 Revision History	2	9 Power Supply Recommendations	16
5 Pin Configuration and Functions	3	10 Layout	17
6 Specifications	4	10.1 Layout Guidelines	17
6.1 Absolute Maximum Ratings	4	10.2 Layout Example	17
6.2 ESD Ratings.....	4	10.3 WSON Mounting	17
6.3 Recommended Operating Conditions.....	4	11 Device and Documentation Support	18
6.4 Thermal Information	4	11.1 Documentation Support	18
6.5 Electrical Characteristics.....	5	11.2 Receiving Notification of Documentation Updates	18
6.6 Typical Characteristics	7	11.3 Community Resources.....	18
7 Detailed Description	9	11.4 Trademarks	18
7.1 Overview	9	11.5 Electrostatic Discharge Caution.....	18
7.2 Functional Block Diagram	9	11.6 Glossary	19
7.3 Feature Description.....	9	12 Mechanical, Packaging, and Orderable	
7.4 Device Functional Modes.....	10	Information	19

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (October 2015) to Revision F Page

- Added links for Webench and changed top navigator icon for TI Designs **1**

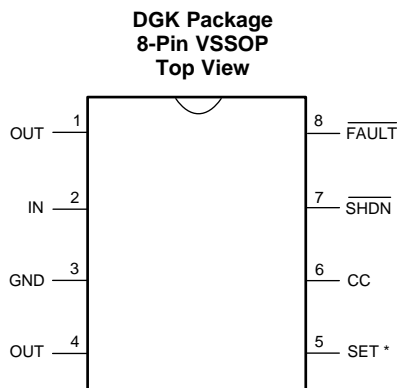
Changes from Revision D (April 2013) to Revision E Page

- Added *Device Information* and *Pin Configuration and Functions* sections, *ESD Ratings* table, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections; update *Thermal Information*... **1**
- Deleted lead temperature from Abs Max table (in POA); revised wording for footnote 4 **4**

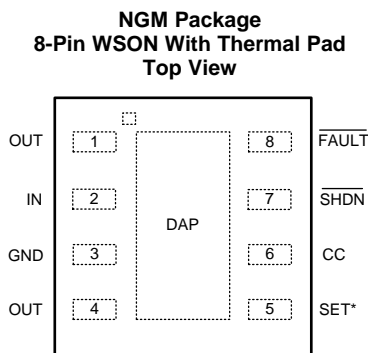
Changes from Revision C (April 2013) to Revision D Page

- Changed layout of National Data Sheet to TI format **9**

5 Pin Configuration and Functions



The SET pin is internally disconnected for the fixed versions.



The SET pin is internally disconnected for the fixed versions.

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CC	6	—	Connect a capacitor between CC pin and ground to reduce the output noise. The optimum value for CC is 33 nF.
FAULT	8	Output	FAULT pin goes low during out of regulation conditions like current limit and thermal shutdown, or when it approaches dropout. Requires a pullup resistor because it is an active-low, open-drain output.
GND	3	Ground	Ground
IN	2	Input	This is the input supply voltage to the regulator.
OUT	1, 4	Output	Regulated output voltage
SET	5	Input	In the adjustable version a resistor divider connected to this pin sets the output voltage. The SET pin is internally disconnected for the fixed versions.
SHDN	7	Input	The SHDN pin allows the part to be turned to an ON or OFF state by pulling SHDN pin high or low.
DAP	√	—	WSON Only - The DAP (Die Attached Pad) is an exposed pad that does not have an internal connection; it functions as a thermal relief when soldered to a copper plane. It is recommend that the DAP be connected to GND. See WSON Mounting section for more information.

6 Specifications

6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾⁽³⁾

	MIN	MAX	UNIT
V_{IN} , V_{OUT} , V_{SHDN} , V_{SET} , V_{CC} , V_{FAULT}	−0.3	6.5	V
Fault sink current		20	mA
Power dissipation	See ⁽⁴⁾		
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	−65	160	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to the potential at the GND pin.
- (3) If Military/Aerospace-specified devices are required, contact Texas Instruments Sales Office/Distributors for availability and specifications.
- (4) In applications where high power dissipation and/or poor thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(MAX)}$) is dependant on the maximum operating junction temperature ($T_{J(MAX-OP)}$), the maximum power dissipation ($P_{D(MAX)}$), and the junction-to-ambient thermal resistance in the application ($R_{\theta JA}$). This relationship is given by: $T_{A(MAX)} = T_{J(MAX-OP)} - (P_{D(MAX)} \times R_{\theta JA})$. The value of the $R_{\theta JA}$ for the WSON package is specifically dependent on the PCB trace area, trace material, and the number of layers and thermal vias. For improved thermal resistance and power dissipation for the WSON package, refer to TI Application Note AN-1187 *Leadless Leadframe Package (LLP)* ([SNOA401](#)).

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
	Machine model	±200	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions⁽¹⁾⁽²⁾

	MIN	NOM	MAX	UNIT
Operating temperature	−40		85	°C
Supply voltage	2.5		6	V

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to the potential at the GND pin.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LP3982		UNIT
		DGK (VSSOP)	NGM (WSON) ⁽²⁾	
		8 PINS	8 PINS	
$R_{\theta JA}$ ⁽³⁾	Junction-to-ambient thermal resistance, High-K	175.2	52.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.0	66.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	95.6	16.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	9.7	1.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	94.2	16.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	11.1	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.
- (2) The PCB for the WSON/NGM package $R_{\theta JA}$ includes thermal vias under the exposed thermal pad per EIA/JEDEC JESD51-5.
- (3) Thermal resistance value $R_{\theta JA}$ is based on the EIA/JEDEC High-K printed circuit board defined by: JESD51-7 - High Effective Thermal Conductivity Test Board for Leadless Surface Mount Packages.

6.5 Electrical Characteristics

Unless otherwise specified, all limits are specified for $V_{IN} = V_{OUT} + 0.5\text{ V}^{(1)}$, $\overline{V_{SHDN}} = V_{IN}$, $C_{IN} = C_{OUT} = 2.2\text{ }\mu\text{F}$, $C_{CC} = 33\text{ nF}$, $T_J = 25^\circ\text{C}$.

PARAMETER		TEST CONDITIONS	MIN ⁽²⁾	TYP ⁽³⁾	MAX ⁽²⁾	UNIT
V_{IN}	Input voltage	For operating temperature extremes: –40°C to 85°C	2.5		6	V
ΔV_{OUT}	Output voltage tolerance	100 $\mu\text{A} \leq I_{OUT} \leq 300\text{ mA}$ $V_{IN} = V_{OUT} + 0.5\text{ V}^{(1)}$ SET = OUT for the ADJ Versions	–2		2	% of V_{OUT} (NOM)
		For operating temperature extremes: –40°C to 85°C	–3		3	
V_{OUT}	Output adjust range	ADJ version only; for operating temperature extremes: –40°C to 85°C	1.25		6	V
I_{OUT}	Maximum output current	Average DC current rating; For operating temperature extremes: –40°C and 85°C	300			mA
I_{LIMIT}	Output current limit			770		mA
		For operating temperature extremes: –40°C to 85°C	330			
I_Q	Supply current	$I_{OUT} = 0\text{ mA}$		90		μA
		$I_{OUT} = 0\text{ mA}$; for operating temperature extremes: –40°C to 85°C			270	
		$I_{OUT} = 300\text{ mA}$		225		
	Shutdown supply current	$V_O = 0\text{ V}$, $\overline{SHDN} = \text{GND}$		0.001	1	μA
V_{DO}	Dropout voltage ⁽¹⁾⁽⁴⁾	$I_{OUT} = 1\text{ mA}$		0.4		mV
		$I_{OUT} = 200\text{ mA}$		80		
		$I_{OUT} = 200\text{ mA}$; for operating temperature extremes: –40°C to 85°C			220	
		$I_{OUT} = 300\text{ mA}$		120		
ΔV_{OUT}	Line regulation	$I_{OUT} = 1\text{ mA}$, ($V_{OUT} + 0.5\text{ V}$) $\leq V_I \leq 6\text{ V}^{(1)}$		0.01		% / V
		$I_{OUT} = 1\text{ mA}$, ($V_{OUT} + 0.5\text{ V}$) $\leq V_I \leq 6\text{ V}^{(1)}$; for operating temperature extremes: –40°C to 85°C	–0.1		0.1	
	Load regulation	100 $\mu\text{A} \leq I_{OUT} \leq 300\text{ mA}$		0.002		% / mA
e_n	Output voltage noise	$I_{OUT} = 10\text{ mA}$, 10 Hz $\leq f \leq 100\text{ kHz}$		37		μV_{RMS}
	Output voltage noise density	10 Hz $\leq f \leq 100\text{ kHz}$, $C_{OUT} = 10\text{ }\mu\text{F}$		190		nV / $\sqrt{\text{Hz}}$
V_{SHDN}	\overline{SHDN} input threshold	V_{IH} , ($V_{OUT} + 0.5\text{ V}$) $\leq V_{IN} \leq 6\text{ V}^{(1)}$; for operating temperature extremes: –40°C to 85°C	2			V
		V_{IL} , ($V_{OUT} + 0.5\text{ V}$) $\leq V_{IN} \leq 6\text{ V}^{(1)}$; for operating temperature extremes: –40°C to 85°C			0.4	
I_{SHDN}	\overline{SHDN} input bias current	$\overline{SHDN} = \text{GND}$ or IN		0.1	100	nA
I_{SET}	SET input leakage	SET = 1.3 V, ADJ version only ⁽⁵⁾		0.1	2.5	nA

(1) Condition does not apply to input voltages below 2.5 V because this is the minimum input operating voltage.

(2) All limits are verified by testing or statistical analysis.

(3) Typical values represent the most likely parametric norm.

(4) Dropout voltage is measured by reducing V_{IN} until V_{OUT} drops 100 mV from its nominal value at $V_{IN} - V_{OUT} = 0.5\text{ V}$. Dropout voltage does not apply to the 1.8-V version.

(5) The SET pin is not externally connected for the fixed versions.

LP3982

SNVS185F –FEBRUARY 2002–REVISED APRIL 2017

www.ti.com
Electrical Characteristics (continued)

Unless otherwise specified, all limits are specified for $V_{IN} = V_{OUT} + 0.5 \text{ V}^{(1)}$, $V_{SHDN} = V_{IN}$, $C_{IN} = C_{OUT} = 2.2 \mu\text{F}$, $C_{CC} = 33 \text{ nF}$, $T_J = 25^\circ\text{C}$.

PARAMETER		TEST CONDITIONS	MIN ⁽²⁾	TYP ⁽³⁾	MAX ⁽²⁾	UNIT
V _{FAULT}	FAULT detection voltage	V _O ≥ 2.5 V, I _{OUT} = 200 mA ⁽⁶⁾	120			mV
		V _{OUT} ≥ 2.5 V, I _{OUT} = 200 mA ⁽⁶⁾ ; for operating temperature extremes: -40°C to 85°C	280			
	FAULT output low voltage	I _{SINK} = 2 mA	0.115			V
		I _{SINK} = 2 mA; for operating temperature extremes: -40°C to 85°C	0.25			
I _{FAULT}	FAULT off-leakage current	FAULT = 3.6 V, SHDN = 0 V		0.1	100	nA
T _{SD}	Thermal shutdown temperature			160		°C
	Thermal shutdown hysteresis			10		
T _{ON}	Start-up time	C _{OUT} = 10 μF, V _{OUT} at 90% of final value		120		μs

(6) The $\overline{\text{FAULT}}$ detection voltage is specified for the input-to-output voltage differential at which the $\overline{\text{FAULT}}$ pin goes active low.

6.6 Typical Characteristics

Unless otherwise specified, $V_{IN} = V_O + 0.5\text{ V}$, $C_{IN} = C_{OUT} = 2.2\text{ }\mu\text{F}$, $C_{CC} = 33\text{ nF}$, $T_J = 25^\circ\text{C}$, $V_{SHDN} = V_{IN}$.

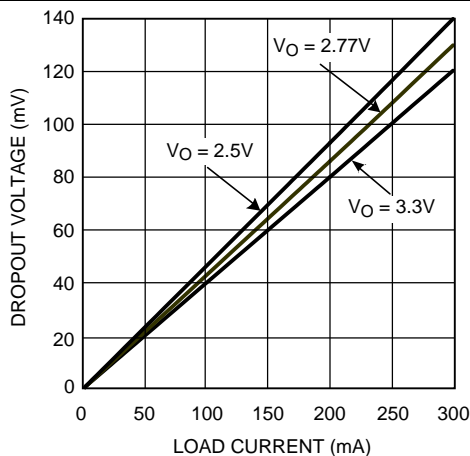


Figure 1. Dropout Voltage vs Load Current (for Different Output Voltages)

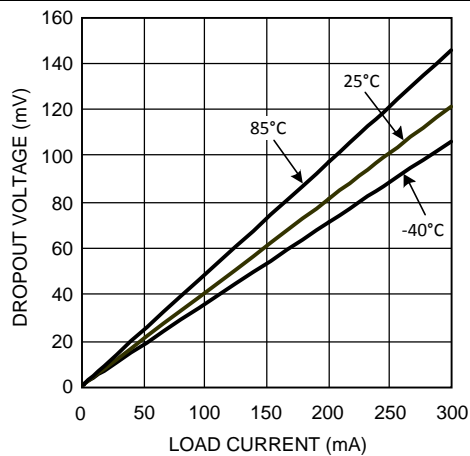


Figure 2. Dropout Voltage vs Load Current (for Different Output Temperatures)

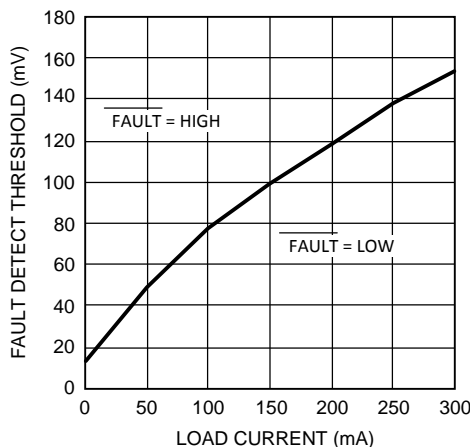


Figure 3. FAULT Detect Threshold vs Load Current

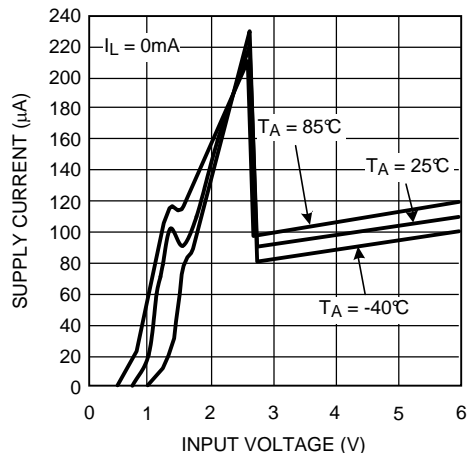


Figure 4. Supply Current vs Input Voltage

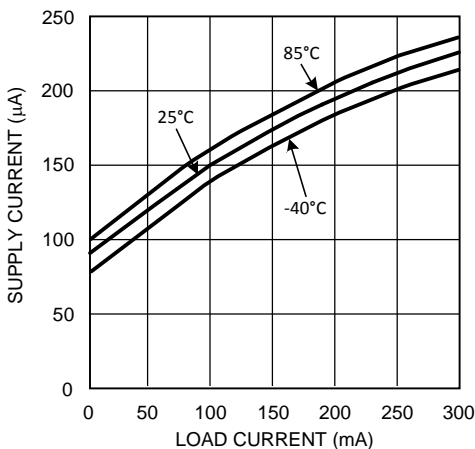


Figure 5. Supply Current vs Load Current

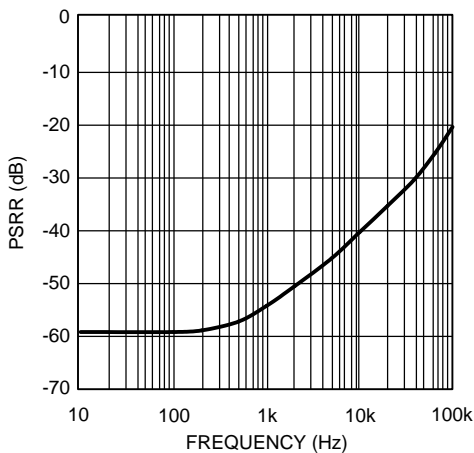


Figure 6. Power Supply Rejection Ratio vs Frequency

Typical Characteristics (continued)

Unless otherwise specified, $V_{IN} = V_O + 0.5\text{ V}$, $C_{IN} = C_{OUT} = 2.2\text{ }\mu\text{F}$, $C_{CC} = 33\text{ nF}$, $T_J = 25^\circ\text{C}$, $V_{SHDN} = V_{IN}$.

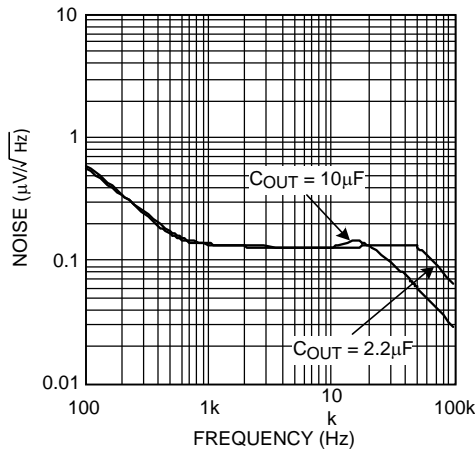


Figure 7. Output Noise Spectral Density

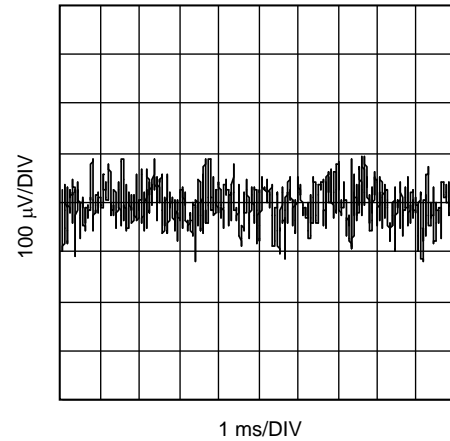


Figure 8. Output Noise (10 Hz to 100 kHz)

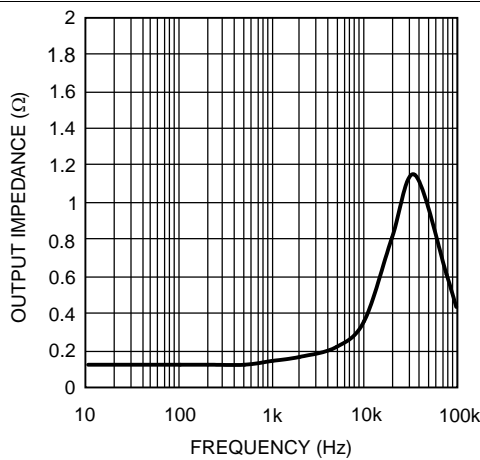


Figure 9. Output Impedance vs Frequency

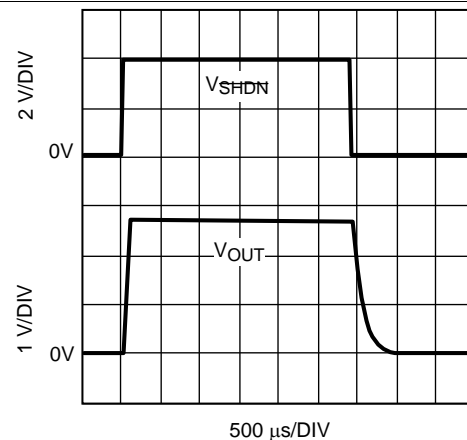


Figure 10. Shutdown Response

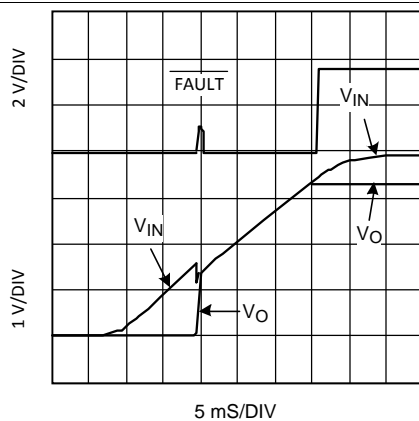


Figure 11. Power-Up Response

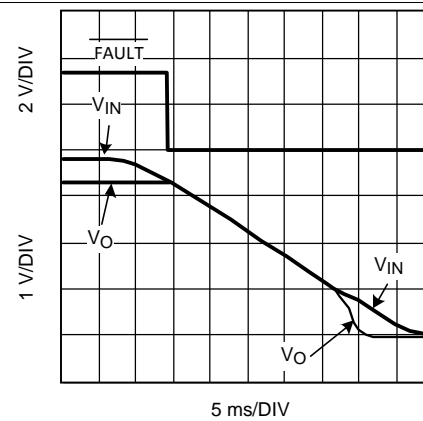


Figure 12. Power-Down Response

7 Detailed Description

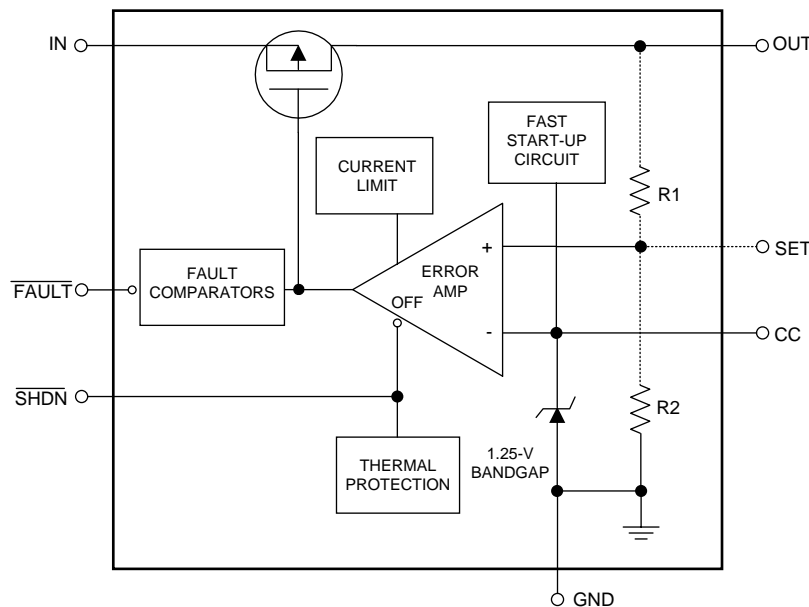
7.1 Overview

The LP3982 is package, pin, and performance compatible with Maxim's MAX8860, excluding reverse battery protection and dual-mode function (fixed and adjustable combined).

A 1.25-V bandgap reference, an error amplifier, and a PMOS pass transistor perform voltage regulation while being supported by shutdown, fault, and the usual temperature and current protection circuitry (see [Functional Block Diagram](#)).

The regulator topology is the classic type with negative feedback from the output to one of the inputs of the error amplifier. Feedback resistors R1 and R2 are either internal or external to the device, depending on whether it is the fixed-voltage version or the adjustable version. The negative feedback and high open loop gain of the error amplifier cause the two inputs of the error amplifier to be virtually equal in voltage. If the output voltage changes due to load changes, the error amplifier provides the appropriate drive to the pass transistor to maintain the error amplifier's inputs as virtually equal. In short, the error amplifier keeps the output voltage constant in order to keep its inputs equal.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 No-Load Stability

The LP3982 remains stable during no-load conditions, a necessary feature for CMOS RAM keep-alive applications.

7.3.2 Fast Start-Up

The LP3982 provides fast start-up time for better system efficiency. The start-up speed is maintained when using the optional noise bypass capacitor. An internal 500- μ A current source charges the capacitor until it reaches about 90% of its final value.

7.4 Device Functional Modes

7.4.1 Shutdown

The LP3982 goes into sleep mode when the $\overline{\text{SHDN}}$ pin is in a logic low condition. During this condition, the pass transistor, error amplifier, and bandgap are turned off, reducing the supply current to 1 nA typical. The maximum voltage for a logic low at the $\overline{\text{SHDN}}$ pin is 0.4 V. A minimum voltage of 2 V at the $\overline{\text{SHDN}}$ pin turns the LP3982 back on. The $\overline{\text{SHDN}}$ pin may be directly tied to V_{IN} to keep the part on. The $\overline{\text{SHDN}}$ pin may exceed V_{IN} but not the maximum of 6.5 V.

Figure 13 shows an application that uses the $\overline{\text{SHDN}}$ pin. It detects when the battery is too low and disconnects the load by turning off the regulator. A micropower comparator (LMC7215) and reference (LM385) are combined with resistors to set the minimum battery voltage. At the minimum battery voltage, the comparator output goes low and turns off the LP3982 and corresponding load. Hysteresis is added to the minimum battery threshold to prevent the battery's recovery voltage from falsely indicating an above minimum condition. When the load is disconnected from the battery, it automatically increases in terminal voltage because of the reduced IR drop across its internal resistance. The minimum battery detector of Figure 13 has a low detection threshold (V_{LT}) of 3.6 V that corresponds to the minimum battery voltage. The upper threshold (V_{UT}) is set for 4.6 V to exceed the recovery voltage of the battery.

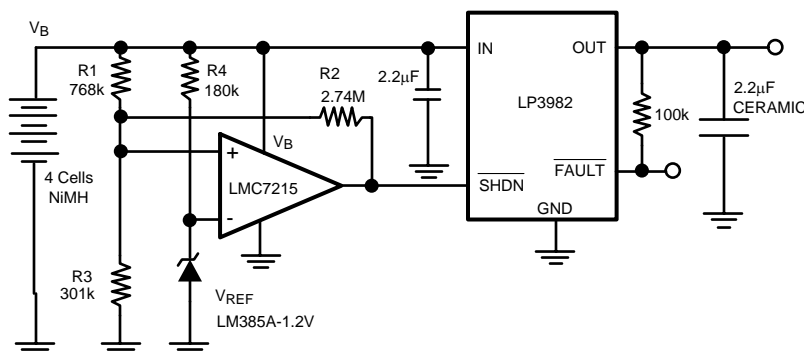


Figure 13. Minimum Battery Detector that Disconnects the Load Via the $\overline{\text{SHDN}}$ Pin of the LP3982

Resistor value for V_{UT} and V_{LT} are determined as follows:

$$G_T = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}$$

$$V_{\text{UT}} = R_1 (V_{\text{REF}}) G_T$$

$$V_{\text{LT}} = R_1 \parallel R_2 (V_{\text{REF}}) G_T \quad (1)$$

(The application of Figure 13 used a G_T of 5 μ mho.)

$$R_1 = \frac{V_{\text{UT}}}{V_{\text{REF}} (G_T)} \quad (2)$$

$$R_2 = \frac{1}{\frac{V_{\text{REF}} (G_T)}{V_{\text{LT}}} - \frac{1}{R_1}} \quad (3)$$

$$R_3 = \frac{1}{G_T - \left[\frac{1}{R_1} + \frac{1}{R_2} \right]} \quad (4)$$

The above procedure assumes a rail-to-rail output comparator. Essentially, R_2 is in parallel with R_1 prior to reaching the lower threshold, then R_2 becomes parallel with R_3 for the upper threshold. Note that the application requires rail-to-rail input as well.

The resistor values shown in Figure 13 are the closest practical to calculated values.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP3982 can provide 300-mA output current with 2.5-V to 6-V input. It is stable with a 2.2- μ F ceramic output capacitor. An optional external bypass capacitor reduces the output noise without slowing down the load transient response. Typical output noise is 37 μ V_{RMS} at frequencies from 10 Hz to 100 kHz. Typical PSRR is 60 dB at 1 kHz.

8.2 Typical Application

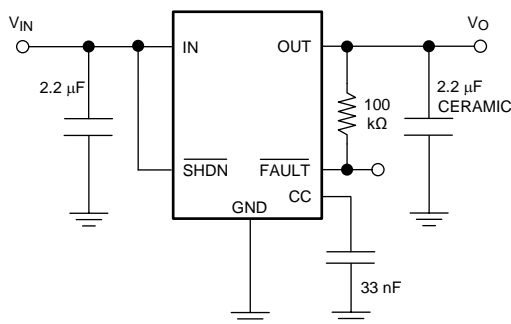


Figure 14. LP3982 Typical Application (Fixed V_{OUT} Version)

8.2.1 Design Requirements

For typical ultra low-dropout CMOS-regulator applications, use the parameters listed in [Table 1](#).

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Minimum input voltage	V _{OUT} + 0.5 V
Nominal output voltage	3.3 V
Maximum output current	300 mA
RMS noise, 10 Hz to 100 kHz	37 μ V _{RMS}
PSRR at 1 kHz	60 dB

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

[Click here](#) to create a custom design using the LP3982 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Output Voltage Setting (ADJ Version Only)

The output voltage is set according to the amount of negative feedback (the pass transistor inverts the feedback signal.) Figure 15 simplifies the topology of the LP3982. This type of regulator can be represented as an op amp configured as non-inverting amplifier and a fixed DC Voltage (V_{REF}) for its input signal. The special characteristic of this op amp is its extra-large output transistor that only sources current. In terms of its non-inverting configuration, the output voltage equals V_{REF} times the closed loop gain:

$$V_O = V_{REF} \left[\frac{R_1}{R_2} + 1 \right] \quad (5)$$

Use Equation 6 for adjusting the output to a particular voltage:

$$R_1 = R_2 \left[\frac{V_O}{1.25V} - 1 \right] \quad (6)$$

Choose $R_2 = 100 \text{ k}\Omega$ to optimize accuracy, power supply rejection, noise, and power consumption.

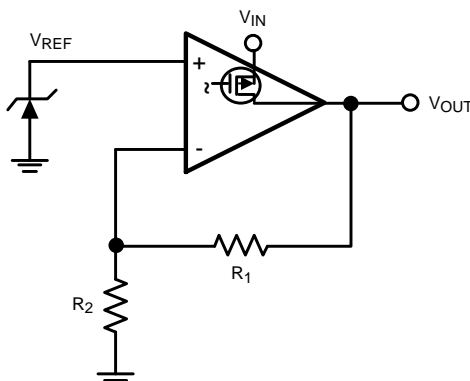


Figure 15. Regulator Topology Simplified

Similarity in the output capabilities exists between op amps and linear regulators. Just as rail-to-rail output op amps allow their output voltage to approach the supply voltage, low dropout regulators (LDOs) allow their output voltage to operate close to the input voltage. Both achieve this by the configuration of their output transistors. Standard operational amplifiers and regulator outputs are at the source (or emitter) of the output transistor. Rail-to-rail op amp and LDO regulator outputs are at the drain (or collector) of the output transistor. This replaces the threshold (or diode drop) limitations on the output with the less restrictive source-to-drain (or V_{SAT}) limitations. There is a trade-off; the output impedance becomes significantly higher, thus providing a critically lower pole when combined with the capacitive load. That is why rail-to-rail operational amplifiers are usually poor at driving capacitive loads and a series output resistor recommended when doing so. LDOs require the same series resistance except that the internal resistance of the output capacitor will usually suffice. Refer to the [Output Capacitance](#) section for more information.

8.2.2.3 Output Capacitance

The LP3982 is specifically designed to employ ceramic output capacitors as low as $2.2 \mu\text{F}$. Ceramic capacitors below $10 \mu\text{F}$ offer significant cost and space savings, along with high frequency noise filtering. Higher values and other types and of capacitor may be used, but their equivalent series resistance (ESR) must be maintained below 0.5Ω .

Ceramic capacitor of the value required by the LP3982 are available in the following dielectric types: Z5U, Y5V, X5R, and X7R. The Z5U and Y5V types exhibit a 50% or more drop in capacitance value as their temperature increases from 25°C, an important consideration. The X5R generally maintain their capacitance value within $\pm 20\%$. The X7R type are desirable for their tighter tolerance of 10% over temperature.

Ceramic capacitors pose a challenge because of their relatively low ESR. Like most other LDOs, the LP3982 relies on a zero in the frequency response to compensate against excessive phase shift in the feedback loop of the regulator. If the phase shift reaches 360° (that is, becomes positive), the regulator oscillates. This compensation usually resides in the zero generated by the combination of the output capacitor with its ESR. The zero is intended to cancel the effects of the pole generated by the load capacitance (C_L) combined with the parallel combination of the load resistance (R_L) and the output resistance (R_O) of the regulator. The challenge posed by low ESR capacitors is that the zero it generates can be too high in frequency for the pole it is intended to compensate. The LP3982 overcomes this challenge by internally generating a strategically placed zero.

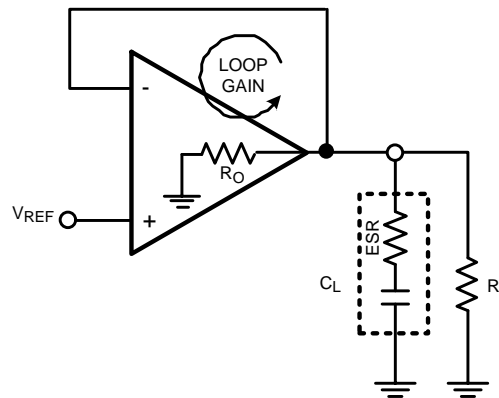


Figure 16. Simplified Model of Regulator Loop Gain Components

Figure 16 shows a basic model for the linear regulator that helps describe what happens to the output signal as it is processed through its feedback loop; that is, describe its loop gain (LG). The LG includes two main transfer functions: the error amplifier and the load. The error amplifier provides voltage gain and a dominant pole, while the load provides a zero and a pole. The LG of the model in Figure 16 is described by Equation 7:

$$LG(j\omega) = \frac{A_O}{1 + j \left[\frac{\omega}{\omega_{POLE}} \right]} * \frac{1 + j\omega (ESR \times C_L)}{1 + j\omega ((ESR + R_O // R_L) C_L)} \quad (7)$$

The first term of Equation 7 expresses the voltage gain (numerator) and a single pole roll-off (denominator) of the error amplifier. The second term expresses the zero (numerator) and pole (denominator) of the load in combination with the R_O of the regulator.

Figure 17 shows a Bode plot that represents a case where the zero contributed by the load is too high to cancel the effect of the pole contributed by the load and R_O . The solid line represents the loop gain while the dashed line represents the corresponding phase shift. Notice that the phase shift at unity gain is a total 360° , the criteria for oscillation.

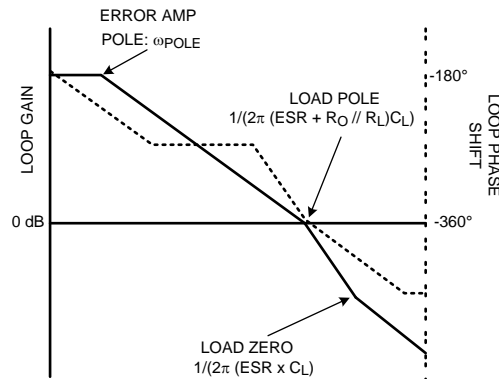


Figure 17. Loop Gain Bode Plot Illustrating Inadequately High Zero for Stability Compensation

The LP3982 generates an internal zero that makes up for the inadequately high zero of the low ESR ceramic output capacitor. This internally generated zero is strategically placed to provide positive phase shift near unity gain, thus providing a stable phase margin.

8.2.2.4 Input Capacitor

The LP3982 requires a minimum input capacitance of about 1 μF . The value may be increased indefinitely. The type is not critical to stability. However, instability may occur with bench set-ups where long supply leads are used, particularly at near dropout and high current conditions. This is attributed to the lead inductance coupling to the output through the gate oxide of the pass transistor; thus, forming a pseudo LCR network within the loop gain. A 10- μF tantalum input capacitor remedies this non-situ condition; its larger ESR acts to dampen the pseudo-LCR network. This may only be necessary for some bench setups. A 1- μF ceramic input capacitor are fine for most end-use applications.

If a tantalum input capacitor is intended for the final application, it is important to consider their tendency to fail in short circuit mode, thus potentially damaging the part.

8.2.2.5 Noise Bypass Capacitor

The noise bypass capacitor (CC) significantly reduces output noise of the LP3982. It connects between pin 6 and ground. The optimum value for CC is 33 nF.

Pin 6 directly connects to the high impedance output of the bandgap. The DC leakage of the CC capacitor must be considered; loading down the reference reduces the output voltage. NPO and COG ceramic capacitors typically offer very low leakage. Polypropylene and polycarbonate film capacitor offer even lower leakage currents.

CC does not affect the transient response; however, it does affect turnon time. The smaller the CC value, the faster the turnon time.

8.2.2.6 Fault Detection

The LP3982 provides a $\overline{\text{FAULT}}$ pin that goes low during out of regulation conditions like current limit and thermal shutdown, or when it approaches dropout. The latter monitors the input-to-output voltage differential and compares it against a threshold that is slightly above the dropout voltage. This threshold also tracks the dropout voltage as it varies with load current. Refer to [Figure 3](#) in the [Typical Characteristics](#) section.

The $\overline{\text{FAULT}}$ pin requires a pullup resistor because it is an open-drain output. This resistor must be large in value to reduce energy drain. A 100-k Ω pullup resistor works well for most applications.

[Figure 18](#) shows the LP3982 with delay added to the $\overline{\text{FAULT}}$ pin for the reset pin of a microprocessor. The output of the comparator stays low for a preset amount of time after the regulator comes out of a fault condition.

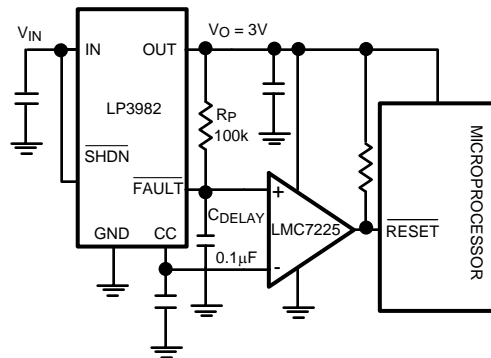


Figure 18. Power-On Delayed Reset Application

The delay time for the application of Figure 18 is set by Equation 8:

$$C_{DELAY} = \frac{-t}{R_{pln} \left[1 - \frac{V_{REF}}{V_O} \right]} \quad (8)$$

The application is set for a reset delay time of 8.8 ms. The comparator must have high impedance inputs so as to not load down the V_{REF} at the CC pin of the LP3982.

8.2.2.7 Power Dissipation

Knowing the device power dissipation and proper sizing of the thermal plane connected to the tab or pad is critical to ensuring reliable operation. Device power dissipation depends on input voltage, output voltage, and load conditions and can be calculated with Equation 9:

$$P_{D(MAX)} = (V_{IN(MAX)} - V_{OUT}) \times I_{OUT(MAX)} \quad (9)$$

Power dissipation can be minimized, and greater efficiency can be achieved, by using the lowest available voltage drop option that would still be greater than the dropout voltage (V_{DO}). However, keep in mind that higher voltage drops result in better dynamic (that is, PSRR and transient) performance. On the WSON (NGM) package, the primary conduction path for heat is through the exposed power pad to the PCB. To ensure the device does not overheat, connect the exposed pad, through thermal vias, to an internal ground plane with an appropriate amount of copper PCB area. On the VSSOP (DGK) package, the primary conduction path for heat is through the pins to the PCB. The maximum allowable junction temperature ($T_{J(MAX)}$) determines maximum power dissipation allowed ($P_{D(MAX)}$) for the device package. Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A), according to Equation 10 or Equation 11:

$$(T_{J(MAX)} = T_{A(MAX)} + (R_{\theta JA} \times P_{D(MAX)}) \quad (10)$$

$$P_{D(MAX)} = (T_{J(MAX)} - T_{A(MAX)}) / R_{\theta JA} \quad (11)$$

$R_{\theta JA}$ is highly dependent on the heat-spreading capability of the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in Thermal Information is determined by the specific EIA/JEDEC JESD51-7 standard for PCB and copper-spreading area, and is to be used only as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is the sum of the package junction-to-case (bottom) thermal resistance ($R_{\theta JCbot}$) plus the thermal resistance contribution by the PCB copper area acting as a heat sink.

Improvements and absolute measurements of the $R_{\theta JA}$ can be estimated by utilizing the thermal shutdown circuitry that is internal to the device. The thermal shutdown turns off the pass transistor of the device when its junction temperature reaches 160°C (typical). The pass transistor does not turn on again until the junction temperature drops about 10°C (hysteresis).

Using the thermal shutdown circuit to estimate, $R_{\theta JA}$ can be as follows: with a low input-to-output voltage differential, set the load current to 300 mA. Increase the input voltage until the thermal shutdown begins to cycle on and off. Then slowly decrease V_{IN} (100-mV increments) until the device stays on. Record the resulting voltage differential (V_D) and use it in Equation 12:

$$R_{\theta JA} = \frac{(160 - T_A)}{(0.300 \times V_D)} \quad (12)$$

8.2.2.8 Estimating Junction Temperature

The EIA/JEDEC standard recommends the use of psi (Ψ) thermal characteristics to estimate the junction temperatures of surface mount devices on a typical PCB board application. These characteristics are not true thermal resistance values, but rather package specific thermal characteristics that offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of copper-spreading area. The key thermal characteristics (Ψ_{JT} and Ψ_{JB}) are given in [Thermal Information](#) and are used in accordance with [Equation 13](#) or [Equation 14](#).

$$T_{J(MAX)} = T_{TOP} + (\Psi_{JT} \times P_{D(MAX)})$$

where

- $P_{D(MAX)}$ is explained in [Equation 9](#).
- T_{TOP} is the temperature measured at the center-top of the device package. (13)

$$T_{J(MAX)} = T_{BOARD} + (\Psi_{JB} \times P_{D(MAX)})$$

where

- $P_{D(MAX)}$ is explained in [Equation 9](#).
- T_{BOARD} is the PCB surface temperature measured 1-mm from the device package and centered on the package edge. (14)

For more information about the thermal characteristics Ψ_{JT} and Ψ_{JB} , see the TI Application Report *Semiconductor and IC Package Thermal Metrics* ([SPRA953](#)), available for download at [www.ti.com](#).

For more information about measuring T_{TOP} and T_{BOARD} , see the TI Application Report *Using New Thermal Metrics* ([SBVA025](#)), available for download at [www.ti.com](#).

For more information about the EIA/JEDEC JESD51 PCB used for validating $R_{\theta JA}$, see the TI Application Report *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* ([SZZA017](#)), available for download at [www.ti.com](#).

8.2.3 Application Curves

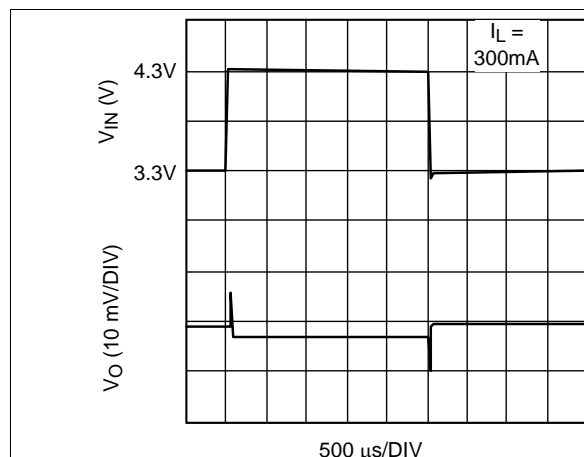


Figure 19. Line Transient Response

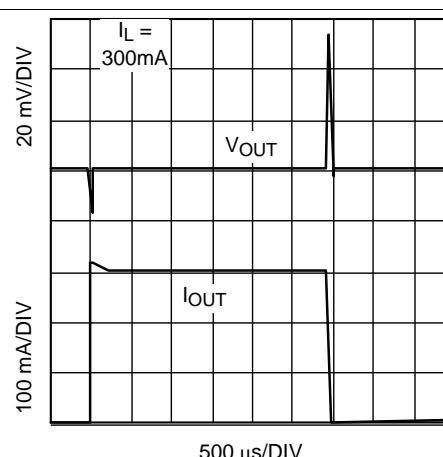


Figure 20. Load Transient

9 Power Supply Recommendations

The LP3982 is designed to operate from an input voltage supply range between 2.5 V and 6 V. The input voltage range provides adequate headroom in order for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help to improve the output noise performance.

10 Layout

10.1 Layout Guidelines

Best performance is achieved by placing C_{IN} , C_{OUT} , and C_{CC} on the same side of the PCB as the LP3982 device, and as close as is practical to the package. The ground connections for C_{IN} and C_{OUT} must be back to the LP3982 device GND pin using as wide and as short of a copper trace as is practical.

Avoid connections using long trace lengths and narrow trace widths. These add parasitic inductances and resistance that results in inferior performance especially during transient conditions.

10.2 Layout Example

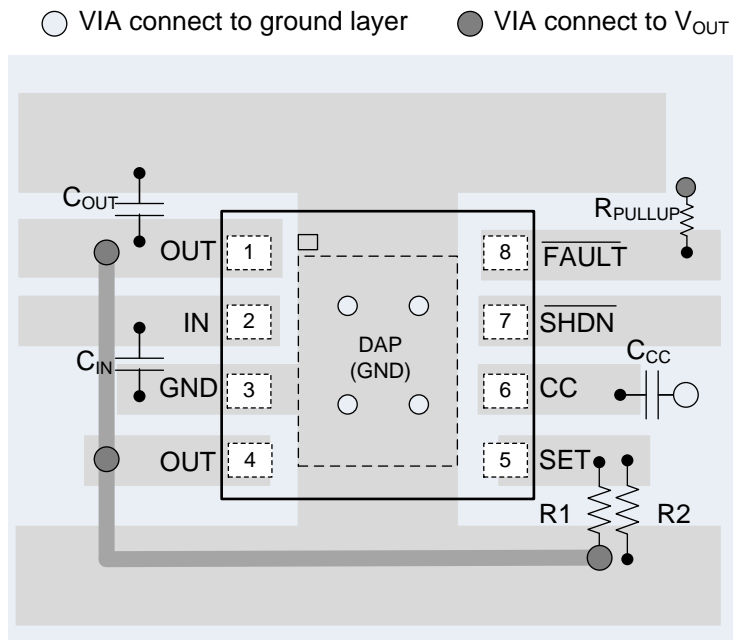


Figure 21. WSON Package Adjustable Version (Not to Scale)

10.3 WSON Mounting

The WSON package requires specific mounting techniques which are detailed in TI Application Report *Leadless Leadframe Package (LLP)* (SNOA401). Referring to the section *PCB Design Recommendations*, the pad style which must be used with the WSON package is the NSMD (non-solder mask defined) type. Additionally, it is recommended the PCB terminal pads be 0.2 mm longer than the package pads to create a solder fillet to improve reliability and inspection. The thermal dissipation of the WSON package is directly related to the printed circuit board construction and the amount of additional copper area connected to the DAP. The DAP (exposed pad) on the bottom of the WSON package is connected to the die substrate with a conductive die attach adhesive. The DAP has no direct electrical (wire) connection to any of the pins. There is a parasitic PN junction between the die substrate and the device ground. As such, it is strongly recommend that the DAP be connected directly to the ground at device pin 3 (GND). Alternately, but not recommended, the DAP may be left floating (no electrical connection). The DAP must not be connected to any potential other than ground.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For additional information, see the following:

- [AN-1187 Leadless Leadframe Package \(LLP\)](#)
- [Semiconductor and IC Package Thermal Metrics](#)
- [Using New Thermal Metrics](#)
- [Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs](#)

11.1.2 Development Support

11.1.2.1 Custom Design With WEBENCH® Tools

[Click here](#) to create a custom design using the LP3982 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.

WEBENCH is a registered trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP3982ILD-1.8/NOPB	Active	Production	WSOP (NGM) 8	1000 SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	LNB
LP3982ILD-2.5/NOPB	Active	Production	WSOP (NGM) 8	1000 SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	LPB
LP3982ILD-3.0/NOPB	Active	Production	WSOP (NGM) 8	1000 SMALL T&R	Yes	NIPDAU SN	Level-3-260C-168 HR	-40 to 85	LTB
LP3982ILD-3.3/NOPB	Active	Production	WSOP (NGM) 8	1000 SMALL T&R	Yes	NIPDAU SN	Level-3-260C-168 HR	-40 to 85	LUB
LP3982ILD-ADJ/NOPB	Active	Production	WSOP (NGM) 8	1000 SMALL T&R	Yes	NIPDAU SN	Level-3-260C-168 HR	-40 to 85	LVB
LP3982IMM-1.8/NOPB	Active	Production	VSSOP (DGK) 8	1000 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LENB
LP3982IMM-2.5/NOPB	Active	Production	VSSOP (DGK) 8	1000 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LEPB
LP3982IMM-3.0/NOPB	Active	Production	VSSOP (DGK) 8	1000 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LETB
LP3982IMM-3.3/NOPB	Active	Production	VSSOP (DGK) 8	1000 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LEUB
LP3982IMM-ADJ	Obsolete	Production	VSSOP (DGK) 8	-	-	Call TI	Call TI	-40 to 85	LEVB
LP3982IMM-ADJ/NOPB	Active	Production	VSSOP (DGK) 8	1000 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LEVB

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3982ILD-1.8/NOPB	WSOP	NGM	8	1000	178.0	12.4	3.3	2.8	1.0	8.0	12.0	Q1
LP3982ILD-2.5/NOPB	WSOP	NGM	8	1000	178.0	12.4	3.3	2.8	1.0	8.0	12.0	Q1
LP3982ILD-3.0/NOPB	WSOP	NGM	8	1000	178.0	12.4	3.3	2.8	1.0	8.0	12.0	Q1
LP3982ILD-3.3/NOPB	WSOP	NGM	8	1000	178.0	12.4	3.3	2.8	1.0	8.0	12.0	Q1
LP3982ILD-ADJ/NOPB	WSOP	NGM	8	1000	178.0	12.4	3.3	2.8	1.0	8.0	12.0	Q1
LP3982ILD-1.8/NOPB	WSOP	NGM	8	4500	330.0	12.4	3.3	2.8	1.0	8.0	12.0	Q1
LP3982ILD-3.3/NOPB	WSOP	NGM	8	4500	330.0	12.4	3.3	2.8	1.0	8.0	12.0	Q1
LP3982ILD-ADJ/NOPB	WSOP	NGM	8	4500	330.0	12.4	3.3	2.8	1.0	8.0	12.0	Q1
LP3982IMM-1.8/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP3982IMM-2.5/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP3982IMM-3.0/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP3982IMM-3.3/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP3982IMM-ADJ/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP3982IMMX-1.8/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP3982IMMX-2.5/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP3982IMMX-2.82/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

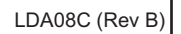
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3982IMMX-ADJ/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3982ILD-1.8/NOPB	WSOP	NGM	8	1000	208.0	191.0	35.0
LP3982ILD-2.5/NOPB	WSOP	NGM	8	1000	208.0	191.0	35.0
LP3982ILD-3.0/NOPB	WSOP	NGM	8	1000	208.0	191.0	35.0
LP3982ILD-3.3/NOPB	WSOP	NGM	8	1000	208.0	191.0	35.0
LP3982ILD-ADJ/NOPB	WSOP	NGM	8	1000	208.0	191.0	35.0
LP3982ILDX-1.8/NOPB	WSOP	NGM	8	4500	356.0	356.0	36.0
LP3982ILDX-3.3/NOPB	WSOP	NGM	8	4500	356.0	356.0	36.0
LP3982ILDX-ADJ/NOPB	WSOP	NGM	8	4500	356.0	356.0	36.0
LP3982IMM-1.8/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LP3982IMM-2.5/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LP3982IMM-3.0/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LP3982IMM-3.3/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LP3982IMM-ADJ/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LP3982IMMX-1.8/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LP3982IMMX-2.5/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LP3982IMMX-2.82/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LP3982IMMX-ADJ/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

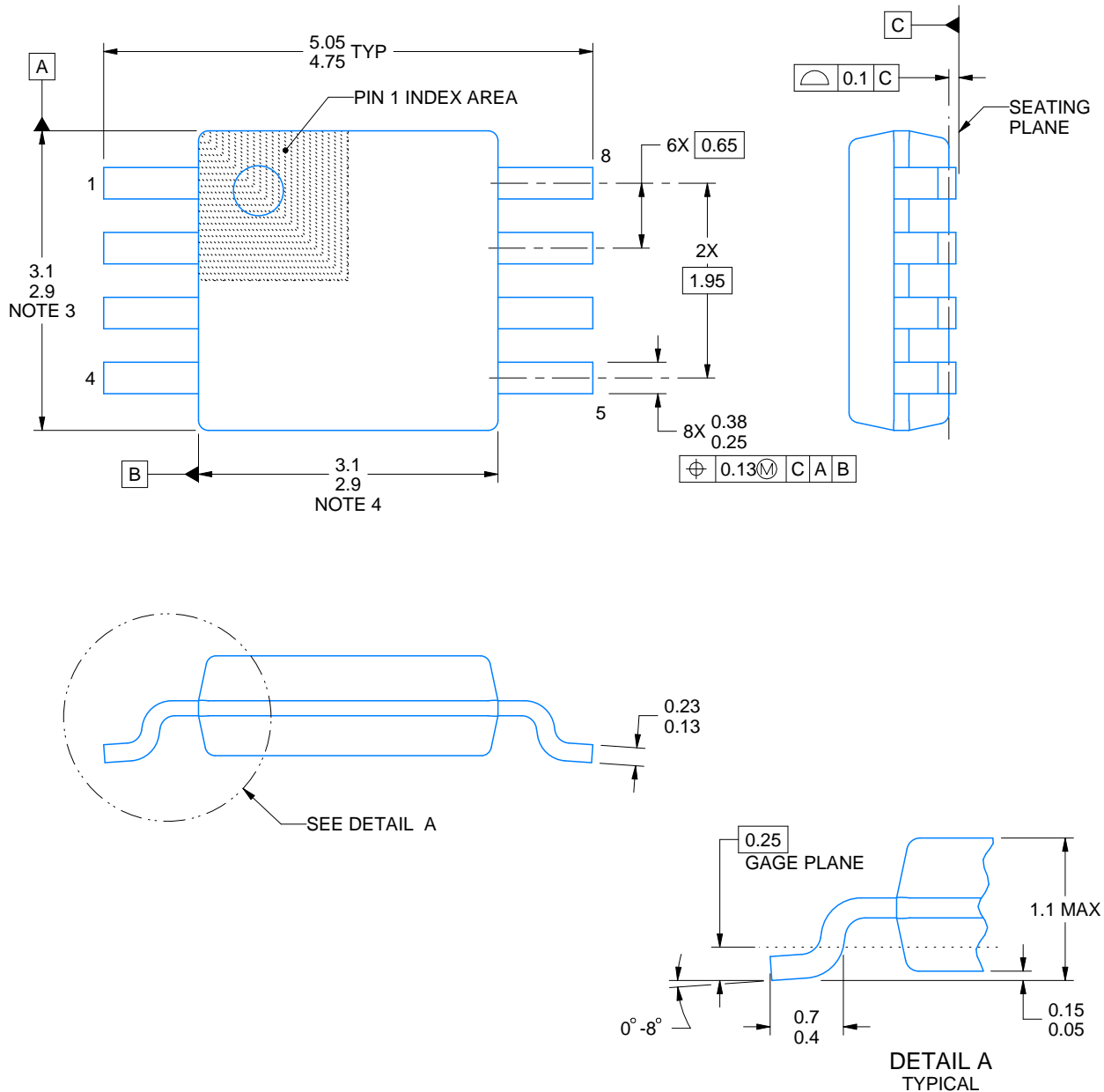


DGK0008A

PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated