Datasheet

LCD Panel Timing Control ICs

WUXGA/FHD LVDS/mini-LVDS Interface LCD Timing Controller for Automotive

BU90AL211-M

General Description

LCD Panel Timing Controller for Automotive

Features

- AEC-Q100 Qualified (Note 1)
- Support WUXGA/FHD Class Resolution
  - Horizontal Active is up to 1920 Pixels
  - Vertical Active is up to 1280 Lines
- Flexible LVDS Input/mini-LVDS Output Mode
  1. Single-in/Single-out (3pair)
  2. Single-in/Single-out (6pair)
  3. Dual-in/Single-out (6pair)
  4. Dual-in/Dual-out (3pair)
- Support 2 Type LVDS Data Mapping (VESA/JEIDA)
- Support mini-LVDS Output Data Skew Control (T/16 Step)
- Support Internal LDO: 1.5V Output (☆) (Note 2)
- Support Internal Oscillator
- Support Fail-Safe Function (DE, LVDS Clock)
- Support SSCG (Spread Spectrum Clock Generator)
- Support 16kbit External EEPROM
- Support BIST (Built-In Self-Test) Function
- Support AGING Function
- Support Source and Gate Driver Control Signal (Programmable Timing) (☆) (Note 2)
- Support Up & Down Gate Driver Scan
- Support Left & Right Direction Data Mapping
- Support Gamma Correction and Dithering
- Support Data Inversion
- Support Blanking Gray Insertion
- Support I^2C Master Function (☆) (Note 2)
- Support I^2C Slave Function (☆) (Note 2)
- Support SPI Slave Function (☆) (Note 2)
- Support Start Pulse Return Detection
- Support CRC (Cyclic Redundancy Check) Function
- Support OSD (On-Screen Display) Function

(Note 1) AEC-Q100 Grade2

(Note 2) (☆): Special Characteristics

Applications

- Car Navigation System
- CID (Center Information Display)
- Camera Monitor System

Key Specifications

- Supply Voltage Range : VDDIO 2.3V to 3.6V
  LVDSVDD 2.3V to 3.6V
  MVDD 2.3V to 3.6V
  VDD15 1.35V to 1.65V
- LVDS Clock Frequency (Single Mode) 20MHz to 120MHz
- LVDS Clock Frequency (Dual Mode) 20MHz to 100MHz
- mini-LVDS Clock Frequency 30MHz to 360MHz
- Operating Temperature Range -40°C to +105°C

Package

	W(Typ) x D(Typ) x H(Max)
UQFP80	10.0mm x 10.0mm x 1.60mm

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Block Diagram

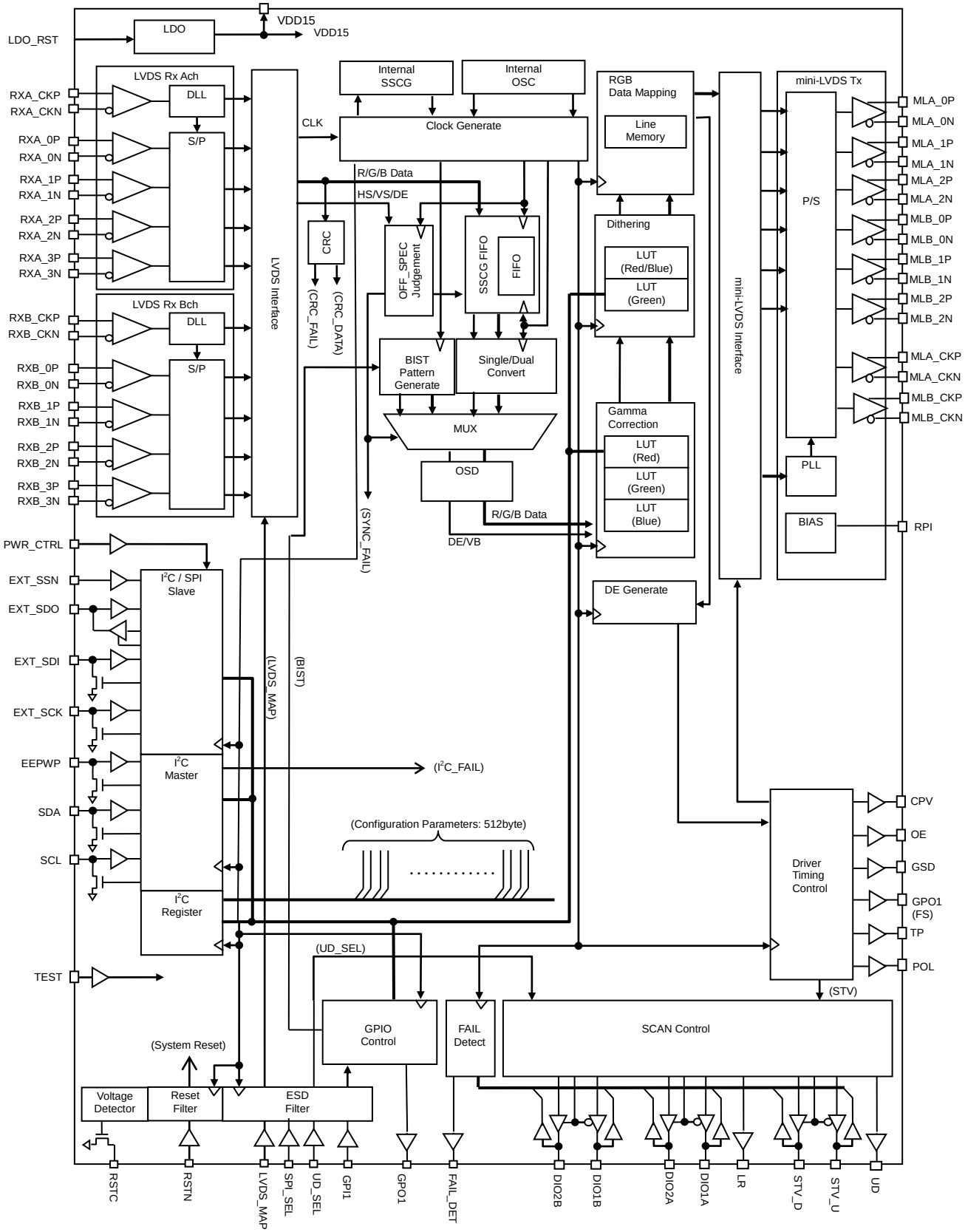


Figure 1. Block Diagram

Pin Configuration

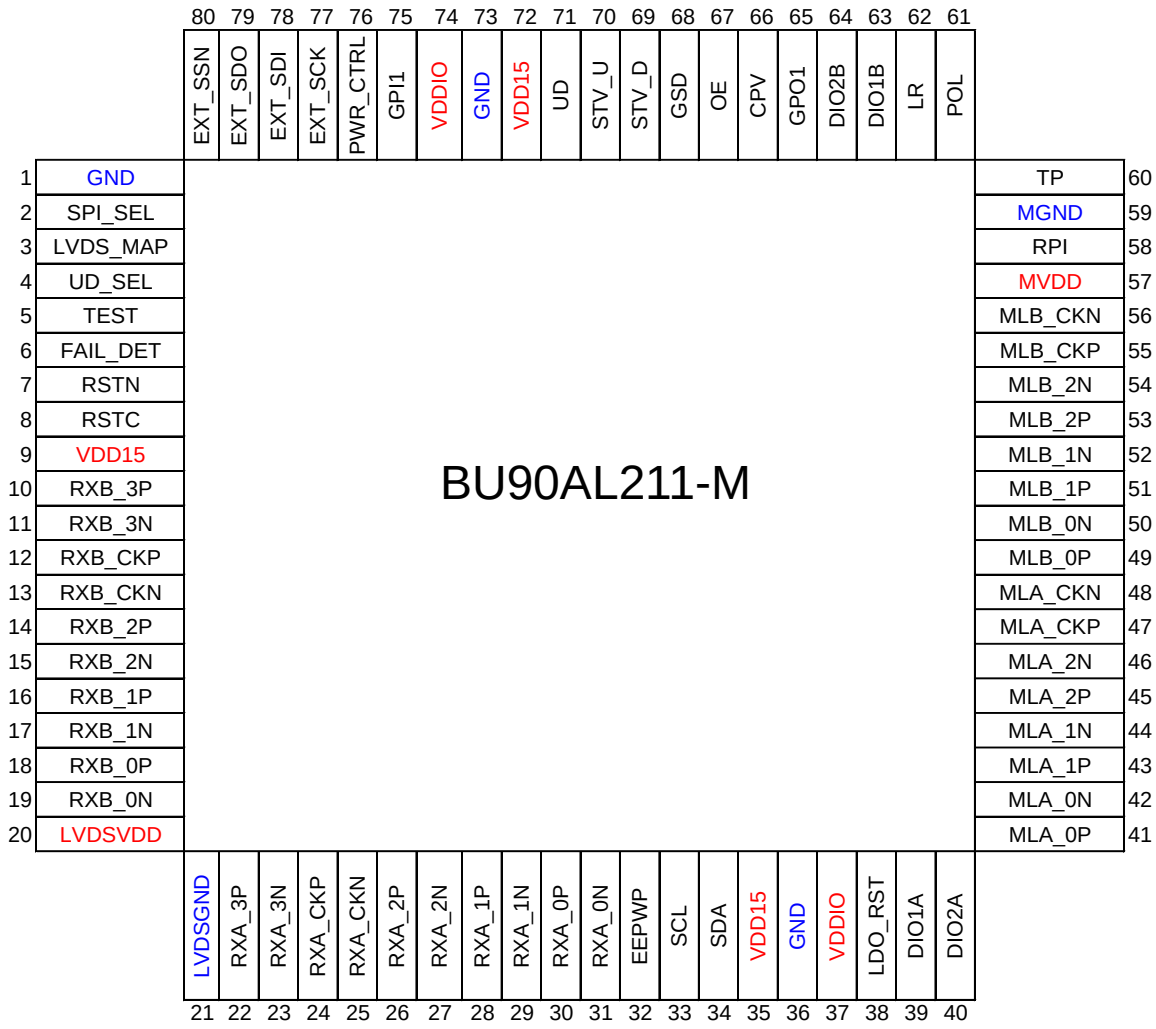


Figure 2. Pin Configuration (TOP VIEW)

Pin Descriptions

(LVDS Receiver Pins)

Pin No.	Pin Name	Direction	Function	Note
31	RXA_0N	IN	LVDS input data0 pair of port A	
30	RXA_0P	IN		
29	RXA_1N	IN	LVDS input data1 pair of port A	
28	RXA_1P	IN		
27	RXA_2N	IN	LVDS input data2 pair of port A	
26	RXA_2P	IN		
23	RXA_3N	IN	LVDS input data3 pair of port A	
22	RXA_3P	IN		
25	RXA_CKN	IN	LVDS input clock pair of port A	
24	RXA_CKP	IN		
19	RXB_0N	IN	LVDS input data0 pair of port B	
18	RXB_0P	IN		
17	RXB_1N	IN	LVDS input data1 pair of port B	
16	RXB_1P	IN		
15	RXB_2N	IN	LVDS input data2 pair of port B	
14	RXB_2P	IN		
11	RXB_3N	IN	LVDS input data3 pair of port B	
10	RXB_3P	IN		
13	RXB_CKN	IN	LVDS input clock pair of port B	
12	RXB_CKP	IN		

(mini-LVDS Transmitter Pins)

Pin No.	Pin Name	Direction	Function	Note
41	MLA_0P	OUT	mini-LVDS output data0 pair of port A	
42	MLA_0N	OUT		
43	MLA_1P	OUT	mini-LVDS output data1 pair of port A	
44	MLA_1N	OUT		
45	MLA_2P	OUT	mini-LVDS output data2 pair of port A	
46	MLA_2N	OUT		
47	MLA_CKP	OUT	mini-LVDS output clock pair of port A	
48	MLA_CKN	OUT		
49	MLB_0P	OUT	mini-LVDS output data0 pair of port B	
50	MLB_0N	OUT		
51	MLB_1P	OUT	mini-LVDS output data1 pair of port B	
52	MLB_1N	OUT		
53	MLB_2P	OUT	mini-LVDS output data2 pair of port B	
54	MLB_2N	OUT		
55	MLB_CKP	OUT	mini-LVDS output clock pair of port B	
56	MLB_CKN	OUT		
58	RPI	IN	mini-LVDS output current bias	

Pin Descriptions - continued

(Function Setting Pins)

Pin No.	Pin Name	Direction	Function	Note
4	UD_SEL	IN	Gate/Source driver scan direction select L : Scan direction non-invert H : Scan direction invert	Internal pull down
75	GPI1	IN	General purpose input pin Usable DISP_ON, BIST, LR_SEL, FAULT_PMIC	Internal pull down
3	LVDS_MAP	IN	LVDS data mapping select L : VESA format H : JEIDA format	Internal pull down
76	PWR_CTRL	IN	Power-on sequence control L : TCON read EEPROM data first H : System write/read TCON/EEPROM data first	Internal pull down Connect VDDIO/GND directly

(I^2C and SPI Interface Pins)

Pin No.	Pin Name	Direction	Function	Note
2	SPI_SEL	IN	Select external access interface (I^2C or SPI) SPI_SEL=H : SPI mode SPI_SEL=L : I^2C mode	Internal pull down
80	EXT_SSN	IN	SPI_SEL=H : SPI chip select signal SPI_SEL=L : DEV_ADR0 signal	Internal pull down
79	EXT_SDO	IN/OUT	SPI_SEL=H : SPI output data signal SPI_SEL=L : Usable for GPO	
77	EXT_SCK	IN/OUT	SPI_SEL=H : SPI clock signal SPI_SEL=L : I^2C slave port (serial clock)	Nch-open drain
78	EXT_SDI	IN/OUT	SPI_SEL=H : SPI input data signal SPI_SEL=L : I^2C slave port (serial data)	Nch-open drain
32	EEPWP	IN/OUT	EEPROM write protect L : Protection invalid Hi-Z : Protection valid	Nch-open drain
33	SCL	IN/OUT	I^2C master port (serial clock)	Nch-open drain
34	SDA	IN/OUT	I^2C master port (serial data)	Nch-open drain

(Timing Control Pins)

Pin No.	Pin Name	Direction	Function	Note
66	CPV	OUT	Shift clock to gate driver	
67	OE	OUT	Output enable signal to gate driver	
68	GSD	OUT	Gate shading timing control signal	
69	STV_D	IN/OUT	Start pulse(down side) to gate driver	
70	STV_U	IN/OUT	Start pulse(up side) to gate driver	
71	UD	OUT	Scan direction control to gate driver(up or down)	
62	LR	OUT	Scan direction control to source driver(left or right)	
61	POL	OUT	Polarity control signal to source driver	
60	TP	OUT	Data latch pulse to source driver	
65	GPO1	OUT	General purpose output pin Usable FS,WAKEUP,BANK_SEL	
39	DIO1A	IN/OUT	Start pulse1 to source driver of port A	
40	DIO2A	IN/OUT	Start pulse2 to source driver of port A	
63	DIO1B	IN/OUT	Start pulse1 to source driver of port B	
64	DIO2B	IN/OUT	Start pulse2 to source driver of port B	
6	FAIL_DET	OUT	Panel fail mode detection signal L : Fail H : Normal	

Pin Descriptions - continued

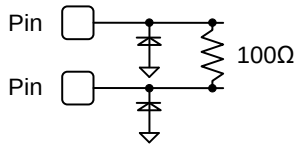
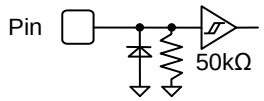
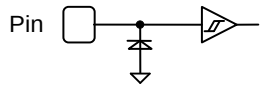
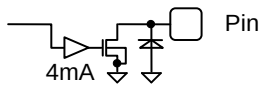
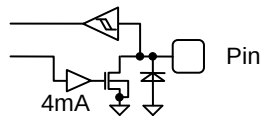
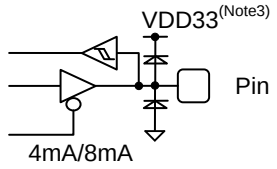
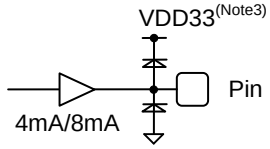
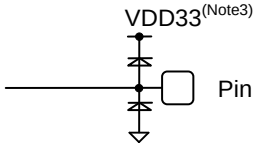
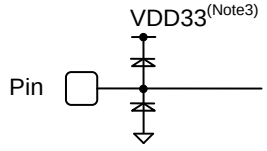
(Others Pins)

Pin No.	Pin Name	Direction	Function	Note
5	TEST	IN	Test mode enable L : Normal operation H : Test mode for vendor	Internal pull down Connect GND directly
7	RSTN	IN	Hardware reset L : Reset active H : Reset non-active	
8	RSTC	OUT	Power on reset voltage detect signal	
38	LDO_RST	IN	LDO reset L : LDO active H : LDO non-active	

(Power and Ground Pins)

Pin No.	Pin Name	Direction	Function	Note
1,36,73	GND	-	Ground	
21	LVDSGND	-	LVDS ground	
59	MGND	-	mini-LVDS ground	
37,74	VDDIO	-	IO power (2.5V/3.3V)	
9,35,72	VDD15	-	Digital power (1.5V)	
20	LVDSVDD	-	LVDS power (2.5V/3.3V)	
57	MVDD	-	mini-LVDS power (2.5V/3.3V)	

I/O Equivalence Circuit

Type	Direction	Circuit Type	Applied Pin	Note
1	IN		RXA_0N, RXA_0P, RXA_1N, RXA_1P, RXA_2N, RXA_2P, RXA_3N, RXA_3P, RXA_CKN, RXA_CKP, RXB_0N, RXB_0P, RXB_1N, RXB_1P, RXB_2N, RXB_2P, RXB_3N, RXB_3P, RXB_CKN, RXB_CKP	LVDS Receiver
2	IN		SPI_SEL, LVDS_MAP, UD_SEL, TEST, GPI1, PWR_CTRL, EXT_SSN	
3	IN		RSTN	
4	OUT		RSTC	Output Drivability 4mA
5	IN/OUT		SCL, SDA, EEPWP, EXT_SCK, EXT_SDI	Output Drivability 4mA
6	IN/OUT		DIO1A, DIO2A, DIO1B, DIO2B, STV_U, STV_D, EXT_SDO	Output Drivability 4mA/8mA Selectable
7	OUT		FAIL_DET, TP, POL, LR, CPV, OE, GSD, UD, GPO1	Output Drivability 4mA/8mA Selectable
8	OUT		MLA_0P, MLA_0N, MLA_1P, MLA_1N, MLA_2P, MLA_2N, MLA_CKP, MLA_CKN, MLB_0P, MLB_0N, MLB_1P, MLB_1N, MLB_2P, MLB_2N, MLB_CKP, MLB_CKN	mini-LVDS Transmitter
9	IN		LDO_RST, RPI	

(Note 3) VDD33: VDDIO, LVDSVDD, MVDD

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Supply Voltage1 (1.5V)	VDD15	-0.3 to +2.1	V	For VDD15
Supply Voltage2 (3.3V)	VDD33	-0.3 to +4.5	V	For VDDIO, LVDSVDD, MVDD
Input Voltage	V_{IN}	-0.3 to VDD33+0.3	V	VDD33+0.3 < 4.5V
Storage Temperature Range	Tstg	-55 to +125	°C	
Maximum Junction Temperature	Tjmax	125	°C	

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Thermal Resistance (Note 4)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s(Note 6)	2s2p(Note 7)	
UQFP80				
Junction to Ambient	θ_{JA}	70.5	40.2	°C /W
Junction to Top Characterization Parameter(Note 5)	Ψ_{JT}	3	1	°C /W

(Note 4) Based on JESD51-2A(Still-Air)

(Note 5) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 6) Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

(Note 7) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

Recommended Operating Conditions

Parameter	Symbol	Limit			Unit	Note
		Min	Typ	Max		
Power Supply Voltage1	VDD15	1.35	1.5	1.65	V	For VDD15 (Internal LDO)
Power Supply Voltage2	VDD33	2.30	3.3	3.60	V	For VDDIO,LVDSVDD,MVDD
LVDS Clock Frequency	f_{IN}	20	-	120	MHz	LVDS Single Mode
		20	-	100	MHz	LVDS Dual Mode
mini-LVDS Clock Frequency	f_{OUT}	30	-	360	MHz	
Operating Temperature	Tj	-40	+25	+105	°C	

Electrical Characteristics

CMOS Digital I/O DC Characteristics

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
High Level Input Voltage	V_{IH}	VDDIOx0.7	-	VDDIO	V	All CMOS Input (☆) (Note 8)
Low Level Input Voltage	V_{IL}	0	-	VDDIOx0.3	V	All CMOS Input (☆) (Note 8)
Hysteresis Voltage	V_H	-	600	-	mV	(Note 9)
Pull Down Resistor	R_{DN}	35	50	65	kΩ	
Input Leakage Current	I_{IZ}	-10	-	+10	μA	V_{IN}=VDDIO or GND (Except LVDS Rx Input)
Output Leakage Current	I_{OZ}	-10	-	+10	μA	V_{IN}=VDDIO or GND
High Level Output Voltage	V_{OH}	VDDIO-0.4	-	-	V	I_{OH} = -4mA/-8mA (☆) (Note 8)
Low Level Output Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 4mA/8mA (☆) (Note 8)

(Note 8) (☆): Special Characteristics
(Note 9) This spec is for schmitt trigger type cell.

LVDS Specification

LVDS Receiver DC Characteristics

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Differential Input Voltage	$\|V_{ID}\|$	100	-	600	mV	
Differential Input “H” Threshold	V_{TH}	-	-	+50	mV	
Differential Input “L” Threshold	V_{TL}	-50	-	-	mV	
Differential Input Common Mode Voltage	V_{CM_RX}	$\|V_{ID}\|/2$	1.2	2.4 $-\|V_{ID}\|/2$	V	VDD33=3.3V (Note 10)
				(VDD33-0.4) $-\|V_{ID}\|/2$		VDD33=2.5V(Note 10)
Differential Input Common Mode Voltage Difference	$V_{CM\_RX\Delta}$	-50	-	+50	mV	(Note 11)
Internal Termination Resistor	R_{TERM}	84	100	116	Ω	
		90	100	110	Ω	Tj=25°C
Differential Input Leakage Current	I_{RXIZ}	-20	-	+20	μA	(Note 12)

(Note 10) VDD33: VDDIO, LVDSVDD, MVDD
(Note 11) $V_{CM\_RX\Delta}$: Voltage Difference of Differential Input Common Mode Voltage.
(Note 12) Leak Current per Pin. (It becomes the double current value on the IC for the internal termination resistor.)

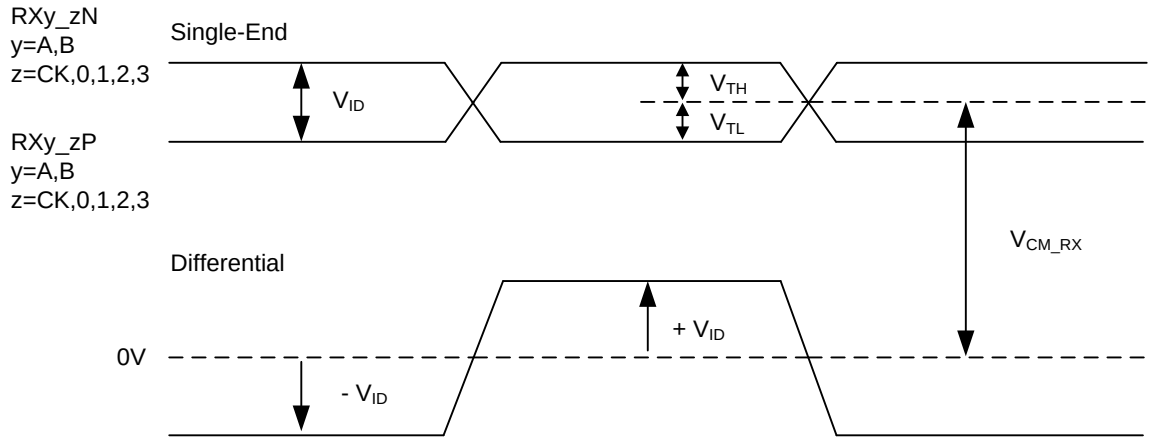


Figure 3. LVDS Receiver DC Characteristics Definition (1)

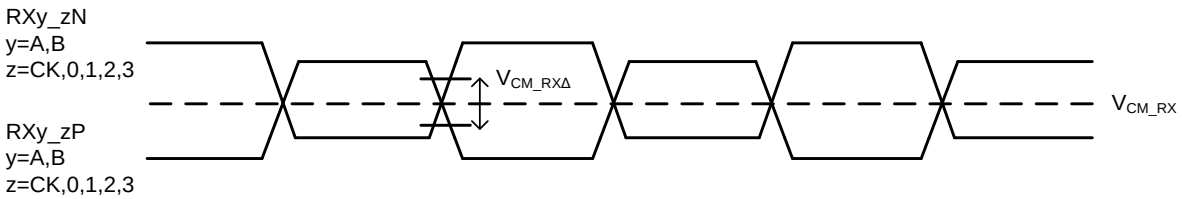


Figure 4. LVDS Receiver DC Characteristics Definition (2)

LVDS Receiver AC Characteristics

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
LVDS Clock Frequency	f_{IN}	20	-	120	MHz	
LVDS Clock Period	t_{RCIP}	8.33	-	50.0	ns	
Receiver Skew Margin	t_{SK}	0	-	0.60	ns	f_{IN}=65MHz
		0	-	0.40	ns	f_{IN}=90MHz
		0	-	0.25	ns	f_{IN}=110MHz
Input Data Position 1	t_{RIP1}	$-t_{SK}$	0	$+t_{SK}$	ns	
Input Data Position 0	t_{RIP0}	$\frac{t_{RCIP}}{7} - t_{SK}$	$\frac{t_{RCIP}}{7}$	$\frac{t_{RCIP}}{7} + t_{SK}$	ns	
Input Data Position 6	t_{RIP6}	$2\frac{t_{RCIP}}{7} - t_{SK}$	$2\frac{t_{RCIP}}{7}$	$2\frac{t_{RCIP}}{7} + t_{SK}$	ns	
Input Data Position 5	t_{RIP5}	$3\frac{t_{RCIP}}{7} - t_{SK}$	$3\frac{t_{RCIP}}{7}$	$3\frac{t_{RCIP}}{7} + t_{SK}$	ns	
Input Data Position 4	t_{RIP4}	$4\frac{t_{RCIP}}{7} - t_{SK}$	$4\frac{t_{RCIP}}{7}$	$4\frac{t_{RCIP}}{7} + t_{SK}$	ns	
Input Data Position 3	t_{RIP3}	$5\frac{t_{RCIP}}{7} - t_{SK}$	$5\frac{t_{RCIP}}{7}$	$5\frac{t_{RCIP}}{7} + t_{SK}$	ns	
Input Data Position 2	t_{RIP2}	$6\frac{t_{RCIP}}{7} - t_{SK}$	$6\frac{t_{RCIP}}{7}$	$6\frac{t_{RCIP}}{7} + t_{SK}$	ns	
Input Modulation Frequency	f_{IMOD}	30	-	300	kHz	
Input Modulation Ratio	r_{IMOD}	-3.0	-	+3.0	%	
DLL Stability Time	t_{DLL}	-	-	100	µs	

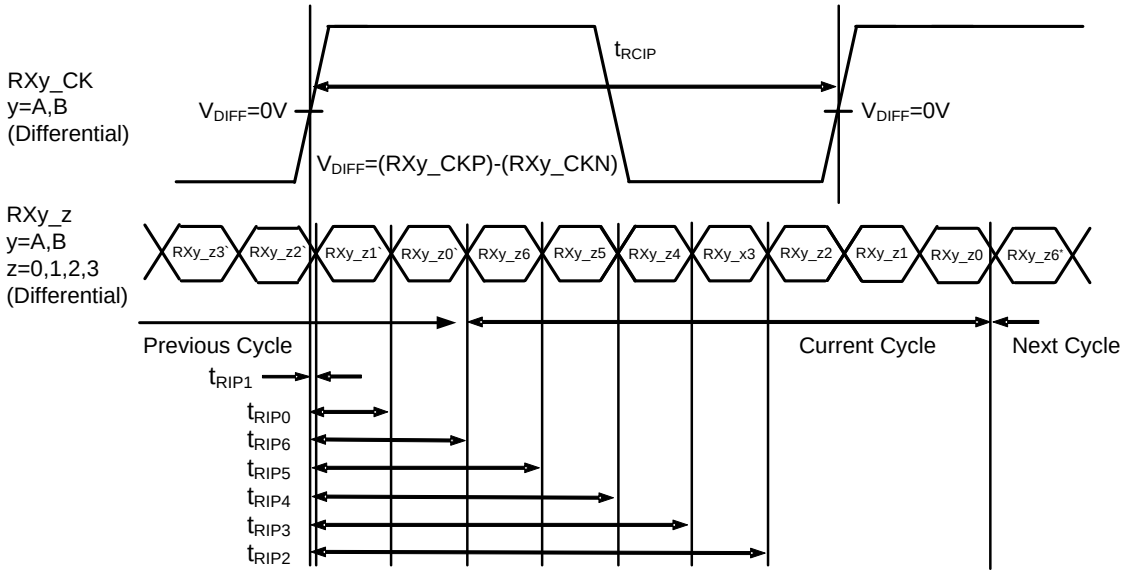


Figure 5. LVDS Receiver AC Characteristics Definition (1)

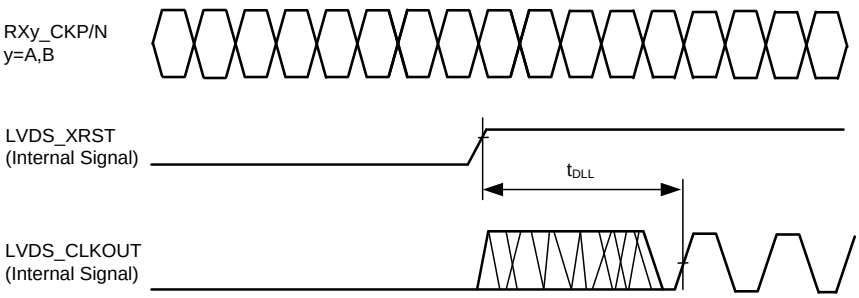


Figure 6. LVDS Receiver AC Characteristics Definition (2)

mini-LVDS Specification

mini-LVDS Transmitter DC Characteristics

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Differential Output Voltage	V_{OD}	200	300	400	mV	R_T=100Ω V_{CM_TX}=1.2V, R_{RPI}=8kΩ
		200	300	400	mV	R_T=100Ω V_{CM_TX}=0.8V, R_{RPI}=5.33kΩ
Common Mode Voltage(Note 13)	V_{CM_TX}	1.0	1.2	1.4	V	(Default)
		0.6	0.8	1.0	V	
PI Resistor	R_{RPI}	5	8	13	kΩ	V_{CM_TX}=1.2V
		3	5.33	9	kΩ	V_{CM_TX}=0.8V

(Note 13) Set it on the parameter of EEPROM.

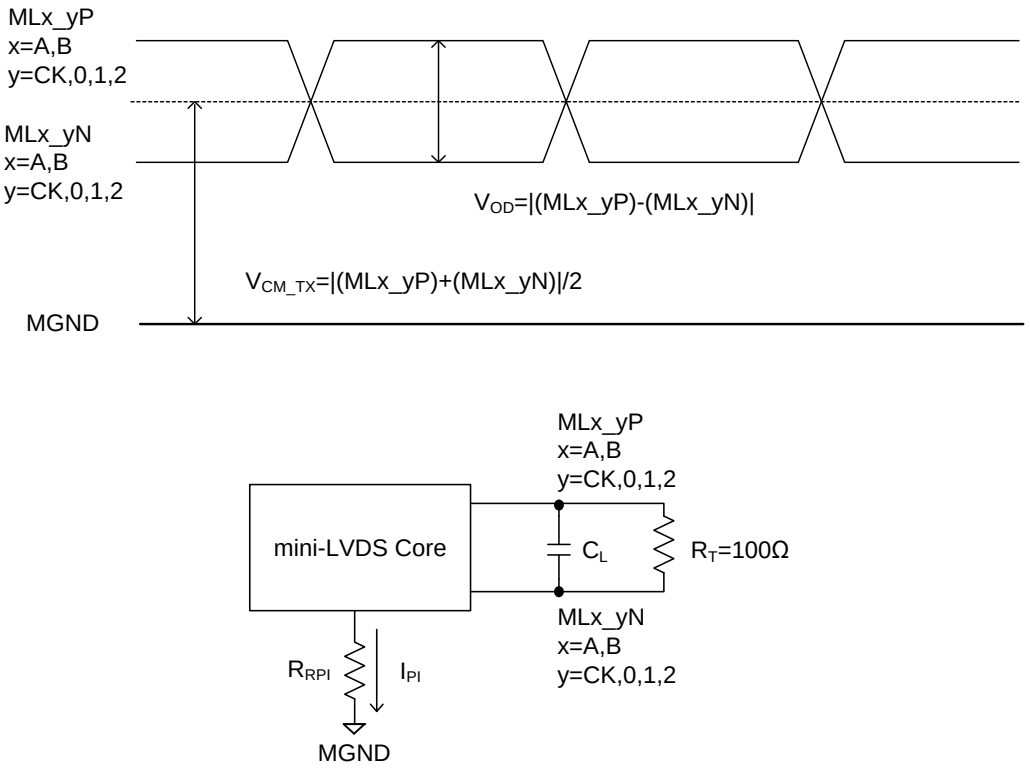


Figure 7. mini-LVDS Transmitter DC Characteristics Definition

mini-LVDS Transmitter DC Characteristics - continued

Differential Output Voltage vs PI Resistor Characteristic

* This data is a simulation value and does not warrant operation.

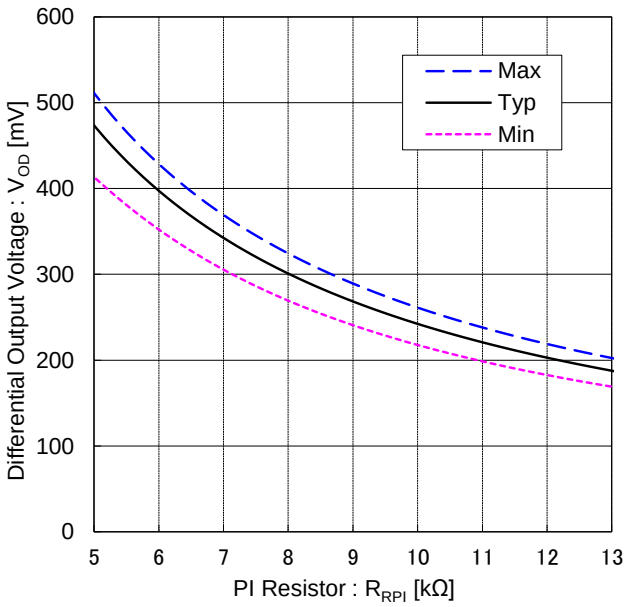


Figure 8. Differential Output Voltage vs PI Resistor (V_{CM_TX}=1.2V)

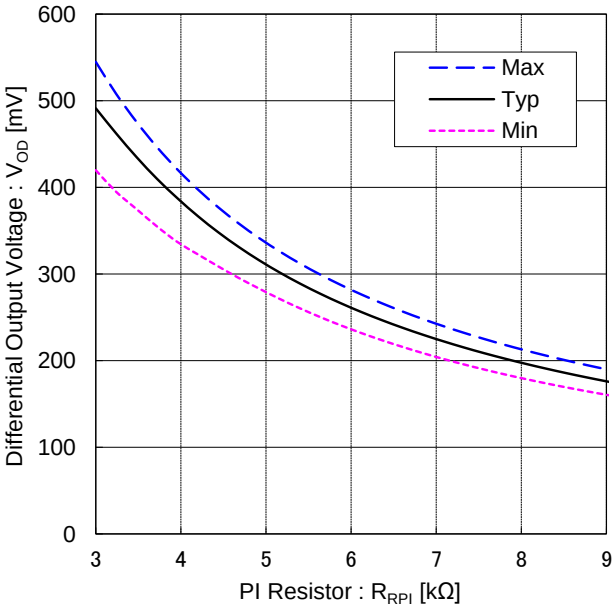


Figure 9. Differential Output Voltage vs PI Resistor (V_{CM_TX}=0.8V)

mini-LVDS Transmitter AC Characteristics

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Clock Frequency	f_{MCLK}	30	-	360	MHz	
Clock Period	t_{MCLK}	2.77	-	33.33	ns	
Data Setup Time	t_{SU}	-	$t_{MCLK}/4$	-	ns	
Data Hold Time	t_H	-	$t_{MCLK}/4$	-	ns	
Clock High Period	t_{MH}	-	$t_{MCLK}/2$	-	ns	
Clock Low Period	t_{ML}	-	$t_{MCLK}/2$	-	ns	
Output Transition Time	t_T	-	500	-	ps	20% to 80%
PLL Lock Up Time	t_{PLL}	-	-	1	ms	

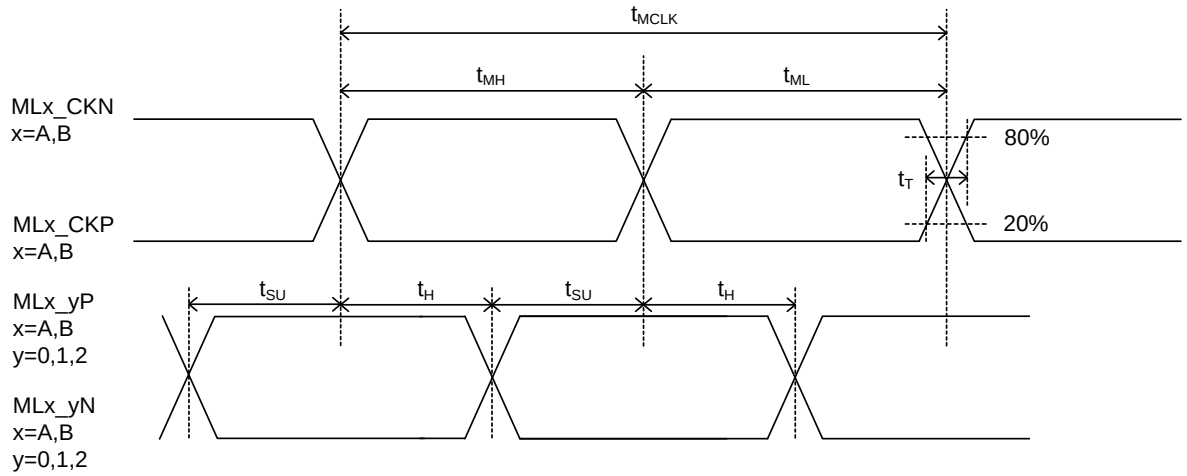


Figure 10. mini-LVDS Transmitter AC Characteristics Definition (1)

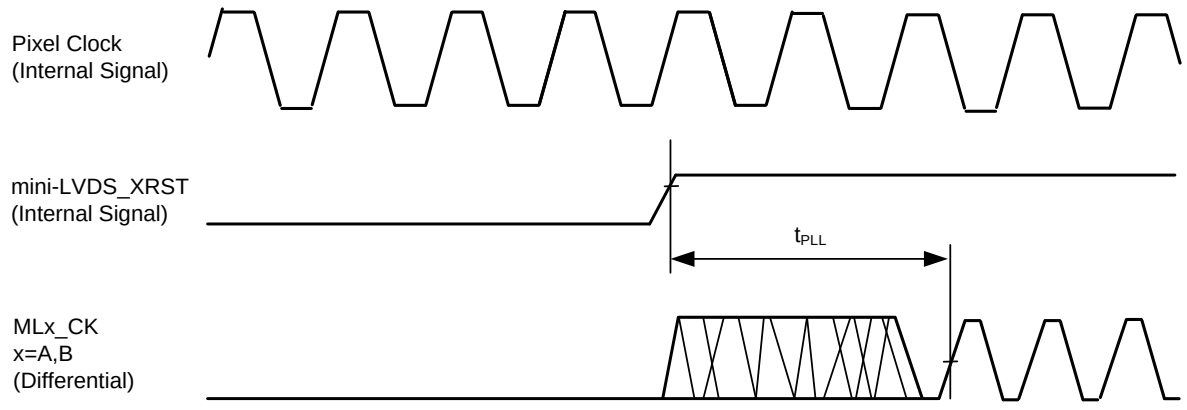


Figure 11. mini-LVDS Transmitter AC Characteristics Definition (2)

mini-LVDS Transmitter AC Characteristics - continued

mini-LVDS Clock Output Phase Adjustment Function

MLVDS_SKEW [2:0] (Note 14)	t_{SU}	t_H
000	$(4/16)t_{MCLK}$	$(4/16)t_{MCLK}$
001	$(3/16)t_{MCLK}$	$(5/16)t_{MCLK}$
010	$(2/16)t_{MCLK}$	$(6/16)t_{MCLK}$
011	$(1/16)t_{MCLK}$	$(7/16)t_{MCLK}$
100	$(4/16)t_{MCLK}$	$(4/16)t_{MCLK}$
101	$(5/16)t_{MCLK}$	$(3/16)t_{MCLK}$
110	$(6/16)t_{MCLK}$	$(2/16)t_{MCLK}$
111	$(7/16)t_{MCLK}$	$(1/16)t_{MCLK}$

(Note 14) Set it on the parameter of EEPROM.

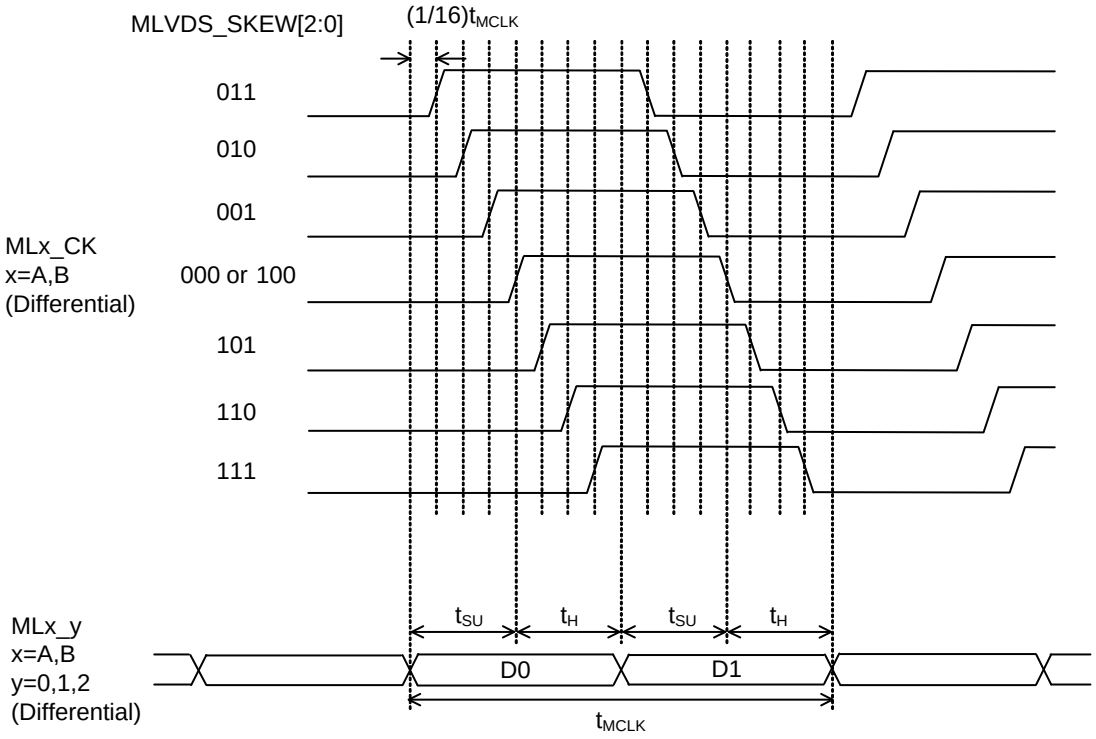


Figure 12. mini-LVDS Transmitter AC Characteristics Definition (3)

Spread Spectrum Clock Generator (SSCG) Specification

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Input Clock Frequency	f_{IN_SS}	20	-	120	MHz	
Output Clock Frequency	f_{OUT_SS}	20	-	120	MHz	
Output Modulation Frequency	f_{OMOD}	30	-	300	kHz	
Output Modulation Ratio	r_{OMOD}	-3.0	-	+3.0	%	(Note 15)
PLL Lock Up Time	t_{PLL_SS}	-	-	100	µs	

(Note 15) The output modulation ratio of up to 3% includes input modulation ratio.

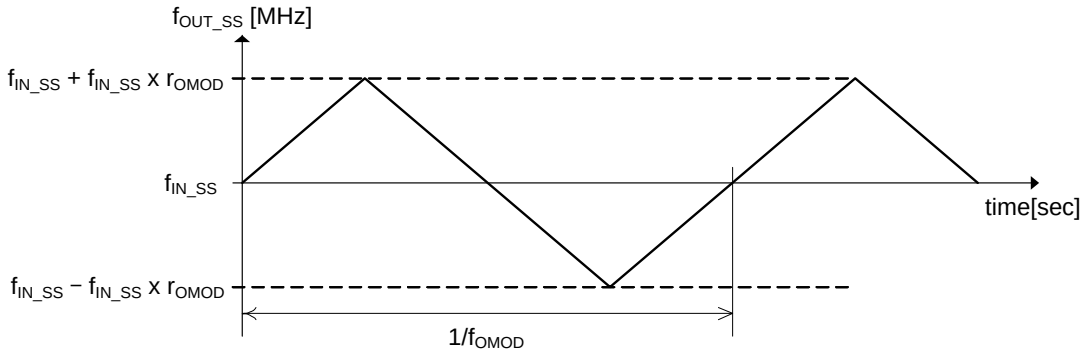


Figure 13. SSCG Profile

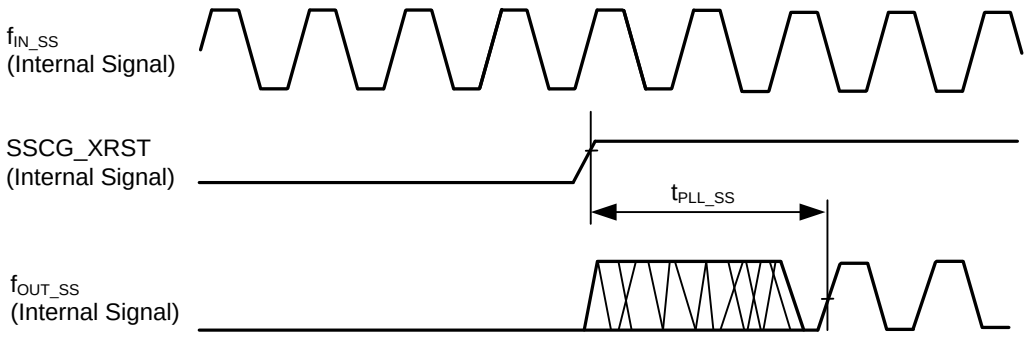


Figure 14. SSCG AC Characteristics Definition

Internal OSC Specification

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Output Clock Frequency(Note 16)	f_{OUT1}	27	30	33	MHz	
	f_{OUT2}	36	40	44	MHz	
	f_{OUT3}	45	50	55	MHz	
	f_{OUT4}	54	60	66	MHz	(Default)
	f_{OUT5}	63	70	77	MHz	
	f_{OUT6}	72	80	88	MHz	
Power On Settling Time	t_{STABLE}	-	-	100	µs	

(Note 16) Set it on the parameter of EEPROM.

I²C/SPI Specification (☆) (Note 17)

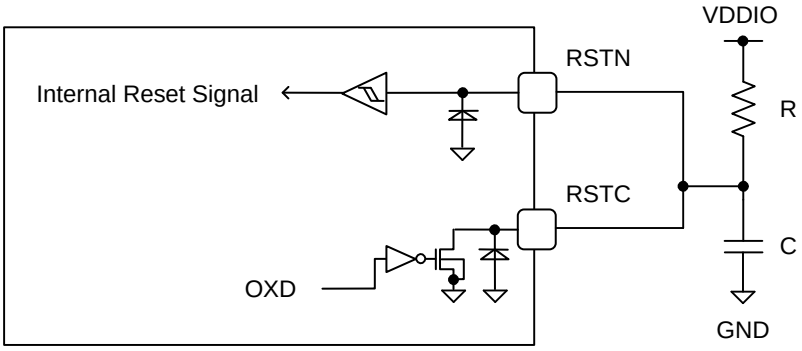
Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
I²C Master Clock Frequency	f_{IMC}	225	250	275	kHz	
I²C Slave Clock Frequency	f_{ISC}	-	-	400	kHz	
SPI Slave Clock Frequency	f_{SSC}	-	-	1000	kHz	

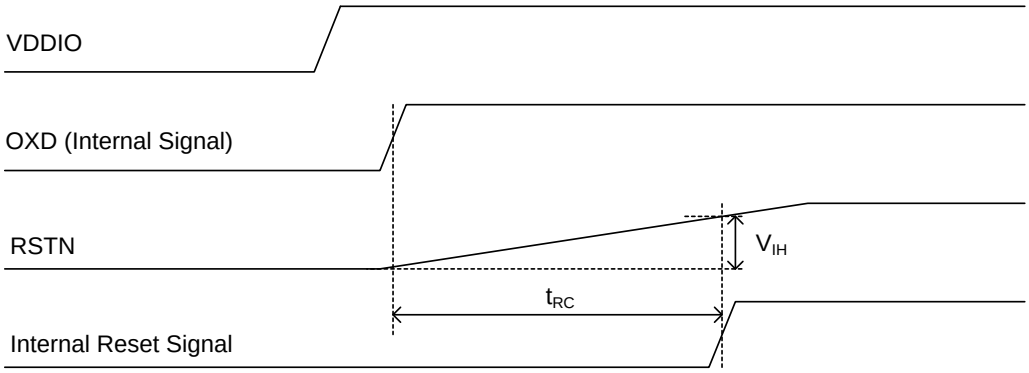
(Note 17) (☆): Special Characteristics

Voltage Detector DC Specification

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Detect Voltage for VDD15	V_{DET15}	0.50	0.70	0.90	V	
Release Voltage for VDD15	V_{RES15}	0.70	0.90	1.10	V	
Hysteresis for VDD15	V_{HYS15}	-	0.2	-	V	$V_{HYS15}=V_{RES15}-V_{DET15}$
Detect Voltage for VDD33(Note 18)	V_{DET33}	1.45	1.65	1.85	V	
Release Voltage for VDD33(Note 18)	V_{RES33}	1.7	1.9	2.1	V	
Hysteresis for VDD33(Note 18)	V_{HYS33}	-	0.25	-	V	$V_{HYS33}=V_{RES33}-V_{DET33}$

(Note 18) VDD33: VDDIO, LVDSVDD, MVDD





t_{RC} : Depend on external R,C value.

V_{IH} : I/O high level input voltage.

Figure 15. Reset Signal Release Timing

Voltage Detector External RC Value

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
RC Time Constant	t_{RC}	1	-	-	ms	
External Resistor	R	8.3	-	20	kΩ	
External Capacitor	C	0.1	-	5	μF	

LDO DC Specification (☆) (Note 19)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Output Voltage	V_{OUT}	1.35	1.50	1.65	V	(Note 20)

(Note 19) (☆): Special Characteristics
(Note 20) Pin No.35 VDD15 connect to GND through 2.2μF capacitor.

Recommended External Capacitor Value

Capacitor Value	Capacitor Change Rate (Tj=-40°C to +105°C)	Tolerance of Capacitor Value
2.2μF	-15% to +15%	-20% to +20%

Timing Chart

Power On/Off Sequence

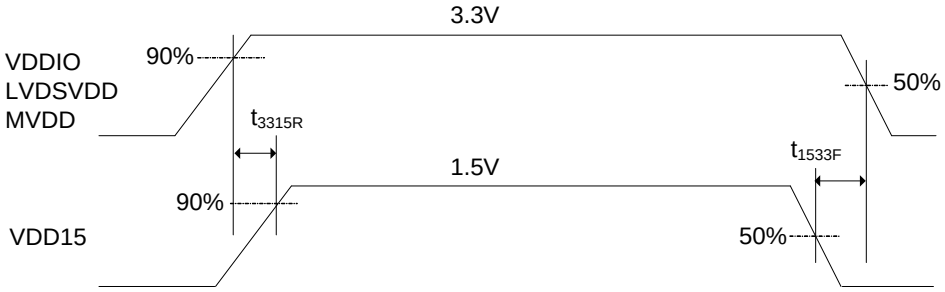


Figure 16. Power Supply Sequence

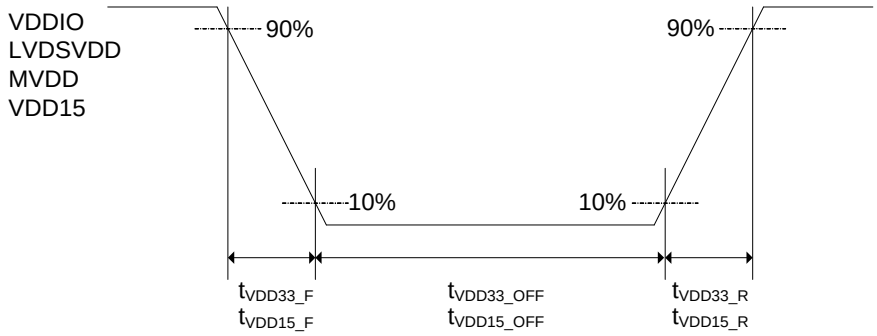


Figure 17. Power Supply Rise and Fall Timing

Power Supply Timing

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
VDD33 to VDD15 Rise Delay Time(Note 21)	t_{3315R}	0	-	-	μs	
VDD15 to VDD33 Fall Delay Time(Note 21)	t_{1533F}	0	-	-	μs	
VDD33 Rise Time(Note 21)	t_{VDD33_R}	-	-	10	ms	
VDD15 Rise Time	t_{VDD15_R}	-	-	10	ms	
VDD33 Fall Time(Note 21)	t_{VDD33_F}	-	-	10	ms	
VDD15 Fall Time	t_{VDD15_F}	-	-	10	ms	
VDD33 Off Time(Note 21)	t_{VDD33_OFF}	100	-	-	ms	
VDD15 Off Time	t_{VDD15_OFF}	100	-	-	ms	

(Note 21) VDD33: VDDIO, LVDSVDD, MVDD

Application Examples

LDO Non-Active Mode, SPI Slave Mode
LVDS: Dual Input (8bit), mini-LVDS: Dual Output 3pair
VDD15 = 1.5V, VDD33 = LVDSVDD = MVDD = VDDIO = 3.3V

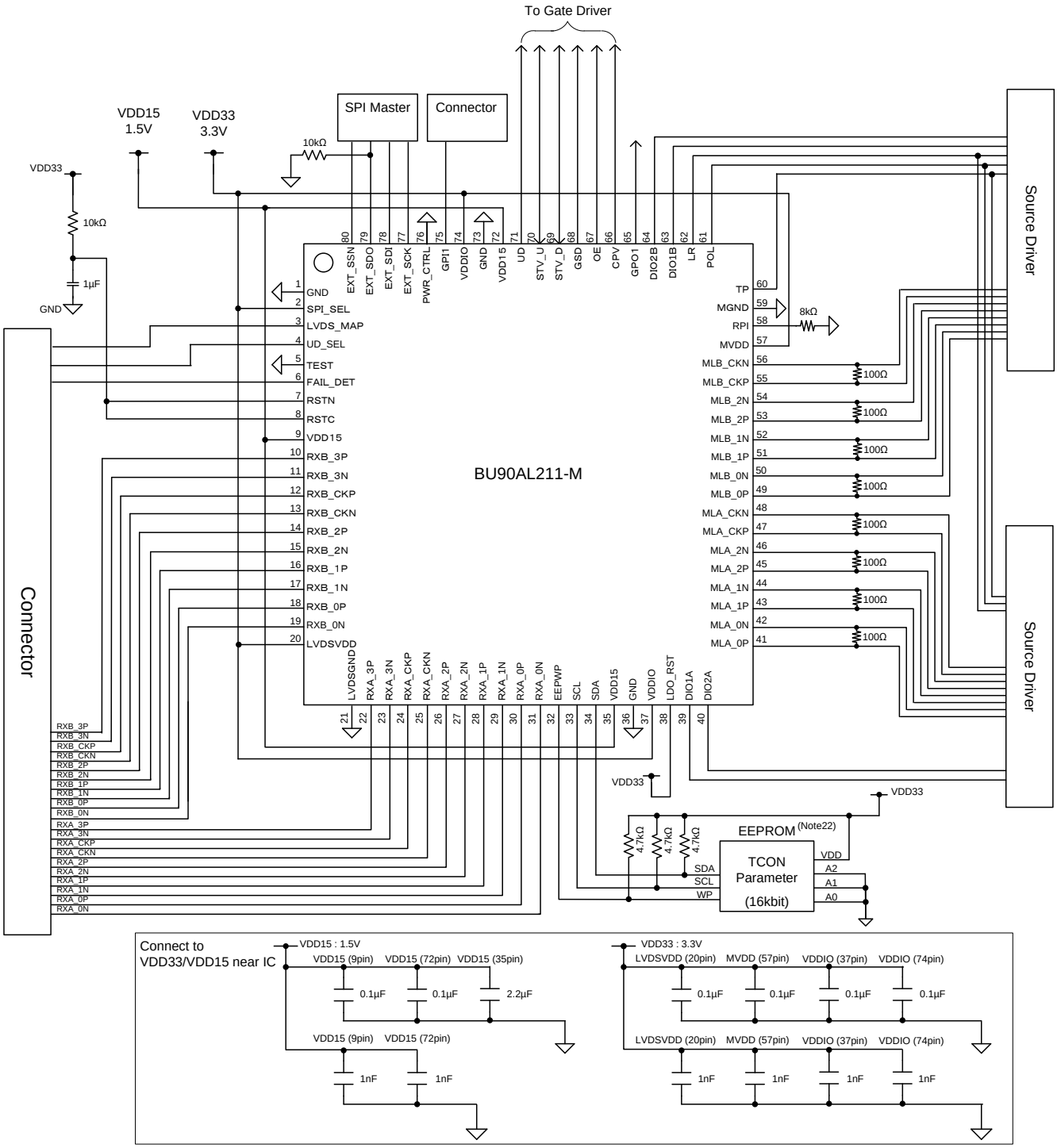


Figure 18. Application Example(1)

(Note 22) Recommended EEPROM: BR24A16F-WM, BR24A16FJ-WM (ROHM)

Application Examples - continued

LDO Active Mode, SPI Slave Mode
LVDS: Dual Input (8bit), mini-LVDS: Single Output 6pair
VDD15 = LDO Output, VDD33 = LVDSVDD = MVDD = VDDIO = 3.3V

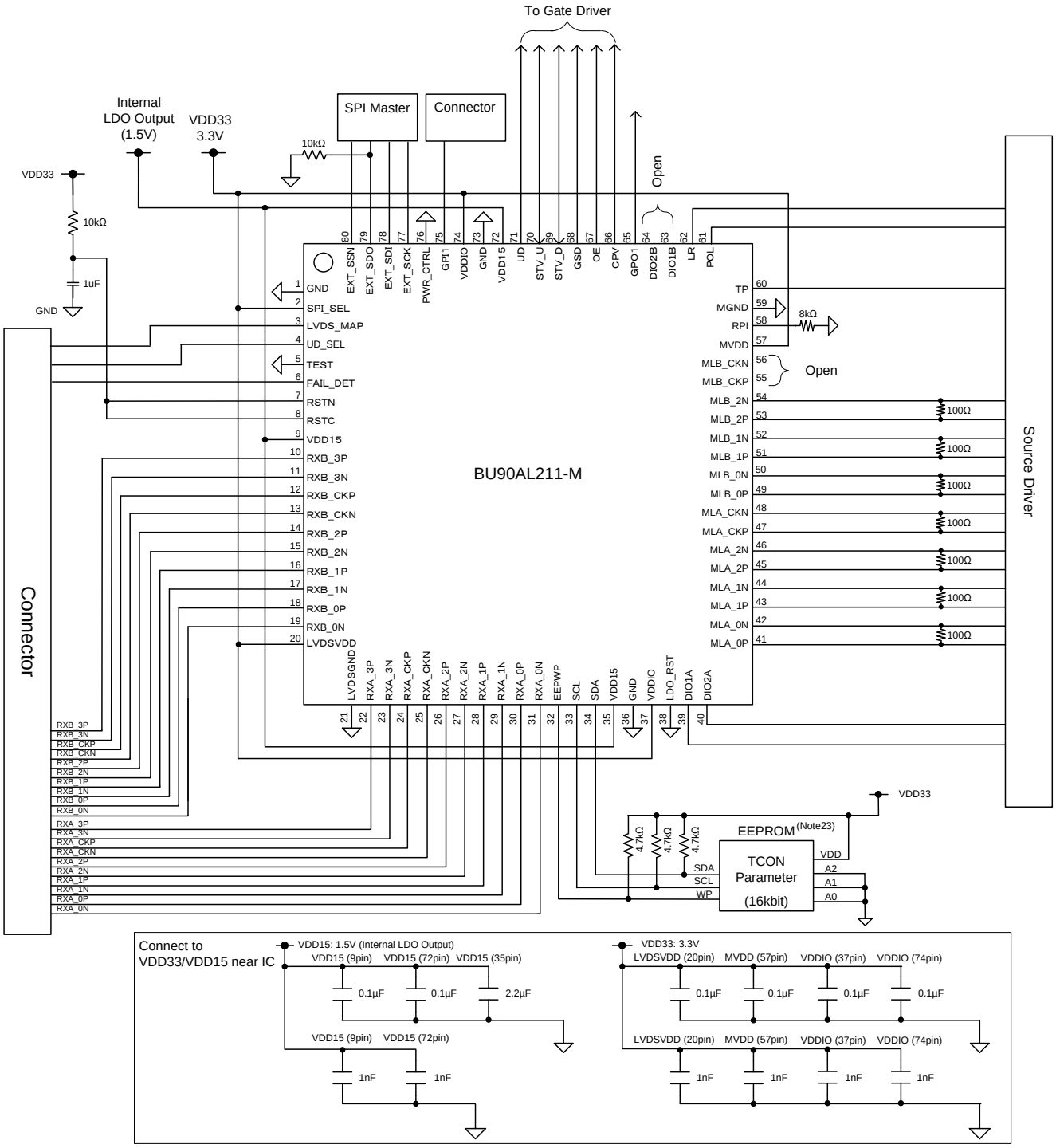


Figure 19. Application Example(2)

(Note 23) Recommended EEPROM: BR24A16F-WM, BR24A16FJ-WM (ROHM)

Application Examples - continued

LDO Active Mode, I²C Slave Mode
LVDS: Single Input (8bit), mini-LVDS: Single Output 6pair
VDD15 = LDO Output, VDD33 = LVDSVDD = MVDD = VDDIO = 3.3V

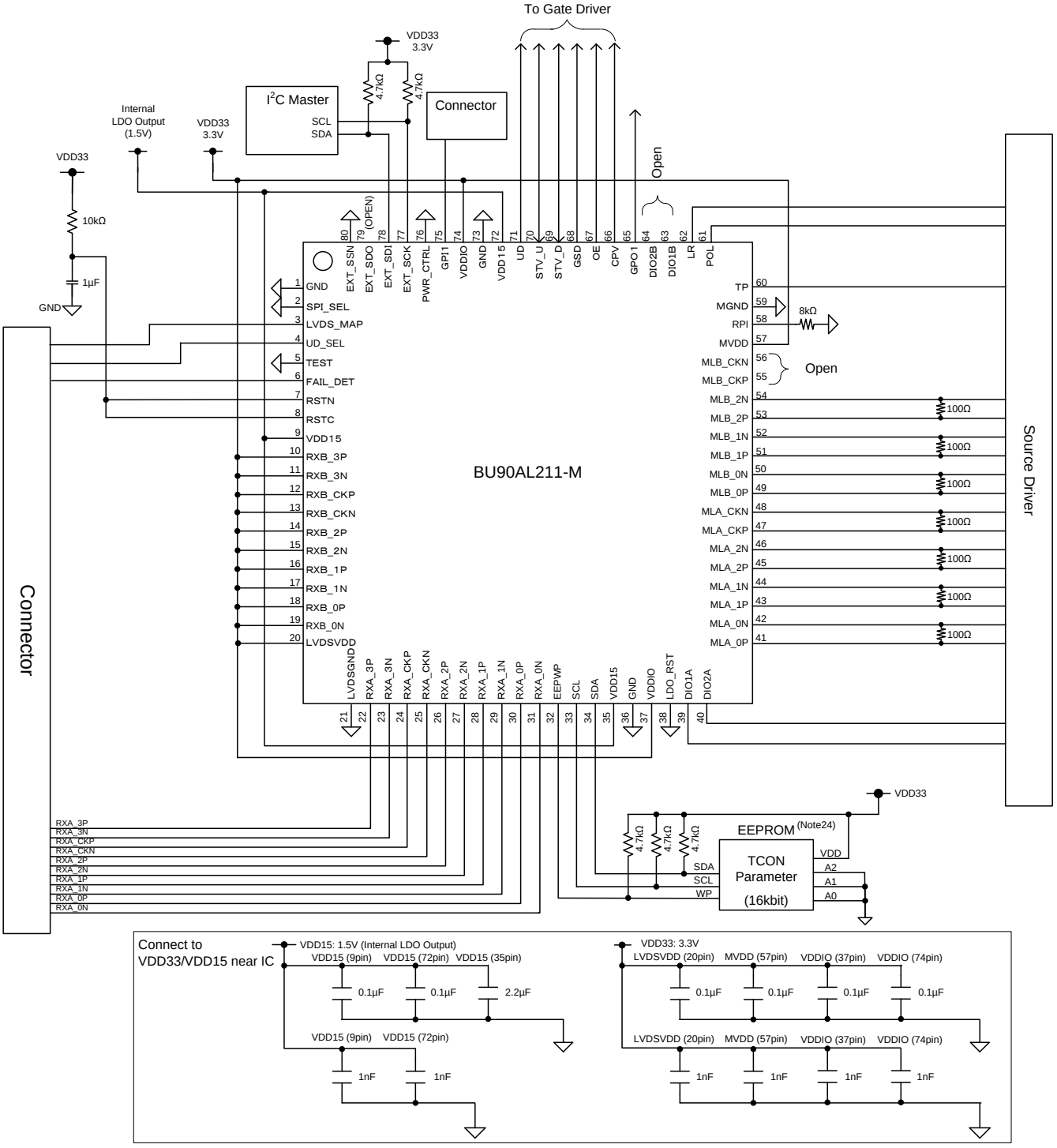


Figure 20. Application Example(3)

(Note 24) Recommended EEPROM: BR24A16F-WM, BR24A16FJ-WM (ROHM)

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the maximum junction temperature rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. **Regarding the Input Pin of the IC**
    In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

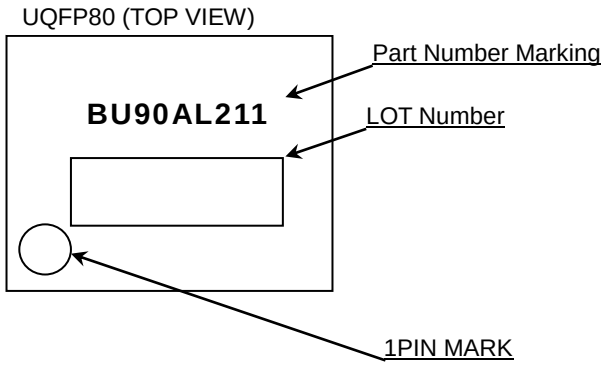
Ordering Information

B U 9 0 A L 2 1 1	-	ME2

Part Number

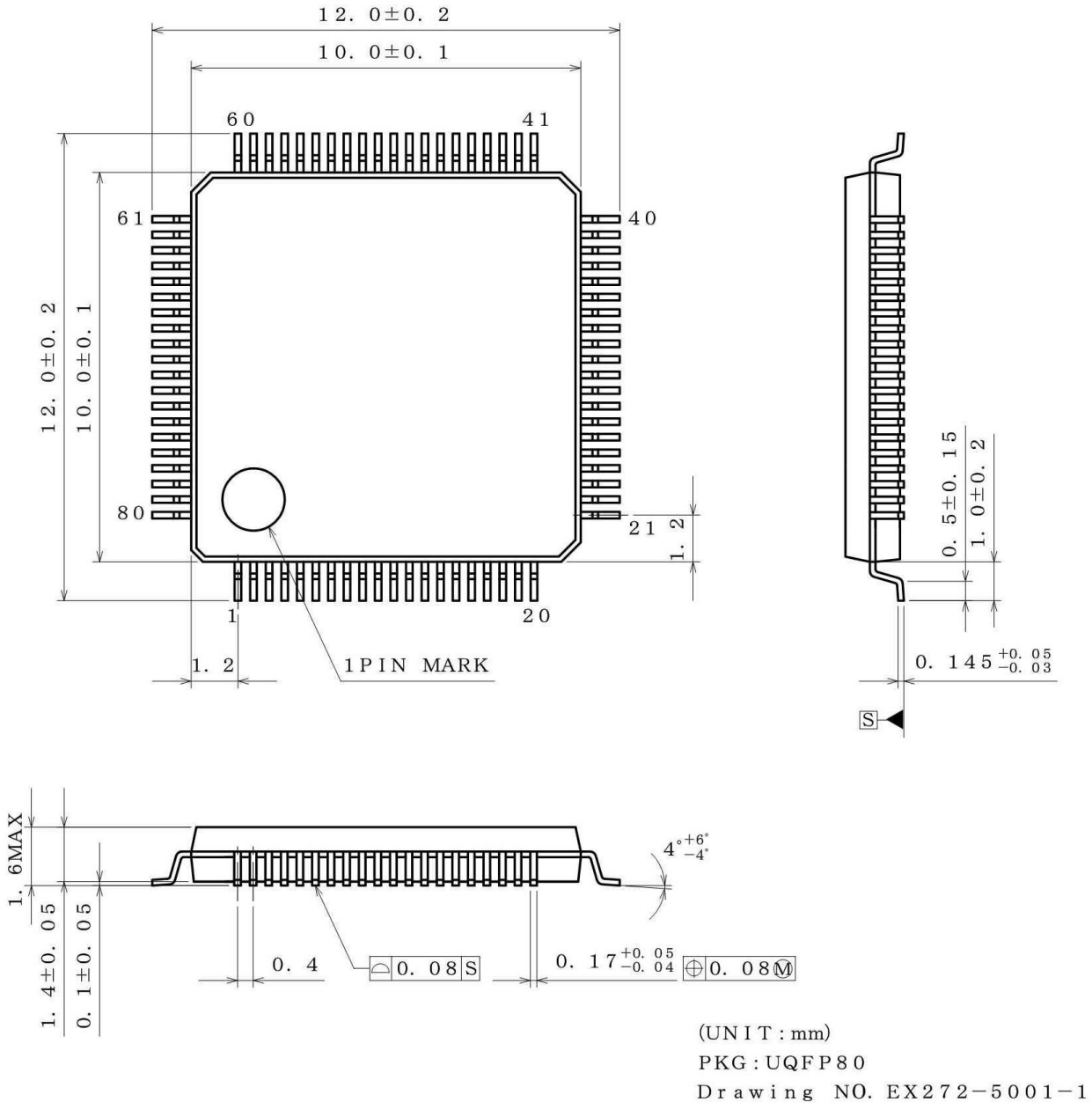
Product Rank
M: Automotive
Packaging and forming specification
E2: Embossed tape and reel

Marking Diagrams



Physical Dimension, Tape and Reel Information

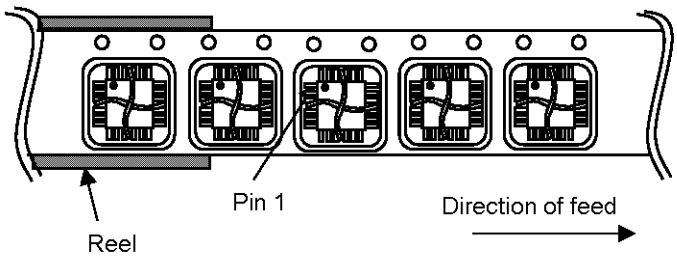
Package Name	UQFP80



(UNIT : mm)
PKG : UQFP80
Drawing NO. EX272−5001−1

< Tape and Reel Information >

Tape	Embossed carrier tape with dry pack
Quantity	1000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
24.Feb.2017	001	New Release

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1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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