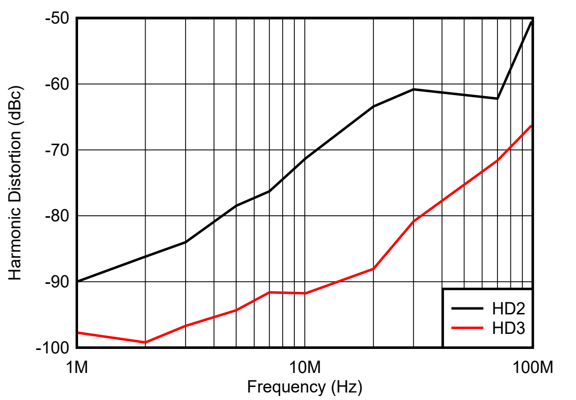
OPA695 具有禁用功能的超宽带电流反馈运算放大器

1 特性

- 高带宽：
  - 1900MHz (G = +1V/V)
  - 600MHz (G = +8V/V)
- 大信号带宽 ($2V_{PP}$)：540MHz
- 输出电压摆幅：±4.05V
- 超高压摆率：5000V/μs
- 输入电压噪声：2nV/√Hz
- 低失真（R_L = 100Ω，V_O = $2V_{PP}$）：
  - 10MHz 时的 HD2、HD3：–65dBc、–92dBc
- 高输出电流：±140mA
- 电源电压范围：5V 至 12V
- 电源电流：14mA
- 关断电流：160μA

2 应用

- 超宽带 ADC 驱动器
- 低成本精密 IF 放大器
- 宽带视频线路驱动器
- 便携式仪器
- 有源滤波器
- 任意波形发生器
- 电流 DAC 驱动器



增益为 +8V/V 时谐波失真随频率的变化

3 说明

OPA695 是一款高带宽电流反馈运算放大器，具有出色的 5000V/μs 压摆率和低输入电压噪声，可提供精密、低失真、高动态范围放大器，以便在高速仪表系统中用作中间增益级。OPA695 针对高增益运行进行了优化，非常适合用于连接电流 DAC 输出，或用作高速数字转换器中的增益级，或用于为电缆调制解调器上行线路驱动器提供高输出功率和低失真。

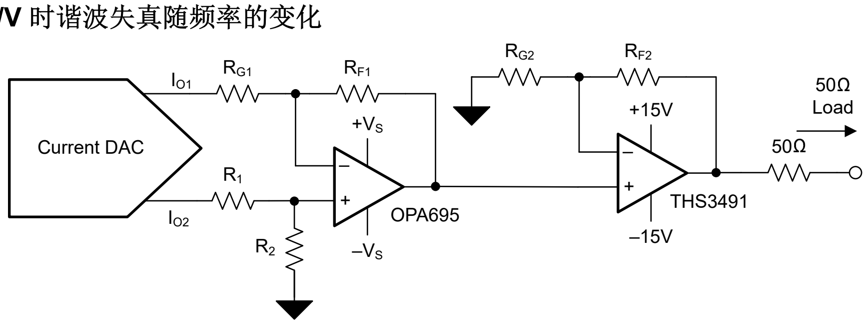
OPA695 具有 14mA 的低电源电流（在 25°C 条件下）。使用可选的禁用控制引脚可以进一步降低系统功耗。该引脚保持开路或保持高电平可使器件正常运行。如果被拉至低电平，OPA695 电源电流将降至小于 160μA。这一省电特性连同出色的 5V 单电源供电特性和超小型 SOT23-6 封装，使得 OPA695 成为便携式应用的理想选择。

OPA695 具有 -40°C 至 +85°C 的宽额定工作温度范围。

封装信息

器件型号	封装[1]	封装尺寸[2]
OPA695	D（SOIC，8）	4.9mm × 6mm
	DBV（SOT-23，6）	2.9mm × 2.8mm
	DGK（VSSOP，8）	3mm × 4.9mm

(1) 有关更多信息，请参阅节 10。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



典型的任意波形发生器输出驱动电路

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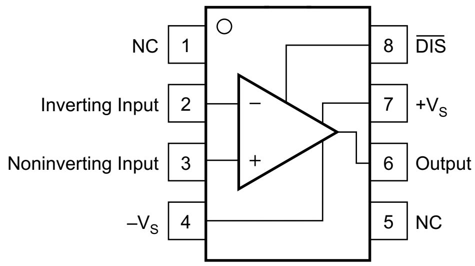
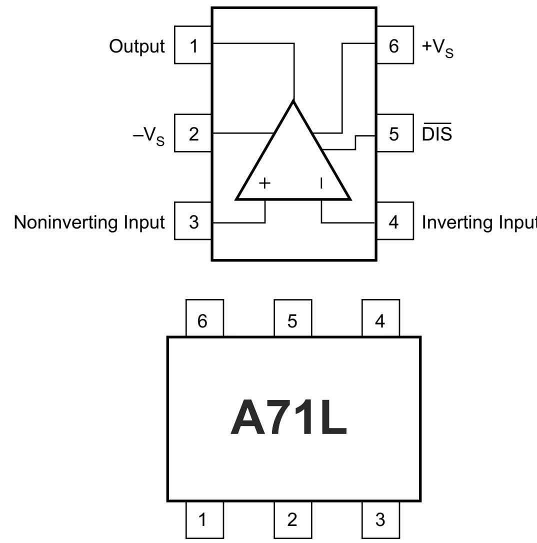
4 Pin Configuration and Functions



NC = No Connection

图 4-1. D Package, 8-Pin SOIC, and DGK Package, 8-Pin VSSOP (Top View)



Pin Orientation/Package Marking

图 4-2. DBV Package, 6-Pin SOT-23 (Top View)

表 4-1. Pin Functions

PIN			TYPE[1]	DESCRIPTION
NAME	NO.			
	D (SOIC), DGK (VSSOP)	DBV (SOT-23)		
$\overline{DIS}$	8	5	I	Not disable (enable)
Inverting input	2	4	I	Inverting input
NC	1, 5	—	—	Not connected
Noninverting input	3	3	I	Noninverting input
Output	6	1	O	Output
– V_S	4	2	P	Negative supply
+V_S	7	6	P	Positive supply

(1) I = input, O = output, P = power

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
V_S	Total supply voltage, $V_S = (V_{S+}) - (V_{S-})$		13	V
V_{ID}	Differential input voltage		±1.2	V
V_I	Input common-mode voltage		$\pm V_S$	V
	Internal power dissipation	See *Thermal Analysis*		
I_{IN}	Continuous input current		±10	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	125	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins expect Inverting Input[(1)]	±1500	V
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, Inverting Input[(1)]	±500	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[(2)]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{S+} - V_{S-}$	Total supply voltage	5		12	V
T_A	Ambient operating air temperature	–40	25	85	°C

5.4 Thermal Information

THERMAL METRIC[(1)]		OPA695			UNIT
		D (SOIC)	DBV (SOT 23)	DGK (VSSOP)	
		8 PINS	6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	136	164	135	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78	80	81	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	85	49	56	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	24	28	8.5	°C/W
Y_{JB}	Junction-to-board characterization parameter	84	49	48	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics V_S = ±5 V, OPA695ID, OPA695IDBV

at T_A = +25°C, G = +8 V/V, R_F = 402 Ω, and R_L = 100 Ω to V_S/2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE							
SSBW	Small-signal bandwidth	V_O = 0.5 V_{PP}	G = +1 V/V, R_F = 523Ω		1900		MHz
			G = +2 V/V, R_F = 511Ω		900		
			G = +8 V/V, R_F = 402Ω		600		
			G = +16 V/V, R_F = 249Ω		500		
	Bandwidth for 0.2-dB gain flatness	V_O = 0.5 V_{PP}, G = +2 V/V, R_F = 511 Ω			120		MHz
	Peaking at a gain of +1V/V	V_O = 0.5 V_{PP}, R_F = 523 Ω			3.7		dB
LSBW	Large-signal bandwidth	V_O = 4 V_{PP}, G = +8 V/V			510		MHz
SR	Slew rate	V_O = 4-V step	G = –8 V/V		5000		V/μs
			G = +8 V/V		5000		V/μs
	Rise and fall time	G = +8 V/V	V_O = 0.5-V step		0.65		ns
			V_O = 4-V step		0.7		
	Settling time	To 0.5%, V_O = 2-V step, G = +8 V/V			10		ns
HD2	2nd-order harmonic distortion	f = 10 MHz	V_O = 2 V_{PP}, R_L = 100 Ω		–75		dBc
			V_O = 2 V_{PP}, R_L = 500 Ω		–78		
HD3	3rd-order harmonic distortion	f = 10 MHz	V_O = 2 V_{PP}, R_L = 100 Ω		–92		dBc
			V_O = 2 V_{PP}, R_L = 500 Ω		–86		
e_n	Input voltage noise	f > 1 MHz			2		nV/√Hz
i_{n+}	Noninverting input current noise	f > 1 MHz			14		pA/√Hz
i_{n-}	Inverting input current noise	f > 1 MHz			22		pA/√Hz
DC PERFORMANCE							
Z_{OL}	Open-loop transimpedance gain			45	300		kΩ
		T_A = –40°C to +85°C		41			
V_{OS}	Input offset voltage	V_{CM} = 0 V			±0.3	±3	mV
			T_A = –40°C to +85°C			±4	
	Average input offset voltage drift	V_{CM} = 0 V, T_A = –40°C to +85°C			3	±15	μV/°C
	Noninverting input bias current	V_{CM} = 0 V			13	±30	μA
			T_A = –40°C to +85°C			±41	
	Average noninverting input bias current drift	V_{CM} = 0 V, T_A = –40°C to +85°C			60	180	nA/°C
	Inverting input bias current	V_{CM} = 0 V			±5	±60	μA
			T_A = –40°C to +85°C			±70	
	Average inverting input bias current drift	V_{CM} = 0 V, T_A = –40°C to +85°C			±16	±160	nA/°C
INPUT CHARACTERISTICS							
CMIR	Common-mode input range[1]			±3.1	±3.4		V
		T_A = –40°C to +85°C		±3.0			
CMRR	Common-mode rejection ratio	V_{CM} = 0 V		51	65		dB
			T_A = –40°C to +85°C	50			
	Noninverting input impedance				450 || 2		kΩ || pF

5.5 Electrical Characteristics V_S = ±5 V, OPA695ID, OPA695IDBV（续）

at T_A = +25°C, G = +8 V/V, R_F = 402 Ω, and R_L = 100 Ω to V_S/2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Inverting input resistance	Open-loop		20		Ω

5.5 Electrical Characteristics V_S = ±5 V, OPA695ID, OPA695IDBV（续）

at T_A = +25°C, G = +8 V/V, R_F = 402 Ω, and R_L = 100 Ω to V_S/2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT CHARACTERISTICS							
	Output voltage swing	No load		±3.95	±4.05		V
			T_A = –40°C to +85°C	±3.85			
		R_L = 100 Ω		±3.65	±3.75		
			T_A = –40°C to +85°C	±3.55			
I_O	Output current, sourcing	V_O = 0 V		90	140		mA
			T_A = –40°C to +85°C	70			
	Output current, sinking	V_O = 0 V			–140	–90	mA
			T_A = –40°C to +85°C			–70	
Z_O	Closed-loop output impedance	G = +8 V/V, f = 100 kHz			0.02		Ω
POWER SUPPLY							
I_Q	Quiescent current			11.7	14	15.6	mA
		T_A = –40°C to +85°C		10		18	
–PSRR	Negative power-supply rejection ratio			51	72		dB
		T_A = –40°C to +85°C		48			
DISABLE (Disabled LOW)							
	Power-down quiescent current	$V_{\overline{DIS}}$ = 0 V			160	200	µA
			T_A = –40°C to +85°C			210	
	Disable time	V_{IN} = ±0.25 V_{DC}			4		µs
	Enable time	V_{IN} = ±0.25 V_{DC}			80		ns
	Off Isolation	G = +8 V/V, f = 10 MHz			70		dB
	Output capacitance in disable				2.5		pF
	Enable voltage threshold				3	3.5	V
		T_A = –40°C to +85°C				3.7	
	Disable voltage threshold			1.7	2.3		V
		T_A = –40°C to +85°C		1.5			
	$\overline{DIS}$ control pin input bias current	$V_{\overline{DIS}}$ = 0 V			95	130	µA
			T_A = –40°C to +85°C			145	

(1) Tested < 3 dB below minimum specified CMRR at ± CMIR limits.

5.6 Electrical Characteristics V_S = 5 V, OPA695ID, OPA695IDBV

at T_A = +25°C, G = +8 V/V, R_F = 348 Ω, and R_L = 100 Ω to V_S/2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE							
SSBW	Small-signal bandwidth	V_O = 0.5 V_{PP}	G = +1 V/V, R_F = 511Ω		1200		MHz
			G = +2 V/V, R_F = 487Ω		700		
			G = +8 V/V, R_F = 348Ω		500		
			G = +16 V/V, R_F = 162Ω		410		
	Bandwidth for 0.2-dB gain flatness	V_O = 0.5 V_{PP}, G = +2 V/V, R_F = 487 Ω			110		MHz
	Peaking at a gain of +1 V/V	V_O = 0.5 V_{PP}, R_F = 511 Ω			2.2		dB
LSBW	Large-signal bandwidth	V_O = 2 V_{PP}, G = +8 V/V			430		MHz
SR	Slew rate	V_O = 2-V step, G = +8 V/V			2500		V/μs
	Rise and fall time	G = +8 V/V	V_O = 0.5-V step		0.7		ns
			V_O = 2-V step		0.8		
	Settling time to 0.5%	V_O = 2-V step. G = +8 V/V			10		ns
HD2	2nd-order harmonic distortion	f = 10 MHz	V_O = 2 V_{PP}, R_L = 100 Ω		–69		dBc
			V_O = 2 V_{PP}, R_L = 500 Ω		–68		
HD3	3rd- order harmonic distortion	f = 10 MHz	V_O = 2 V_{PP}, R_L = 100 Ω		–62		dBc
			V_O = 2 V_{PP}, R_L = 500 Ω		–63		
e_n	Input voltage noise	f > 1 MHz			1.9		nV/√Hz
i_{n+}	Noninverting input current noise	f > 1 MHz			14		pA/√Hz
i_{n-}	Inverting input current noise	f > 1 MHz			22		pA/√Hz
DC PERFORMANCE							
Z_{OL}	Open-loop transimpedance gain			40	250		kΩ
		T_A = –40°C to +85°C		36			
V_{OS}	Input offset voltage	V_{CM} = V_S/2			±0.3	±3	mV
			T_A = –40°C to +85°C			±4	
	Average input offset voltage drift	V_{CM} = V_S/2, T_A = –40°C to +85°C			±4	±15	μV/°C
	Noninverting input bias current	V_{CM} = V_S/2			15	±40	μA
			T_A = –40°C to +85°C			±50	
	Average noninverting input bias current drift	V_{CM} = V_S/2, T_A = –40°C to +85°C			60	±170	nA/°C
	Inverting input bias current	V_{CM} = V_S/2			±5	±60	μA
			T_A = –40°C to +85°C			±70	
	Average inverting input bias current drift	V_{CM} = V_S/2, T_A = –40°C to +85°C			±16	±160	nA/°C
INPUT CHARACTERISTICS							
CMIR	Common-mode input range (positive)			3.2	3.4		V
		T_A = –40°C to +85°C		3.1			
	Common-mode input range (negative)				1.6	1.8	
		T_A = –40°C to +85°C				1.9	
CMRR	Common-mode rejection ratio	V_{CM} = V_S/2		51	65		dB
			T_A = –40°C to +85°C	50			

5.6 Electrical Characteristics V_S = 5 V, OPA695ID, OPA695IDBV（续）

at T_A = +25°C, G = +8 V/V, R_F = 348 Ω, and R_L = 100 Ω to V_S/2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Noninverting input resistance			250 || 2		kΩ || pF
	Inverting input resistance	Open-loop		21		Ω

5.6 Electrical Characteristics V_S = 5 V, OPA695ID, OPA695IDBV（续）

at T_A = +25°C, G = +8 V/V, R_F = 348 Ω, and R_L = 100 Ω to V_S/2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT CHARACTERISTICS							
V_O	Output voltage swing (most positive)	No load		3.95	4.05		V
			T_A = –40°C to 85°C	3.75			
	Output voltage swing (least positive)	No load			0.9	1.05	
			T_A = –40°C to +85°C			1.25	
I_O	Output current, sourcing	V_O = V_S/2		70	100		mA
			T_A = –40°C to +85°C	66			
	Output current, sinking	V_O = V_S/2			–100	–70	
			T_A = –40°C to +85°C			–60	
Z_{OUT}	Closed-loop output impedance	G = +2 V/V, f = 100 kHz			0.02		Ω
POWER SUPPLY							
I_Q	Quiescent current			10.9	13	14.4	mA
		T_A = –40°C to +85°C		9.1		17.1	
–PSRR	Negative power-supply rejection ratio				69		dB
DISABLE (Disabled LOW)							
	Power-down quiescent current (+V_S)	$V_{\overline{DIS}}$ = 0 V			120	160	µA
			T_A = –40°C to +85°C			180	
	Disable time	V_{IN} = ±0.25 V_{DC}			5		µs
	Enable time	V_{IN} = ±0.25 V_{DC}			80		ns
	Off isolation	G = +8 V/V, f = 10 MHz			70		dB
	Output capacitance in disable				2.5		pF
	Enable voltage threshold				3.1	3.5	V
		T_A = –40°C to +85°C				3.7	
	Disable voltage threshold			1.7	2.4		V
		T_A = –40°C to +85°C		1.5			
	$\overline{DIS}$ control pin input bias current				95	130	µA
		T_A = –40°C to +85°C				149	

5.7 Electrical Characteristics V_S = ±5 V, OPA695IDGK

at T_A = +25°C, G = +8 V/V, V_S = ± 5 V, R_F = 402 Ω, and R_L = 100 Ω to V_S /2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE							
SSBW	Small-signal bandwidth	V_O = 0.5 V_{PP}	G = +1 V/V, R_F = 523Ω		1700		MHz
			G = +2 V/V, R_F = 511Ω		1400		
			G = +8 V/V, R_F = 402Ω		450		
			G = +16 V/V, R_F = 249Ω		350		
	Bandwidth for 0.2-dB gain flatness	G = +2 V/V, V_O = 0.5 V_{PP}, R_F = 511 Ω			320		MHz
	Peaking at a gain of +1V/V	R_F = 523 Ω, V_O = 0.5 V_{PP}			4.6		dB
LSBW	Large-signal bandwidth	G = +8 V/V, V_O = 4 V_{PP}			450		MHz
SR	Slew rate	V_O = 4-V step	G = –8 V/V		4300		V/μs
			G = +8 V/V		2900		
	Rise and fall time	G = +8 V/V	V_O = 0.5-V step		0.8		ns
			V_O = 4-V step		1		
	Settling time	V_O = 2-V step, 0.02%			16		ns
		V_O = 2-V step, 0.1%			10		
HD2	2nd-order harmonic distortion	f = 10 MHz	V_O = 2 V_{PP}, R_L = 100 Ω		–65		dBc
			V_O = 2 V_{PP}, R_L = 500 Ω		–78		
HD3	3rd-order harmonic distortion	f = 10 MHz	V_O = 2 V_{PP}, R_L = 100 Ω		–86		dBc
			V_O = 2 V_{PP}, R_L = 500 Ω		–86		
e_n	Input voltage noise	f > 1 MHz			1.8		nV/√Hz
i_{n+}	Noninverting input current noise	f > 1 MHz			18		pA/√Hz
i_{n-}	Inverting input current noise	f > 1 MHz			22		pA/√Hz
DC PERFORMANCE							
Z_{OL}	Open-loop transimpedance gain	V_O = 0 V		45	85		kΩ
			T_A = –40°C to +85°C	41			
V_{OS}	Input offset voltage	V_{CM} = 0 V			±0.3	±3	mV
			T_A = –40°C to +85°C			±4	
	Average input offset voltage drift	V_{CM} = 0 V, T_A = –40°C to +85°C				±15	μV/°C
	Noninverting input bias current	V_{CM} = 0 V			13	±30	μA
			T_A = T_A = –40°C to +85°C			±41	
	Average noninverting input bias current drift	V_{CM} = 0 V, T_A = T_A = –40°C to +85°C				+150	nA/°C
	Inverting input bias current	V_{CM} = 0 V			±20	±60	μA
			T_A = T_A = –40°C to +85°C			±70	
	Average inverting input bias current drift	V_{CM} = 0 V, T_A = T_A = –40°C to +85°C				±160	nA/°C
INPUT CHARACTERISTICS							
CMIR	Common-mode input range[1]			±3.1	±3.3		V
		T_A = –40°C to +85°C		±3			
CMRR	Common-mode rejection ratio	V_{CM} = 0 V		51	56		dB
			T_A = –40°C to +85°C	50			

5.7 Electrical Characteristics V_S = ±5 V, OPA695IDGK（续）

at T_A = +25°C, G = +8 V/V, V_S = ± 5 V, R_F = 402 Ω, and R_L = 100 Ω to V_S /2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Noninverting input impedance			280 || 1.2		kΩ || pF
R_I	Inverting input resistance	Open-loop		29		Ω

5.7 Electrical Characteristics V_S = ±5 V, OPA695IDGK （续）

at T_A = +25°C, G = +8 V/V, V_S = ± 5 V, R_F = 402 Ω, and R_L = 100 Ω to V_S /2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT CHARACTERISTICS							
V_O	Output voltage swing	No load		±4	±4.2		V
			T_A = –40°C to +85°C	±3.9			
		R_L = 100 Ω		±3.7	±3.9		V
			T_A = –40°C to +85°C	±3.6			
I_O	Output current, sourcing	V_O = 0 V		90	120		mA
			T_A = –40°C to +85°C	70			
	Output current, sinking	V_O = 0 V			–120	–90	mA
			T_A = –40°C to +85°C			–70	mA
Z_{OUT}	Closed-loop output impedance	G = +8 V/V, f = 100 kHz			0.04		Ω
POWER SUPPLY							
I_Q	Quiescent current			12.6	12.9	13.3	mA
		T_A = –40°C to +85°C		11		14.1	
–PSRR	Negative power-supply rejection ratio			51	55		dB
		T_A = –40°C to +85°C		48			
DISABLE (Disabled LOW)							
	Power-down quiescent current (+V_S)	$V_{\overline{DIS}}$ = 0 V			100	170	μA
			T_A = –40°C to +85°C			192	
	Disable time	V_{IN} = ±0.25 V_{DC}			1		μs
	Enable time	V_{IN} = ±0.25 V_{DC}			25		ns
	Off Isolation	G = +8 V/V, f = 10 MHz			70		dB
	Output capacitance in disable				4		pF
	Turn-on glitch	G = +2 V/V, R_L = 150 Ω, V_{IN} = 0 V			±100		mV
	Turn-off glitch	G = +2 V/V, R_L = 150 Ω, V_{IN} = 0 V			±20		mV
	Enable voltage threshold				3.3	3.5	V
		T_A = –40°C to +85°C				3.7	
	Disable voltage threshold			1.7	1.8		V
		T_A = –40°C to +85°C		1.5			
	$\overline{DIS}$ control pin input bias current				75	130	μA
		T_A = –40°C to +85°C				145	

(1) Tested < 3 dB below minimum specified CMRR at ± CMIR limits.

5.8 Electrical Characteristics V_S = 5 V, OPA695IDGK

at T_A = +25°C, G = +8 V/V, V_S = 5 V, R_F = 348 Ω, and R_L = 100 Ω to V_S /2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE							
SSBW	Small-signal bandwidth	V_O = 0.5 V_{PP}	G = +1 V/V, R_F = 511Ω		1400		MHz
			G = +2 V/V, R_F = 487Ω		960		
			G = +8 V/V, R_F = 348Ω		395		
			G = +16 V/V, R_F = 162Ω		235		
	Bandwidth for 0.2-dB gain flatness	G = +2, V_O = 0.5 V_{PP}, R_F = 487 Ω			230		MHz
	Peaking at a gain of +1 V/V	R_F = 511 Ω, V_O = 0.5 V_{PP}			1	2	dB
LSBW	Large-signal bandwidth	G = +8 V/V, V_O = 2 V_{PP}			310		MHz
SR	Slew rate	G = +8 V/V, V_O = 2-V step			1700		V/μs
	Rise and fall time (10% to 90%)	G = +8 V/V	V_O = 0.5-V step		1		ns
			V_O = 2-V step		1		
	Settling time	To 0.02%, V_O = 2-V step			16		ns
		To 0.1%, V_O = 2-V step			10		ns
HD2	2nd-order harmonic distortion	f = 10 MHz	V_O = 2 V_{PP}, R_L = 100 Ω		–62	–58	dBc
			V_O = 2 V_{PP}, R_L = 500 Ω		–70	–66	
HD3	3rd-order harmonic distortion	f = 10 MHz	V_O = 2 V_{PP}, R_L = 100 Ω		–66	–64	dBc
			V_O = 2 V_{PP}, R_L = 500 Ω		–65	–63	
e_n	Input voltage noise	f > 1 MHz			1.8	2	nV/√Hz
i_{n+}	Noninverting input current noise	f > 1 MHz			18	19	pA/√Hz
i_{n-}	Inverting input current noise	f > 1 MHz			22	24	pA/√Hz
DC PERFORMANCE							
Z_{OL}	Open-loop transimpedance gain	V_O = V_S/2		40	70		kΩ
			T_A = –40°C to +85°C	36			
	Input offset voltage	V_{CM} = V_S/2			±0.3	±3	mV
			T_A = –40°C to +85°C			±4	
	Average input offset voltage drift	V_{CM} = V_S/2, T_A = –40°C to +85°C				±15	μV/°C
	Noninverting input bias current	V_{CM} = V_S/2			±5	±40	μA
			T_A = –40°C to +85°C			±50	
	Average noninverting input bias current drift	V_{CM} = V_S/2, T_A = –40°C to +85°C				±170	nA/°C
	Inverting input bias current	V_{CM} = V_S/2			±5	±60	μA
			T_A = –40°C to +85°C			±70	
	Average inverting input bias current drift	V_{CM} = V_S/2, T_A = –40°C to +85°C				±160	nA/°C
INPUT CHARACTERISTICS							
CMIR	Common-mode input range (positive)[1]			3.2	3.3		V
		T_A = –40°C to +85°C		3.1			
	Common-mode input range (negative)[1]				1.7	1.8	
		T_A = –40°C to +85°C				1.9	
CMRR	Common-mode rejection ratio	V_{CM} = V_S/2		51	54		dB
			T_A = –40°C to +85°C	50			

5.8 Electrical Characteristics V_S = 5 V, OPA695IDGK（续）

at T_A = +25°C, G = +8 V/V, V_S = 5 V, R_F = 348 Ω, and R_L = 100 Ω to V_S /2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Noninverting input resistance			280 || 1.2		kΩ || pF
	Inverting input resistance	Open-loop		32		Ω

5.8 Electrical Characteristics V_S = 5 V, OPA695IDGK（续）

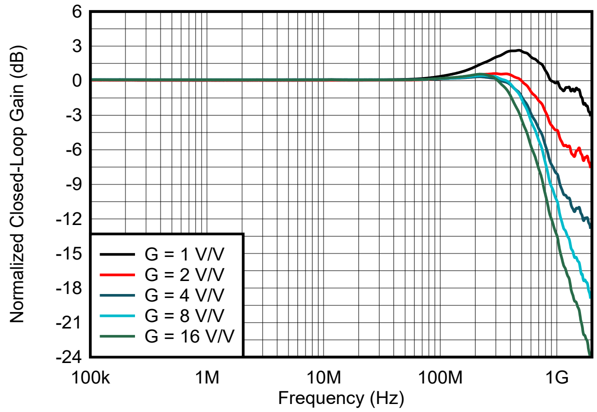
at T_A = +25°C, G = +8 V/V, V_S = 5 V, R_F = 348 Ω, and R_L = 100 Ω to V_S/2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT CHARACTERISTICS							
V_O	Output voltage swing (most positive)	No load		4.0	4.2		V
			T_A = –40°C to +85°C	3.8			
		R_L = 100 Ω		3.9	4		V
			T_A = –40°C to +85°C	3.7			
	Output voltage swing (least positive)	No load			0.8	1	V
			T_A = –40°C to +85°C			1.2	
		R_L = 100 Ω			1	1.1	V
			T_A = –40°C to +85°C			1.3	
I_O	Output current, sourcing	V_O = V_S/2		70	90		mA
			T_A = –40°C to +85°C	66			
	Output current, sinking	V_O = V_S/2			–90	–70	mA
			T_A = –40°C to +85°C			–66	
Z_{OUT}	Closed-loop output impedance	G = +2 V/V, f = 100 kHz			0.05		Ω
POWER SUPPLY							
I_Q	Quiescent current			10.9	11.4	12	mA
		T_A = –40°C to +85°C		9.1		12.9	
–PSRR	Negative power-supply rejection ratio				56		dB
DISABLE (Disabled LOW)							
	Power-down quiescent current	$V_{\overline{DIS}}$ = 0 V			95	160	µA
			T_A = –40°C to +85°C			180	
	Disable time	V_{IN} = ±0.25 V_{DC}			1		µs
	Enable time	V_{IN} = ±0.25 V_{DC}			25		ns
	Off isolation	G = +8 V/V, f = 10 MHz			70		dB
	Output capacitance in disable				4		pF
	Turn-on glitch	G = +2 V/V, R_L = 150 Ω, V_{IN} = 0 V			±100		mV
	Turn-off glitch	G = +2 V/V, R_L = 150 Ω, V_{IN} = 0 V			±20		mV
	Enable voltage				3.3	3.5	V
		T_A = –40°C to +85°C				3.7	
	Disable voltage threshold			1.7	1.8		V
		T_A = –40°C to +85°C		1.5			
	$\overline{DIS}$ control pin input bias current				75	130	µA
		T_A = –40°C to +85°C				149	

(1) Tested < 3 dB below minimum specified CMRR at ± CMIR limits.

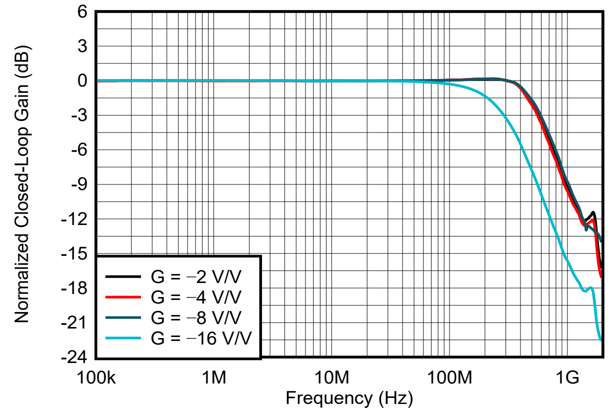
5.9 Typical Characteristics: V_S = ±5 V, OPA695IDBV, OPA695ID

at T_A = +25°C, G = +8 V/V, R_F = 402 Ω, and R_L = 100 Ω (unless otherwise noted)



V_{OUT} = 500 mV_{PP}

图 5-1. Noninverting Small-Signal Frequency Response



V_{OUT} = 500 mV_{PP}

图 5-2. Inverting Small-Signal Frequency Response

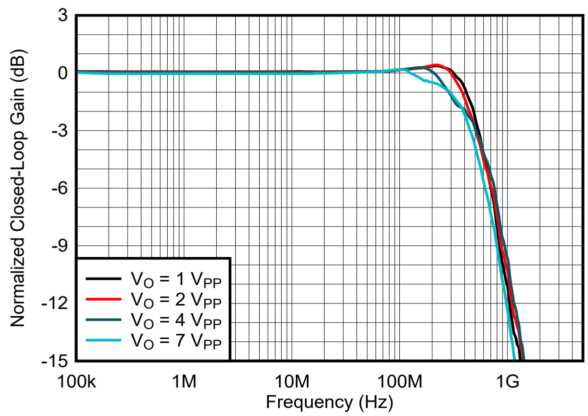
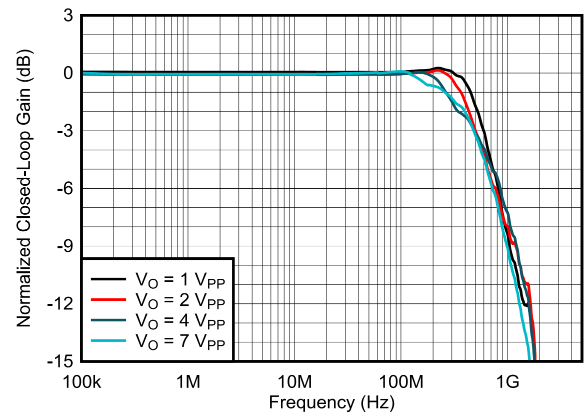


图 5-3. Noninverting Large-Signal Frequency Response



G = –8V/V

图 5-4. Inverting Large-Signal Frequency Response

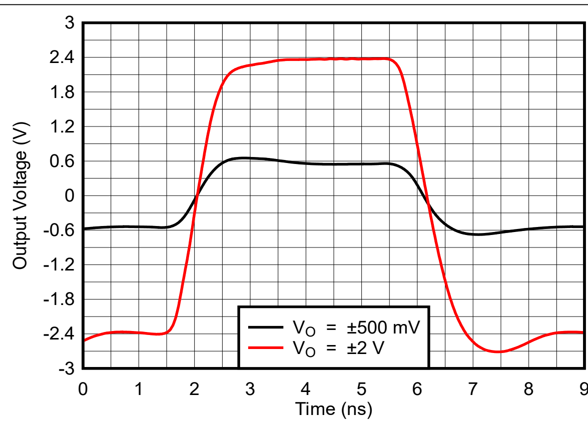
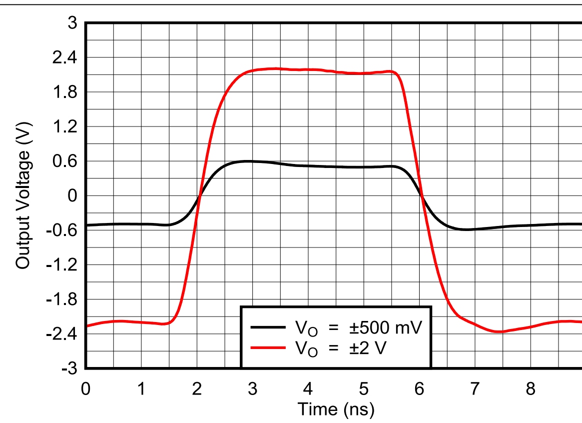


图 5-5. Noninverting Large and Small-Signal Frequency Response

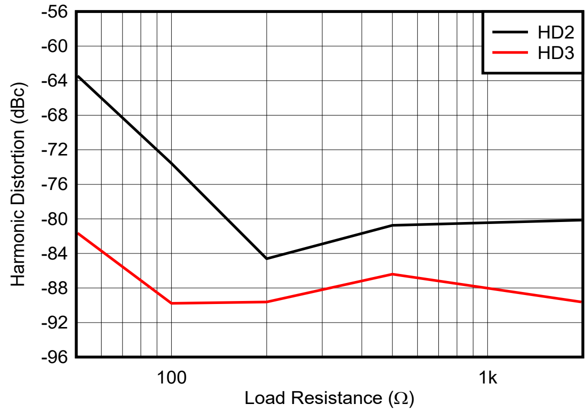


G = –8V/V

图 5-6. Inverting Large and Small-Signal Frequency Response

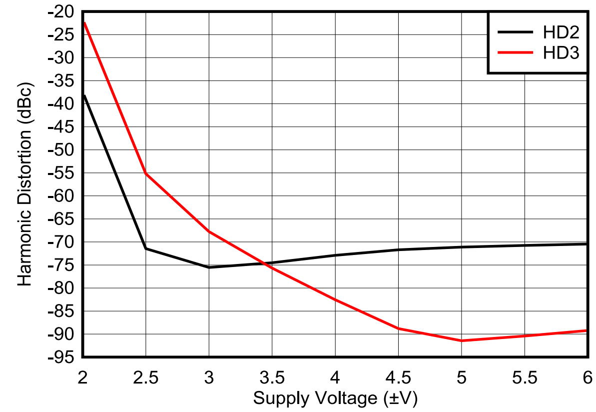
5.9 Typical Characteristics: V_S = ±5 V, OPA695IDBV, OPA695ID (continued)

at T_A = +25°C, G = +8 V/V, R_F = 402 Ω, and R_L = 100 Ω (unless otherwise noted)



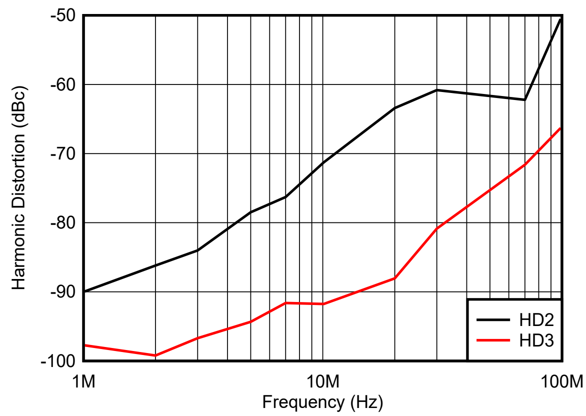
$V_{OUT} = 2\ V_{PP}$

图 5-7. 10-MHz Harmonic Distortion vs Load Resistance



$V_{OUT} = 2\ V_{PP}$

图 5-8. 10-MHz Harmonic Distortion vs Supply Voltage



$V_{OUT} = 2\ V_{PP}$

图 5-9. Harmonic Distortion vs Frequency

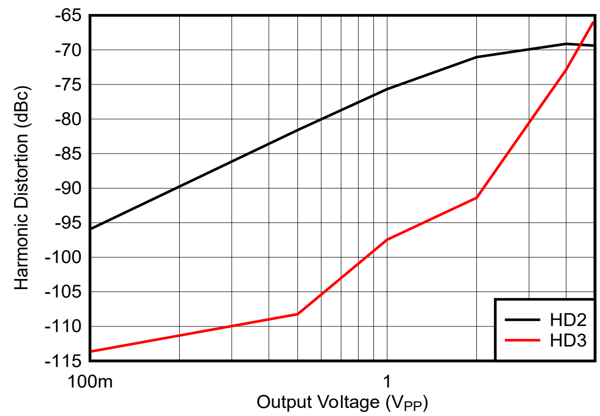
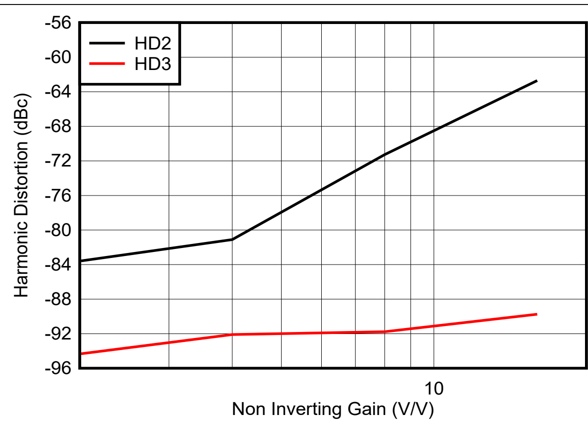
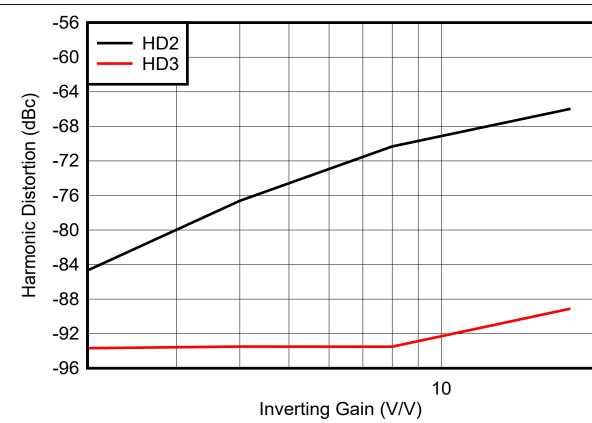


图 5-10. 10-MHz Harmonic Distortion vs Output Voltage



$V_{OUT} = 2\ V_{PP}$

图 5-11. 10-MHz Harmonic Distortion vs Noninverting Gain



$V_{OUT} = 2\ V_{PP}$

图 5-12. 10-MHz Harmonic Distortion vs Inverting Gain

5.9 Typical Characteristics: V_S = ±5 V, OPA695IDBV, OPA695ID (continued)

at T_A = +25°C, G = +8 V/V, R_F = 402 Ω, and R_L = 100 Ω (unless otherwise noted)

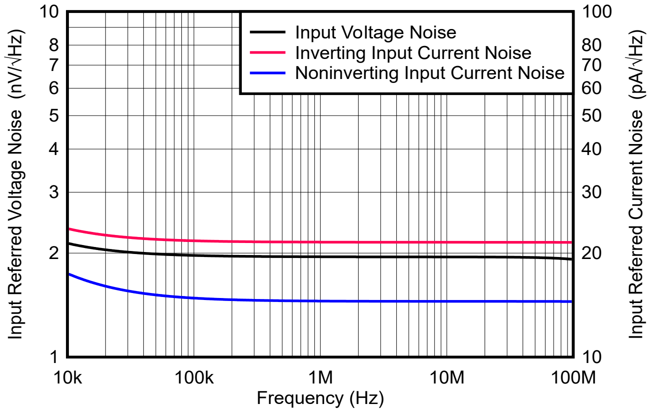


图 5-13. Input Voltage and Current Noise Density

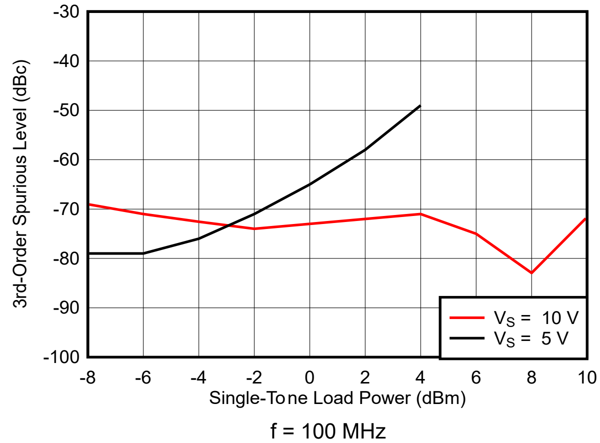


图 5-14. Two-Tone 3rd-Order Intermodulation Distortion vs Frequency

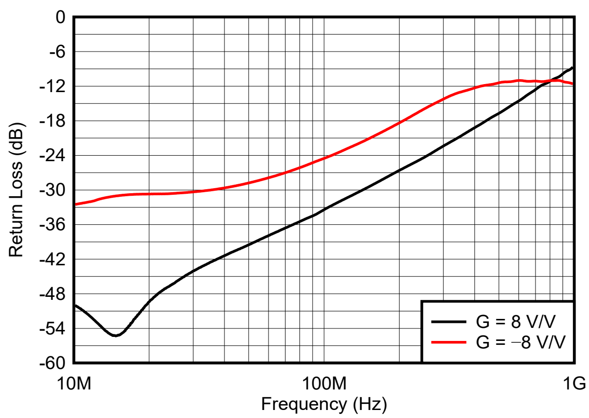


图 5-15. Input Return Loss vs Frequency (S_{11})

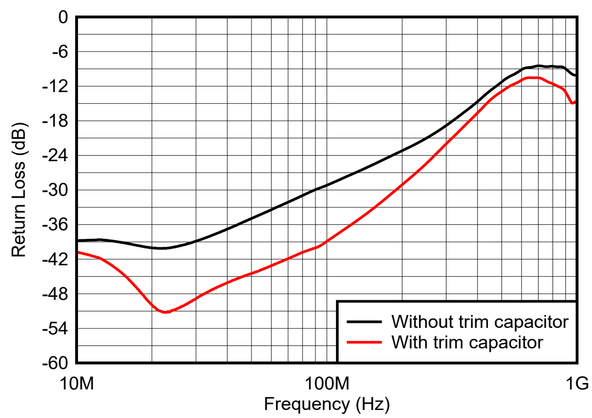


图 5-16. Output Return Loss vs Frequency (S_{22})

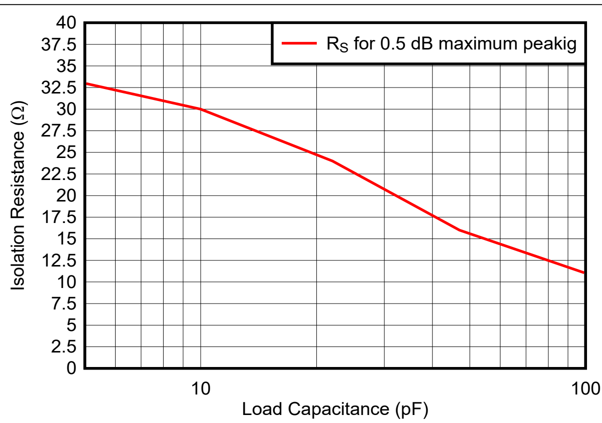


图 5-17. R_S vs Capacitive Load

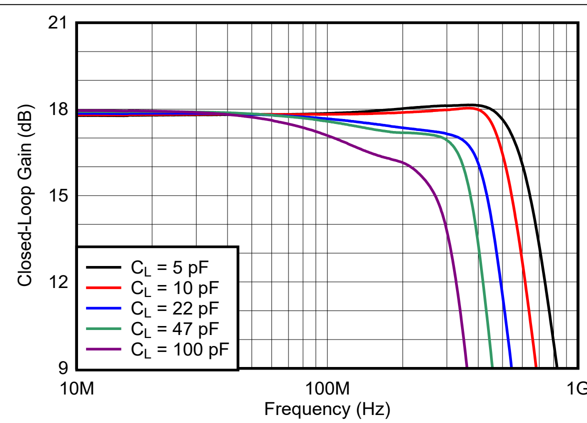


图 5-18. Small-Signal Frequency Response vs Capacitive Load

5.9 Typical Characteristics: V_S = ±5 V, OPA695IDBV, OPA695ID (continued)

at T_A = +25°C, G = +8 V/V, R_F = 402 Ω, and R_L = 100 Ω (unless otherwise noted)

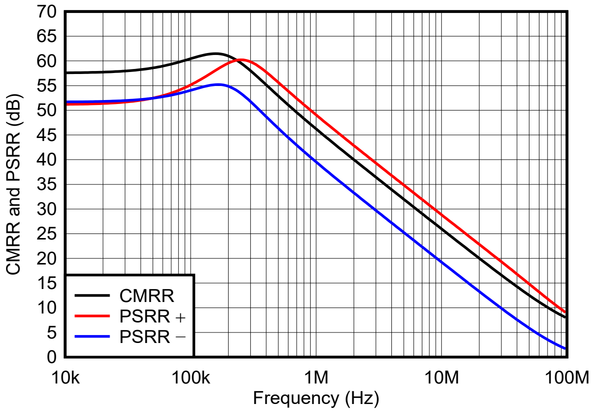


图 5-19. CMRR and PSRR vs Frequency

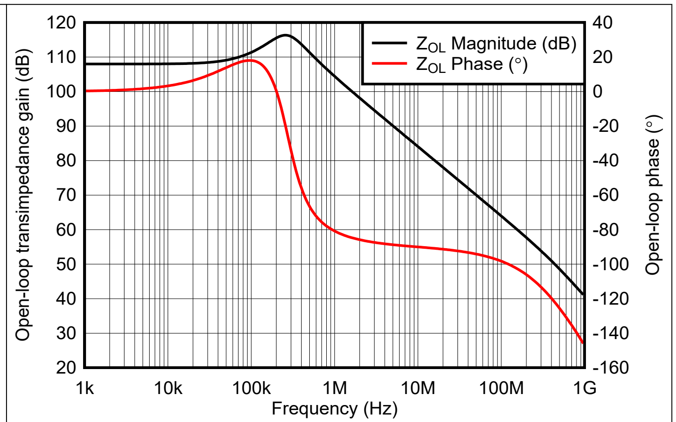


图 5-20. Open-Loop Transimpedance Gain and Phase

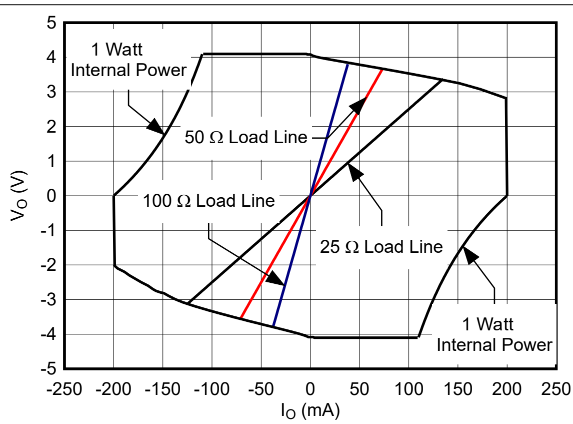


图 5-21. Output Voltage and Current Limitations

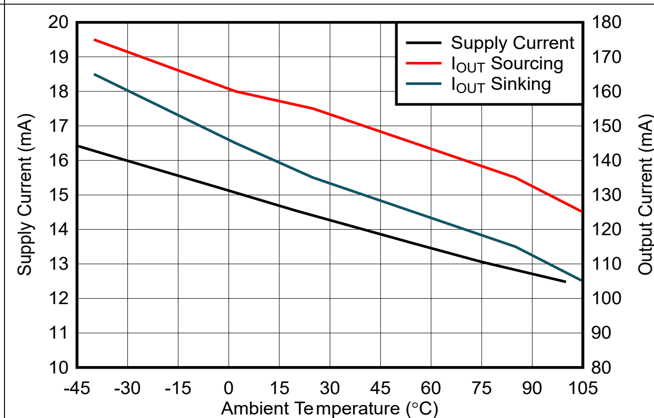


图 5-22. Supply and Output Current vs Temperature

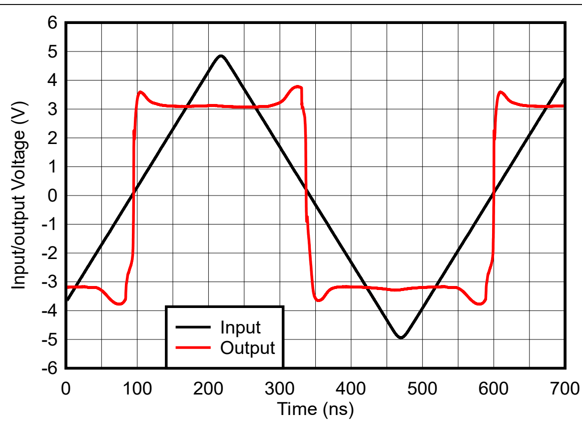


图 5-23. Noninverting Overdrive Recovery

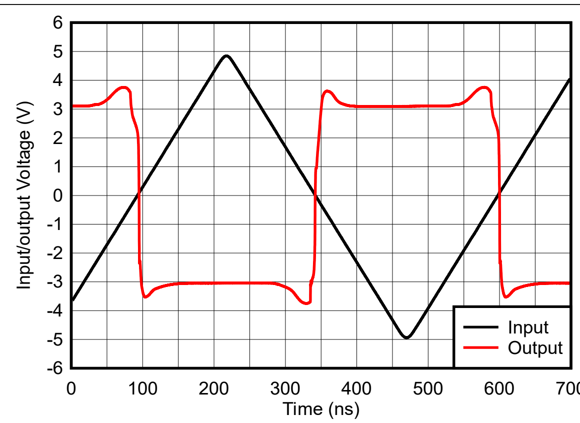


图 5-24. Inverting Overdrive Recovery

5.9 Typical Characteristics: V_S = ±5 V, OPA695IDBV, OPA695ID (continued)

at T_A = +25°C, G = +8 V/V, R_F = 402 Ω, and R_L = 100 Ω (unless otherwise noted)

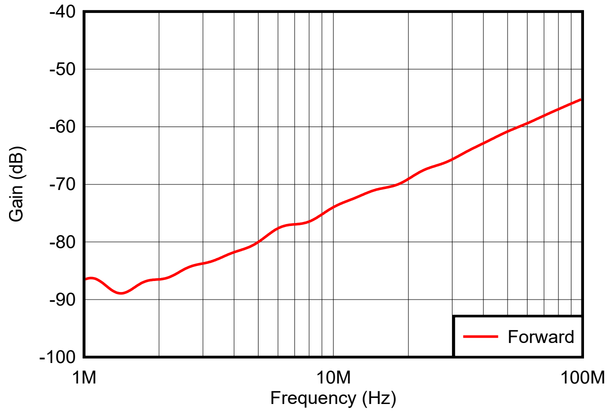


图 5-25. Disabled Feedthrough vs Frequency

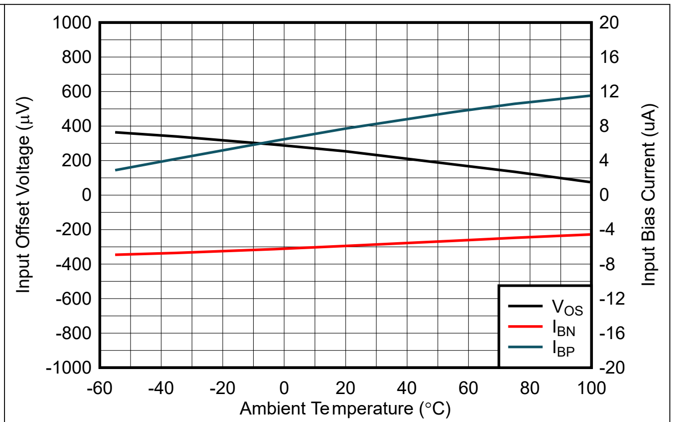


图 5-26. Typical DC Drift Over Temperature

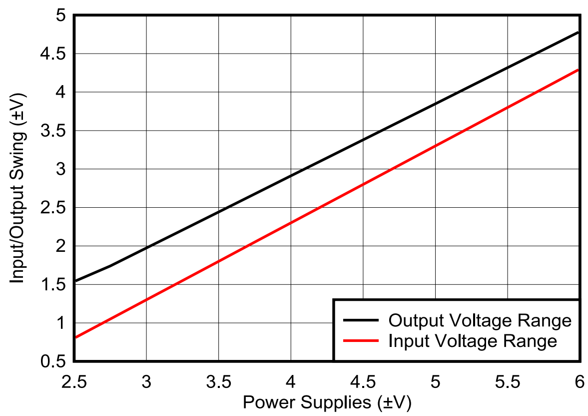


图 5-27. Common-Mode Input and Output Swing vs Supply Voltage

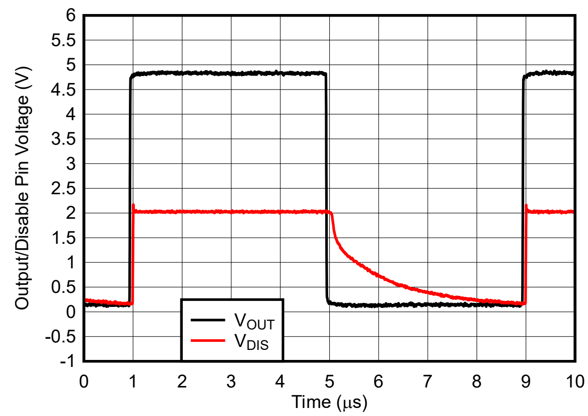
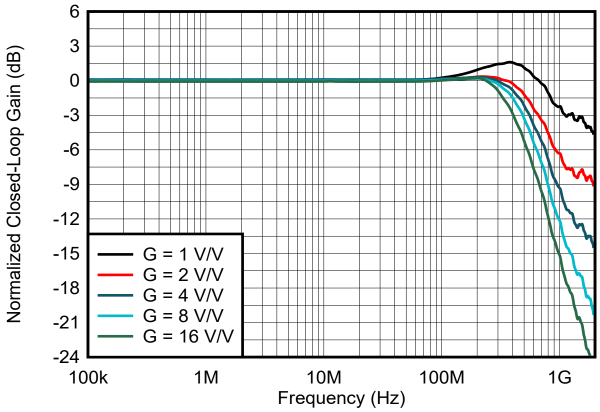


图 5-28. Large-Signal Disable and Enable Response

5.10 Typical Characteristics: V_S = 5 V, OPA695IDBV, OPA695ID

at G = +8 V/V, R_F = 348 Ω, and R_L = 100 Ω (unless otherwise noted)



V_{OUT} = 500 mV_{PP}

图 5-29. Noninverting Small-Signal Frequency Response

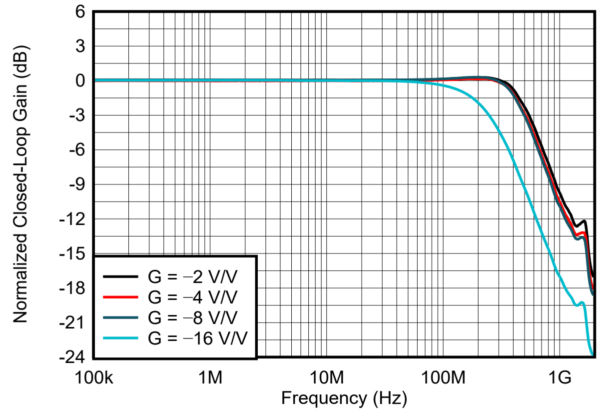


图 5-30. Inverting Small-Signal Frequency Response

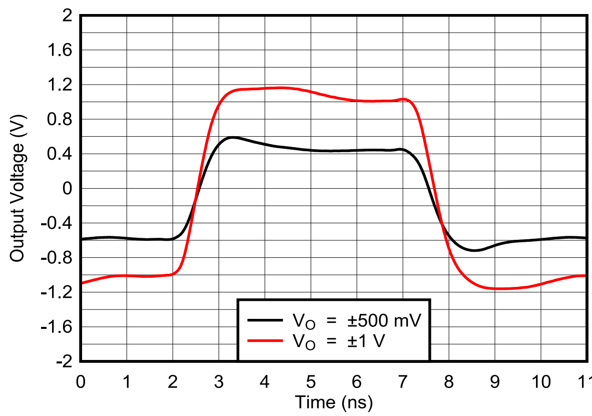
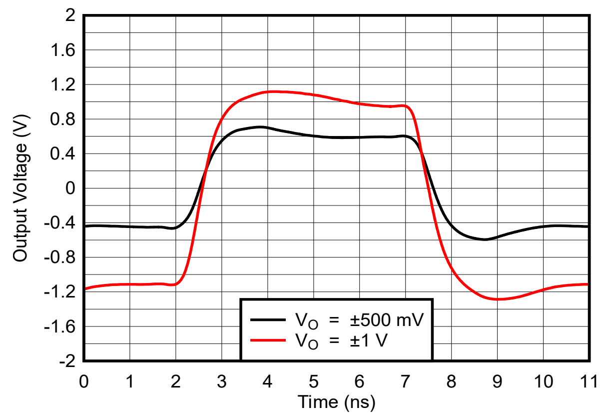


图 5-31. Noninverting Pulse Response



G = –8 V/V

图 5-32. Inverting Pulse Response

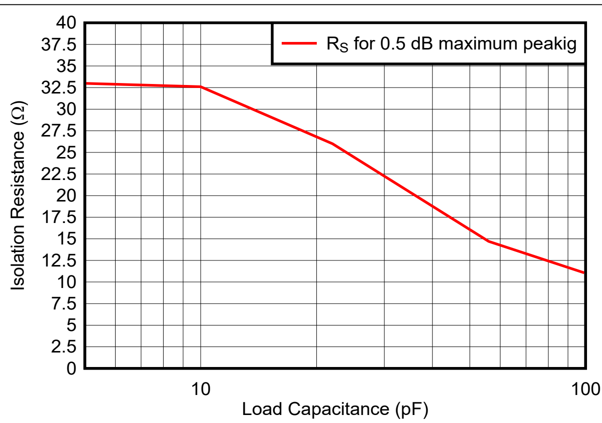


图 5-33. R_S vs Capacitive Load

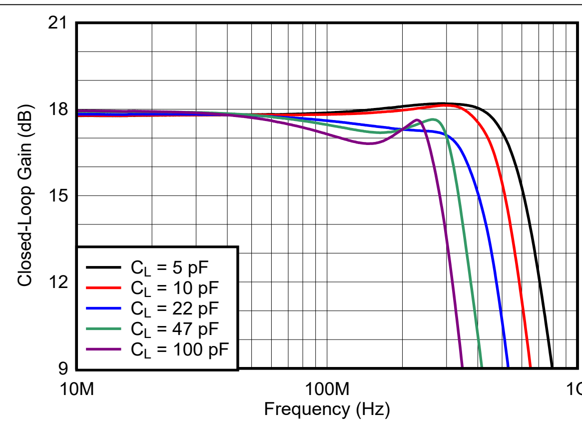
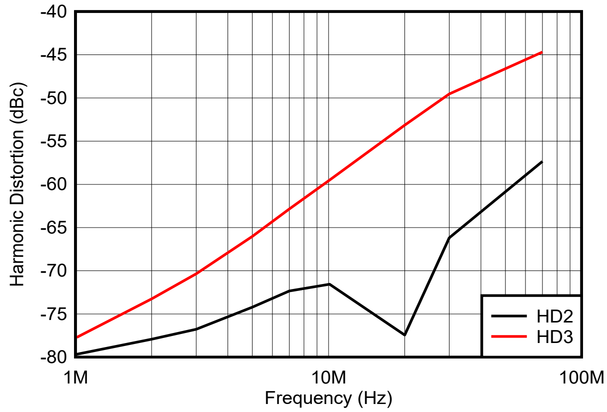


图 5-34. Small-Signal Frequency Response vs Capacitive Load

5.10 Typical Characteristics: V_S = 5 V, OPA695IDBV, OPA695ID (continued)

at G = +8 V/V, R_F = 348 Ω, and R_L = 100 Ω (unless otherwise noted)



V_{OUT} = 2 V_{PP}

图 5-35. Harmonic Distortion vs Frequency

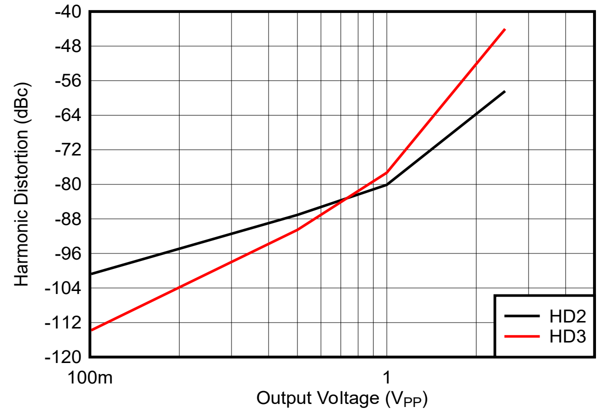
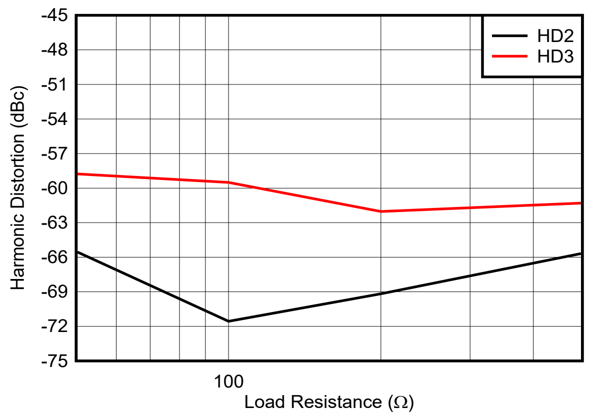
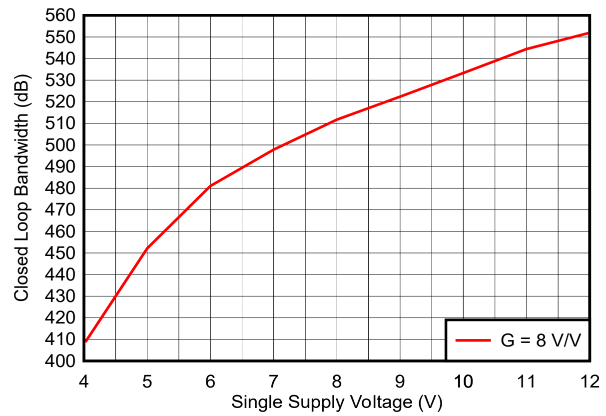


图 5-36. 10-MHz Harmonic Distortion vs Output Voltage



V_{OUT} = 2 V_{PP}

图 5-37. 10-MHz Harmonic Distortion vs Load Resistance



V_{OUT} = 500 mV_{PP}

图 5-38. Small-Signal BW vs Single-Supply Voltage

5.11 Typical Characteristics: V_S = ±5 V, OPA695IDGK

at G = +8 V/V, R_F = 402 Ω, and R_L = 100 Ω (unless otherwise noted)

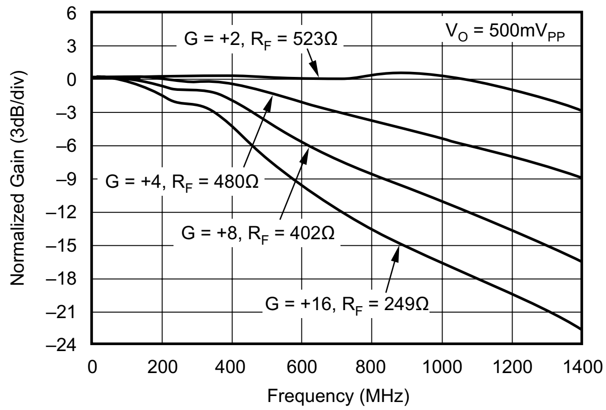


图 5-39. Noninverting Small-Signal Frequency Response

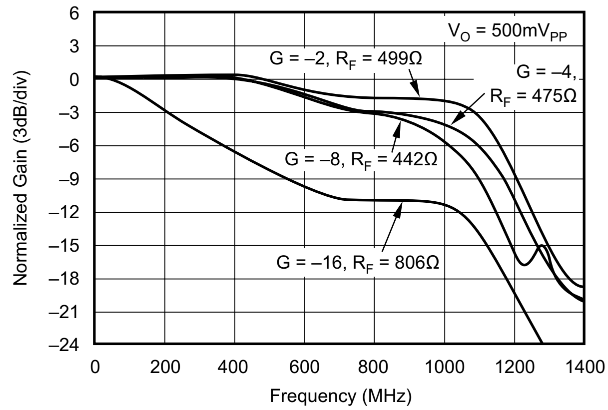


图 5-40. Inverting Small-Signal Frequency Response

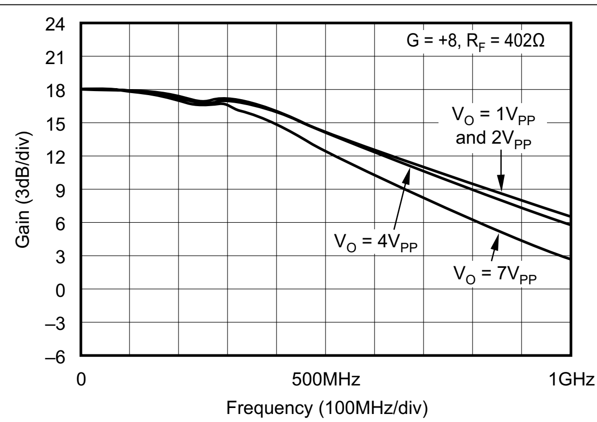


图 5-41. Noninverting Large-Signal Frequency Response

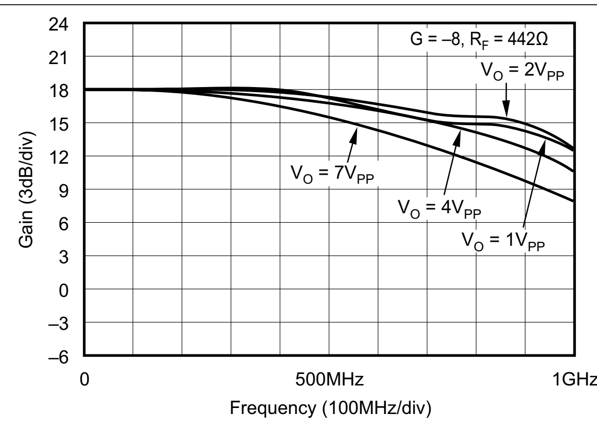


图 5-42. Inverting Large-Signal Frequency Response

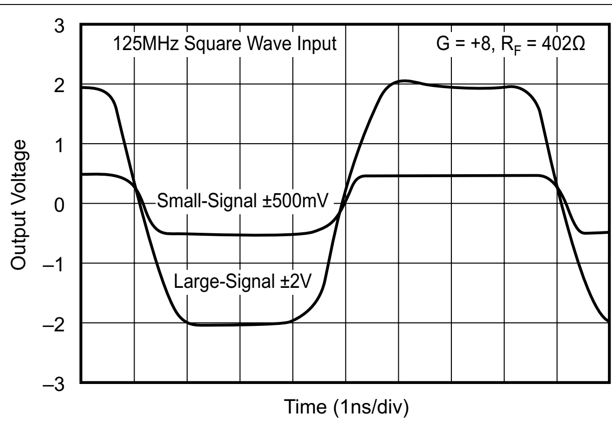


图 5-43. Noninverting Large- and Small-Signal Frequency Responses

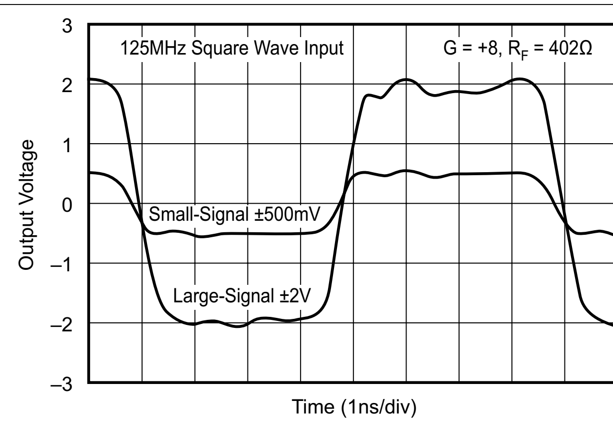


图 5-44. Inverting Large- and Small-Signal Frequency Responses

5.11 Typical Characteristics: V_S = ±5 V, OPA695IDGK (continued)

at G = +8 V/V, R_F = 402 Ω, and R_L = 100 Ω (unless otherwise noted)

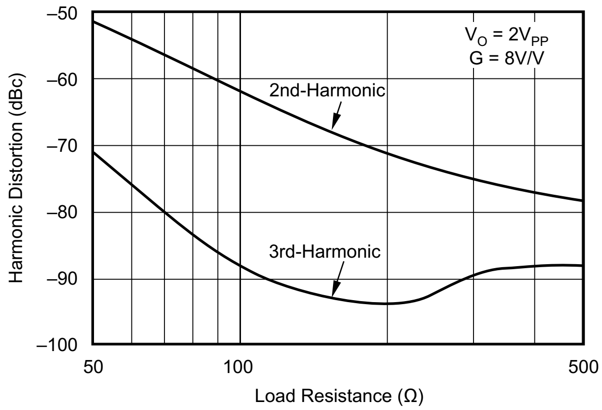


图 5-45. 10-MHz Harmonic Distortion vs Load Resistance

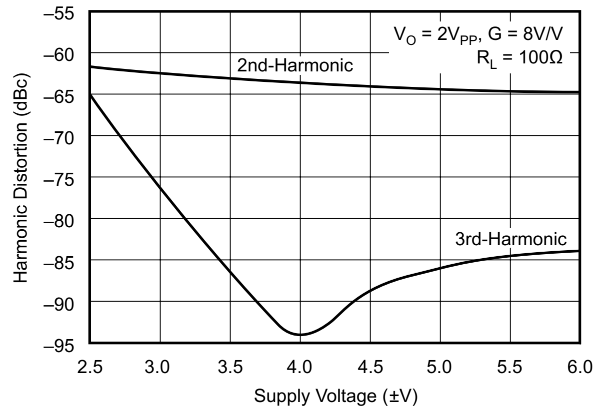


图 5-46. 10-MHz Harmonic Distortion vs Supply Voltage

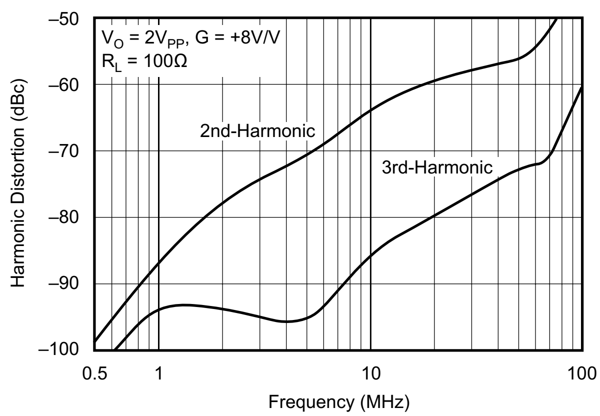


图 5-47. Harmonic Distortion vs Frequency

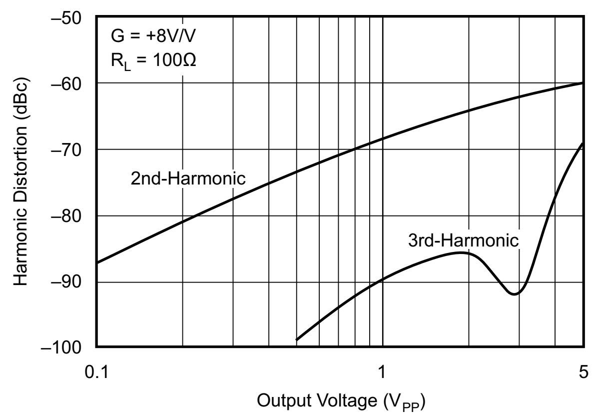


图 5-48. 10-MHz Harmonic Distortion vs Output Voltage

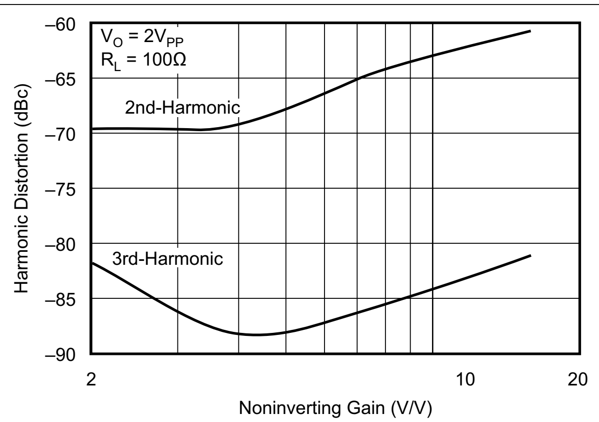


图 5-49. 10-MHz Harmonic Distortion vs Noninverting Gain

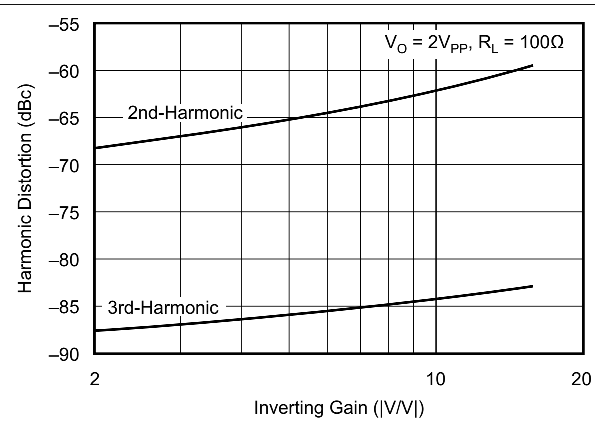


图 5-50. 10-MHz Harmonic Distortion vs Inverting Gain

5.11 Typical Characteristics: V_S = ±5 V, OPA695IDGK (continued)

at G = +8 V/V, R_F = 402 Ω, and R_L = 100 Ω (unless otherwise noted)

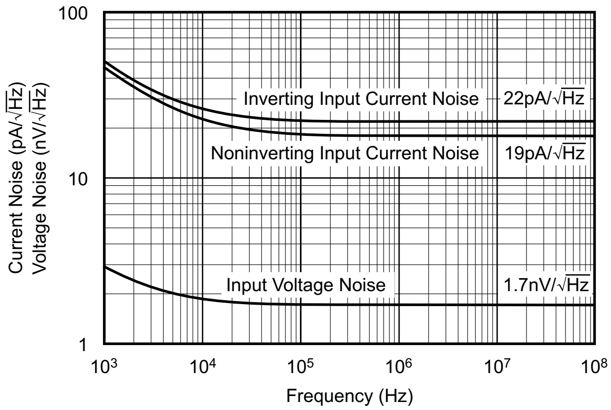


图 5-51. Input Voltage and Current Noise Density

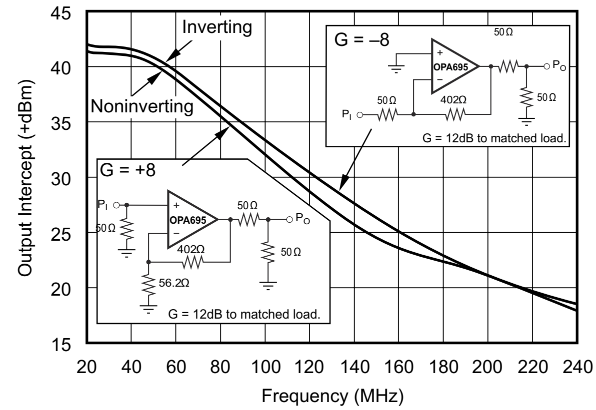


图 5-52. Two-Tone 3rd-Order Intermodulation Intercept

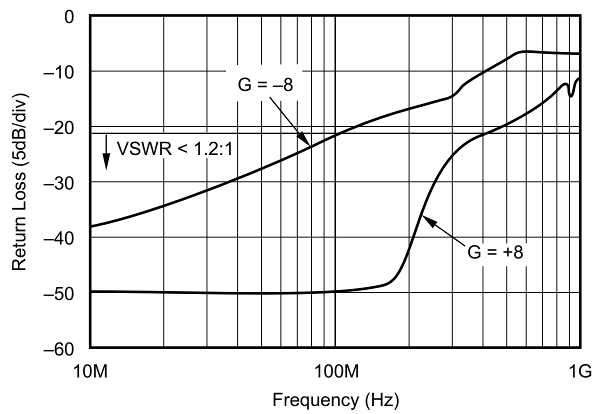


图 5-53. Input Return Loss vs Frequency (S_{11})

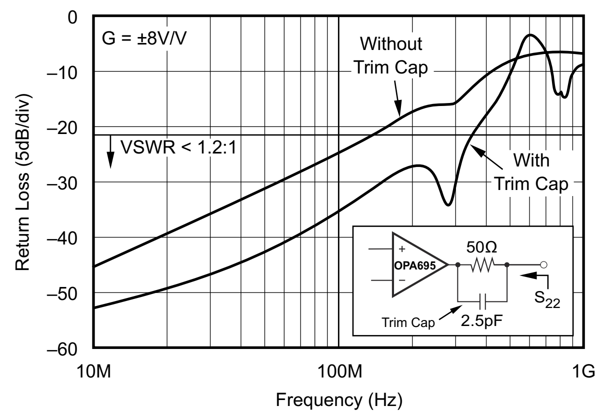


图 5-54. Output Return Loss vs Frequency (S_{22})

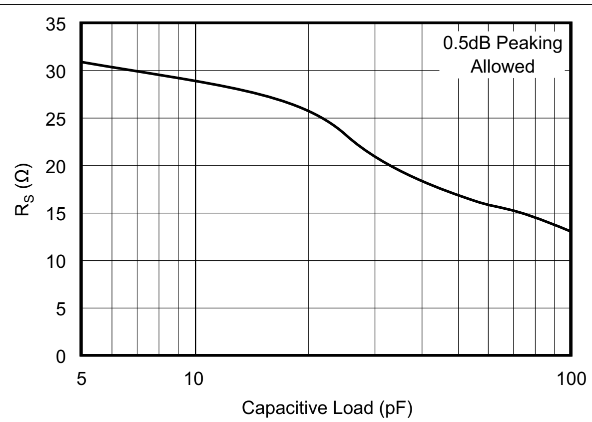


图 5-55. R_S vs Capacitive Load

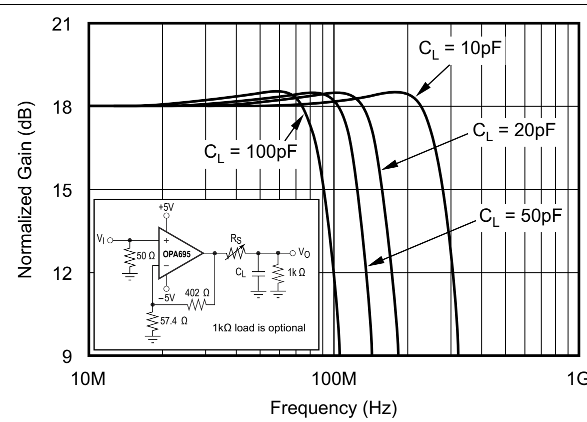


图 5-56. Small-Signal Frequency Response vs Capacitive Load

5.11 Typical Characteristics: V_S = ±5 V, OPA695IDGK (continued)

at G = +8 V/V, R_F = 402 Ω, and R_L = 100 Ω (unless otherwise noted)

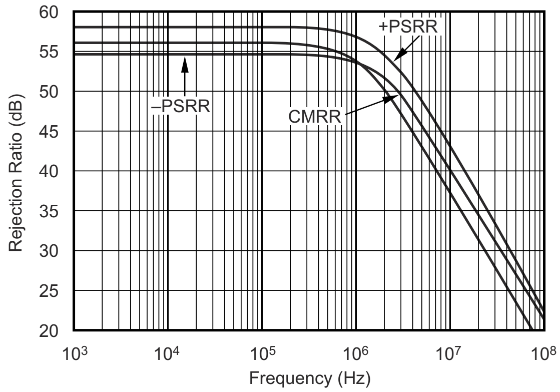


图 5-57. CMRR and PSRR vs Frequency

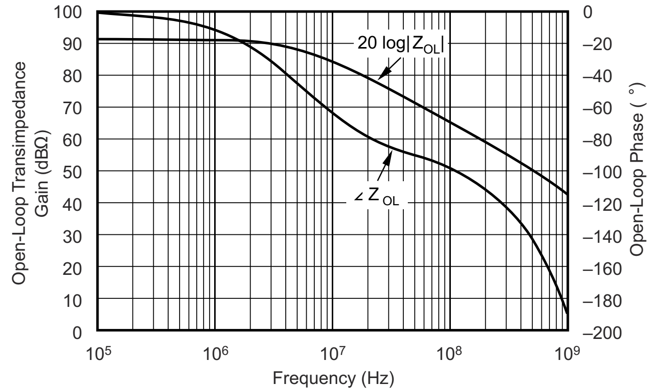


图 5-58. Open-Loop Transimpedance Gain and Phase

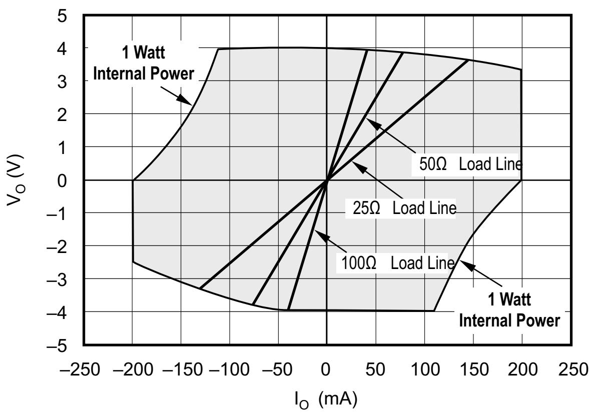


图 5-59. Output Voltage and Current Limitations

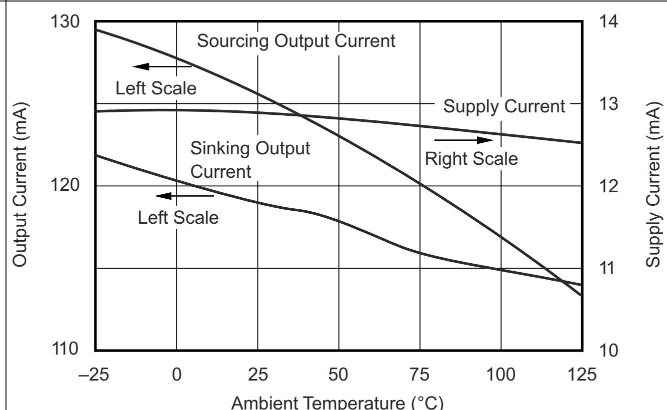


图 5-60. Supply and Output Current vs Temperature

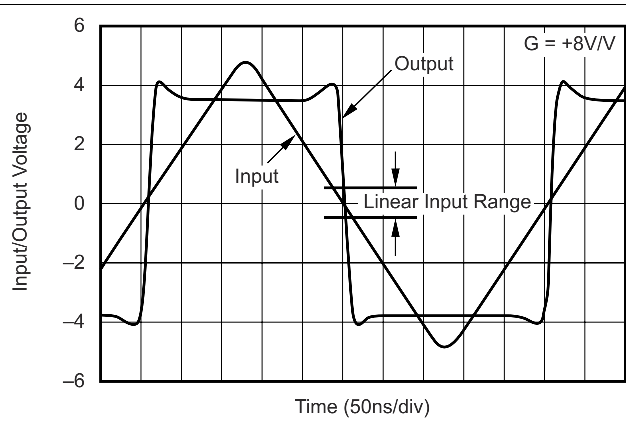


图 5-61. Noninverting Overdrive Recovery

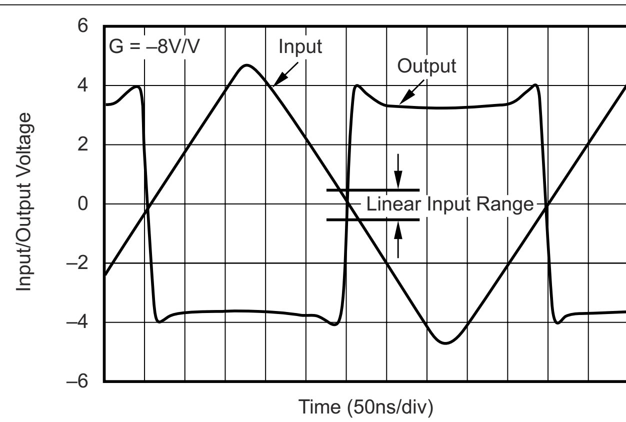


图 5-62. Inverting Overdrive Recovery

5.11 Typical Characteristics: V_S = ±5 V, OPA695IDGK (continued)

at G = +8 V/V, R_F = 402 Ω, and R_L = 100 Ω (unless otherwise noted)

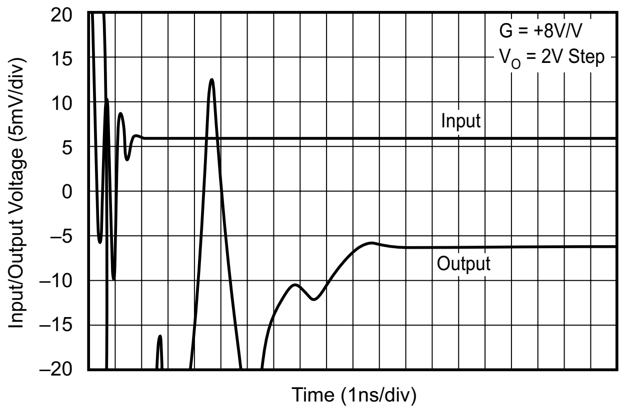


图 5-63. Settling Time

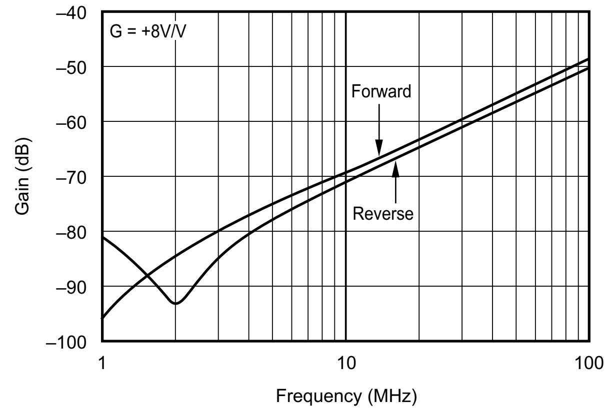


图 5-64. Disabled Feedthrough vs Frequency

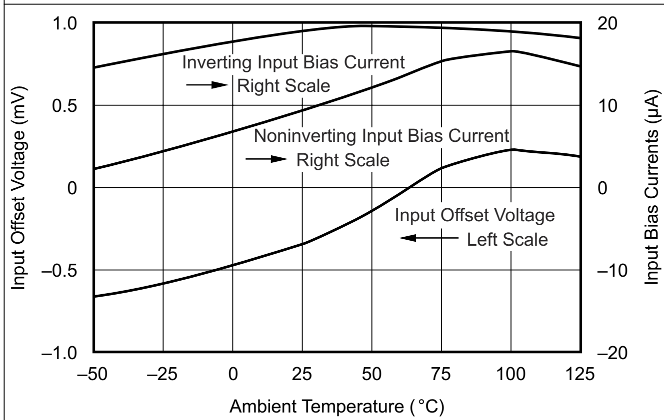


图 5-65. Typical DC Drift Over Temperature

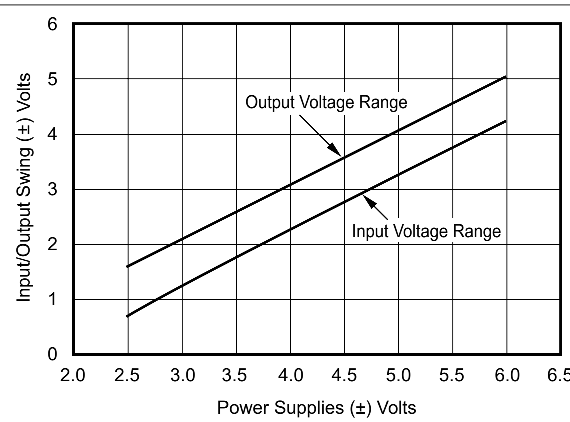


图 5-66. Common-Mode Input and Output Swing vs Supply Voltage

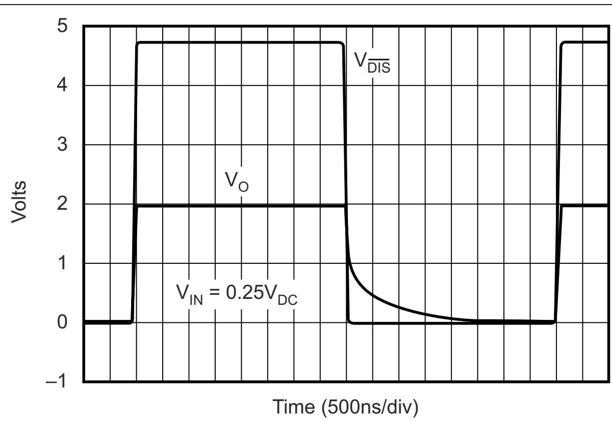


图 5-67. Large-Signal Disable and Enable Responses

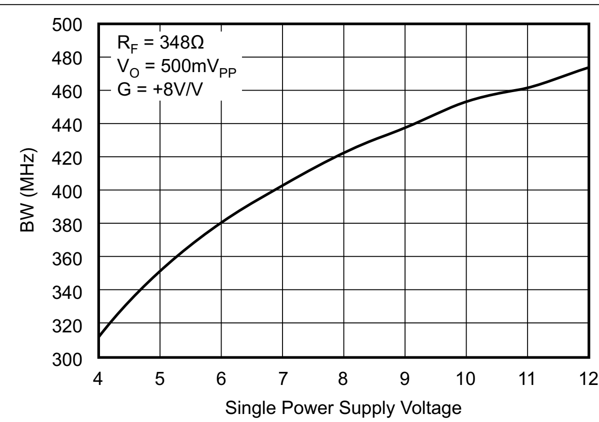


图 5-68. Small-Signal BW vs Single-Supply Voltage

5.12 Typical Characteristics: V_S = 5 V, OPA695IDGK

at G = +8 V/V, R_F = 348 Ω, and R_L = 100 Ω (unless otherwise noted)

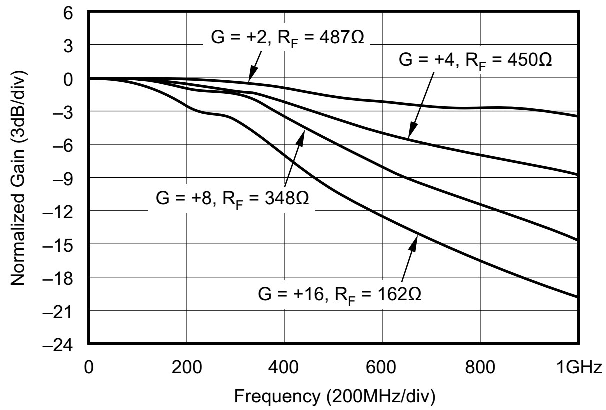


图 5-69. Noninverting Small-Signal Frequency Response

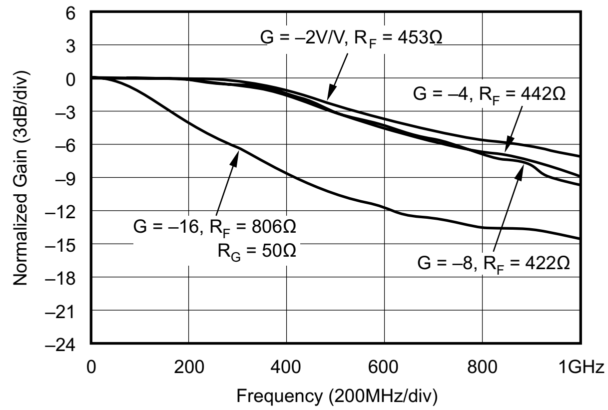


图 5-70. Inverting Small-Signal Frequency Response

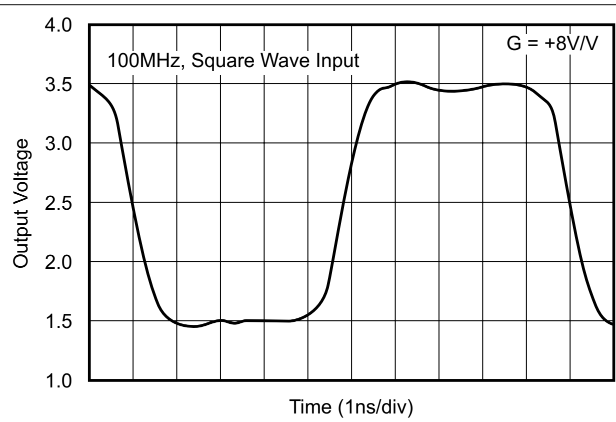


图 5-71. Noninverting Pulse Response

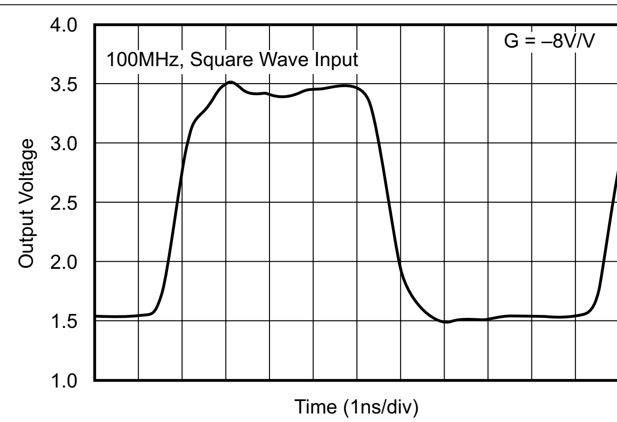


图 5-72. Inverting Pulse Response

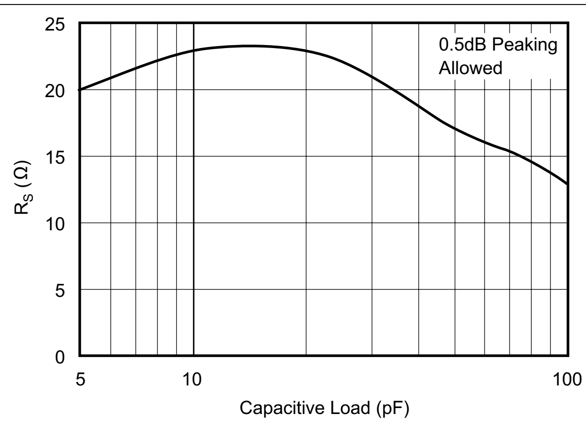


图 5-73. R_S vs Capacitive Load

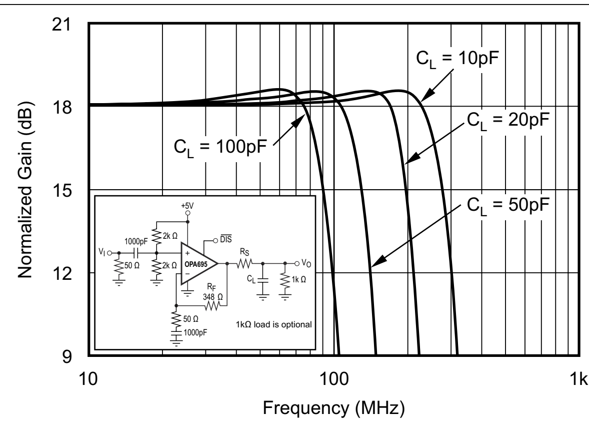


图 5-74. Small-Signal Frequency Response vs Capacitive Load

5.12 Typical Characteristics: V_S = 5 V, OPA695IDGK (continued)

at G = +8 V/V, R_F = 348 Ω, and R_L = 100 Ω (unless otherwise noted)

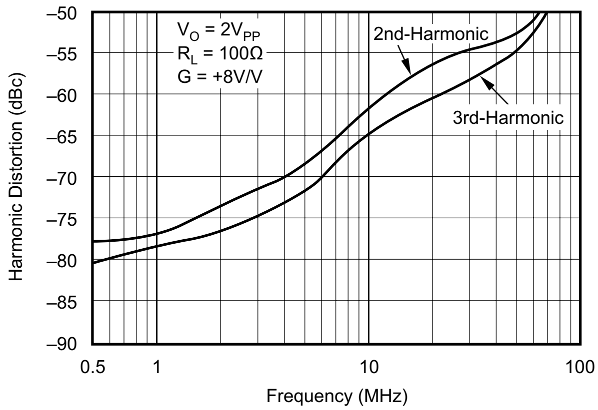


图 5-75. Harmonic Distortion vs Frequency

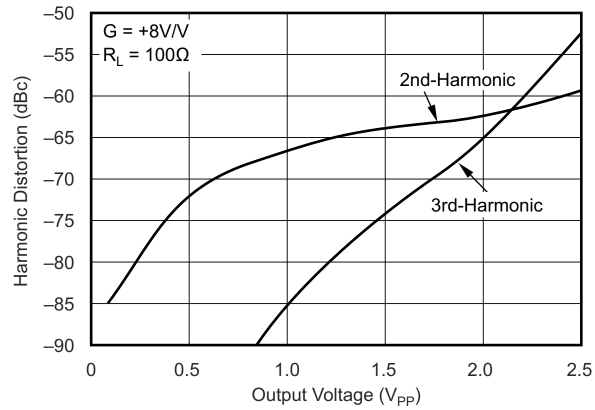


图 5-76. 10-MHz Harmonic Distortion vs Output Voltage

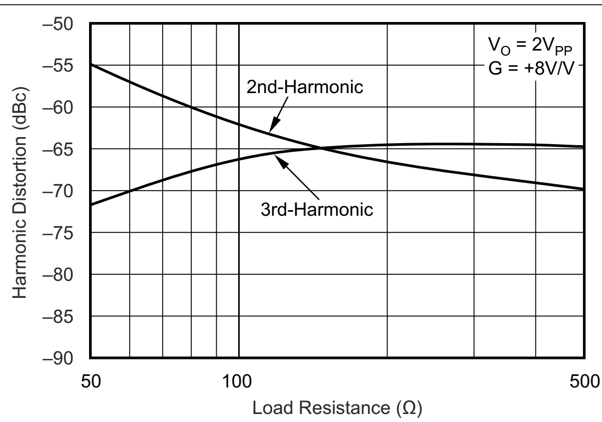


图 5-77. 10-MHz Harmonic Distortion vs Load Resistance

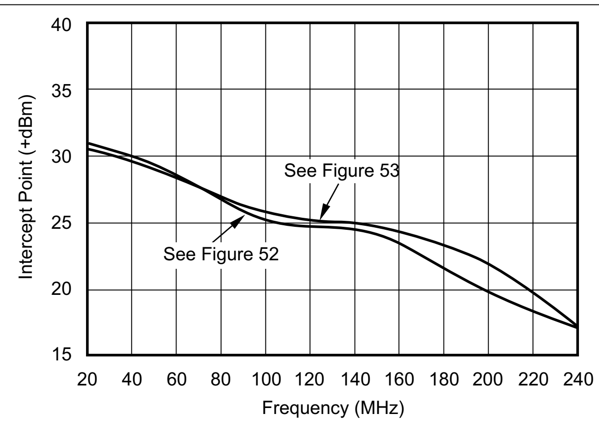


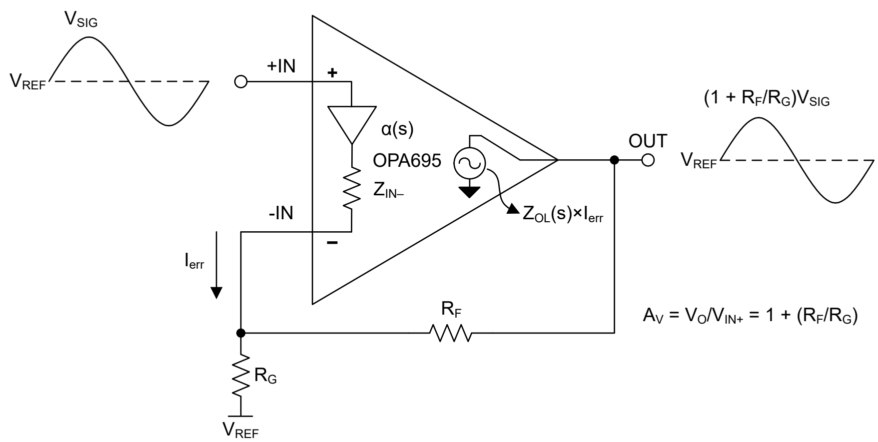
图 5-78. Two-Tone, 3rd-Order Intermodulation Intercept

6 Detailed Description

6.1 Overview

The OPA695 is a high-speed current-feedback amplifier (CFA) designed to operate over a wide supply range of ±2.5 V (5 V) to ±6 V (12 V) for applications requiring low distortion along with wide-bandwidth and high slew-rate. Common applications for current-feedback operational amplifiers include gain blocks in high-speed data-acquisition systems, coaxial cable drivers, analog-to-digital converter (ADC) drivers, and digital-to-analog converters(DAC) drivers. The OPA695 features a power-down pin that puts the amplifier in low-power standby mode and lowers the quiescent current from 14 mA to 160 µA.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Wideband Current-Feedback Operation

The OPA695 provides a new level of performance in wideband current-feedback operational amplifiers. The nearly constant ac performance over a wide gain range, along with 5000-V/µs slew rate and ultra-low distortion makes this device an excellent choice for high-speed data acquisition gain stages. While optimized at a gain of +8 V/V (12 dB to a matched 50-Ω load) to give 600-MHz bandwidth, applications from gains of 1 V/V to 40 V/V can be supported. At gains above 20 V/V, the signal bandwidth starts to decrease, but still exceeds 180 MHz up to a gain of 40 V/V (26 dB to a matched 50-Ω load). Single +5-V supply operation is also supported with similar bandwidths but reduced output power capability.

图 6-1 shows the dc-coupled, gain of +8 V/V, dual-power supply circuit used as the basis of the ±5-V specifications and typical characteristic curves. The total effective load is 100 Ω || 458 Ω = 82 Ω. The disable control line ($\overline{DIS}$) is typically left open for normal amplifier operation. Assert the disable line low to shut off the OPA695. 图 6-2 shows the dc-coupled, gain of –8 V/V, dual-power supply circuit used as the basis of the inverting typical characteristic curves. Inverting operation offers several performance benefits. There is no common-mode signal across the input stage; therefore, the distortion performance is slightly improved. In addition to the usual power-supply decoupling capacitors to ground, a 0.01-µF capacitor is included between the two power-supply pins. In practical PCB layouts, this optional added capacitor typically improves the 2nd-harmonic distortion performance by 3 dB to 6 dB for bipolar-supply operation.

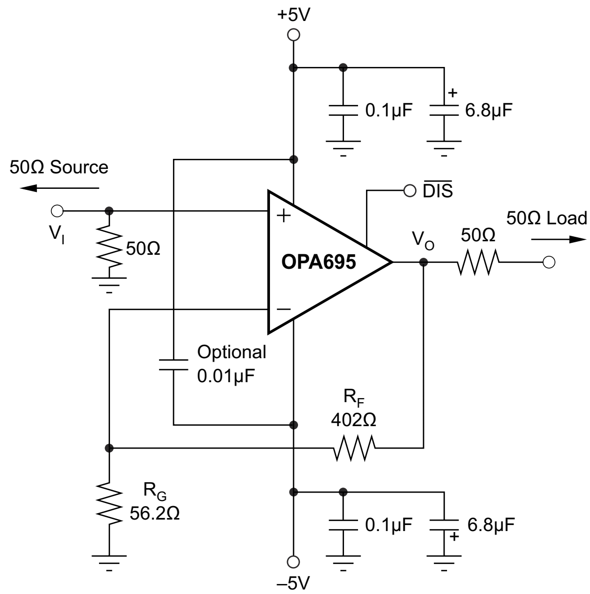


图 6-1. DC-Coupled, G = +8 V/V, Bipolar Supply Specifications and Test Circuit

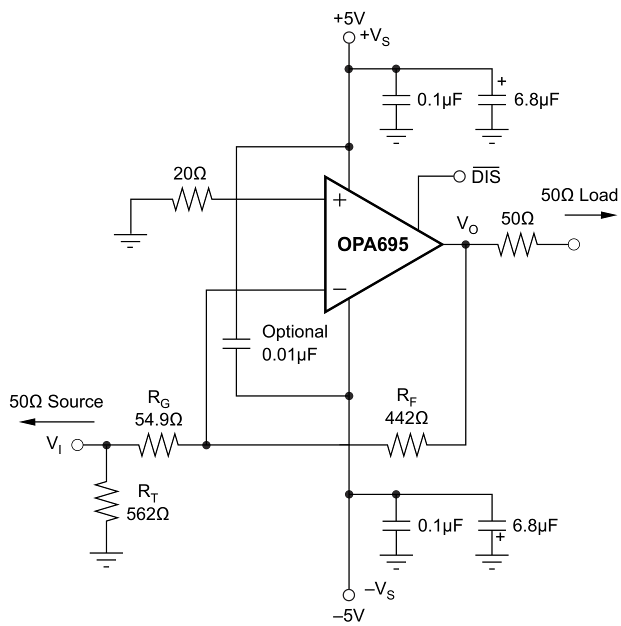


图 6-2. DC-Coupled, G = – 8 V/V, Bipolar Supply Specifications and Test Circuit

6.3.2 Input and ESD Protection

The OPA695 is built using a very high-speed, complementary bipolar process. The internal junction breakdown voltages are relatively low for these small geometry devices. These breakdowns are reflected in the *Absolute Maximum Ratings*, where an absolute maximum ±6.5-V supply is reported. All device pins have limited ESD protection using internal diodes to the power supplies, as shown in 图 6-3.

These diodes also provide moderate protection to input overdrive voltages above the supplies. The protection diodes can typically support 10-mA continuous current. Where higher currents are possible (for example, in systems with ±15-V supply parts driving into the OPA695), add current-limiting series resistors into the two inputs. Keep these resistor values as low as possible because high values degrade both noise performance and frequency response.

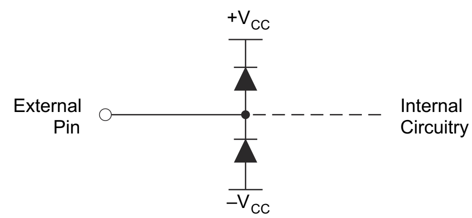


图 6-3. Internal ESD Protection

6.4 Device Functional Modes

The OPA695 has two functional modes: enabled and disabled. While operating on a bipolar supply of V_S = ±5V the first functional mode is accessed by applying a logic 1 (> 3.5 V) to the ($\overline{DIS}$) pin. In this mode, the amplifier is fully enabled and draws a supply current of 14mA.

The second functional mode is the disabled state. The disabled state is accessed by applying a logic 0 (< 1.7V) to the $\overline{DIS}$ pin. In this mode, the amplifier is fully disabled and draws a current of only 160µA. When disabled, the output and input nodes go to a high-impedance state. When the OPA695 operates in a gain of +1V/V, a very high impedance at the output and exceptional signal isolation occur. When operating at a gain greater than +1V/V, the total feedback network resistance appears as an impedance at the output, but the circuit still shows very high forward and reverse isolation. If configured as an inverting amplifier, the input and output are connected through the feedback network resistance, giving relatively poor input-to-output isolation.

7 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 Application Information

7.1.1 Operating Suggestions

7.1.1.1 Setting Resistor Values to Optimize Bandwidth

A current-feedback operational amplifier such as the OPA695 can hold an almost constant bandwidth over signal gain settings with the proper adjustment of the external resistor values. 节 5.9 shows this feature. The small-signal bandwidth decreases only slightly with increasing gain. These curves also show that the feedback resistor has been changed for each gain setting. The absolute values of R_F on the inverting side of the circuit for a current-feedback operational amplifier can be treated as frequency response compensation elements, whereas the ratios of R_F and R_G set the signal gain. 图 7-1 shows the analysis circuit for the OPA695 small-signal frequency response.

The key elements of this current feedback operational amplifier model are:

- α ⇒ Buffer gain from the noninverting input to the inverting input.
- R_I ⇒ Buffer output impedance
- i_{ERR} ⇒ Feedback error current signal
- Z(s) ⇒ Frequency-dependent, open-loop transimpedance gain from i_{ERR} to V_O

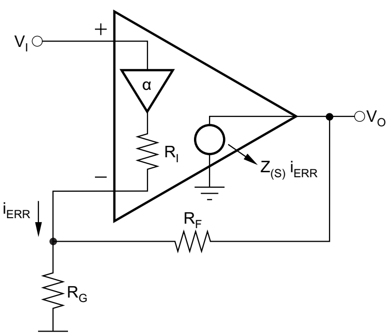


图 7-1. Current-Feedback Transfer Function Analysis Circuit

A current-feedback operational amplifier senses an error current in the inverting node (as opposed to a differential input error voltage for a voltage-feedback operational amplifier) and passes this on to the output through an internal frequency-dependent transimpedance gain. *节 5.9* show this open-loop transimpedance response. This is analogous to the open-loop voltage gain curve for a voltage-feedback operational amplifier. Refer to the training videos shown in TI Precision Labs for further understanding on the CFA operating theory

The values for R_F versus gain shown in 图 7-2 are approximately equal to the values used to generate the typical characteristics and give a good starting point for designs where bandwidth optimization is desired.

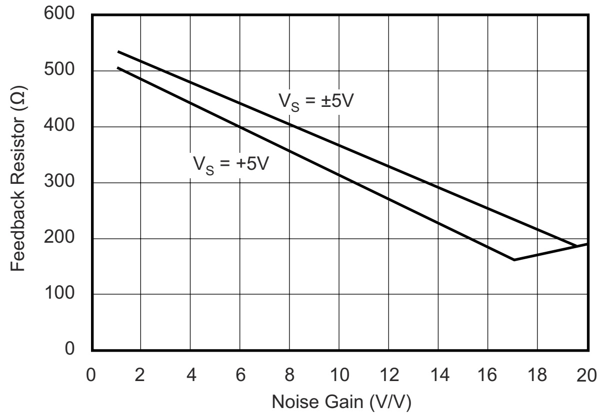


图 7-2. Recommended Feedback Resistor vs Noise Gain

7.1.1.2 Output Current and Voltage

The OPA695 provides output voltage and current capabilities consistent with driving doubly-terminated 50-Ω lines. For a 100-Ω load at a gain of +8 V/V (see 图 6-1), the total load is the parallel combination of the 100-Ω load and the 456-Ω total feedback network impedance. This 82-Ω load requires no more than 45 mA of output current to support the ±3.7-V minimum output voltage swing specified for 100-Ω loads. This value is much less than the minimum ±100-mA specifications.

For the specifications described previously, consider voltage and current limits separately. In many applications, the voltage times the current (or V-I product) is more relevant to circuit operation; see also 图 5-21. The X and Y axes of this graph show the zero-voltage output current limit and the zero-current output voltage limit, respectively. The four quadrants provide a more detailed view of the OPA695 output drive capabilities. Superimposing resistor load lines onto the plot shows the available output voltage and current for specific loads.

To maintain maximum output-stage linearity, no output short-circuit protection is provided. No short-circuit protection is not normally a problem, as most applications include a series-matching resistor at the output that limits the internal power dissipation if the output side of this resistor is shorted to ground.

However, shorting the output pin directly to the adjacent positive power supply pin, in most cases, destroys the amplifier. If additional short-circuit protection is required, consider a small series resistor in the power-supply leads. Under heavy output loads, this series resistor reduces the available output voltage swing. A 5-Ω series resistor in each power-supply lead limits the internal power dissipation to less than 1 W for an output short circuit, while decreasing the available output voltage swing only 0.25 V for up to 50-mA desired load currents. Always place the 0.1-µF power supply decoupling capacitors directly on the supply pins after these supply current-limiting resistors.

7.1.1.3 Driving Capacitive Loads

One of the most demanding, and yet very common, load conditions for an operational amplifier is capacitive loading. Often, the capacitive load is the input of an ADC, including additional external capacitance that can be recommended to improve ADC linearity. A high-speed, high-open-loop-gain amplifier like the OPA695 can be susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the open-loop output resistance of the amplifier is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity, and distortion, the simplest and most effective solution is to isolate the capacitive load (C_L) from the feedback loop by inserting a series isolation resistor (R_{ISO}) between the amplifier output and the capacitive load. 图 7-3 shows this configuration. This configuration does not eliminate the pole from the loop response, but shifts the pole and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

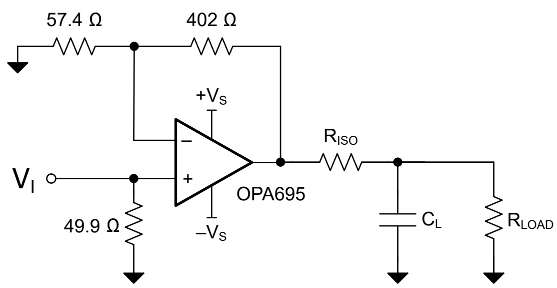


图 7-3. Driving a Large Capacitive Load Using an Output Series Isolation Resistor

The *Typical Characteristics* show the recommended R_S versus capacitive load and the resulting frequency response at the load. Parasitic capacitive loads greater than 2 pF can begin to degrade the performance of the OPA695. Long PCB traces, unmatched cables, and connections to multiple devices can exceed this value. Always consider this effect carefully and add the recommended series resistor as close as possible to the OPA695 output pin (see *节 7.4.1*).

7.1.1.4 Distortion Performance

The OPA695 provides good distortion performance into a 100-Ω load on ±5-V supplies. Compared to other devices, the OPA695 holds lower distortion at higher frequencies (> 20 MHz). Generally, until the fundamental signal reaches very high frequency or power levels, the 2nd-harmonic dominates the distortion with a negligible 3rd-harmonic component. Focusing on the 2nd-harmonic, increasing the load impedance directly improves distortion; the total load includes the feedback network. In the noninverting configuration (see 图 6-1), this feedback network load is the sum of $R_F + R_G$, while in the inverting configuration, the feedback network load is only R_F. Also, providing an additional supply decoupling capacitor (0.01 µF) between the supply pins (for bipolar operation) improves the 2nd-order distortion.

7.1.1.5 Noise Performance

The OPA695 offers an excellent balance between voltage and current noise terms to achieve low output noise. The inverting current noise (22 pA/ √ Hz) is lower than most other current-feedback operational amplifiers, while the input voltage noise (1.8 nV/ √ Hz) is lower than any unity-gain stable, wideband, voltage-feedback operational amplifier. This low-input voltage noise was achieved at the price of a higher noninverting input current noise (18 pA/ √ Hz). As long as the ac source impedance looking out of the noninverting node is less than 50 Ω, this current noise does not contribute significantly to the total output noise. The operational amplifier input voltage noise and the two input current noise terms combine to give low output noise under a wide variety of operating conditions. 图 7-4 shows the operational amplifier noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/ √ Hz or pA/ √ Hz.

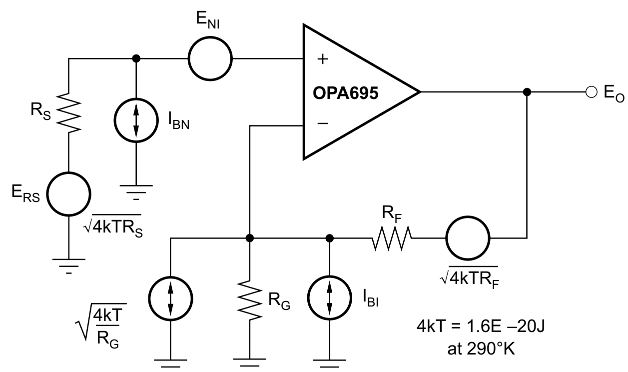


图 7-4. Operational Amplifier Noise Figure Analysis Model

The total output spot-noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. 方程式 1 shows the general form for the output noise voltage using the terms shown in 图 7-8.

$$E_O = \sqrt{\left(E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S\right)G_N^2 + (I_{BI}R_F)^2 + 4kTR_FG_N} \tag{1}$$

Dividing this expression by the noise gain ($NG = (1 + R_F/R_G)$) gives the equivalent input referred spot-noise voltage at the noninverting input, as shown in 方程式 2:

$$E_N = \sqrt{E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \tag{2}$$

Evaluating these two equations for the OPA695 circuit and component values shown in 图 6-1 gives a total output spot-noise voltage of 18.7 nV/ √ Hz and a total equivalent input spot-noise voltage of 2.3 nV/ √ Hz. This total input referred spot-noise voltage is higher than the 1.8-nV/ √ Hz specification for the operational amplifier voltage noise alone. This reflects the noise added to the output by the inverting current noise times the feedback resistor. If the feedback resistor is reduced in high-gain configurations (as suggested previously), the total input referred voltage noise given by 方程式 2 just approaches the 1.8 nV/ √ Hz of the operational amplifier. For example, going to a gain of +20 (using R_F = 200 Ω) gives a total input referred noise of 2.0 nV/ √ Hz.

For a more complete discussion of operational amplifier noise calculation, see the *Noise Analysis for High Speed Op Amps* application note, available through www.ti.com.

7.1.1.6 Thermal Analysis

The OPA695 does not require an additional heat sink for most applications. The maximum desired junction temperature sets the maximum allowed internal power dissipation as described in this section. Do not exceed the maximum junction temperature of 150°C.

Operating junction temperature (T_J) is given by $T_A + P_D \times \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the device. P_{DL} depends on the required output signal and load. However, for a grounded resistive load, P_{DL} is at a maximum when the output is fixed at a voltage equal to one-half of either supply voltage (for equal bipolar supplies). Under this condition, $P_{DL} = V_S 2 / (4 \times R_L)$, where R_L includes feedback network loading.

Note that the power in the output stage and not into the load determines internal power dissipation.

As an absolute worst-case example, compute the maximum T_J using an OPA695IDBV (SOT23-6 package) in the circuit of 图 6-1 operating at the maximum specified ambient temperature of +85°C and driving a grounded 100-Ω load.

$$P_D = 10\ V \times 14.1\ mA + 52 / (4 \times (100\ \Omega\ ||\ 458\ \Omega)) = 217\ mW \quad (3)$$

$$\text{Maximum } T_J = +85°C + (0.22\ W \times 150°C/W) = 118°C \quad (4)$$

This maximum operating junction temperature is much less than most system level targets. Most applications are lower as an absolute worst-case output stage power was assumed in this calculation.

7.1.2 LO Buffer Amplifier

The OPA695 can also be used to buffer the local oscillator (LO) from the mixer. Operating at a voltage gain of +2 V/V, the OPA695 provides excellent load isolation for the LO, with a net gain of 0 dB to the mixer. Applications through a 1.4-GHz LO can be considered, but best operation is for an LO < 1.0 GHz at a gain of +2 V/V. Gain can also be provided by the OPA695 to drive higher power levels into the mixer. 图 7-5 shows one option for the OPA695 as an LO buffer. The OPA695 can drive multiple output loads; therefore, two identical LO signals can be delivered to the mixers in a diversity receiver by tapping the output off through two series 50-Ω output resistors. This circuit is set up for a voltage gain of +2 V/V to the output pin for a gain of +1 V/V (0 dB) to the mixers, but can be easily adjusted to deliver higher gains.

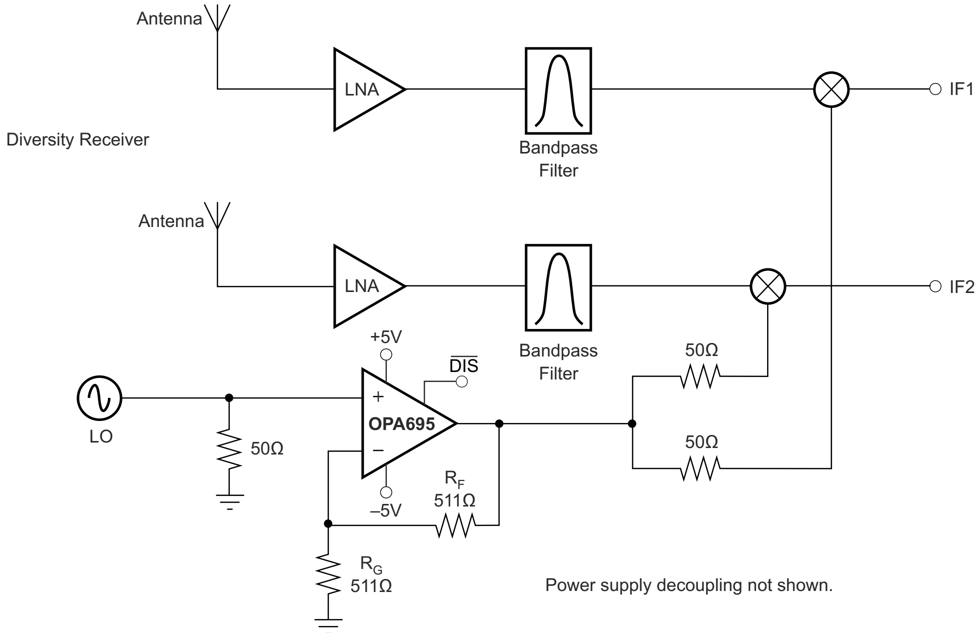


图 7-5. Dual Output LO Buffer

7.1.3 Wideband Cable Driving Applications

The high slew rate and bandwidth of the OPA695 can be used to meet the most demanding cable driving applications.

7.1.3.1 Cable Modem Return Path Driver

The standard cable modem upstream driver is typically required to drive high power over a 5-MHz to 65-MHz bandwidth while delivering < –50-dBc distortion. Highly-integrated solutions (including programmable gain stages) often fall short of this target as a result of high losses from the amplifier output to the line. The higher gain-operating capability of the OPA695 and the very high slew rate provide a low-cost device for delivering this signal with the required spurious-free dynamic range. 图 7-6 shows one example of using the OPA695 as an upstream driver for a cable modem return path. In this case, the input impedance of the driver is set to 75 Ω by the gain resistor (R_G). The required input level from the adjustable gain stage is significantly reduced by the 15.5-dB gain provided by the OPA695. In this example, the physical 75-Ω output matching resistor, along with the 3-dB loss in the diplexer, attenuate the output swing by 9 dB on the line. In this example, a single +12-V supply id used to achieve the lowest harmonic distortion for the 6-V_{PP} output pin voltage through 65 MHz. Measured performance for this example gives a 600-MHz small-signal bandwidth and < –54-dBc distortion through 65 MHz for a 6-V_{PP} output pin voltage swing.

An alternative to this circuit that gives even lower distortion is a differential driver using two OPA695 devices driving into an output transformer. The differential driver can be used to either double the available line power or improve distortion by cutting the required output swing in half for each stage. The channel disable required by the MCNS specification must be implemented by using the PGA disable feature. The MCNS disable specification requires that an output impedance match be maintained with the signal channel shut off. The disable feature of the OPA695 is intended principally for power savings and puts the output and inverting input pins into a high-impedance mode, but does not maintain the required output-impedance matching. Turning off the signal at the input of 图 7-6, while keeping the OPA695 active, maintains the impedance matching while putting very little noise on the line. The line noise in disable for the circuit of 图 7-6 (with the PGA source turned off, but still presenting a 75-Ω source impedance) is a very low 4 nV/√Hz (–157 dBm/Hz) as a result of the low input noise of the OPA695.

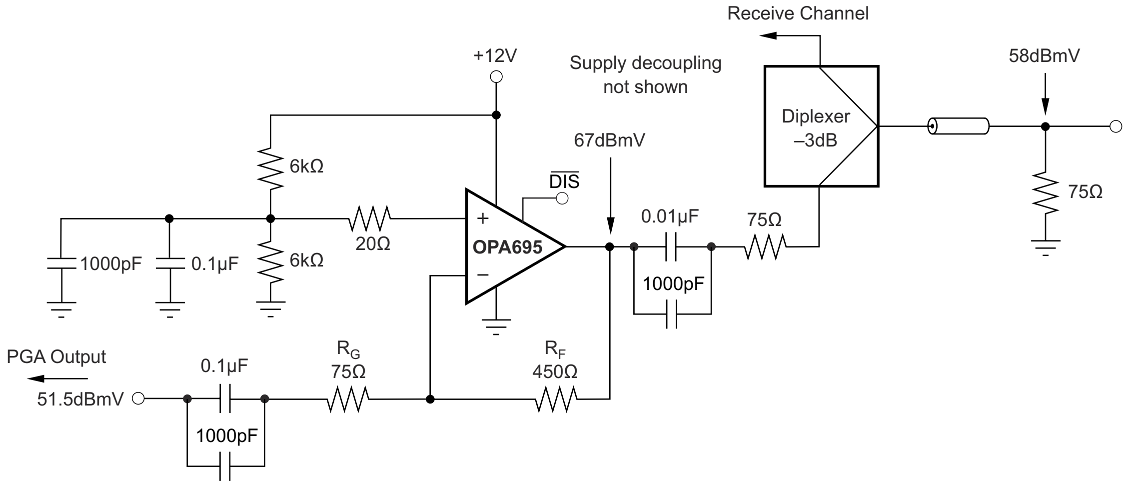


图 7-6. Cable Modem Upstream Driver

7.1.3.2 Arbitrary Waveform Driver

The OPA695 can be used as the output stage for moderate output power arbitrary waveform driver applications. Driving out through a series 50-Ω matching resistor into a 50-Ω matched load allows up to a 4.0-V_{PP} swing at the matched load (15 dBm) when operating the OPA695 on a ±5-V power supply. This level of power is available for gains of either ±8 V/V with a flat response through 100 MHz. When interfacing directly from a complementary current output DAC, consider the circuit of 图 7-7, modified for the peak output currents of the particular DAC being considered. Where purely ac-coupled output signals are required from a complementary current output DAC, consider a push-pull output stage using the circuit of 图 7-7. The resistor values here have been calculated for a 20-mA peak output current DAC, which produces up to a 5-V_{PP} swing at the matched load (18 dBm). This approach gives higher power at the load, with lower 2nd-harmonic distortion.

For a 20-mA peak output current DAC, the midscale current of 10 mA gives a 2-V dc output common-mode operating voltage, due to the 200-Ω resistor to ground at the outputs. The total ac impedance at each output is 50 Ω, giving a ±0.5-V swing around this 2-V common-mode voltage for the DAC. These resistors also act as a current divider, sending 75% of the DAC output current through the feedback resistor (464 Ω). The blocking capacitor references the OPA695 output voltage to ground, and turns the unipolar DAC output current into a bipolar swing of 0.75 × 20 mA × 464 Ω = 7 V_{PP} at each amplifier output. Each output is exactly 180° out-of-phase from the other, producing double 7 V_{PP} into the matching resistors. To limit the peak output current and improve distortion, the circuit of 图 7-7 is set up with a 1.4:1 step-down transformer. This reflects the 50-Ω load to be 100 Ω at the primary side of the transformer. For the maximum 14-V_{PP} swing across the outputs of the two amplifiers, the matching resistors drop this to 7 V_{PP} at the input of the transformer, then down to 5-V_{PP} maximum at the 50-Ω load at the output of the transformer. This step-down approach reduces the peak output current to 14 V_P/(200 Ω) = 70 mA.

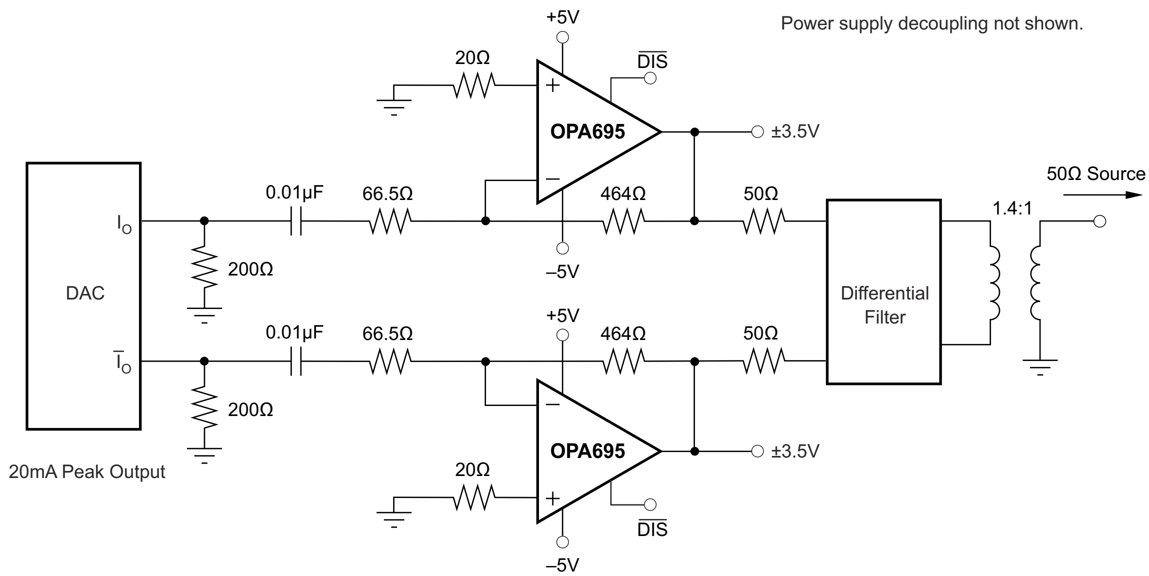


图 7-7. High Power, Wideband AC-Coupled Arbitrary Waveform Driver

7.1.4 Differential I/O Applications

The OPA695 offers very low 3rd-order distortion terms with a dominant 2nd-order distortion for the single amplifier operation. For the lowest distortion, particularly where differential outputs are needed, operating two OPA695 devices in a differential I/O design suppresses these even-order terms, delivering extremely low harmonic distortion through high frequencies and powers. Differential outputs are often preferred for high-performance ADCs, twisted-pair driving, and mixer interfaces. Two basic approaches to differential I/Os are the noninverting or inverting configurations. Because the output is differential, the signal polarity is somewhat meaningless; the noninverting and inverting terminology applies here to where the input is brought into the two OPA695s. Each approach has advantages and disadvantages. 图 7-8 shows a basic starting point for noninverting differential I/O applications.

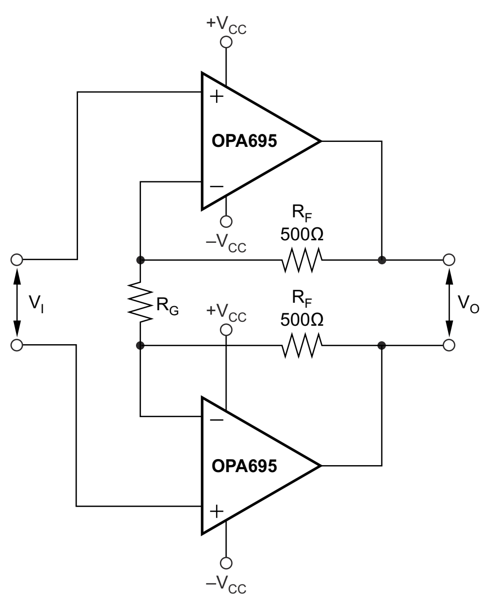


图 7-8. Noninverting Input Differential I/O Amplifier

This approach allows for a source termination impedance independent of the signal gain. For instance, simple differential filters can be included in the signal path directly to the noninverting inputs without interacting with the gain setting. The differential signal gain for the circuit of 图 7-8 is:

$$A_D = 1 + 2 \times R_F / R_G \quad (5)$$

Because the OPA695 is a current-feedback amplifier, bandwidth is principally controlled with the feedback resistor value: 图 7-8 shows a typical value of 500 Ω. However, the differential gain can be adjusted with considerable freedom using just the R_G resistor. R_G can be a reactive network providing an isolated shaping to the differential frequency response. AC-coupled applications often include a blocking capacitor in series with R_G. This blocking capacitor reduces the gain to +1 V/V at low frequency, rising to the A_D expression shown previously at higher frequencies.

图 7-9 shows a differential I/O stage configured as an inverting amplifier. In this case, the gain resistors (R_G) become part of the input resistance for the source. This configuration provides a better noise performance than the noninverting configuration, but limits the flexibility in setting the input impedance separately from the gain.

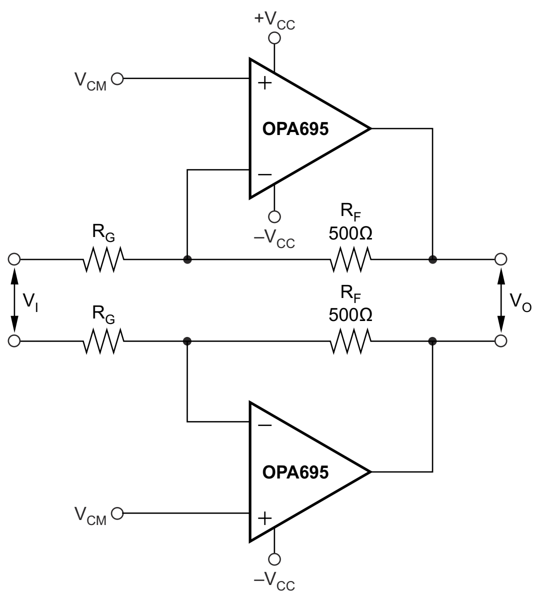


图 7-9. Inverting Input Differential I/O Amplifier

The two noninverting inputs provide an easy common-mode control input, particularly if the source is ac-coupled through either blocking caps or a transformer. In either case, the common-mode input voltages on the two noninverting inputs again have a gain of +1 V/V to the output pins, giving easy common-mode control for single-supply operation. In this configuration, the OPA695 constrains the feedback to the 500-Ω region for best frequency response. With R_F fixed, the input resistors can be adjusted to the desired gain, but also change the input impedance. The high-frequency common-mode gain for this circuit from input to output is the same as for the signal gain. Again, if the source includes an undesired common-mode signal, the signal can be rejected at the input using blocking caps (for low-frequency and dc common-mode) or a transformer coupling. The differential signal gain in the circuit of 图 7-9 is:

$$A_D = R_F / R_G \quad (6)$$

Using this configuration suppresses the 2nd-harmonics, leaving only 3rd-harmonic terms as the limit to output SFDR. The higher slew rate of the inverting configuration also extends the full-power bandwidth and the range of low intermodulation distortion over the performance bandwidth available from the circuit of 图 7-8.

7.2 Typical Application

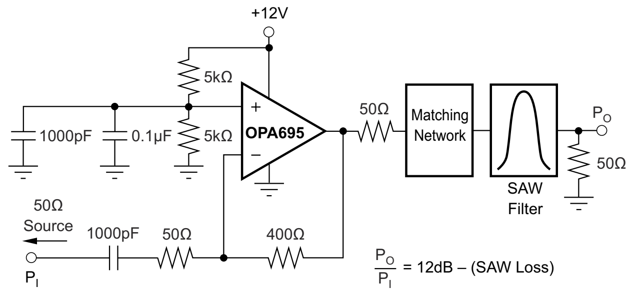


图 7-10. IF Amplifier Driving SAW Filter

7.2.1 Design Requirements

7.2.1.1 Saw Filter Buffer

One common requirement in an IF strip is to buffer the output of a mixer with enough gain to recover the insertion loss of a narrow-band SAW filter. 图 7-10 shows one possible configuration driving a SAW filter. 图 7-11 shows the intercept at the 50-Ω load. Operating in the inverting mode at a voltage gain of –8 V/V, this circuit provides a 50-Ω input match using the gain set resistor, has the feedback optimized for maximum bandwidth (700 MHz in this case), and drives through a 50-Ω output resistor into the matching network at the input of the SAW filter. If the SAW filter gives a 12-dB insertion loss, a net gain of 0 dB to the 50-Ω load at the output of the SAW (which can be the input impedance of the next IF amplifier or mixer) is delivered in the pass band of the SAW filter. Using the OPA695 in this application isolates the first mixer from the impedance of the SAW filter and provides very low two-tone, 3rd-order spurious levels in the SAW filter bandwidth. Inverting operation gives the broadest bandwidth up to a gain of –12 V/V (15.6 dB). Noninverting operation gives higher bandwidth at gain settings higher than this, but also gives a slight reduction in intercept and noise figure performance.

7.2.2 Detailed Design Procedure

The design procedure begins with calculating the required signal gain and signal swing. After the gain and swing requirements are determined the appropriate amplifier is selected along with the required supply voltage. As a result of the input impedance of 50 Ω, the gain and the input impedance require a feedback resistor value of 400 Ω.

In this application, the supply voltage is 12 V and single ended. To provide the proper dc operating point, apply a midsupply voltage to the noninverting input by using a resistive voltage divider composed of two 1% precision 5-kΩ resistors along with two ceramic bypass capacitors. These components provide an accurate and low ac impedance reference voltage for the noninverting input. The inverting input requires only an ac-coupling capacitor to isolate the 6-V operating voltage from the signal source. In this example, a ceramic 1000-pF capacitor is used.

The circuit in 图 7-10 shows an output resistor value of 50 Ω. Adjust this resistor to accommodate the SAW input impedance. Additional L/C components can be required as well; consult the SAW manufacturer's design guidelines for more details.

7.2.3 Application Curve

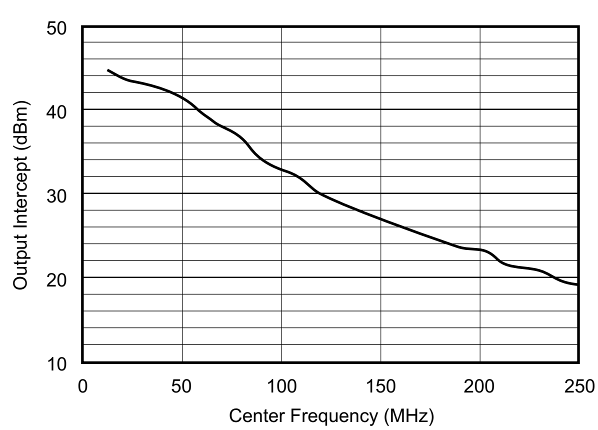


图 7-11. 2-Tone, 3rd-Order Intermodulation Intercept

7.3 Power Supply Recommendations

High-speed amplifiers require low inductance power supply traces and low ESR bypass capacitors. When possible, use both power and ground planes in the printed circuit board design, and the power plane must be adjacent to the ground plane in the board stack-up. Center the power-supply voltage on the desired amplifier output voltage, so for ground-referenced output signals, split supplies are required. Use a power-supply voltage from 5 V to 12 V.

7.4 Layout

7.4.1 Layout Guidelines

Achieving optimized performance with a high-frequency amplifier like the OPA695 requires careful attention to board layout parasitics and external component types. Recommendations to optimize performance include:

- **Minimize parasitic capacitance to any ac ground for all of the signal I/O pins.** Parasitic capacitance on the output and inverting input pins can cause instability; on the noninverting input, parasitic capacitance can react with the source impedance to cause unintentional band-limiting. To reduce unwanted capacitance, a open a window around the signal I/O pins in all of the ground and power planes around those pins. Otherwise, ground and power planes must be unbroken elsewhere on the board.
- **Minimize the distance (< 0.25") from the power supply pins to high frequency 0.1-µF decoupling capacitors.** At the device pins, the ground and power plane layout must not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Always decouple the power-supply connections with these capacitors. An optional supply-decoupling capacitor across the two power supplies (for bipolar operation) improves 2nd-harmonic distortion performance. Larger (2.2 µF to 6.8 µF) decoupling capacitors, effective at a lower frequency, must also be used on the main supply pins. These decoupling capacitors can be placed somewhat farther from the device, and can be shared among several devices in the same area of the PCB.
- **Careful selection and placement of external components preserves the high-frequency performance of the OPA695.** Use low-reactance-type resistors. Surface-mount resistors work best and allow a tighter overall layout. Metal-film and carbon composition, axially-leaded resistors can also provide good high-frequency performance. Keep the leads and PCB trace length as short as possible. Never use wirewound-type resistors in a high frequency application. The output pin and inverting input pin are the most sensitive to parasitic capacitance; therefore, always position the feedback and series output resistor, if any, as close as possible to the output pin. Place other network components, such as noninverting input termination resistors, close to the package. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. The frequency response is primarily determined by the feedback resistor value. Increasing the value reduces the bandwidth, while decreasing the value gives a more peaked frequency response. The 402-Ω feedback resistor (used in the typical performance specifications at a gain of +8 on ±5-V supplies) is a good starting point for design. Note that a 523-Ω feedback resistor, rather than a direct short, is required for the unity gain follower application. A current-feedback operational amplifier requires a feedback resistor, even in the unity gain follower configuration, to control stability.
- **Connections to other wideband devices on the board can be made with short direct traces or through onboard transmission lines.** For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 mils to 100 mils) must be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set the series isolation resistance from the isolation resistance versus capacitive load characteristics. If a long trace is required, and the 6-dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50-Ω environment is usually not necessary on board. In fact, a higher impedance environment improves distortion, as shown in the distortion versus load plots. With a characteristic board trace impedance defined (based on board material and trace dimensions), use a matching series resistor into the trace from the output of the OPA695. Also use terminating shunt resistor at the input of the destination device. Remember that the terminating impedance is the parallel combination of

the shunt resistor and the input impedance of the destination device; set this total effective impedance to match the trace impedance. The high output voltage and current capability of the OPA695 allows multiple destination devices to be handled as separate transmission lines, each with series and shunt terminations. If the 6-dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case, and set the series isolation resistance from the isolation resistance versus capacitive load characteristics. This setting does not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, some signal attenuation occurs due to the voltage divider formed by the series output into the terminating impedance.

- **Socketing a high-speed part like the OPA695 is not recommended.** The additional lead length and pin-to-pin capacitance introduced by the socket can create a troublesome parasitic network, which makes achieving a smooth, stable frequency response almost impossible. Best results are obtained by soldering the OPA695 directly onto the board.

7.4.2 Layout Example

As detailed in *节 7.4.1* and illustrated in 图 7-12, place the input termination resistor, output resistor, and bypass capacitors close to the amplifier. Power and ground planes can be placed under the amplifier, but must be removed under the input and output pins as shown in 图 7-12.

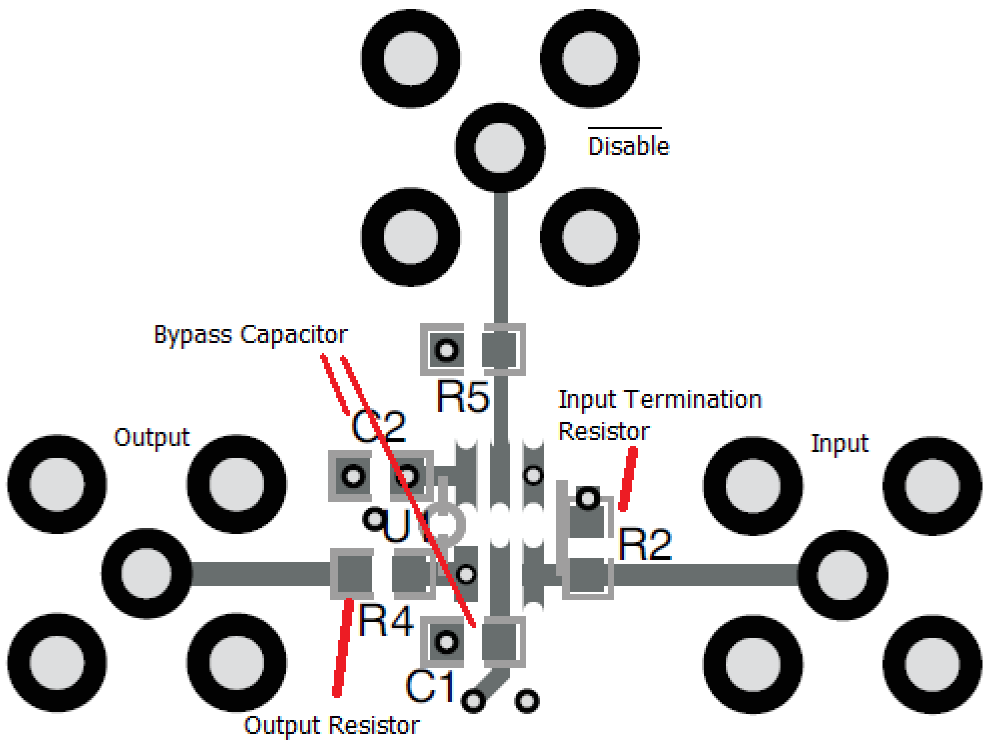


图 7-12. SBOS293 Layout

8 Device and Documentation Support

8.1 Device Support

8.1.1 Design-In Tools

8.1.1.1 Demonstration Fixtures

Two printed circuit boards (PCBs) are available to assist in the initial evaluation of circuit performance using the OPA695 in the two package options. Both of these are offered free of charge as unpopulated PCBs, delivered with a user's guide. 表 8-1 shows the summary information for these fixtures.

表 8-1. Demonstration Boards

PRODUCT	PACKAGE	ORDERING NUMBER	USER'S GUIDE LITERATURE NUMBER
OPA695ID	VSSOP-8	DEM-OPA-SO-1B	SBOU026
OPA691IDBV	SOT23-6	DEM-OPA-SOT-1B	SBOU027

The demonstration fixtures can be requested at the Texas Instruments web site (www.ti.com) through the OPA695 product folder.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Absolute Maximum Ratings for Soldering*
- Texas Instruments, *Current Feedback Op Amp Applications Circuit Guide, Application Note OA--07*
- Texas Instruments, *Frequent Faux Pas in Applying Wideband Current Feedback Amplifiers, Application Note OA-15*
- Texas Instruments, *Noise Analysis for Comlinear Amplifiers, Application Note OA-12*
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics*

8.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.4 支持资源

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链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

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8.6 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision H (April 2015) to Revision I (October 2024) **Page**

- 更新了整个文档中的表格、图和交叉参考的编号格式 1
- Changed the supply voltage specification from ±6.5 V to 13 V in *Absolute Maximum Ratings* 4
- Updated the footnote in *Absolute Maximum Ratings* to add clarification 4
- Added continuous input current specification to *Absolute Maximum Ratings* 4
- Deleted machine model (MM) specification from *ESD Ratings* 4
- Updated thermal specifications for D and DBV package in *Thermal Information* 4
- Deleted T_A = 0°C to +70°C specifications from across all *Electrical Characteristics* Table 5
- Deleted the minimum, maximum, and over temperature specifications in the *Electrical Characteristics: AC Performance* sections 5
- Changed SSBW at G = +1 V/V from 1700 MHz to 1900 MHz in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table 5
- Changed SSBW at G = +2 V/V from 1400 MHz to 900 MHz in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table 5
- Changed typical SSBW at G = +8 V/V from 450 MHz to 600 MHz in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table 5
- Changed SSBW at G = +16 V/V from 350 MHz to 500 MHz in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table 5
- Changed Bandwidth for 0.2-dB gain flatness from 320 MHz to 120 MHz in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table 5
- Changed typical Peaking at a gain of +1V/V from 4.6 dB to 3.7 dB in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table 5
- Changed LSBW at G = 8 V/V from 450 MHz to 510 MHz in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table 5
- Changed typical Slew rate at G = –8 V/V from 4300 V/μs to 5000 V/μs in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table 5
- Changed typical Slew rate at G = +8 V/V from 4300 V/μs to 5000 V/μs in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table 5
- Changed Rise and fall time at V_O = 0.5-V Step from 0.8 ns to 0.65 ns in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table 5
- Changed Rise and fall time at V_O = 4-V Step from 1 ns to 0.7 ns in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table 5
- Changed Settling time to 0.5% of 10 ns from Settling time to 0.1% of 10 ns in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table 5
- Deleted settling time to 0.02% and 0.1% from *Electrical Characteristics Table* 5
- Changed typical 2nd-order Harmonic Distortion at R_L = 100 Ω from –65 dBc to –75 dBc in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table 5
- Changed typical 3rd-order Harmonic Distortion at R_L = 100 Ω from –86 dBc to –92 dBc in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table 5
- Changed typical Input voltage noise from 1.8 nV/√Hz to 2 nV/√Hz in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table 5
- Changed typical noninverting input current noise from 18 pA/√Hz to 14 pA/√Hz in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table 5
- Deleted differential gain and differential phase specifications from across all *Electrical Characteristics* 5
- Changed typical Open-loop transimpedance gain from 85 kΩ to 300 kΩ in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table 5

- Changed typical Inverting input bias current from ±20 μA to ±5 μA in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table.......... 5
- Added typical specification for Average inverting input bias current drift in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table.......... 5
- Changed typical Common-mode input range from ±3.3 V to ±3.4 V in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table.......... 5
- Changed typical Common-mode rejection ratio from 56 dB to 65 dB in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table.......... 5
- Changed Noninverting input impedance from 280 || 1.2 (kΩ || pF) to 450 || 2 (kΩ || pF) in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table.......... 5
- Changed Inverting input resistance from 29 Ω to 20 Ω in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table.......... 5
- Changed minimum Output voltage swing at no load from ±4 V to ±3.95 V in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table.......... 5
- Changed typical Output voltage swing at no load from ±4.2 V to ±4.05 V in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table.......... 5
- Changed minimum Output voltage swing at no load, T_A = –40°C to +85°C from ±3.9 V to ±3.85 V in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table.......... 5
- Changed minimum Output voltage swing at R_L = 100 Ω from ±3.7 V to ±3.65 V in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table.......... 5
- Changed typical Output voltage swing at R_L = 100 Ω from ±3.9 V to ±3.75 V in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table.......... 5
- Changed minimum Output voltage swing at R_L = 100 Ω, T_A = –40°C to +85°C from ±3.6 V to ±3.55 V in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table.......... 5
- Changed typical Output current sourcing from 120 mA to 140 mA in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table.......... 5
- Changed typical Output current sourcing from –120 mA to –140 mA in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table.......... 5
- Changed Closed-Loop output impedance from 0.04 Ω to 0.02 Ω in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table.......... 5
- Changed typical Quiescent current from 12.9 mA to 14 mA in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table.......... 5
- Changed minimum and maximum Quiescent current from 12.6 mA and 13.3 mA to 11.7 mA and 15.6 mA in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table.......... 5
- Changed minimum and maximum Quiescent current, T_A = –40°C to +85°C from 11 mA and 14.1 mA to 10 mA and 18 mA in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table.......... 5
- Changed typical negative power-supply rejection ratio from 55 dB to 72 dB in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table.......... 5
- Changed minimum Power-down quiescent current from –170 μA to 200 μA in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table.......... 5
- Changed typical Power-down quiescent current from –100 μA to 160 μA in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table.......... 5
- Changed minimum Power-down quiescent current, T_A = –40°C to +85°C from –192 μA to 210 μA in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table.......... 5
- Changed Disable time from 1 μs to 4 μs in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table.......... 5
- Changed Enable time from 25 ns to 80 ns in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table.......... 5
- Changed Output capacitance in disable from 4 pF to 2.5 pF in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table.......... 5

- Changed typical Enable voltage threshold from 3.3 V to 3 V in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table....... 5
- Changed typical Disable voltage threshold from 1.8 V to 2.3 V in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table....... 5
- Changed typical Disable Control pin input bias current from 75 µA to 95 µA in *Electrical Characteristics: V_S = ±5 V, OPA695D, OPA695DBV* Table....... 5
- Updated test level related and current polarity footnote across the *Electrical Characteristics* 5
- Changed SSBW at G = 1 V/V from 1400 MHz to 1200 MHz in *Electrical Characteristics: V_S = 5 V, OPA695D, OPA695DBV* 8
- Changed SSBW at G = 2 V/V from 960 MHz to 700 MHz in *Electrical Characteristics: V_S = 5 V, OPA695D, OPA695DBV* 8
- Changed typical SSBW at G = 8 V/V from 395 MHz to 500 MHz in *Electrical Characteristics: V_S = 5 V, OPA695D, OPA695DBV* 8
- Changed typical SSBW at G = 16 V/V from 235 MHz to 410 MHz in *Electrical Characteristics: V_S = 5 V, OPA695D, OPA695DBV* 8
- Changed Bandwidth for 0.2-dB gain flatness from 230 MHz to 110 MHz in *Electrical Characteristics: V_S = 5 V, OPA695D, OPA695DBV* 8
- Changed typical Peaking at a gain of +1V/V from 1 dB to 2.2 dB in *Electrical Characteristics: V_S = 5 V, OPA695D, OPA695DBV* 8
- Changed LSBW at G = 8 V/V from 310 MHz to 430 MHz in *Electrical Characteristics: V_S = 5 V, OPA695D, OPA695DBV* 8
- Changed typical Slew rate at G = +8 V/V from 1700 V/µs to 2500 V/µs in *Electrical Characteristics: V_S = 5 V, OPA695D, OPA695DBV* 8
- Changed Rise and fall time at V_O = 0.5-V step from 1 ns to 0.7 ns in *Electrical Characteristics: V_S = 5 V, OPA695D, OPA695DBV* 8
- Changed Rise and fall time at V_O = 2-V step from 1 ns to 0.8 ns in *Electrical Characteristics: V_S = 5 V, OPA695D, OPA695DBV* 8
- Changed Settling time to 0.5% of 10 ns from Settling time to 0.1% of 10 ns in *Electrical Characteristics: V_S = 5 V, OPA695D, OPA695DBV* 8
- Changed typical 2nd-order harmonic distortion at R_L = 100 Ω to –69 dBc from –62 dBc in *Electrical Characteristics: V_S = 5 V, OPA695D, OPA695DBV* 8
- Changed typical 2nd-order harmonic distortion at R_L = 500 Ω to –68 dBc from –70 dBc in *Electrical Characteristics: V_S = 5 V, OPA695D, OPA695DBV* 8
- Changed typical 3rd-order harmonic distortion at R_L = 100 Ω to –62 dBc from –66 dBc in *Electrical Characteristics: V_S = 5 V, OPA695D, OPA695DBV* 8
- Changed typical 3rd -order harmonic distortion at R_L = 500 Ω to –63 dBc from –65 dBc in *Electrical Characteristics: V_S = 5 V, OPA695D, OPA695DBV* 8
- Changed typical Input voltage noise from 1.8 nV/√Hz to 1.9 nV/√Hz in *Electrical Characteristics: V_S = 5 V, OPA695D, OPA695DBV* 8
- Changed typical Noninverting input current noise from 18 pA/√Hz to 14 pA/√Hz in *Electrical Characteristics: V_S = 5 V, OPA695D, OPA695DBV* 8
- Changed typical Open-loop transimpedance gain from 70 kΩ to 250 kΩ in *Electrical Characteristics: V_S = 5 V, OPA695D, OPA695DBV* 8
- Changed typical Noninverting input bias current from ±5 µA to +15 µA in *Electrical Characteristics: V_S = 5 V, OPA695D, OPA695DBV* 8
- Changed typical Common-mode input range (positive) from 3.3 V to 3.4 V in *Electrical Characteristics: V_S = 5 V, OPA695D, OPA695DBV* 8
- Changed typical Common-mode input range (negative) from 1.7 V to 1.6 V in *Electrical Characteristics: V_S = 5 V, OPA695D, OPA695DBV* 8
- Changed typical Common-mode rejection ratio from 54 dB to 65 dB in *Electrical Characteristics: V_S = 5 V, OPA695D, OPA695DBV* 8

- Changed Noninverting input impedance from 280 || 1.2 (kΩ || pF) to 250 || 2 (kΩ || pF) in *Electrical Characteristics: V_S = 5 V, OPA695D, OPA695DBV* 8
- Changed Inverting input resistance from 32 Ω to 21 Ω in *Electrical Characteristics: V_S = 5 V, OPA695D, OPA695DBV* 8
- Changed typical Output voltage (positive) at no load from 4.2 V to 4.05 V in *Electrical Characteristics: V_S = 5 V, OPA695D, OPA695DBV* 8
- Changed minimum Output voltage swing (positive) at no load from 4 V to 3.95 V in *Electrical Characteristics: V_S = 5 V, OPA695D, OPA695DBV* 8
- Changed minimum Output voltage swing (positive) at no load, T_A = –40°C to +85°C from 3.8 V to 3.75 V in *Electrical Characteristics: V_S = 5 V, OPA695D, OPA695DBV* 8
- Changed maximum Output voltage swing (negative) at no load from 1 V to 1.05 V in *Electrical Characteristics: V_S = 5 V, OPA695D, OPA695DBV* 8
- Changed typical Output voltage swing (negative) at no load from 0.8 V to 0.9 V in *Electrical Characteristics: V_S = 5 V, OPA695D, OPA695DBV* 8
- Changed maximum Output voltage swing (negative) at no load, T_A = –40°C to +85°C from 1.2 V to 1.25 V in *Electrical Characteristics: V_S = 5 V, OPA695D, OPA695DBV* 8
- Changed typical Output current sourcing from 90 mA to 100 mA in *Electrical Characteristics: V_S = 5 V, OPA695D, OPA695DBV* 8
- Changed minimum Output current sinking, T_A = –40°C to +85°C from –66 mA to –60 mA in *Electrical Characteristics: V_S = 5 V, OPA695D, OPA695DBV* 8
- Changed Closed-loop output impedance from 0.05 Ω to 0.02 Ω in *Electrical Characteristics: V_S = 5 V, OPA695D, OPA695DBV* 8
- Changed maximum Quiescent current from 12 mA to 14.4 mA in *Electrical Characteristics: V_S = 5 V, OPA695D, OPA695DBV* 8
- Changed maximum Quiescent current, T_A = –40°C to +85°C from 12.9 mA to 17.1 mA in *Electrical Characteristics: V_S = 5 V, OPA695D, OPA695DBV* 8
- Changed typical Negative power-supply rejection ratio from 51 dB to 69 dB in *Electrical Characteristics: V_S = 5 V, OPA695D, OPA695DBV* Table....8
- Changed typical Power-down quiescent current from -95 μA to 120 μA in *Electrical Characteristics: V_S = 5 V, OPA695D, OPA695DBV* Table....8
- Changed Disable time from 1 μs to 5 μs in *Electrical Characteristics: V_S = 5 V, OPA695D, OPA695DBV* 8
- Changed Enable time from 25 ns to 80 ns in *Electrical Characteristics: V_S = 5 V, OPA695D, OPA695DBV* 8
- Changed typical Enable voltage threshold from 3.3 V to 3.1 V in *Electrical Characteristics: V_S = 5 V, OPA695D, OPA695DBV* 8
- Changed typical Disable voltage threshold from 1.8 V to 2.4 V in *Electrical Characteristics: V_S = 5 V, OPA695D, OPA695DBV* 8
- Changed typical Disable Control pin input bias current from 75 μA to 95 μA in *Electrical Characteristics: V_S = 5 V, OPA695D, OPA695DBV* Table....8
- Deleted Composite Video dG/dϕ plot from *Typical Characteristics: V_S = ±5 V, OPA695IDGK* 24
- Deleted the differential operation plots from *Typical Characteristics: V_S = ±5 V, OPA695IDGK* and differential small signal parameter measurement information section....24
- Deleted *RF Specifications and Applications, Input Return Loss (S11), Output Return Loss (S22), Forward Gain (S21), Reverse Isolation* and *Limits to Dynamic Range* from *Feature Description* 31
- Deleted *SAW Filter Buffer* and *RGB Video Line Driver* sections from *Application Information* 34

Changes from Revision G (April 2009) to Revision H (April 2015) **Page**

- 添加了 *ESD 等级* 表、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及 *机械、封装和可订购信息* 部分....1

Changes from Revision F (July 2006) to Revision G (April 2009)	Page
• 向*封装订购信息* 表和*电气特性* 表中的热阻规格添加了 DGK (MSOP-8) 封装	1

Changes from Revision E (March 2006) to Revision F (July 2006)	Page
• Changed Storage Temperature Range from −40°C to +125°C to −65°C to +125°C	4

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA695DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	O695
OPA695ID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	OPA 695
OPA695IDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A71L
OPA695IDBVT	Obsolete	Production	SOT-23 (DBV) | 6	-	-	Call TI	Call TI	-40 to 85	A71L
OPA695IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	695
OPA695IDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	695
OPA695IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 695

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

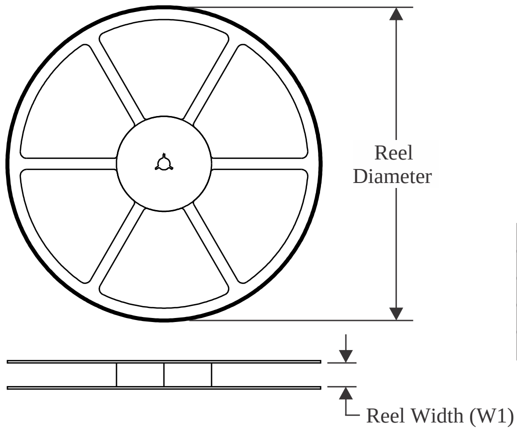
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

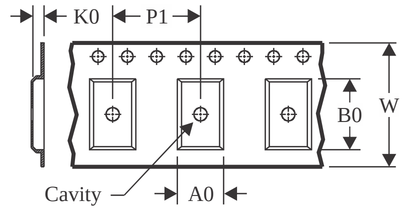
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

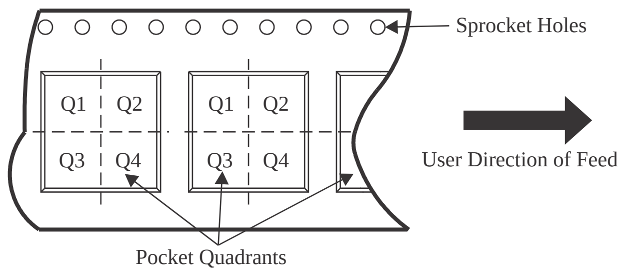


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

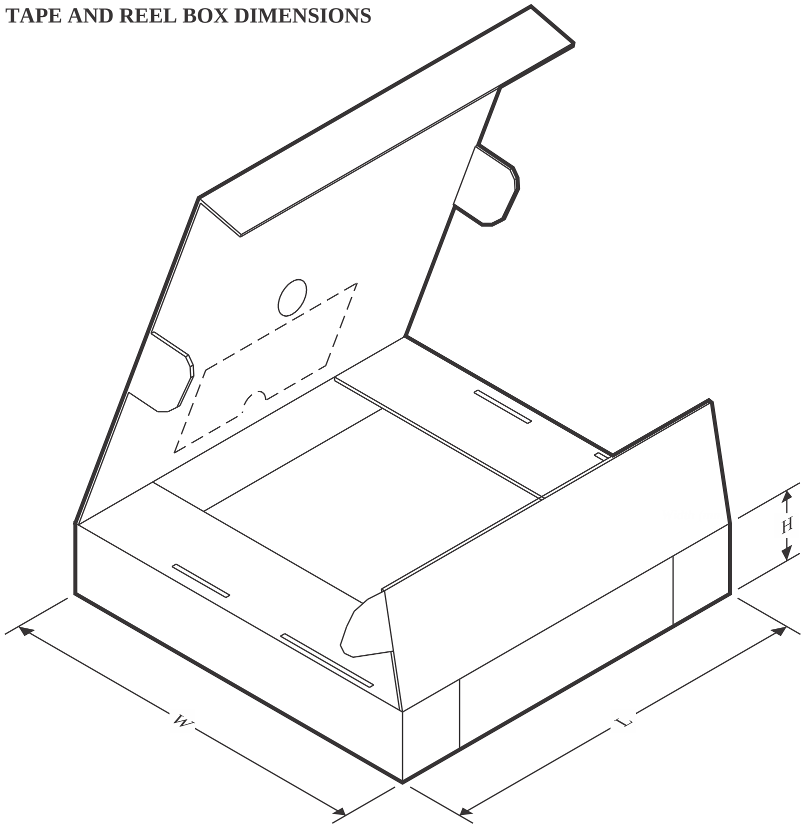
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

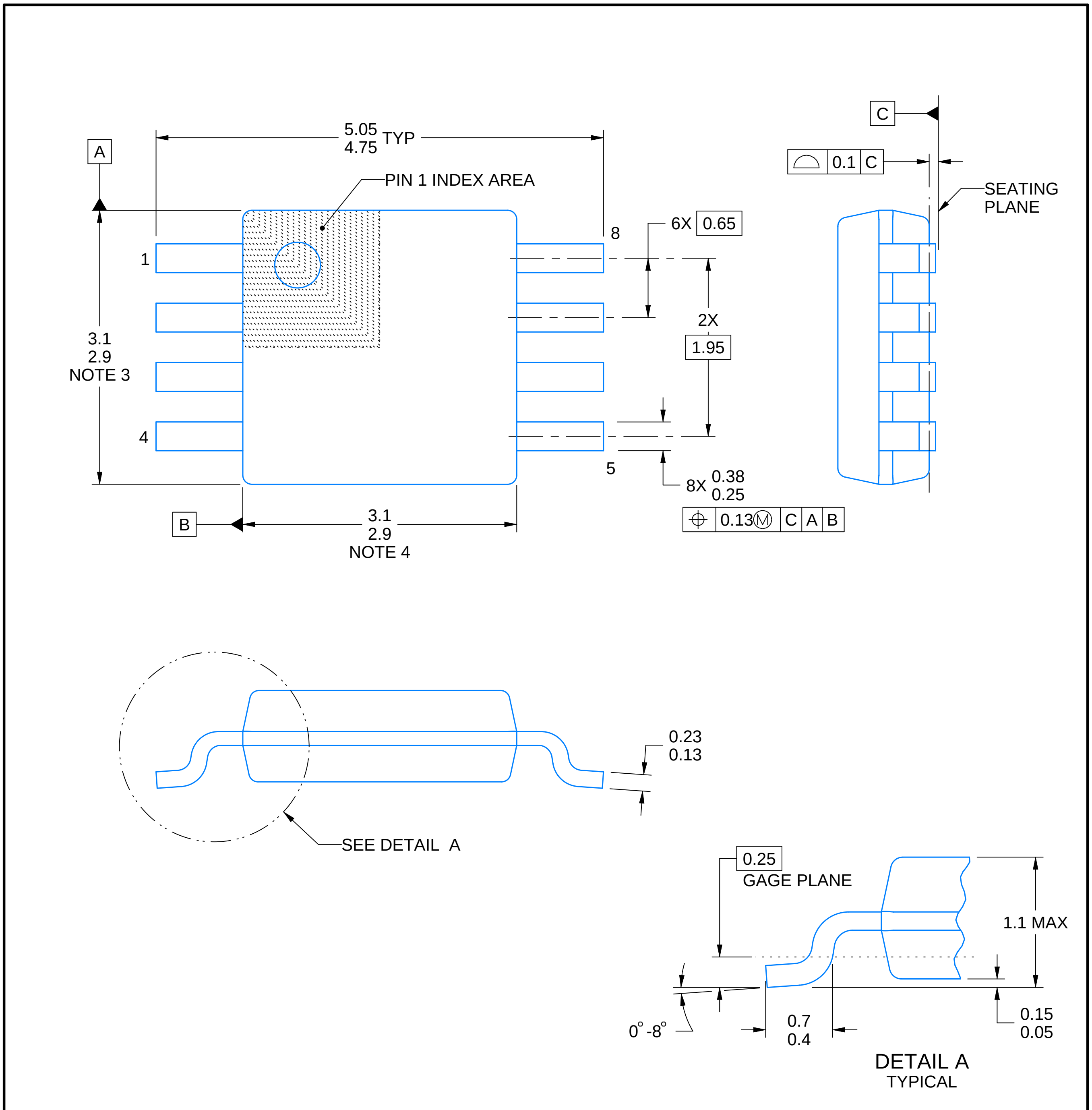
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA695DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
OPA695IDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA695IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA695IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA695IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA695IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA695DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
OPA695IDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
OPA695IDGKR	VSSOP	DGK	8	2500	356.0	356.0	35.0
OPA695IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA695IDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA695IDR	SOIC	D	8	2500	353.0	353.0	32.0

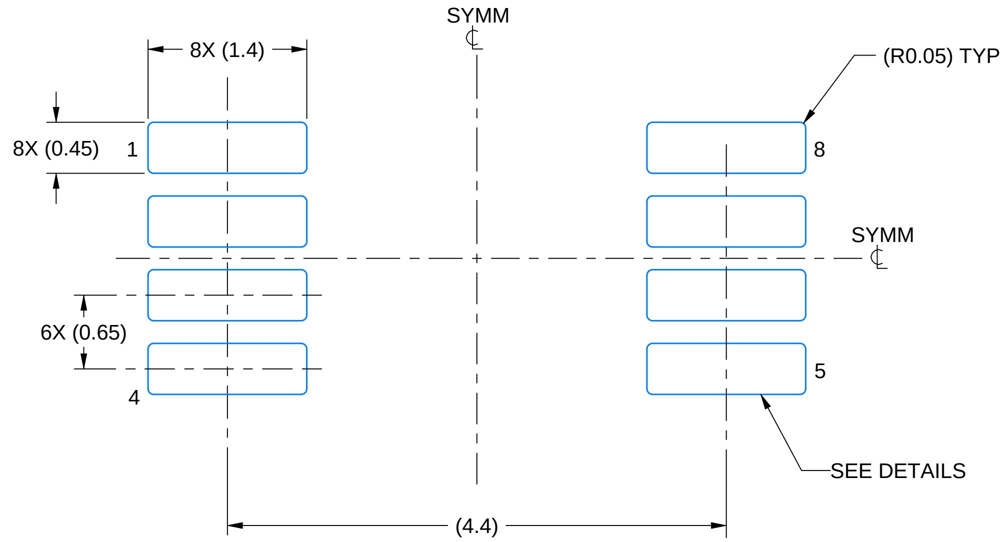


4214862/A 04/2023

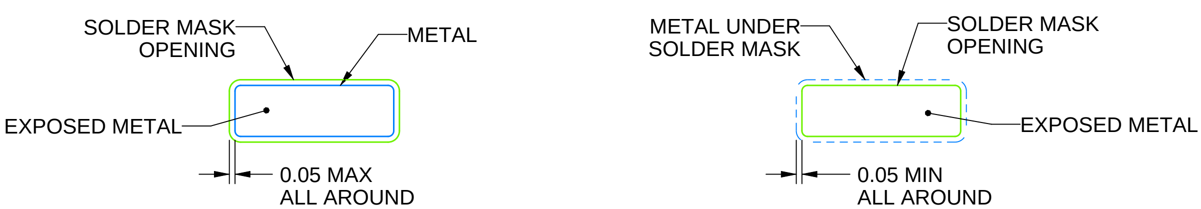
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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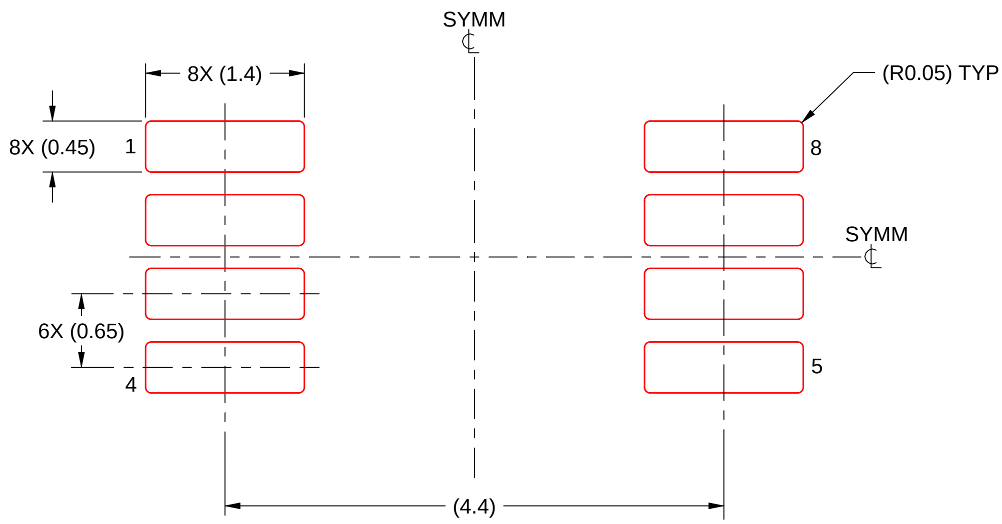
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

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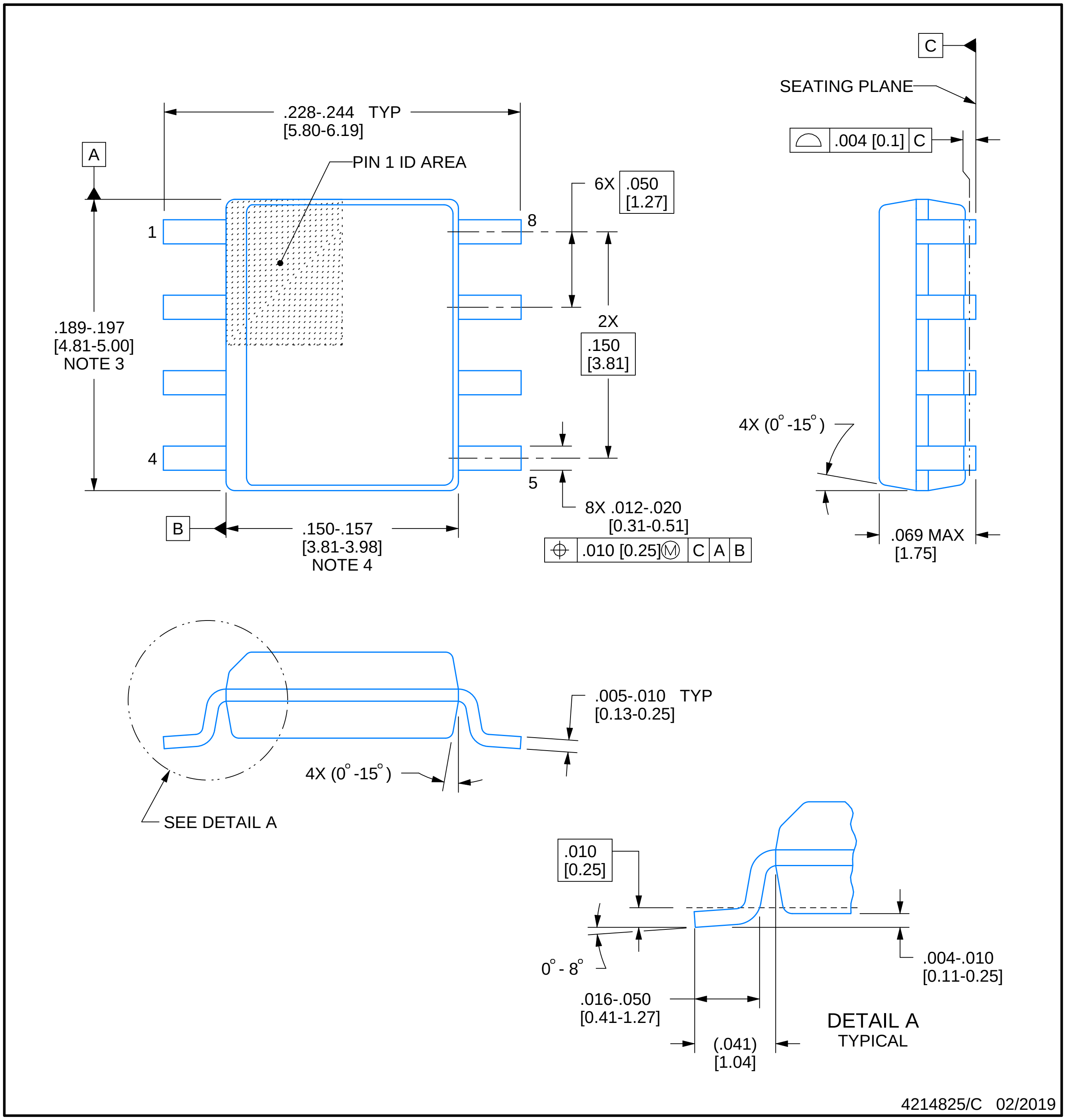
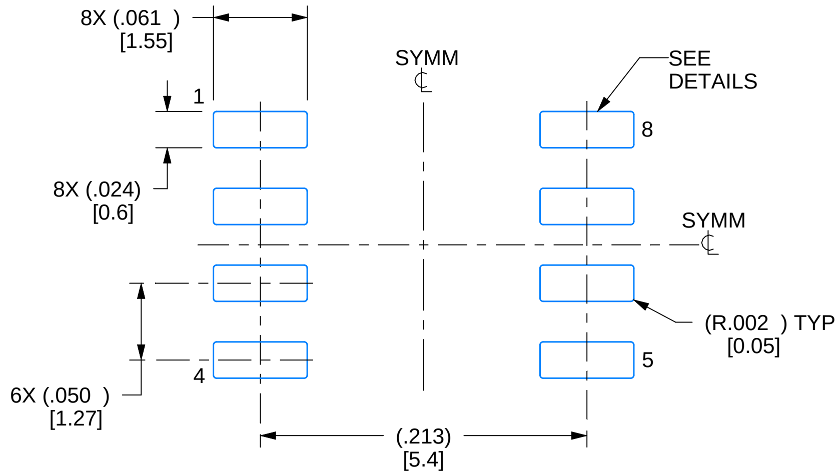
NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

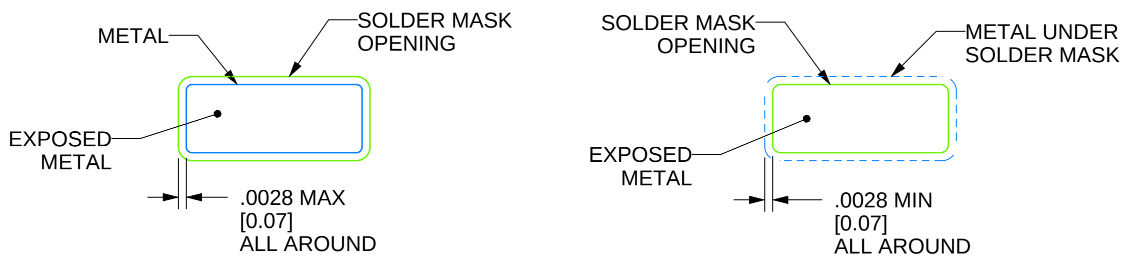


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

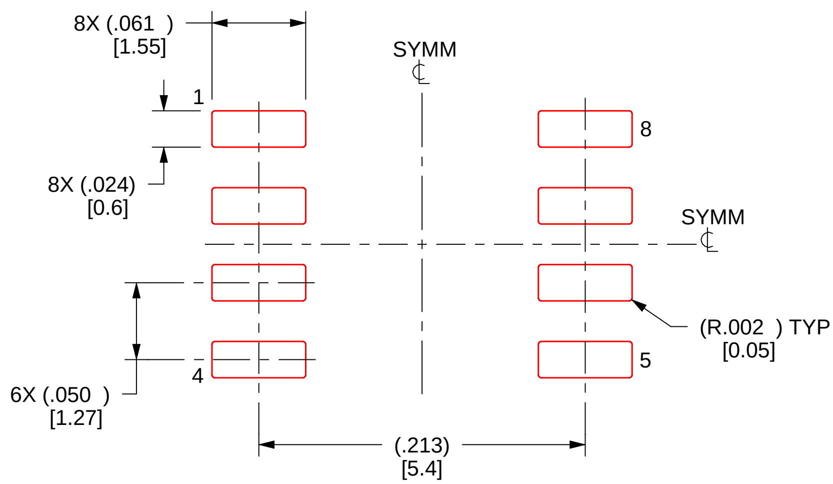
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

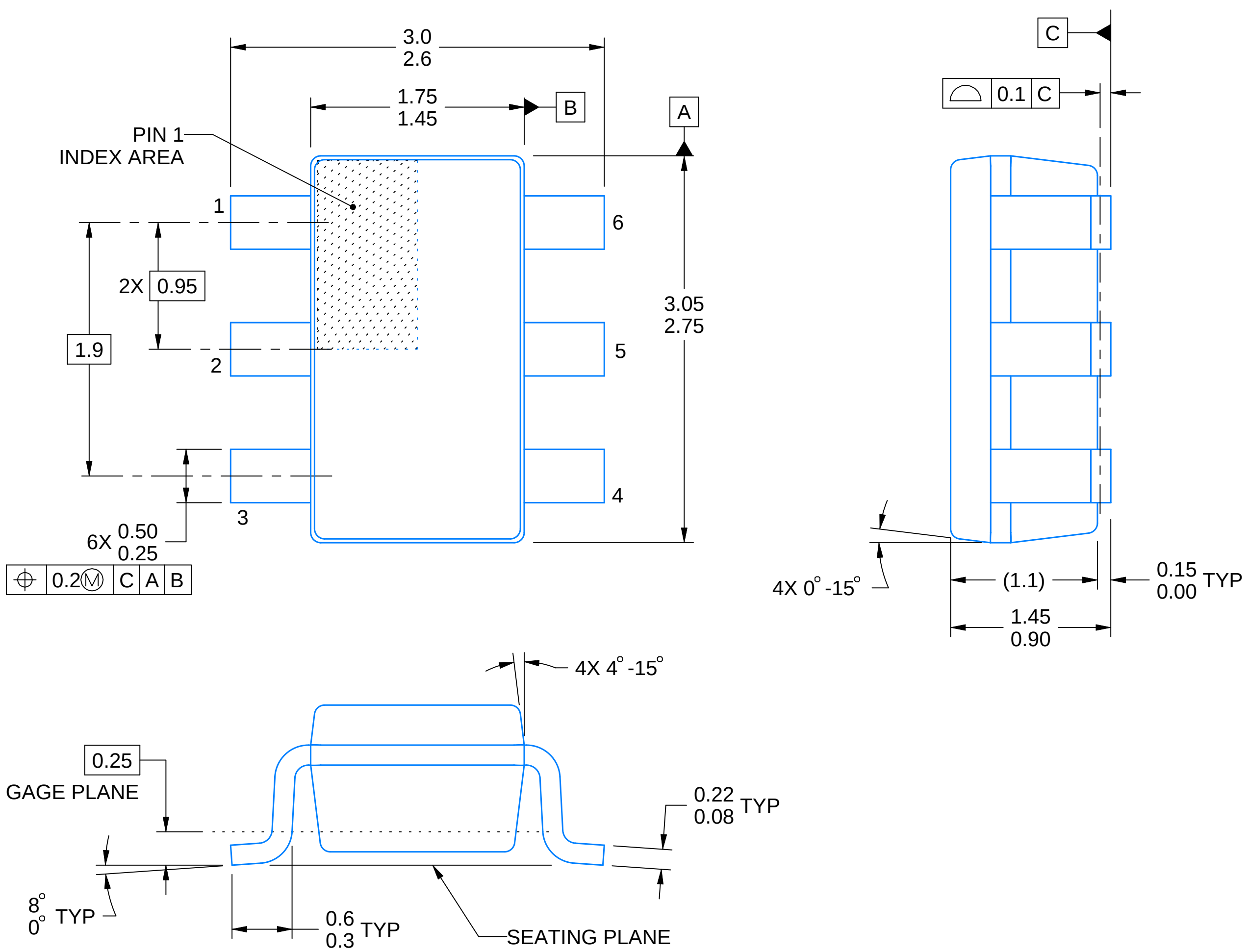


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

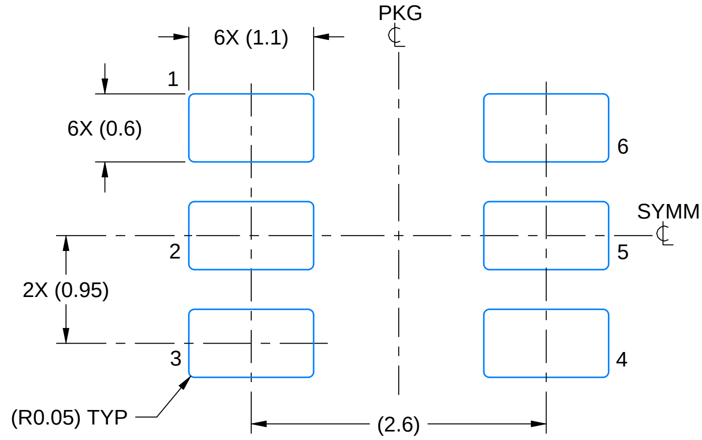
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



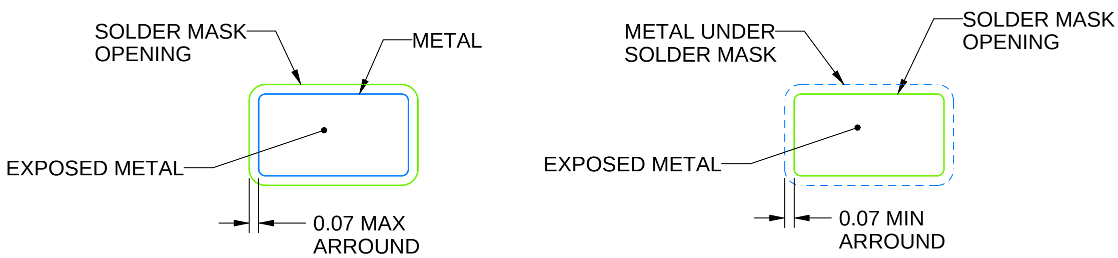
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

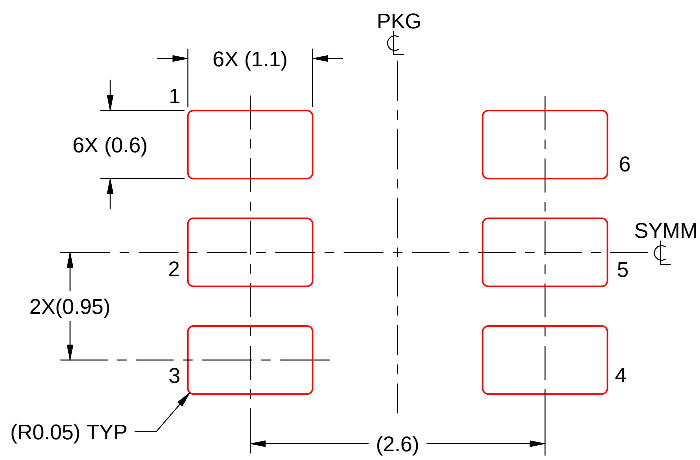


SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

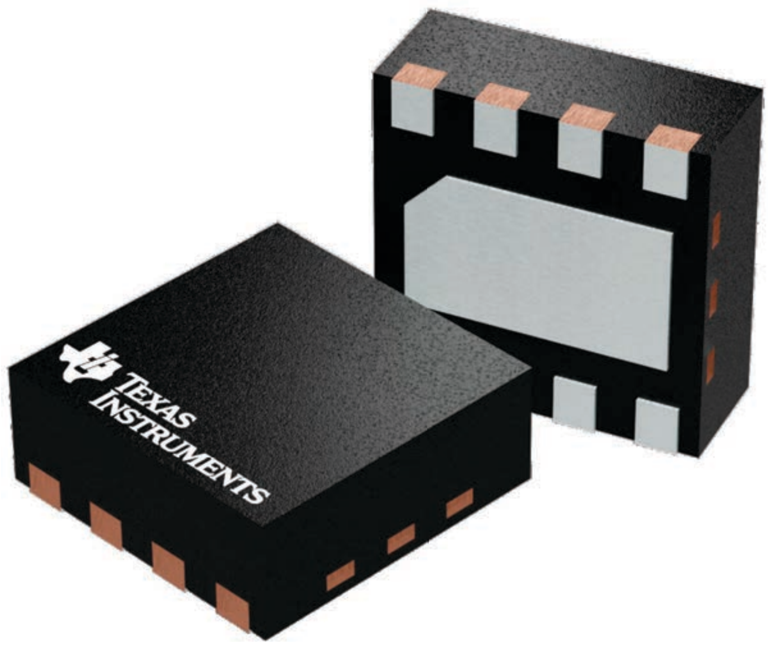
DSG 8

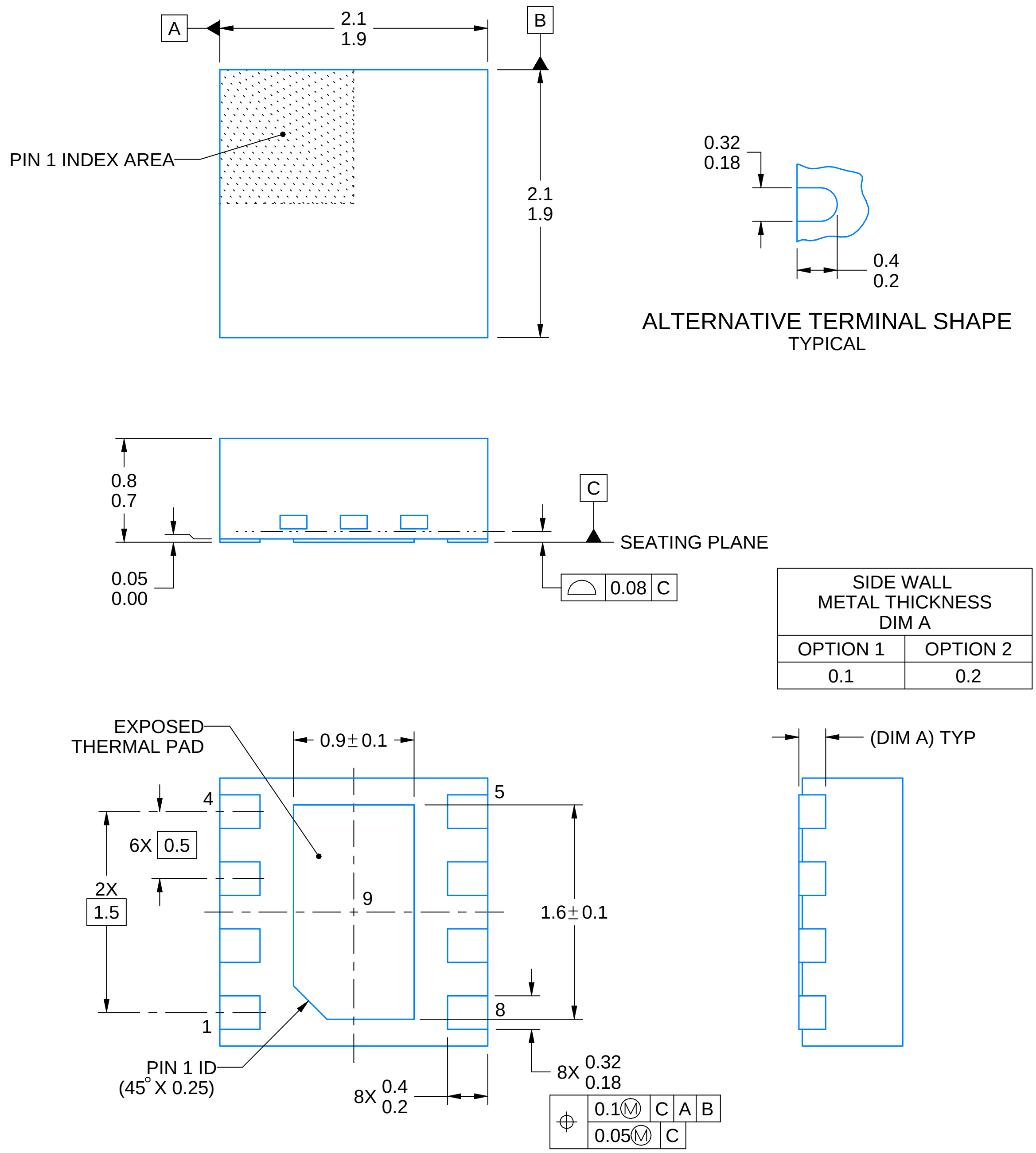
WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



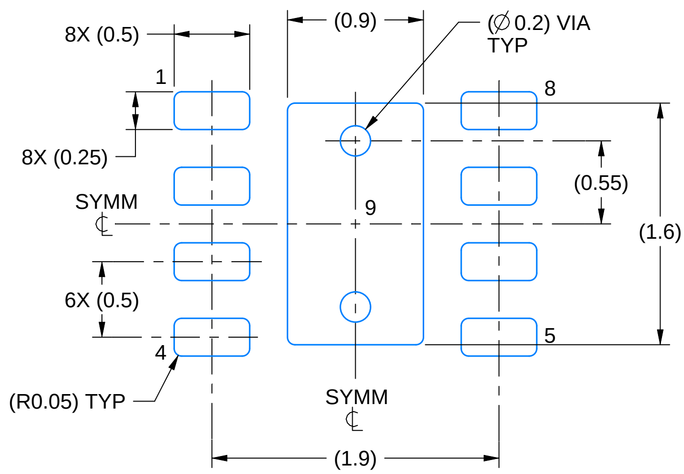


SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

4218900/E 08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

NON SOLDER MASK
DEFINED
(PREFERRED)

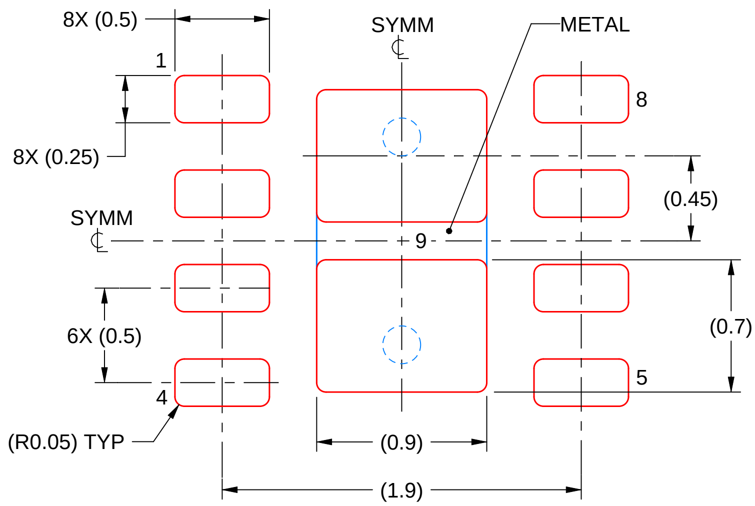
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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