



## TS5A3157 10-Ω SPDT Analog Switch

### 1 Features

- Low ON-State Resistance (10 Ω)
- Control Inputs Are 5-V Tolerant
- Low Charge Injection
- Excellent ON-State Resistance Matching
- Low Total Harmonic Distortion (THD)
- 1.65-V to 5.5-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

### 2 Applications

- Sample-and-Hold Circuits
- Battery-Powered Equipment
- Audio and Video Signal Routing
- Communication Circuits

### 3 Description

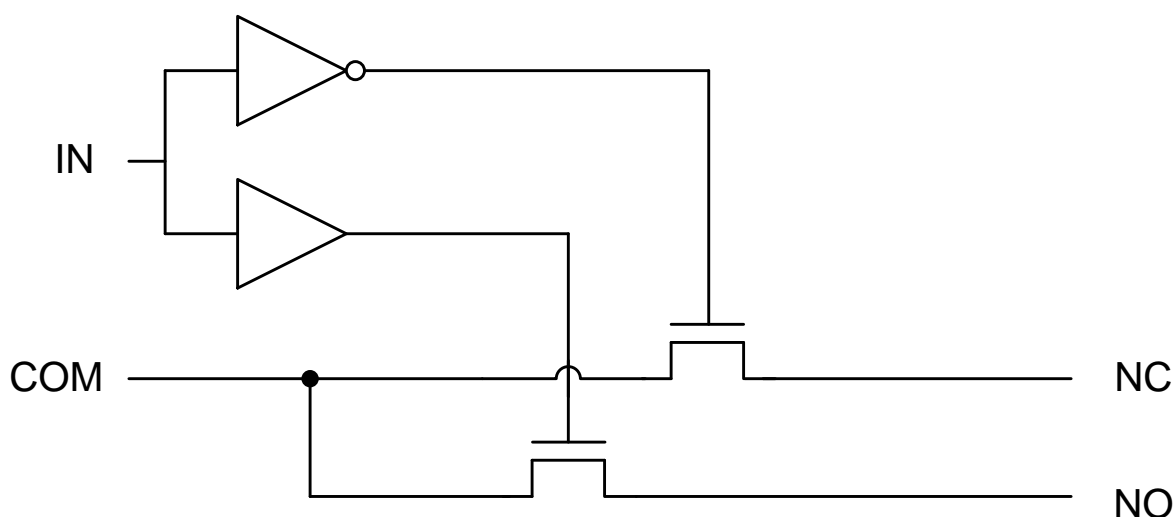
The TS5A3157 device is a single-pole double-throw (SPDT) analog switch that is designed to operate from 1.65 V to 5.5 V. This device can handle both digital and analog signals, and signals up to  $V_+$  can be transmitted in either direction.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS5A3157	SOT-23 (6)	2.90 mm × 1.60 mm
	SC70 (6)	2.00 mm × 1.25 mm
	DSBGA (6)	1.39 mm × 0.89 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Block Diagram



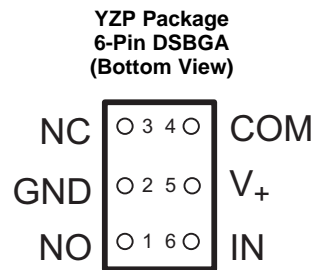
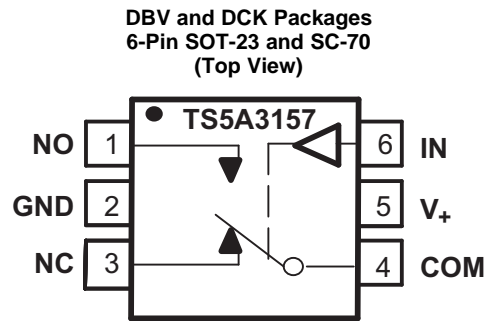
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## 4 Revision History

Changes from Revision A (September 2004) to Revision B	Page
<ul style="list-style-type: none"> <li>Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....</li> <li>Removed <i>Ordering Information</i> table. ....</li> </ul>	<b>1</b>
Changes from Original (August 2004) to Revision A	Page
<ul style="list-style-type: none"> <li>Updated document to new TI data sheet format - no specification changes. ....</li> </ul>	<b>1</b>

## 5 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	NO	I/O	Normally open switch port
2	GND	—	Ground
3	NC	I/O	Normally closed switch port
4	COM	I/O	Common switch port
5	V+	—	Power supply
6	IN	I	Switch select. High = COM connected to NO; Low = COM connected to NC.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)(2)</sup>

		MIN	MAX	UNIT
$V_+$	Supply voltage <sup>(3)</sup>	−0.5	6.5	V
$V_{NO}$ $V_{NC}$ $V_{COM}$	Analog voltage <sup>(3)(4)(5)</sup>	−0.5	$V_+ + 0.5$	V
$I_K$	Analog port diode current $V_{NC}, V_{NO}, V_{COM} < 0$ or $V_{NO}, V_{NC}, V_{COM} > V_+$	−50	50	mA
$I_{NO}$ $I_{NC}$ $I_{COM}$	On-state switch current $V_{NC}, V_{NO}, V_{COM} = 0$ to $V_+$	−50	50	mA
$V_I$	Digital input voltage <sup>(3)(4)</sup>	−0.5	6.5	V
$I_{IK}$	Digital input clamp current $V_I < 0$	−50		mA
$I_+$	Continuous current through $V_+$	−100	100	mA
$I_{GND}$	Continuous current through GND	−100	100	mA
$T_{stg}$	Storage temperature	−65	150	°C

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
- (3) All voltages are with respect to ground, unless otherwise specified.
- (4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (5) This value is limited to 5.5 V maximum.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{IO}$	Switch input/output voltage	0	$V_+$	V
$V_+$	Supply voltage	1.65	5.5	V
$V_I$	Control input voltage	0	5.5	V
$T_A$	Operating temperature	−40	85	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TS5A3157			UNIT
		DBV (SOT-23)	DCK (SC-70)	YZP (DSBGA)	
		6 PINS	6 PINS	6 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	206	252	132	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics for 5-V Supply

 $V_+ = 4.5 \text{ V to } 5.5 \text{ V}$ ,  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$  (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS		T <sub>A</sub>	V <sub>+</sub>	MIN	TYP	MAX	UNIT
Analog Switch									
V <sub>COM</sub> , V <sub>NO</sub> , V <sub>NC</sub>	Analog signal range					0		V <sub>+</sub>	V
r <sub>on</sub>	ON-state resistance	0 ≤ (V <sub>NO</sub> or V <sub>NC</sub> ) ≤ V <sub>+</sub> , I <sub>COM</sub> = −30 mA,	Switch ON, see <a href="#">Figure 12</a>	25°C	4.5 V	5.5		10	Ω
				Full				12	
Δr <sub>on</sub>	ON-state resistance match between channels	V <sub>NO</sub> or V <sub>NC</sub> = 3.15 V, I <sub>COM</sub> = −30 mA,	Switch ON, see <a href="#">Figure 12</a>	25°C	4.5 V	0.15		0.2	Ω
				Full				0.3	
r <sub>on(flat)</sub>	ON-state resistance flatness	0 ≤ (V <sub>NO</sub> or V <sub>NC</sub> ) ≤ V <sub>+</sub> , I <sub>COM</sub> = −30 mA,	Switch ON, see <a href="#">Figure 12</a>	25°C	4.5 V	4		5	Ω
				Full				6	
I <sub>NO(OFF)</sub> , I <sub>NC(OFF)</sub>	NO, NC OFF leakage current	V <sub>NO</sub> or V <sub>NC</sub> = 1 V, V <sub>COM</sub> = 4.5 V, or V <sub>NO</sub> or V <sub>NC</sub> = 4.5 V, V <sub>COM</sub> = 1 V,	Switch OFF, see <a href="#">Figure 13</a>	25°C	5.5 V	−0.1	0.05	0.1	μA
				Full			−0.2	0.1	
I <sub>NO(ON)</sub> , I <sub>NC(ON)</sub>	NO, NC ON leakage current	V <sub>NO</sub> = 1 V, V <sub>COM</sub> = Open, or V <sub>NO</sub> = 4.5 V, V <sub>COM</sub> = Open,	Switch ON, see <a href="#">Figure 14</a>	25°C	5.5 V	−0.1	0.05	0.1	μA
				Full			−0.2	0.1	
I <sub>COM(ON)</sub>	COM ON leakage current	V <sub>COM</sub> = 1 V, V <sub>NO</sub> or V <sub>NC</sub> = Open, or V <sub>COM</sub> = 4.5 V, V <sub>NO</sub> or V <sub>NC</sub> = Open,	Switch ON, see <a href="#">Figure 14</a>	25°C	5.5 V	−0.1	0.05	0.1	μA
				Full			−0.2	0.1	
Digital Control Input (IN)									
V <sub>IH</sub>	Input logic high			Full		V <sub>+</sub> × 0.7		5.5	V
V <sub>IL</sub>	Input logic low			Full		0		V <sub>+</sub> × 0.3	V
I <sub>IH</sub> , I <sub>IL</sub>	Input leakage current	V <sub>I</sub> = 5.5 V or 0		25°C	5.5 V	−0.1	0.05	0.1	μA
				Full			−1		
Dynamic									
t <sub>ON</sub>	Turnon time	V <sub>COM</sub> = 3 V, R <sub>L</sub> = 300 Ω,	C <sub>L</sub> = 35 pF, see <a href="#">Figure 16</a>	25°C	5 V	1	6	8.5	ns
				Full	4.5 V to 5.5 V	1		9.5	
t <sub>OFF</sub>	Turnoff time	V <sub>COM</sub> = 3 V, R <sub>L</sub> = 300 Ω,	C <sub>L</sub> = 35 pF, see <a href="#">Figure 16</a>	25°C	5 V	1	3.5	6.5	ns
				Full	4.5 V to 5.5 V	1		7.5	
t <sub>BBM</sub>	Break-before-make time	V <sub>NC</sub> = V <sub>NO</sub> = V <sub>+</sub> / 2, R <sub>L</sub> = 50 Ω,	C <sub>L</sub> = 35 pF, see <a href="#">Figure 17</a>	25°C	5 V	1.8	2	3	ns
				Full	4.5 V to 5.5 V	1.8		3.5	
Q <sub>C</sub>	Charge injection	V <sub>GEN</sub> = 0, R <sub>GEN</sub> = 0,	C <sub>L</sub> = 0.1 nF, see <a href="#">Figure 21</a>	25°C	5 V		7		pC
C <sub>NO(OFF)</sub> , C <sub>NC(OFF)</sub>	NO, NC OFF capacitance	V <sub>NO</sub> or V <sub>NC</sub> = V <sub>+</sub> or GND,	Switch OFF, see <a href="#">Figure 15</a>	25°C	5 V		5.5		pF
C <sub>NO(ON)</sub> , C <sub>NC(ON)</sub>	NO, NC ON capacitance	V <sub>NO</sub> or V <sub>NC</sub> = V <sub>+</sub> or GND,	Switch ON, see <a href="#">Figure 15</a>	25°C	5 V		17.5		pF
C <sub>COM(ON)</sub>	COM ON capacitance	V <sub>COM</sub> = V <sub>+</sub> or GND,	Switch ON, see <a href="#">Figure 15</a>	25°C	5 V		17.5		pF
C <sub>I</sub>	Digital input capacitance	V <sub>I</sub> = V <sub>+</sub> or GND,	See <a href="#">Figure 15</a>	25°C	5 V		2.8		pF

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

## Electrical Characteristics for 5-V Supply (continued)

 $V_+ = 4.5 \text{ V to } 5.5 \text{ V}$ ,  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$  (unless otherwise noted)<sup>(1)</sup>

PARAMETER	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
BW Bandwidth	$R_L = 50 \Omega$ , Switch ON, see Figure 18	$25^\circ\text{C}$	5 V		300		MHz
$O_{ISO}$ OFF isolation	$R_L = 50 \Omega$ , $f = 10 \text{ MHz}$ , Switch OFF, see Figure 19	$25^\circ\text{C}$	5 V		–65		dB
$X_{TALK}$ Crosstalk	$R_L = 50 \Omega$ , $f = 10 \text{ MHz}$ , Switch ON, see Figure 20	$25^\circ\text{C}$	5 V		–66		dB
THD Total harmonic distortion	$R_L = 600 \Omega$ , $C_L = 50 \text{ pF}$ , $f = 20 \text{ Hz to } 20 \text{ kHz}$ , see Figure 22	$25^\circ\text{C}$	5 V		0.01%		
<b>Supply</b>							
$I_+$ Positive supply current	$V_I = V_+$ or GND, Switch ON or OFF	$25^\circ\text{C}$ Full	5.5 V		2.5	5 10	$\mu\text{A}$

## 6.6 Electrical Characteristics for 3.3-V Supply

 $V_+ = 3 \text{ V to } 3.6 \text{ V}$ ,  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$  (unless otherwise noted)<sup>(1)</sup>

PARAMETER	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Analog Switch</b>							
$V_{COM}$ , $V_{NO}$ , $V_{NC}$ Analog signal range				0		$V_+$	V
$r_{on}$ ON-state resistance	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -24 \text{ mA}$ , Switch ON, see Figure 12	$25^\circ\text{C}$ Full	3 V		12	20 20	$\Omega$
$\Delta r_{on}$ ON-state resistance match between channels	$V_{NO} \text{ or } V_{NC} = 2.1 \text{ V}$ , $I_{COM} = -24 \text{ mA}$ , Switch ON, see Figure 12	$25^\circ\text{C}$ Full	3 V		0.2	0.4 0.3	$\Omega$
$r_{on(Flat)}$ ON-state resistance flatness	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -24 \text{ mA}$ , Switch ON, see Figure 12	$25^\circ\text{C}$ Full	3 V		9	11 12	$\Omega$
$I_{NO(OFF)}$ , $I_{NC(OFF)}$ NO, NC OFF leakage current	$V_{NO} \text{ or } V_{NC} = 1 \text{ V}$ , $V_{COM} = 3 \text{ V}$ , or $V_{NO} \text{ or } V_{NC} = 3 \text{ V}$ , $V_{COM} = 1 \text{ V}$ , Switch OFF, see Figure 13	$25^\circ\text{C}$ Full	3.6 V	–0.1 –0.2	0.05 0.1	0.1 0.2	$\mu\text{A}$
$I_{NO(ON)}$ , $I_{NC(ON)}$ NO, NC ON leakage current	$V_{NO} \text{ or } V_{NC} = 1 \text{ V}$ , $V_{COM} = \text{Open}$ , or $V_{NO} \text{ or } V_{NC} = 3 \text{ V}$ , $V_{COM} = \text{Open}$ , Switch ON, see Figure 14	$25^\circ\text{C}$ Full	3.6 V	–0.1 –0.2	0.05 0.1	0.1 0.2	$\mu\text{A}$
$I_{COM(ON)}$ COM ON leakage current	$V_{COM} = 1 \text{ V}$ , $V_{NO} \text{ or } V_{NC} = \text{Open}$ , or $V_{COM} = 3 \text{ V}$ , $V_{NO} \text{ or } V_{NC} = \text{Open}$ , Switch ON, see Figure 14	$25^\circ\text{C}$ Full	3.6 V	–0.1 –0.2	0.05 0.1	0.1 0.2	$\mu\text{A}$
<b>Digital Control Input (IN)</b>							
$V_{IH}$ Input logic high		Full		$V_+ \times 0.7$		5.5	V
$V_{IL}$ Input logic low		Full		0		$V_+ \times 0.3$	V
$I_{IH}$ , $I_{IL}$ Input leakage current	$V_I = 5.5 \text{ V or } 0$	$25^\circ\text{C}$ Full	3.6 V	–0.1 –1	0.05	0.1 1	$\mu\text{A}$
<b>Dynamic</b>							
$t_{ON}$ Turnon time	$V_{COM} = 2 \text{ V}$ , $R_L = 300 \Omega$ , $C_L = 35 \text{ pF}$ , see Figure 16	$25^\circ\text{C}$ Full	3.3 V 3 V to 3.6 V	3.5 1.5	7	9.5 10.5	ns

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

## Electrical Characteristics for 3.3-V Supply (continued)

 $V_+ = 3\text{ V to }3.6\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)<sup>(1)</sup>

PARAMETER	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
$t_{\text{OFF}}$ Turnoff time	$V_{\text{COM}} = 2\text{ V}$ , $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ , see <a href="#">Figure 16</a>	25°C	3.3 V	1	3.5	6.5	ns
		Full	3 V to 3.6 V	1		7.5	
$t_{\text{BBM}}$ Break-before-make time	$V_{\text{NC}} = V_{\text{NO}} = V_+ / 2$ , $R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$ , see <a href="#">Figure 17</a>	25°C	3.3 V	2.5	3	5	ns
		Full	3 V to 3.6 V	2		5	
$Q_C$ Charge injection	$V_{\text{GEN}} = 0$ , $R_{\text{GEN}} = 0$ , $C_L = 0.1\text{ nF}$ , see <a href="#">Figure 21</a>	25°C	3.3 V		3		pC
$C_{\text{NO(OFF)}}$ NO, NC OFF capacitance	$V_{\text{NO}}$ or $V_{\text{NC}} = V_+$ or GND, Switch OFF, see <a href="#">Figure 15</a>	25°C	3.3 V		5.5		pF
$C_{\text{NO(ON)}}$ NO, NC ON capacitance	$V_{\text{NO}}$ or $V_{\text{NC}} = V_+$ or GND, Switch ON, see <a href="#">Figure 15</a>	25°C	3.3 V		17.5		pF
$C_{\text{COM(ON)}}$ COM ON capacitance	$V_{\text{COM}} = V_+$ or GND, Switch ON, see <a href="#">Figure 15</a>	25°C	3.3 V		17.5		pF
$C_I$ Digital input capacitance	$V_I = V_+$ or GND, See <a href="#">Figure 15</a>	25°C	3.3 V		2.8		pF
BW Bandwidth	$R_L = 50\ \Omega$ , Switch ON, see <a href="#">Figure 18</a>	25°C	3.3 V		300		MHz
$O_{\text{ISO}}$ OFF isolation	$R_L = 50\ \Omega$ , $f = 10\text{ MHz}$ , Switch OFF, see <a href="#">Figure 19</a>	25°C	3.3 V		-65		dB
$X_{\text{TALK}}$ Crosstalk	$R_L = 50\ \Omega$ , $f = 10\text{ MHz}$ , Switch ON, see <a href="#">Figure 20</a>	25°C	3.3 V		-66		dB
THD Total harmonic distortion	$R_L = 600\ \Omega$ , $C_L = 50\text{ pF}$ , $f = 20\text{ Hz to }20\text{ kHz}$ , see <a href="#">Figure 22</a>	25°C	3.3 V		0.015 %		
<b>Supply</b>							
$I_+$ Positive supply current	$V_I = V_+$ or GND, Switch ON or OFF	25°C	3.6 V		2.5	5	$\mu\text{A}$
		Full			10		

## 6.7 Electrical Characteristics for 2.5-V Supply

 $V_+ = 2.3\text{ V to }2.7\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)<sup>(1)</sup>

PARAMETER	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Analog Switch</b>							
$V_{\text{COM}}$ , $V_{\text{NO}}$ , $V_{\text{NC}}$ Analog signal range				0		$V_+$	V
$r_{\text{on}}$ ON-state resistance	$0 \leq (V_{\text{NO}} \text{ or } V_{\text{NC}}) \leq V_+$ , $I_{\text{COM}} = -8\text{ mA}$ , Switch ON, see <a href="#">Figure 12</a>	25°C	2.3 V		35	45	$\Omega$
		Full				50	
$\Delta r_{\text{on}}$ ON-state resistance match between channels	$V_{\text{NO}}$ or $V_{\text{NC}} = 1.6\text{ V}$ , $I_{\text{COM}} = -8\text{ mA}$ , Switch ON, see <a href="#">Figure 12</a>	25°C	2.3 V		0.3	0.5	$\Omega$
		Full				0.7	
$r_{\text{on(flat)}}$ ON-state resistance flatness	$0 \leq (V_{\text{NO}} \text{ or } V_{\text{NC}}) \leq V_+$ , $I_{\text{COM}} = -8\text{ mA}$ , Switch ON, see <a href="#">Figure 12</a>	25°C	2.3 V		30	40	$\Omega$
		Full				40	
$I_{\text{NO(OFF)}}$ , $I_{\text{NC(OFF)}}$ NO, NC OFF leakage current	$V_{\text{NO}}$ or $V_{\text{NC}} = 0.5\text{ V}$ , $V_{\text{COM}} = 2.2\text{ V}$ , or $V_{\text{NO}}$ or $V_{\text{NC}} = 2.2\text{ V}$ , $V_{\text{COM}} = 0.5\text{ V}$ , Switch OFF, see <a href="#">Figure 13</a>	25°C	2.7 V	-0.1	0.05	0.1	$\mu\text{A}$
		Full		-0.2	0.1	0.2	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

## Electrical Characteristics for 2.5-V Supply (continued)

 $V_+ = 2.3 \text{ V to } 2.7 \text{ V}$ ,  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$  (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS		T <sub>A</sub>	V <sub>+</sub>	MIN	TYP	MAX	UNIT
I <sub>NO(ON)</sub> , I <sub>NC(ON)</sub>	NO, NC ON leakage current	V <sub>NO</sub> or V <sub>NC</sub> = 0.5 V, V <sub>COM</sub> = Open, or V <sub>NO</sub> or V <sub>NC</sub> = 2.2 V, V <sub>COM</sub> = Open,	Switch ON, see <a href="#">Figure 14</a>	25°C	2.7 V	−0.1	0.05	0.1	μA
				Full		−0.2	0.1	0.2	
I <sub>COM(ON)</sub>	COM ON leakage current	V <sub>COM</sub> = 0.5 V, V <sub>NO</sub> or V <sub>NC</sub> = Open, or V <sub>COM</sub> = 2.2 V, V <sub>NO</sub> or V <sub>NC</sub> = Open,	Switch ON, see <a href="#">Figure 14</a>	25°C	2.7 V	−0.1	0.05	0.1	μA
				Full		−0.2	0.1	0.2	
Digital Control Input (IN)									
V <sub>IH</sub>	Input logic high			Full		V <sub>+</sub> × 0.7		5.5	V
V <sub>IL</sub>	Input logic low			Full		0		V <sub>+</sub> × 0.3	V
I <sub>IH</sub> , I <sub>IL</sub>	Input leakage current	V <sub>I</sub> = 5.5 V or 0		25°C	2.7 V	−0.1	0.05	0.1	μA
				Full		−1		1	
Dynamic									
t <sub>ON</sub>	Turnon time	V <sub>COM</sub> = 1.5 V, R <sub>L</sub> = 300 Ω,	C <sub>L</sub> = 35 pF, see <a href="#">Figure 16</a>	25°C	2.5 V	5	8	13.5	ns
				Full	2.3 V to 2.7 V	3.5		14	
t <sub>OFF</sub>	Turnoff time	V <sub>COM</sub> = 1.5 V, R <sub>L</sub> = 300 Ω,	C <sub>L</sub> = 35 pF, see <a href="#">Figure 16</a>	25°C	2.5 V	1	3.5	6.5	ns
				Full	2.3 V to 2.7 V	1		7.5	
t <sub>BBM</sub>	Break-before- make time	V <sub>NC</sub> = V <sub>NO</sub> = V <sub>+</sub> / 2, R <sub>L</sub> = 50 Ω,	C <sub>L</sub> = 35 pF, see <a href="#">Figure 17</a>	25°C	2.5 V	3.5	5	7	ns
				Full	2.3 V to 2.7 V	3		7.5	
Q <sub>C</sub>	Charge injection	V <sub>GEN</sub> = 0, R <sub>GEN</sub> = 0,	C <sub>L</sub> = 0.1 nF, see <a href="#">Figure 21</a>	25°C	2.5 V	2			pC
C <sub>NO(OFF)</sub> , C <sub>NC(OFF)</sub>	NO, NC OFF capacitance	V <sub>NO</sub> or V <sub>NC</sub> = V <sub>+</sub> or GND,	Switch OFF, see <a href="#">Figure 15</a>	25°C	2.5 V	5.5			pF
C <sub>NO(ON)</sub> , C <sub>NC(ON)</sub>	NO, NC ON capacitance	V <sub>NO</sub> or V <sub>NC</sub> = V <sub>+</sub> or GND,	Switch ON, see <a href="#">Figure 15</a>	25°C	2.5 V	17.5			pF
C <sub>COM(ON)</sub>	COM ON capacitance	V <sub>COM</sub> = V <sub>+</sub> or GND,	Switch ON, see <a href="#">Figure 15</a>	25°C	2.5 V	17.5			pF
C <sub>I</sub>	Digital input capacitance	V <sub>I</sub> = V <sub>+</sub> or GND,	See <a href="#">Figure 15</a>	25°C	2.5 V	2.8			pF
BW	Bandwidth	R <sub>L</sub> = 50 Ω, Switch ON,	See <a href="#">Figure 18</a>	25°C	2.5 V	300			MHz
O <sub>ISO</sub>	OFF isolation	R <sub>L</sub> = 50 Ω, f = 10 MHz,	Switch OFF, see <a href="#">Figure 19</a>	25°C	2.5 V	−65			dB
X <sub>TALK</sub>	Crosstalk	R <sub>L</sub> = 50 Ω, f = 10 MHz,	Switch ON, see <a href="#">Figure 20</a>	25°C	2.5 V	−66			dB
THD	Total harmonic distortion	R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 50 pF,	f = 20 Hz to 20 kHz, see <a href="#">Figure 22</a>	25°C	2.5 V	0.025 %			
Supply									
I <sub>+</sub>	Positive supply current	V <sub>I</sub> = V <sub>+</sub> or GND,	Switch ON or OFF	25°C	2.7 V	2.5		5	μA
				Full		10			



## 6.8 Electrical Characteristics for 1.8-V Supply

 $V_+ = 1.65 \text{ V to } 1.95 \text{ V}$ ,  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$  (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS		T <sub>A</sub>	V <sub>+</sub>	MIN	TYP	MAX	UNIT
Analog Switch									
V <sub>COM</sub> , V <sub>NO</sub> , V <sub>NC</sub>	Analog signal range					0		V <sub>+</sub>	V
r <sub>on</sub>	ON-state resistance	0 ≤ (V <sub>NO</sub> or V <sub>NC</sub> ) ≤ V <sub>+</sub> , I <sub>COM</sub> = −4 mA,	Switch ON, see <a href="#">Figure 12</a>	25°C Full	1.65 V	140		160 160	Ω
Δr <sub>on</sub>	ON-state resistance match between channels	V <sub>NO</sub> or V <sub>NC</sub> = 1.16 V, I <sub>COM</sub> = −4 mA,	Switch ON, see <a href="#">Figure 12</a>	25°C Full	1.65 V	0.5		0.6 0.75	Ω
r <sub>on(flat)</sub>	ON-state resistance flatness	0 ≤ (V <sub>NO</sub> or V <sub>NC</sub> ) ≤ V <sub>+</sub> , I <sub>COM</sub> = −4 mA,	Switch ON, see <a href="#">Figure 12</a>	25°C Full	1.65 V	125		130 140	Ω
I <sub>NO(OFF)</sub> , I <sub>NC(OFF)</sub>	NO, NC OFF leakage current	V <sub>NO</sub> or V <sub>NC</sub> = 0.3 V, V <sub>COM</sub> = 1.65 V, or V <sub>NO</sub> or V <sub>NC</sub> = 1.65 V, V <sub>COM</sub> = 0.3 V,	Switch OFF, see <a href="#">Figure 13</a>	25°C Full	1.95 V	−0.1 −0.2	0.05 0.1	0.1 0.2	μA
I <sub>NO(ON)</sub> , I <sub>NC(ON)</sub>	NO, NC ON leakage current	V <sub>NO</sub> or V <sub>NC</sub> = 0.3 V, V <sub>COM</sub> = Open, or V <sub>NO</sub> or V <sub>NC</sub> = 1.65 V, V <sub>COM</sub> = Open,	Switch ON, see <a href="#">Figure 14</a>	25°C Full	1.95 V	−0.1 −0.2	0.05 0.1	0.1 0.2	μA
I <sub>COM(ON)</sub>	COM ON leakage current	V <sub>COM</sub> = 0.3 V, V <sub>NO</sub> or V <sub>NC</sub> = Open, or V <sub>COM</sub> = 1.65 V, V <sub>NO</sub> or V <sub>NC</sub> = Open,	Switch ON, see <a href="#">Figure 14</a>	25°C Full	1.95 V	−0.1 −0.2	0.05 0.1	0.1 0.2	μA
Digital Control Input (IN)									
V <sub>IH</sub>	Input logic high			Full		V <sub>+</sub> × 0.65		5.5	V
V <sub>IL</sub>	Input logic low			Full		0		V <sub>+</sub> × 0.35	V
I <sub>IH</sub> , I <sub>IL</sub>	Input leakage current	V <sub>I</sub> = 5.5 V or 0		25°C Full	1.95 V	−0.1 −1	0.05	0.1 1	μA
Dynamic									
t <sub>ON</sub>	Turnon time	V <sub>COM</sub> = 1.3 V, R <sub>L</sub> = 300 Ω,	C <sub>L</sub> = 35 pF, see <a href="#">Figure 16</a>	25°C Full	1.8 V 1.65 V to 1.95 V	5 7	15	23 24	ns
t <sub>OFF</sub>	Turnoff time	V <sub>COM</sub> = 1.3 V, R <sub>L</sub> = 300 Ω,	C <sub>L</sub> = 35 pF, see <a href="#">Figure 16</a>	25°C Full	1.8 V 1.65 V to 1.95 V	1 1	3.5	6.5 7.5	ns
t <sub>BBM</sub>	Break-before-make time	V <sub>NC</sub> = V <sub>NO</sub> = V <sub>+</sub> / 2, R <sub>L</sub> = 50 Ω,	C <sub>L</sub> = 35 pF, see <a href="#">Figure 17</a>	25°C Full	1.8 V 1.65 V to 1.95 V	5.5 5.2	7.5	9 12	ns
Q <sub>C</sub>	Charge injection	V <sub>GEN</sub> = 0, R <sub>GEN</sub> = 0,	C <sub>L</sub> = 0.1 nF, see <a href="#">Figure 21</a>	25°C	1.8 V	1			pC
C <sub>NO(OFF)</sub> , C <sub>NC(OFF)</sub>	NO, NC OFF capacitance	V <sub>NO</sub> or V <sub>NC</sub> = V <sub>+</sub> or GND,	Switch OFF, see <a href="#">Figure 15</a>	25°C	1.8 V	5.5			pF
C <sub>NO(ON)</sub> , C <sub>NC(ON)</sub>	NO, NC ON capacitance	V <sub>NO</sub> or V <sub>NC</sub> = V <sub>+</sub> or GND,	Switch ON, see <a href="#">Figure 15</a>	25°C	1.8 V	17.5			pF
C <sub>COM(ON)</sub>	COM ON capacitance	V <sub>COM</sub> = V <sub>+</sub> or GND,	Switch ON, see <a href="#">Figure 15</a>	25°C	1.8 V	17.5			pF

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

**TS5A3157**

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**Electrical Characteristics for 1.8-V Supply (continued)**
 $V_+ = 1.65\text{ V to }1.95\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS		$T_A$	$V_+$	MIN	TYP	MAX	UNIT
$C_I$	Digital input capacitance	$V_I = V_+$ or GND,	See <a href="#">Figure 15</a>	25°C	1.8 V		2.8		pF
BW	Bandwidth	$R_L = 50\ \Omega$ ,	Switch ON, see <a href="#">Figure 18</a>	25°C	1.8 V		300		MHz
$O_{ISO}$	OFF isolation	$R_L = 50\ \Omega$ , $f = 10\text{ MHz}$ ,	Switch OFF, see <a href="#">Figure 19</a>	25°C	1.8 V		–65		dB
$X_{TALK}$	Crosstalk	$R_L = 50\ \Omega$ , $f = 10\text{ MHz}$ ,	Switch ON, see <a href="#">Figure 20</a>	25°C	1.8 V		–66		dB
THD	Total harmonic distortion	$R_L = 10\text{ k}\Omega$ , $C_L = 50\text{ pF}$ ,	$f = 20\text{ Hz to }20\text{ kHz}$ , see <a href="#">Figure 22</a>	25°C	1.8 V		0.015 %		
<b>Supply</b>									
$I_+$	Positive supply current	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	1.95 V		2.5	5	$\mu\text{A}$
				Full			10		

## 6.9 Typical Characteristics

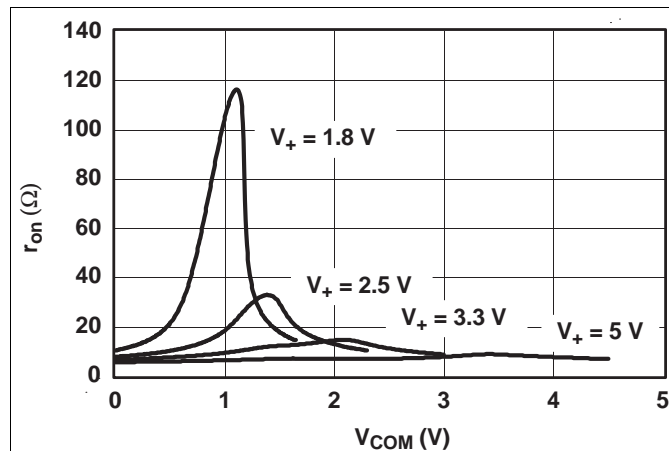


Figure 1.  $r_{on}$  vs  $V_{COM}$

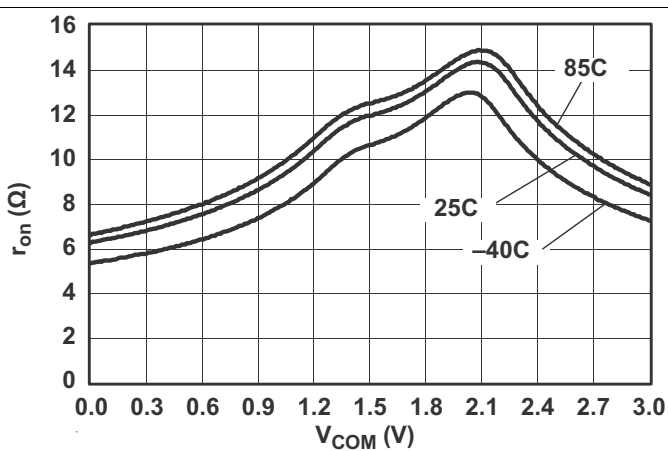


Figure 2.  $r_{on}$  vs  $V_{COM}$  ( $V_+ = 3$  V)

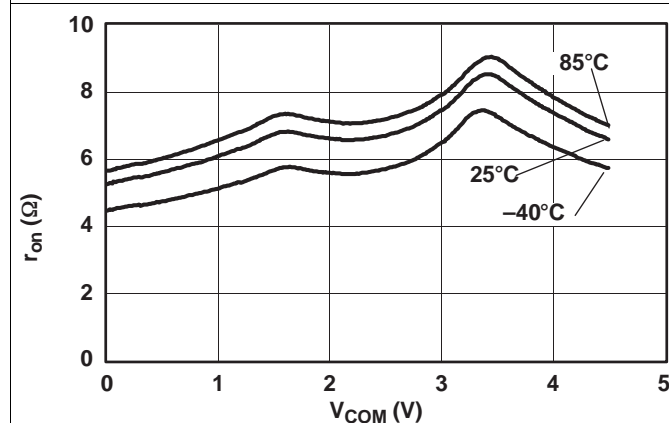


Figure 3.  $r_{on}$  vs  $V_{COM}$  ( $V_+ = 4.5$  V)

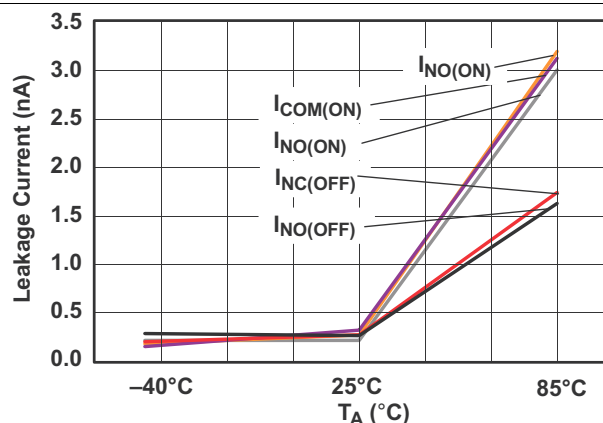


Figure 4. Leakage Current vs Temperature ( $V_+ = 5.5$  V)

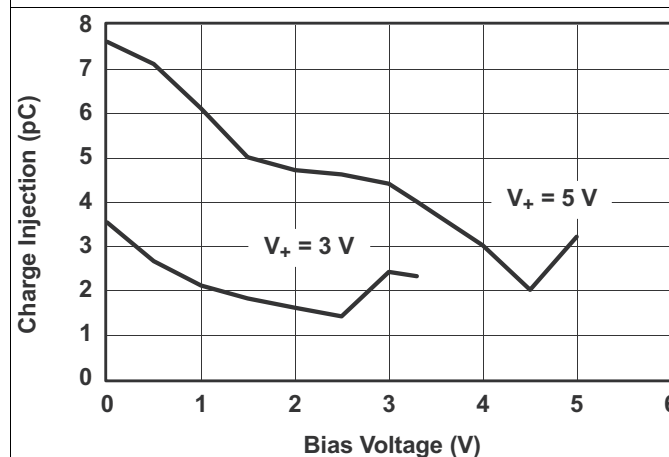


Figure 5. Charge Injection ( $Q_C$ ) vs  $V_{COM}$

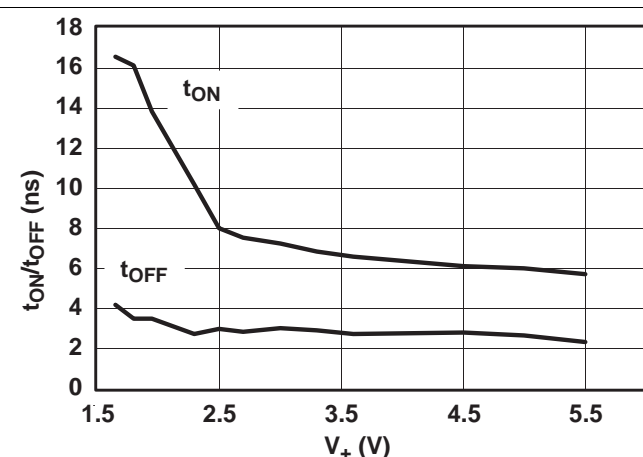


Figure 6.  $t_{ON}$  and  $t_{OFF}$  vs Supply Voltage

## Typical Characteristics (continued)

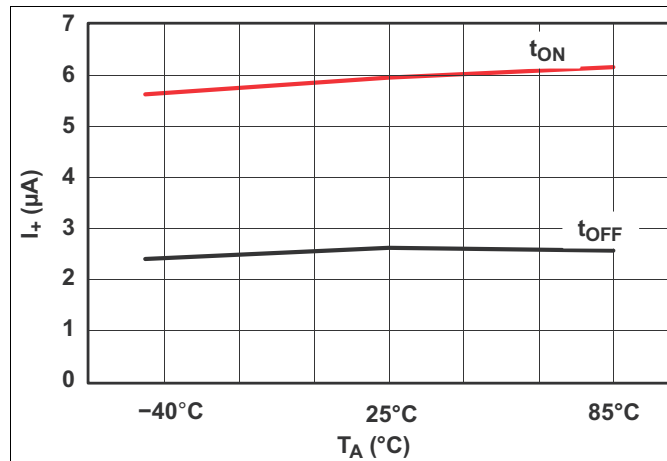


Figure 7.  $t_{ON}$  and  $t_{OFF}$  vs Temperature ( $V_+ = 5$  V)

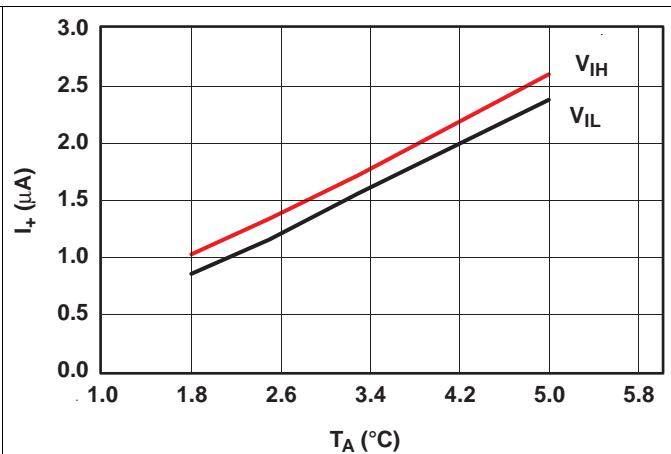


Figure 8. Logic-Level Threshold vs  $V_+$

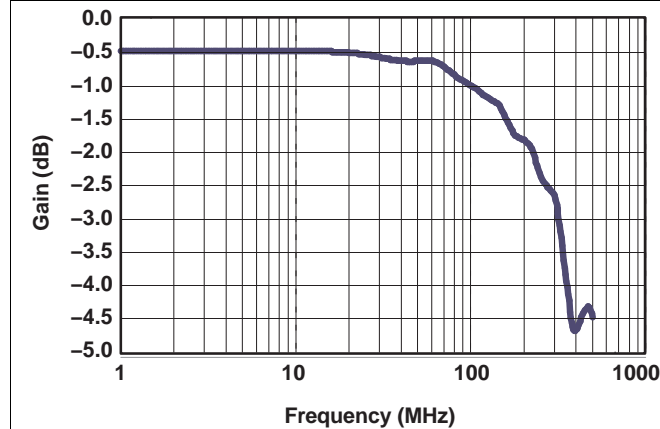


Figure 9. Bandwidth (Gain vs Frequency) ( $V_+ = 5$  V)

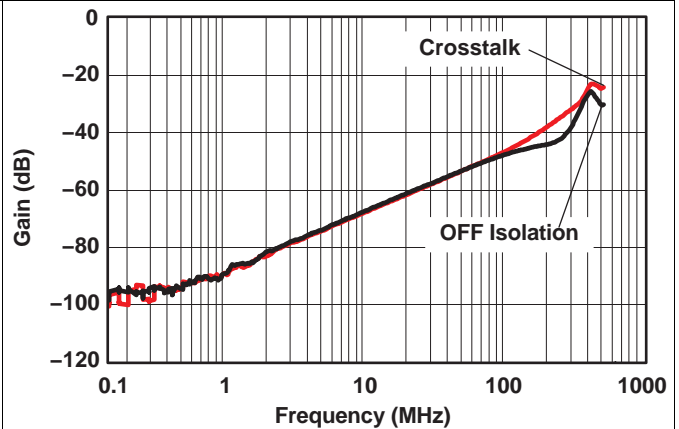


Figure 10. OFF Isolation ( $V_+ = 5$  V)

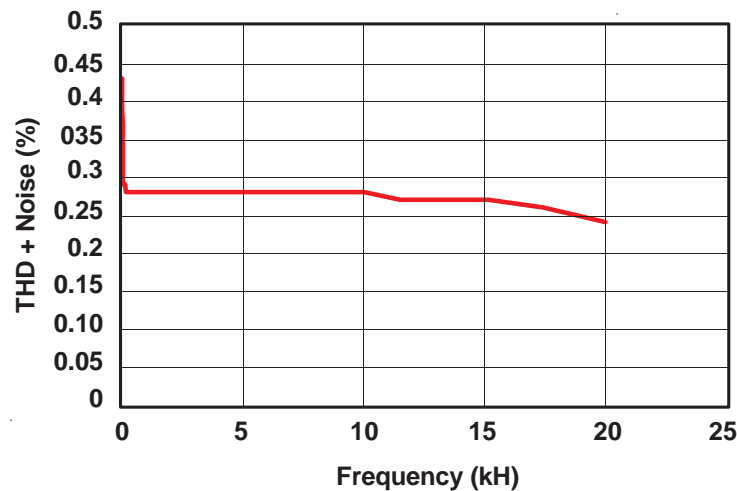


Figure 11. Total Harmonic Distortion vs Frequency

## 7 Parameter Measurement Information

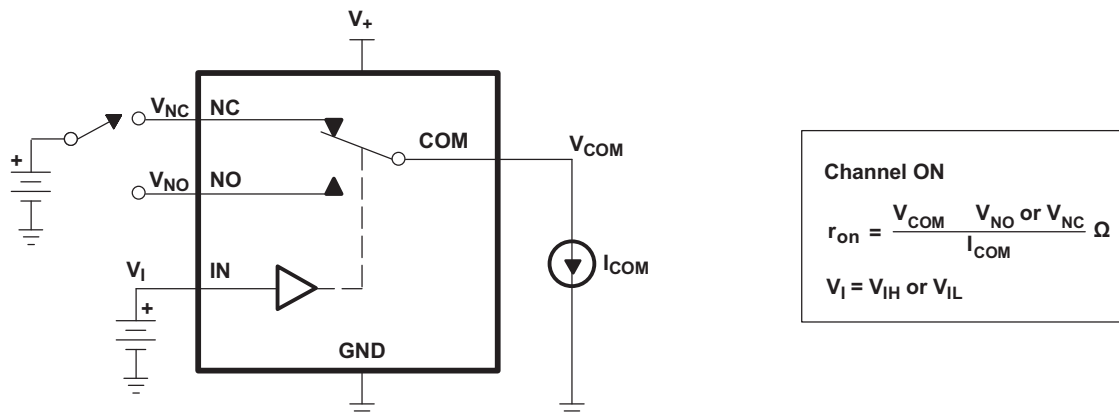


Figure 12. ON-State Resistance ( $r_{on}$ )

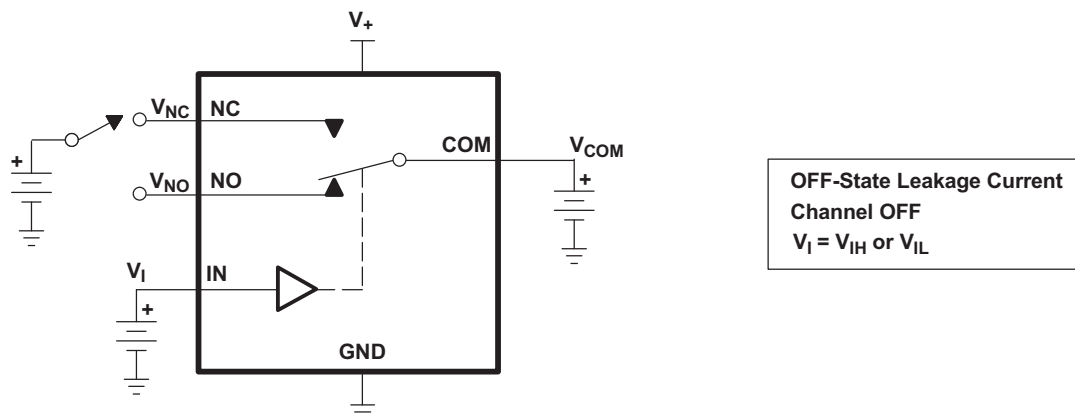


Figure 13. OFF-State Leakage Current ( $I_{NC(OFF)}$ ,  $I_{NO(OFF)}$ )

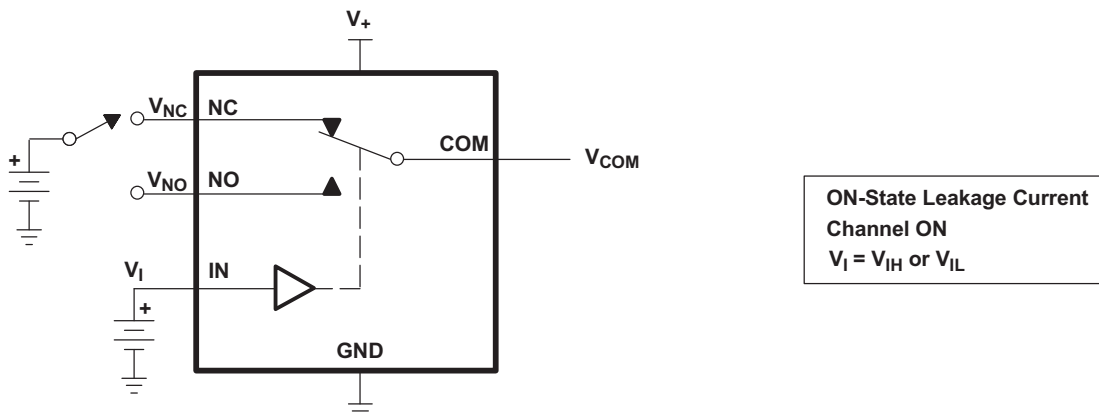


Figure 14. ON-State Leakage Current ( $I_{COM(ON)}$ ,  $I_{NC(ON)}$ ,  $I_{NO(ON)}$ )

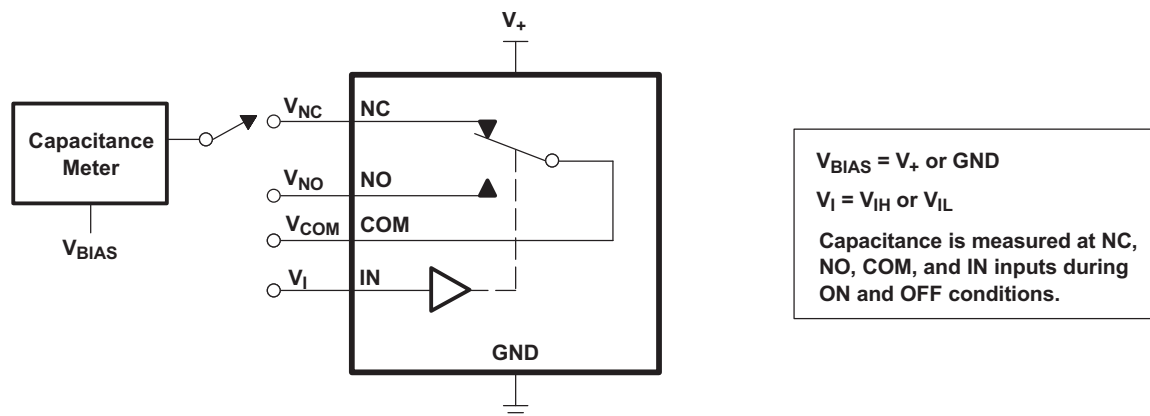
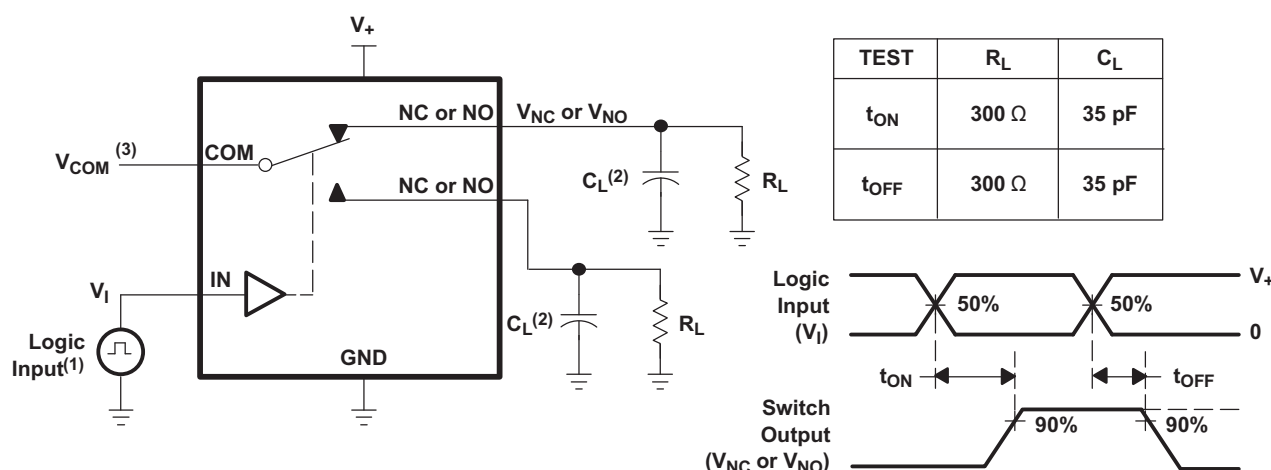
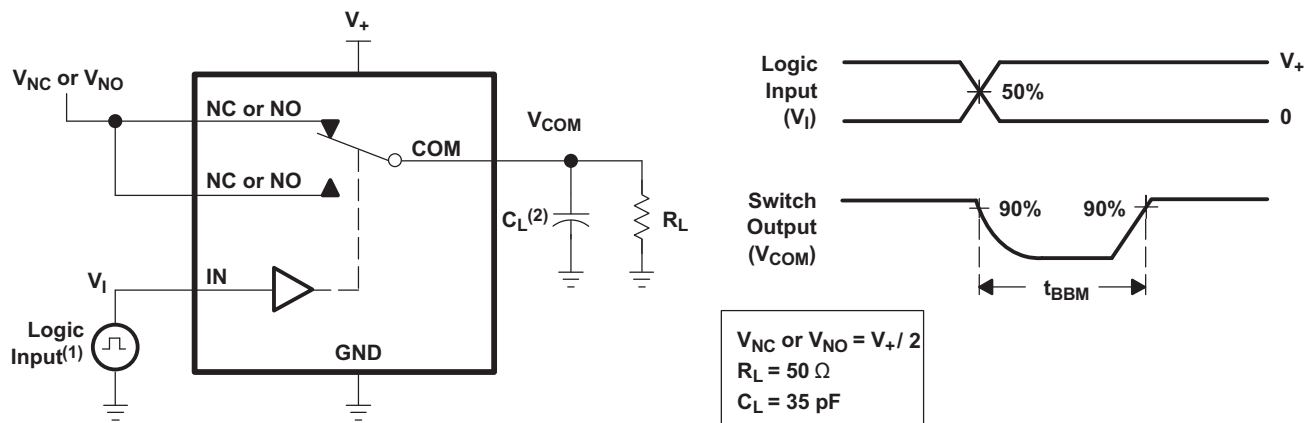


Figure 15. Capacitance ( $C_I$ ,  $C_{COM(ON)}$ ,  $C_{NC(OFF)}$ ,  $C_{NO(OFF)}$ ,  $C_{NC(ON)}$ ,  $C_{NO(ON)}$ )



- (1) All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r < 5$  ns.
- (2)  $C_L$  includes probe and jig capacitance.
- (3) See Electrical Characteristics for  $V_{COM}$ .

Figure 16. Turnon ( $t_{ON}$ ) and Turnoff Time ( $t_{OFF}$ )



- (1) All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\ \text{MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r < 5\ \text{ns}$ ,  $t_f < 5\ \text{ns}$ .
- (2)  $C_L$  includes probe and jig capacitance.

Figure 17. Break-Before-Make Time ( $t_{BBM}$ )

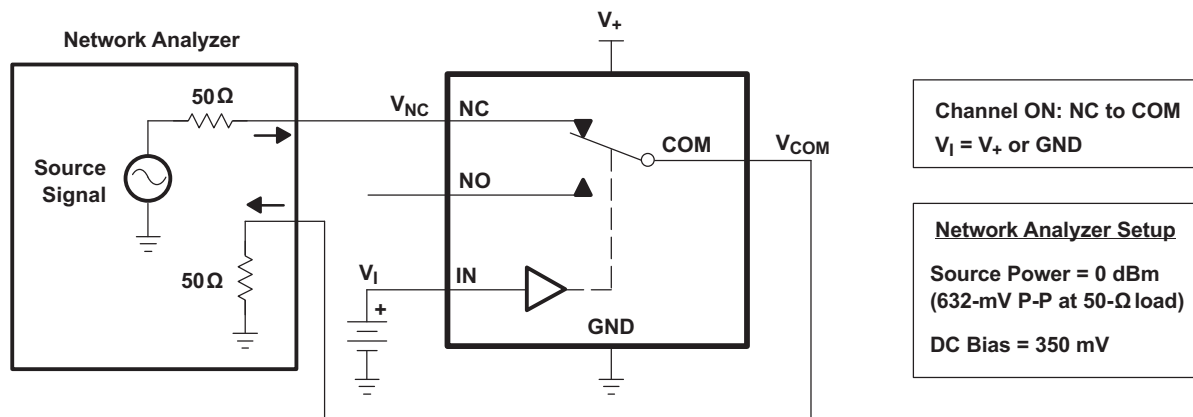


Figure 18. Bandwidth (BW)

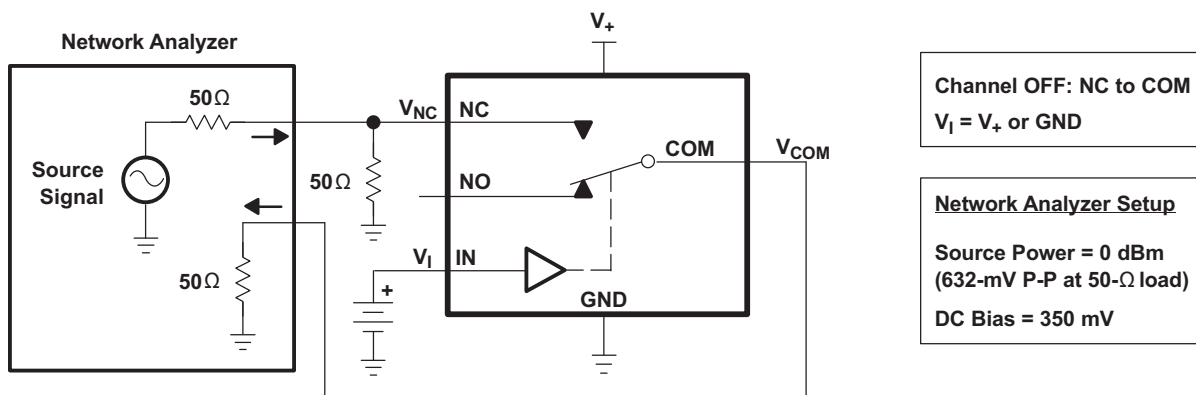
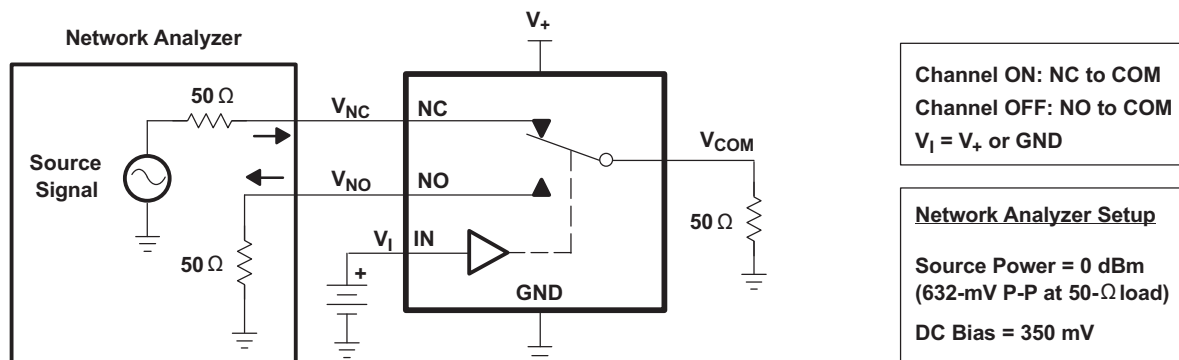
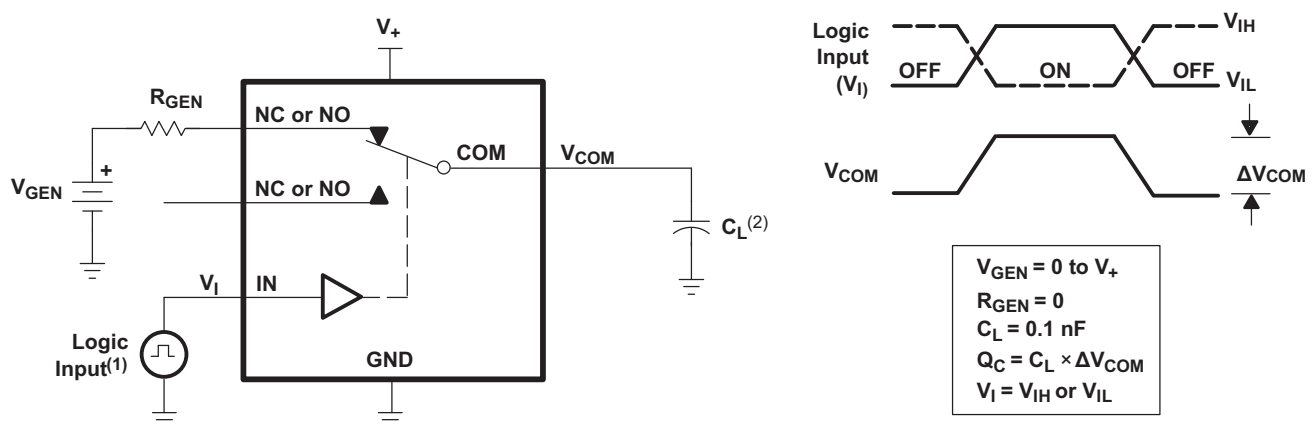


Figure 19. OFF Isolation ( $O_{Iso}$ )

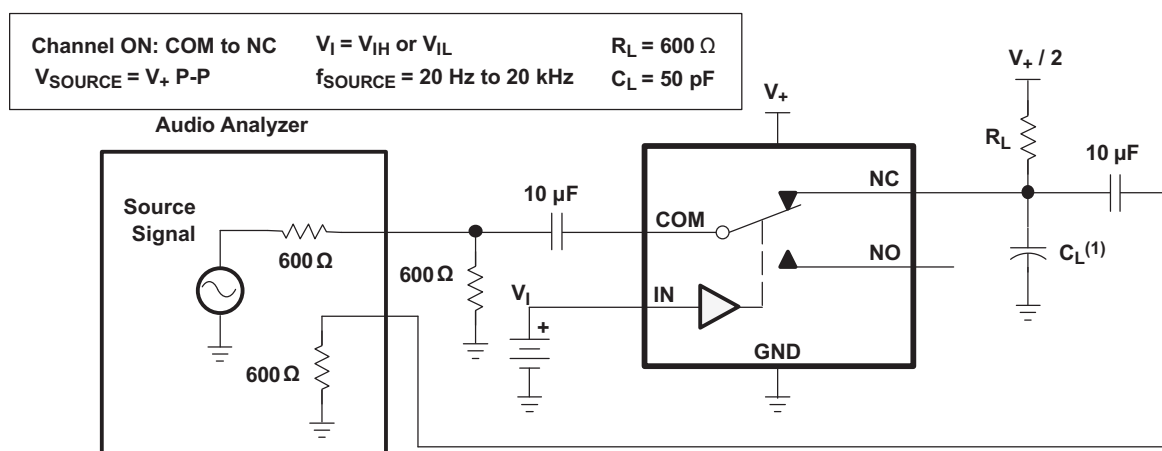


**Figure 20. Crosstalk ( $X_{TALK}$ )**



- (1) All input pulses are supplied by generators having the following characteristics:  $\text{PRR} \leq 10 \text{ MHz}$ ,  $Z_0 = 50 \Omega$ ,  $t_r < 5 \text{ ns}$ ,  $t_f < 5 \text{ ns}$ .
- (2)  $C_L$  includes probe and jig capacitance.

**Figure 21. Charge Injection ( $Q_c$ )**



- (1)  $C_L$  includes probe and jig capacitance.

**Figure 22. Total Harmonic Distortion (THD)**



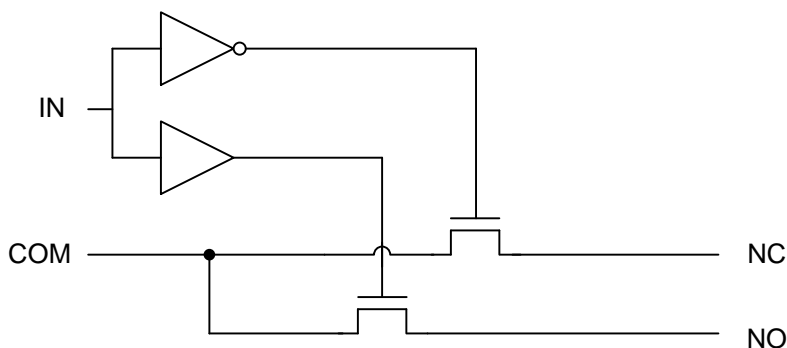
## 8 Detailed Description

### 8.1 Overview

The TS5A3157 is a single-pole-double-throw (SPDT) solid-state analog switch. The TS5A3157, like all analog switches, is bidirectional. When powered on, each COM pin is connected to the NC pin. For this device, NC stands for *normally closed* and NO stands for *normally open*. If IN is low, COM is connected to NC. If IN is high, COM is connected to NO.

The TS5A3157 is a break-before-make switch. This means that during switching, a connection is broken before a new connection is established. The NC and NO pins are never connected to each other.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

The low ON-state resistance, ON-state resistance matching, and charge injection in the TS5A3157 make this switch an excellent choice for analog signals that require minimal distortion. In addition, the low THD allows audio signals to be preserved more clearly as they pass through the device.

The 1.65-V to 5.5-V operation allows compatibility with more logic levels, and the bidirectional I/Os can pass analog signals from 0 V to  $V_+$  with low distortion. The control inputs are 5-V tolerant, allowing control signals to be present without  $V_{CC}$ .

### 8.4 Device Functional Modes

**Table 1. Function Table**

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

## 9 Application and Implementation

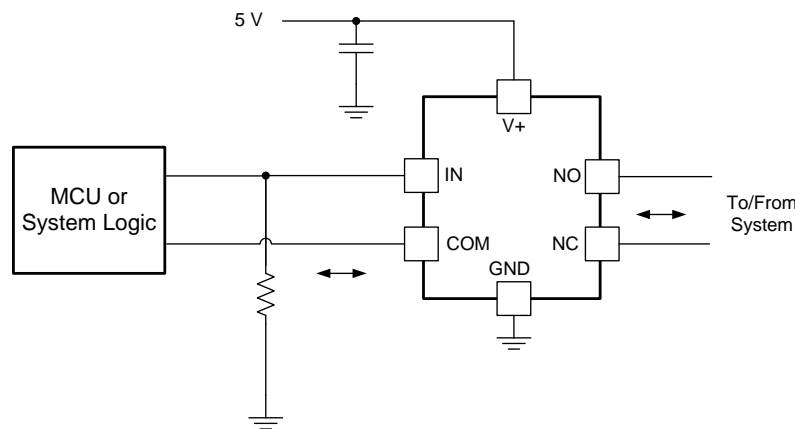
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The TS5A3157 can be used in a variety of customer systems. The TS5A3157 can be used anywhere multiple analog or digital signals must be selected to pass across a single line.

### 9.2 Typical Application



**Figure 23. System Schematic for TS5A3157**

#### 9.2.1 Design Requirements

In this particular application,  $V_+$  was 1.8 V, although  $V_+$  is allowed to be any voltage specified in [Recommended Operating Conditions](#). A decoupling capacitor is recommended on the  $V_+$  pin. See [Power Supply Recommendations](#) for more details.

#### 9.2.2 Detailed Design Procedure

In this application, IN is, by default, pulled low to GND. Choose the resistor size based on the current driving strength of the GPIO, the desired power consumption, and the switching frequency (if applicable). If the GPIO is open-drain, use pullup resistors instead.

## Typical Application (continued)

### 9.2.3 Application Curve

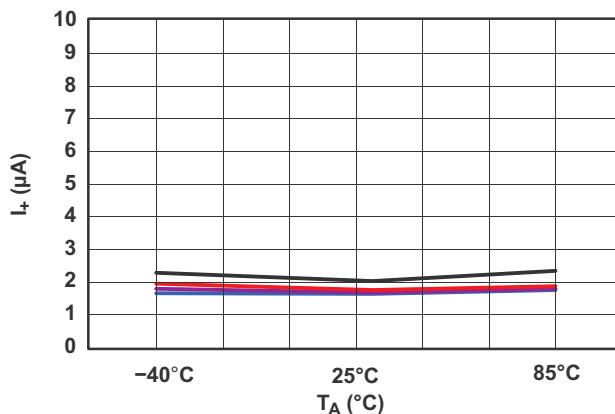


Figure 24. Power-Supply Current vs Temperature  
( $V_+ = 5\text{ V}$ )

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#).

Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-μF bypass capacitor is recommended. If there are multiple pins labeled  $V_{CC}$ , then a 0.01-μF or 0.022-μF capacitor is recommended for each  $V_{CC}$  because the VCC pins will be tied together internally. For devices with dual supply pins operating at different voltages, for example  $V_{CC}$  and  $V_{DD}$ , a 0.1-μF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

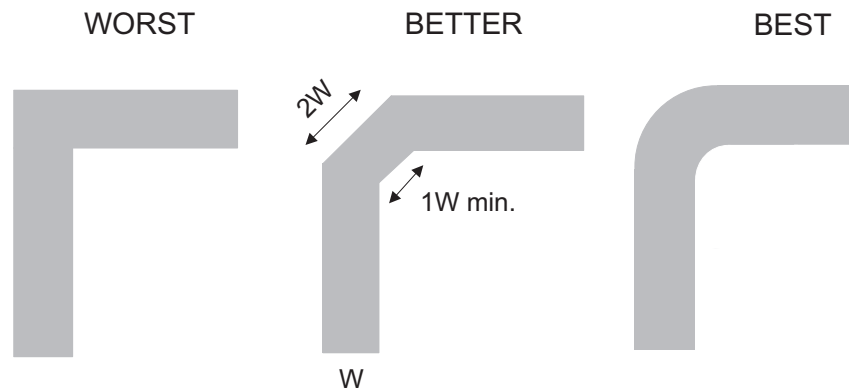
## 11 Layout

### 11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. Below figure shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

Unused switch I/Os, such as NO, NC, and COM, can be left floating or tied to GND. However, the IN pin must be driven high or low. Due to partial transistor turnon when control inputs are at threshold levels, floating control inputs can cause increased  $I_{CC}$  or unknown switch selection states.

## 11.2 Layout Example



**Figure 25. Trace Example**

## 12 Device and Documentation Support

### 12.1 Device Support

#### 12.1.1 Device Nomenclature

**Table 2. Parameter Description**

SYMBOL	DESCRIPTION
$V_{COM}$	Voltage at COM
$V_{NC}$	Voltage at NC
$V_{NO}$	Voltage at NO
$r_{on}$	Resistance between COM and NC or COM and NO ports when the channel is ON
$\Delta r_{on}$	Difference of $r_{on}$ between channels in a specific device
$r_{on(Flat)}$	Difference between the maximum and minimum value of $r_{on}$ in a channel over the specified range of conditions
$I_{NC(OFF)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state
$I_{NC(ON)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) open
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the ON state and the output (NC or NO) open
$V_{IH}$	Minimum input voltage for logic high for the control input (IN)
$V_{IL}$	Maximum input voltage for logic low for the control input (IN)
$V_I$	Voltage at the control input (IN)
$I_{IH}, I_{IL}$	Leakage current measured at the control input (IN)
$t_{ON}$	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM, NC, or NO) signal when the switch is turning ON.
$t_{OFF}$	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM, NC, or NO) signal when the switch is turning OFF.
$t_{BBM}$	Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO) when the control signal changes state.
$Q_C$	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC, NO, or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$ , $C_L$ is the load capacitance and $\Delta V_{COM}$ is the change in analog output voltage.
$C_{NC(OFF)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
$C_{NO(OFF)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
$C_{NC(ON)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
$C_{NO(ON)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is ON
$C_I$	Capacitance of control input (IN)
$O_{ISO}$	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state.
$X_{TALK}$	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency where the gain of an ON channel is –3 dB below the DC gain.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of fundamental harmonic.
$I_+$	Static power-supply current with the control (IN) pin at $V_+$ or GND

## 12.2 Documentation Support

### 12.2.1 Related Documentation

For related documentation, see the following:

- *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#)

## 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 12.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

## 12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TS5A3157DBVR</a>	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	NIPDAU   NIPDAU	Level-1-260C-UNLIM	-40 to 85	JC5R
<a href="#">TS5A3157DCKR</a>	Active	Production	SC70 (DCK)   6	3000   LARGE T&R	Yes	NIPDAU   SN   NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JC5, JCF, JCJ, JC R)
<a href="#">TS5A3157YZPR</a>	Active	Production	DSBGA (YZP)   6	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	JCN

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A3157DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TS5A3157DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TS5A3157YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1



## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A3157DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TS5A3157DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
TS5A3157YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0



## SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

# EXAMPLE BOARD LAYOUT

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



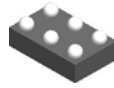
SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

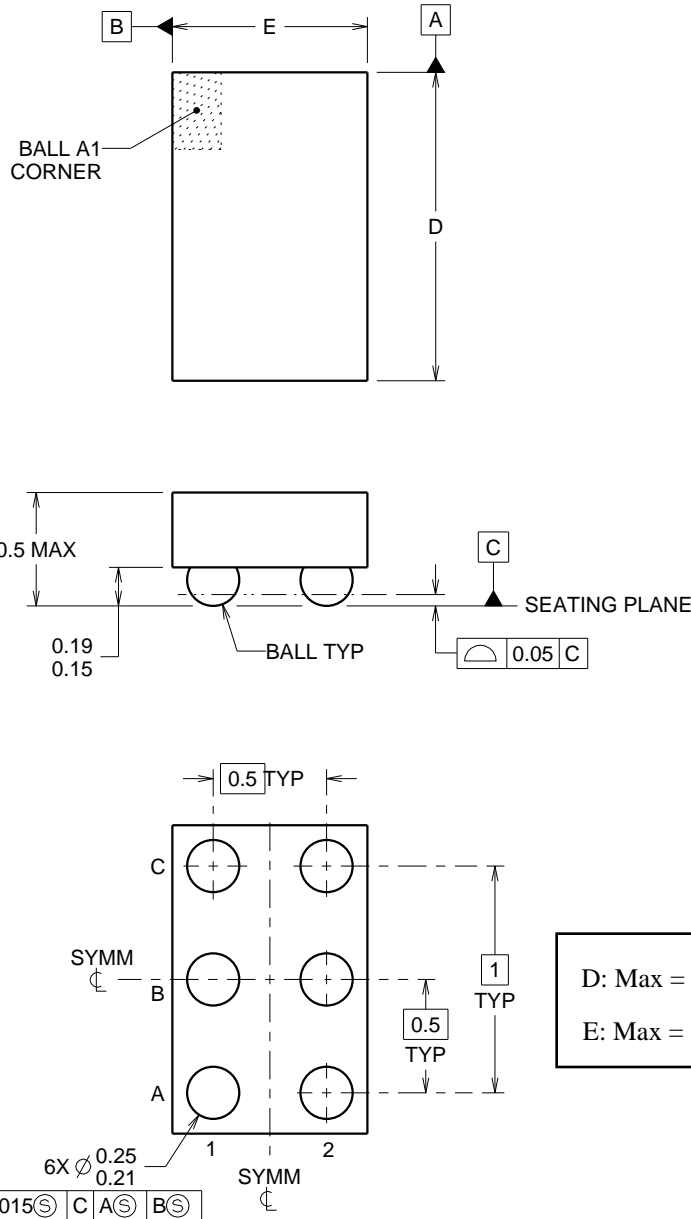
YZP0006



# PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.418 mm, Min = 1.358 mm

E: Max = 0.918 mm, Min = 0.858 mm

4219524/A 06/2014

## NOTES:

NanoFree Is a trademark of Texas Instruments.

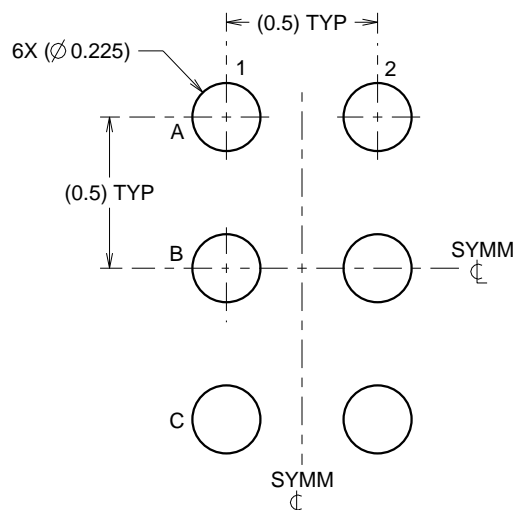
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.

# EXAMPLE BOARD LAYOUT

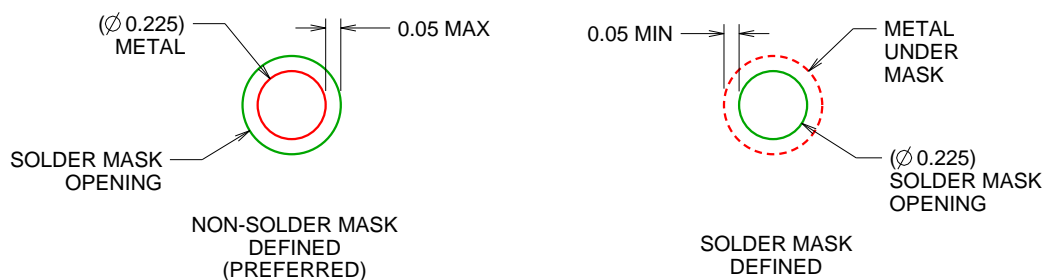
YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:40X



SOLDER MASK DETAILS  
NOT TO SCALE

4219524/A 06/2014

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 ([www.ti.com/lit/sbva017](http://www.ti.com/lit/sbva017)).

## EXAMPLE STENCIL DESIGN

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:40X

4219524/A 06/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

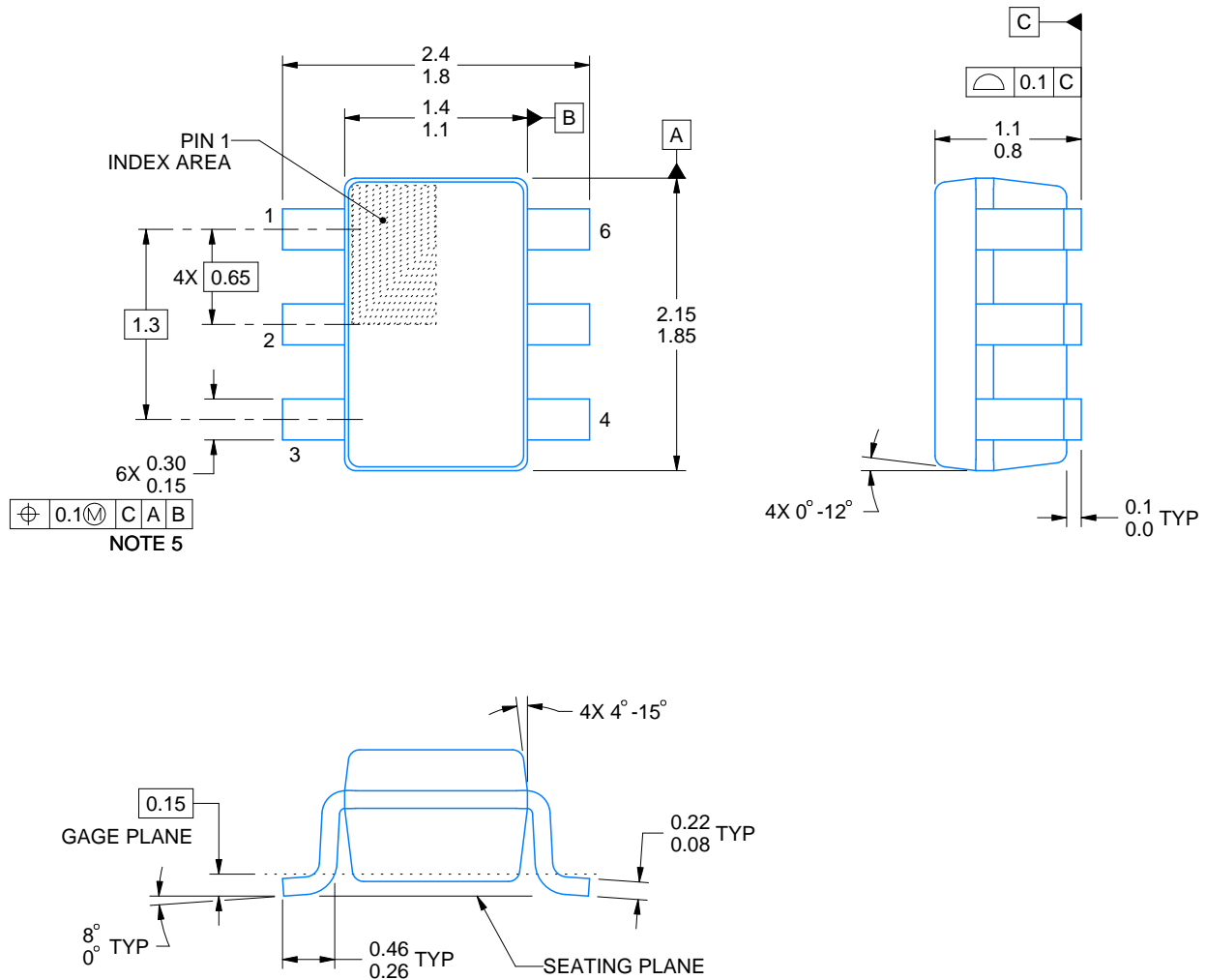
DCK0006A



## PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214835/D 11/2024

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



# EXAMPLE BOARD LAYOUT

DCK0006A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



SOLDER MASK DETAILS

4214835/D 11/2024

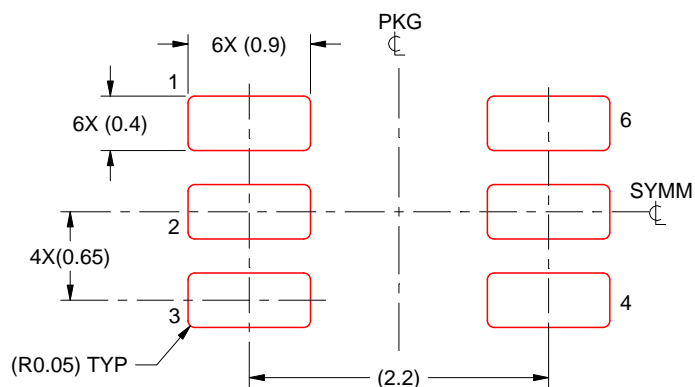
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

**DCK0006A**

### SOT - 1.1 max height

## SMALL OUTLINE TRANSISTOR



**SOLDER PASTE EXAMPLE**  
**BASED ON 0.125 THICK STENCIL**  
**SCALE:18X**

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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