

TPS3435-Q1 Automotive Nano IQ Precision Timeout Watchdog Timer

1 Features

- AEC-Q100 qualified with the following results:
 - Device temperature grade 1: –40°C to 125°C ambient operating temperature range
- Factory programmed or user-programmable watchdog timeout
 - ±10% Accurate timer (maximum)
 - Factory programmed: 1ms to 100s
- Factory programmed or user-programmable reset delay
 - ±10% Accurate timer (maximum)
 - Factory programmed option: 2ms to 10s
- Input voltage range: $V_{DD} = 1.04V$ to 6.0V
- Ultra low supply current: $I_{DD} = 250nA$ (typical)
- Open-drain, push-pull; active-low outputs
- Various programmability options:
 - Watchdog enable-disable
 - Watchdog startup delay: no delay to 10s
 - On the fly timer extension: 1X to 256X
 - Latched output option
- $\overline{MR}$ functionality support

2 Applications

- On-board (OBC) and wireless charger
- Driver monitoring
- Battery Management System (BMS)
- Front camera
- Surround view system ECU

3 Description

The TPS3435-Q1 is an ultra-low power consumption (250nA typical) device offering a programmable timeout watchdog timer.

The TPS3435-Q1 offers a high accuracy timeout watchdog timer with a host of features for a wide variety of applications. The timeout watchdog timer can be factory programmed or user programmed using an external capacitor. The timer value can be changed on-the-fly using a combination of logic pins. The watchdog also offers unique features such as enable-disable, start-up delay.

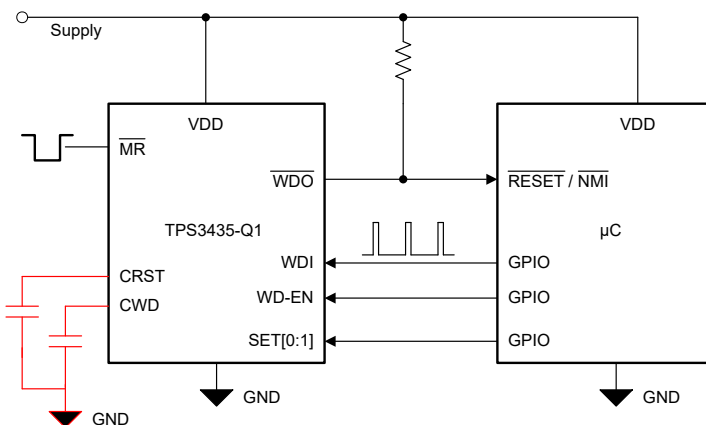
The $\overline{WDO}$ delay can be set by factory-programmed default delay settings or programmed by an external capacitor. The device also offers a latched output operation where the output is latched until the watchdog fault is cleared.

The TPS3435-Q1 provides a performance upgrade alternative to [TPS3431-Q1](#) device family. The TPS3435-Q1 is available in a small 8-pin SOT-23 package.

Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM) (2)
TPS3435-Q1	DDF (8)	2.90mm × 1.60mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.



TPS3435-Q1 offers various pinout options to support different features.
Choose the suitable pinout based on application needs.

Typical Application Circuit

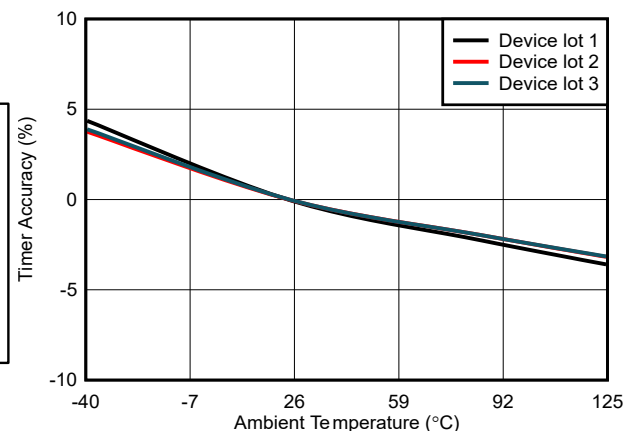


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4 Device Comparison

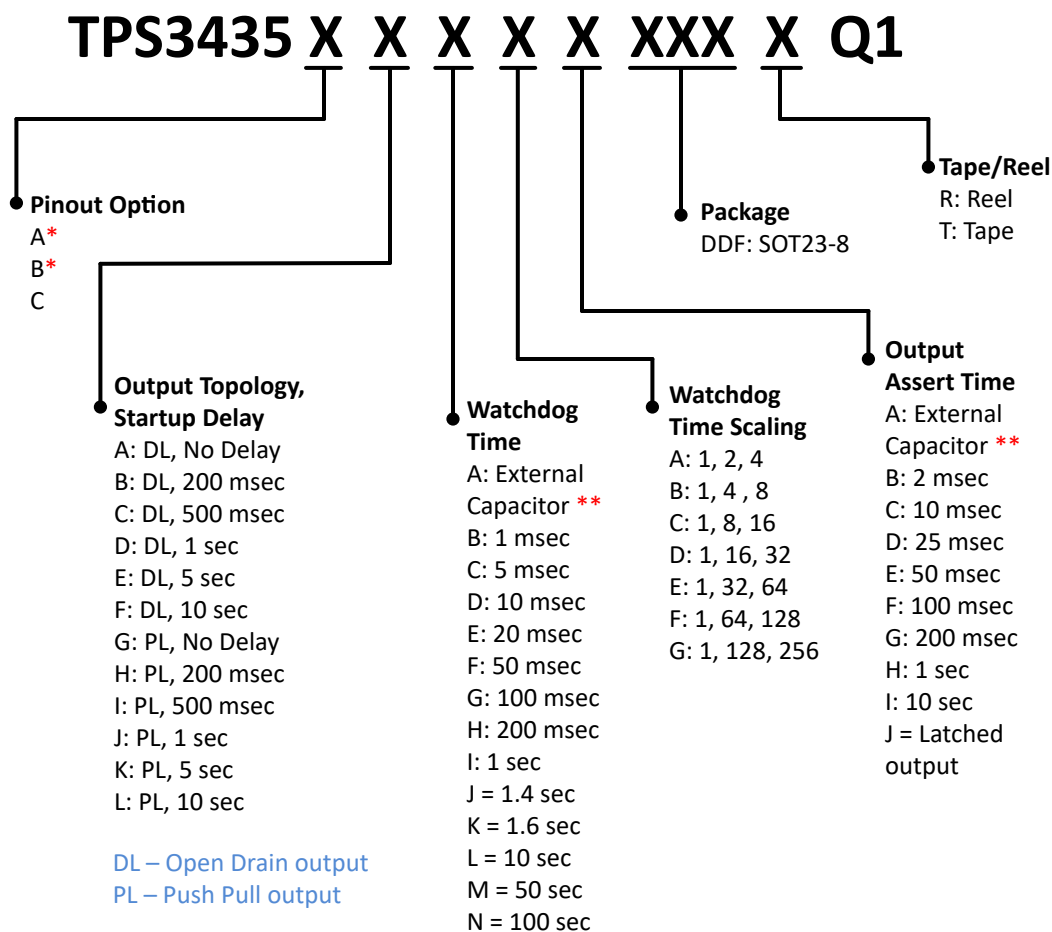
Figure 4-1 shows the device naming nomenclature of the TPS3435-Q1. For all possible output types, watchdog time options and output assert delay options, see Section 7 or Table 4-1 for more details. Contact TI sales representatives or on TI's [E2E forum](#) for detail and availability of other options.

Table 4-1. Available devices

Device	Function ⁽¹⁾	Pinout ⁽²⁾	WD Timeout	Startup-Delay	Time Scaling	Output Pulse	Output Topology	Vit-
TPS3435CAEBJDDFR	WD	C	20ms	0	1, 4, 8	Latched	open-drain	N/A
TPS3435CAGBJDDFRQ1	WD	C	100ms	0	1, 4, 8	Latched	open-drain	N/A
TPS3435CBHAJDDFR	WD	C	200ms	200ms	1, 2, 4	Latched	open-drain	N/A
TPS3435CCGAJDDFR	WD	C	100ms	500ms	1, 2, 4	Latched	open-drain	N/A
TPS3435CECAJDDFRQ1	WD	C	5ms	5s	1, 2, 4	Latched	open-drain	N/A
TPS3435CGLEFDDFR	WD	C	10s	0	1, 32, 64	100ms	push-pull	N/A
TPS3435CAKAGDDFR	WD	C	1.6s	0	1, 2, 4	200ms	open-drain	N/A
TPS3435AFACADDFRQ1	WD	A	Adjustable	10s	1, 8	Adjustable	open-drain	N/A
TPS3435CAKAGDDFRQ1	WD	C	1.6s	0	1, 2, 4	200ms	open-drain	N/A
TPS3435CAIEGDDFR	WD	C	1s	0	1, 32, 64	200ms	open-drain	N/A
TPS3435JAJAJDSER	WD	J	1.4s	0	1, 2	Latched	open-drain	N/A
TPS3435JFMAFDSER	WD	J	50s	10s	1, 2	100ms	open-drain	N/A
TPS35CA38GACDDFRQ1	WD + SVS	C	100ms	0	1, 2, 4	10ms	open-drain	2.9V
TPS35DA40GCJDDFR	WD + SVS	D	100ms	0	1, 8, 16	Latched	open-drain	3V
TPS35DA69GADDDFRQ1	WD + SVS	D	100ms	0	1, 2, 4	25ms	open-drain	4.45V
TPS35JE42IADDSER	WD + SVS	J	1s	20ms	1, 2	25ms	open-drain	3.1V
TPS35AA17AGADDFR	WD + SVS	A	Adjustable	0	1, 128	Adjustable	open-drain	1.85V
TPS35JE35JADDSER	WD + SVS	J	1.4s	5s	1, 2	25ms	open-drain	2.75V
TPS35AA38AGADDFRQ1	WD + SVS	A	Adjustable	0	1, 128	Adjustable	open-drain	2.9V
TPS35CA43DACDDFRQ1	WD + SVS	C	10ms	0	1, 2, 4	10ms	open-drain	3.15V
TPS35CA38IAGDDFRQ1	WD + SVS	C	1s	0	1, 2, 4	200ms	open-drain	2.9V

(1) WD = Watchdog , SVS = Voltage Supervisor

(2) Please refer to Section 5 for pinout information



* Pinout option supports Start up Delay settings of “No Delay” and “10 sec” only.

** Capacitor programmable time feature available with pinout options A & B. For fixed time and latched output features use pinout option C.

Refer ‘Mechanical, Packaging and Orderable Information’ section for list of released orderable. For any other orderable, contact local TI support.

Figure 4-1. Device Naming Nomenclature

TPS3435-Q1 belongs to family of pin compatible devices offering different feature sets as highlighted in [Table 4-2](#).

Table 4-2. Pin Compatible Device Families

DEVICE	VOLTAGE SUPERVISOR	TYPE OF WATCHDOG
TPS35-Q1	Yes	Timeout
TPS36-Q1	Yes	Window
TPS3435-Q1	No	Timeout
TPS3436-Q1	No	Window

5 Pin Configuration and Functions

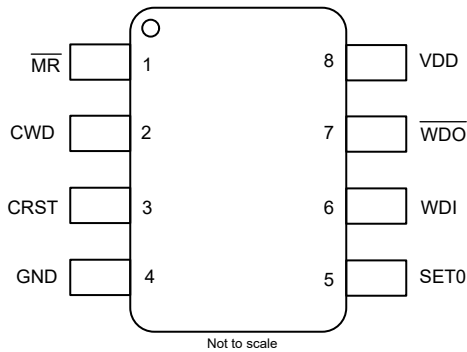


Figure 5-1. Pin Configuration Option A
DDF Package, 8-Pin SOT-23,
TPS3435-Q1 Top View

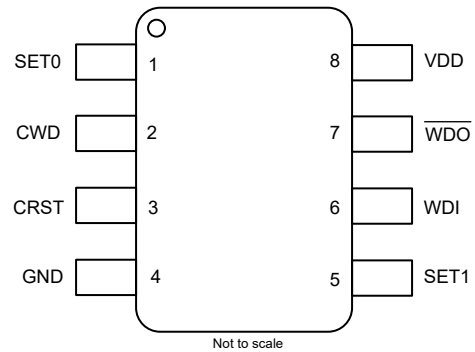


Figure 5-2. Pin Configuration Option B
DDF Package, 8-Pin SOT-23,
TPS3435-Q1 Top View

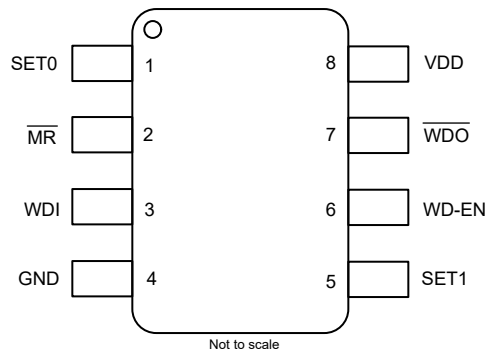


Figure 5-3. Pin Configuration Option C
DDF Package, 8-Pin SOT-23,
TPS3435-Q1 Top View

Table 5-1. Pin Functions

PIN NAME	PIN NUMBER			I/O	DESCRIPTION
	PINOUT A	PINOUT B	PINOUT C		
CRST	3	3	—	I	Programmable WDO assert time pin. Connect a capacitor between this pin and GND to program the WDO assert time period. See Section 7.3.3 for more details.
CWD	2	2	—	I	Programmable watchdog timeout input. Watchdog timeout is set by connecting a capacitor between this pin and ground. See Section 7.3.1.1 for more details.
GND	4	4	4	—	Ground pin
MR	1	—	2	I	Manual reset pin. A logic low on this pin asserts the $\overline{\text{WDO}}$ output. See Section 7.3.2 for more details.
$\overline{\text{WDO}}$	7	7	7	O	Watchdog output. Connect $\overline{\text{WDO}}$ to VDD using pull up resistance when using open drain output. $\overline{\text{WDO}}$ is asserted when a watchdog error occurs or MR pin is driven LOW. See Section 7.3.3 for more details.
SET0	5	1	1	I	Logic input. SET0, SET1, and WD-EN pins select the watchdog timer scaling and enable-disable the watchdog; see Section 7.3.1.4 for more details.
SET1	—	5	5	I	Logic input. SET0, SET1, and WD-EN pins select the watchdog timer scaling and enable-disable the watchdog; see Section 7.3.1.4 for more details.
VDD	8	8	8	I	Supply voltage pin. For noisy systems, connecting a 0.1 μF bypass capacitor is recommended.
WD-EN	—	—	6	I	Logic input. Logic high input enables the watchdog monitoring feature. See Section 7.3.1.2 for more details.
WDI	6	6	3	I	Watchdog input. A falling transition (edge) must occur at this pin before the timeout expires in order for $\overline{\text{WDO}}$ to not assert. See Section 7.3.1 for more details.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted⁽¹⁾

		MIN	MAX	UNIT
Voltage	VDD	−0.3	6.5	V
Voltage	C _{WD} , C _{RST} , WD–EN, SETx, WDI, $\overline{\text{MR}}$ ⁽²⁾ , $\overline{\text{WDO}}$ (Push Pull)	−0.3	V _{DD} +0.3 ⁽³⁾	V
	$\overline{\text{WDO}}$ (Open Drain)	−0.3	6.5	
Current	$\overline{\text{WDO}}$ pin	−20	20	mA
Temperature ⁽⁴⁾	Operating ambient temperature, T _A	−40	125	°C
Temperature	Storage, T _{stg}	−65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) If the logic signal driving $\overline{\text{MR}}$ is less than V_{DD}, then additional current flows into V_{DD} and out of $\overline{\text{MR}}$.
- (3) The absolute maximum rating is (V_{DD} + 0.3)V or 6.5V, whichever is smaller
- (4) As a result of the low dissipated power in this device, it is assumed that T_J = T_A.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000	V
		Charged device model (CDM), per AEC Q100-011	±750	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Voltage	VDD (Active Low output)	0.9		6	V
	C _{WD} , C _{RST} , WD–EN, SETx, WDI, $\overline{\text{MR}}$ ⁽¹⁾	0		VDD	
	$\overline{\text{WDO}}$ (Open Drain)	0		6	
	$\overline{\text{WDO}}$ (Push Pull)	0		VDD	
Current	$\overline{\text{WDO}}$ pin current	−5		5	mA
C _{RST}	C _{RST} pin capacitor range	1.5		1800	nF
C _{WD}	C _{WD} pin capacitor range	1.5		1000	nF
T _A	Operating ambient temperature	−40		125	°C

- (1) If the logic signal driving $\overline{\text{MR}}$ is less than V_{DD}, then additional current flows into V_{DD} and out of $\overline{\text{MR}}$. V_{MR} should not be higher than V_{DD}.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS3435-Q1	UNIT
		DDF (SOT23-8)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	175.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	94.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	92.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	8.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	91.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

At $1.04\text{V} \leq V_{DD} \leq 6\text{V}$, $\overline{\text{MR}} = \text{Open}$, $\overline{\text{WDO}}$ pull-up resistor ($R_{\text{pull-up}}$) = $100\text{k}\Omega$ to V_{DD} , output load (C_{LOAD}) = 10pF and over operating free-air temperature range -40°C to 125°C , unless otherwise noted. V_{DD} ramp rate $\leq 1\text{V}/\mu\text{s}$. Typical values are at $T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
COMMON PARAMETERS						
V _{DD}	Input supply voltage	Active LOW output	1.04		6	V
I _{DD}	Supply current into VDD pin ⁽¹⁾	T _A = −40°C to 85°C		0.25	0.8	μA
				0.25	3	
V _{IL}	Low level input voltage WD–EN, WDI, SETx, MR ⁽¹⁾				0.3V _{DD}	V
V _{IH}	High level input voltage WD–EN, WDI, SETx, MR ⁽¹⁾		0.7V _{DD}			V
R _{MR}	Manual reset internal pull-up resistance			100		kΩ
WDO (Open-drain active-low)						
V _{OL}	Low level output voltage	V _{DD} = 1.5V I _{OUT(Sink)} = 500μA			300	mV
		V _{DD} = 3.3V I _{OUT(Sink)} = 2mA			300	
I _{lkg(OD)}	Open-Drain output leakage current	V _{DD} = V _{PULLUP} = 6V T _A = −40°C to 85°C		10	30	nA
		V _{DD} = V _{PULLUP} = 6V		10	60	nA
WDO (Push-pull active-low)						
V _{POR}	Power on WDO voltage ⁽²⁾	V _{OH(min)} = 0.8 VDD I _{out (source)} = 15μA			900	mV
V _{OL}	Low level output voltage	V _{DD} = 1.5V I _{OUT(Sink)} = 500μA			300	mV
		V _{DD} = 3.3V I _{OUT(Sink)} = 2mA			300	
V _{OH}	High level output voltage	V _{DD} = 1.8V I _{OUT(Source)} = 500μA	0.8V _{DD}			V
		V _{DD} = 3.3V I _{OUT(Source)} = 500μA	0.8V _{DD}			
		V _{DD} = 6V I _{OUT(Source)} = 2mA	0.8V _{DD}			

(1) If the logic signal driving $\overline{\text{MR}}$ is less than V_{DD} , then additional current flows into V_{DD} and out of $\overline{\text{MR}}$.

(2) V_{POR} is the minimum V_{DD} voltage level for a controlled output state

6.6 Timing Requirements

At $1.04\text{V} \leq V_{DD} \leq 6\text{V}$, $\overline{\text{MR}}$ = Open, $\overline{\text{WDO}}$ pull-up resistor ($R_{\text{pull-up}}$) = 100k Ω to VDD, output RESET / WDO load (C_{LOAD}) = 10pF and over operating free-air temperature range -40°C to 125°C , unless otherwise noted. VDD ramp rate $\leq 1\text{V}/\mu\text{s}$. Typical values are at $T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{\overline{\text{MR_PW}}}$	$\overline{\text{MR}}$ pin pulse duration to assert output			100		ns
$t_{\text{P-WD}}$	WDI pulse duration to start next frame ⁽¹⁾		500			ns
$t_{\text{HD-WDEN}}$	WD-EN hold time to enable or disable WD operation ⁽¹⁾		200			μs
$t_{\text{HD-SETx}}$	SETx hold time to change WD timer setting ⁽¹⁾		150			μs
t_{WD}	Watchdog timeout period	Orderable Option TPS3435xxB	0.8	1	1.2	ms
		Orderable Option TPS3435xxC	4	5	6	
		Orderable Option TPS3435xxD	9	10	11	
		Orderable Option TPS3435xxE	18	20	22	
		Orderable Option TPS3435xxF	45	50	55	
		Orderable Option TPS3435xxG	90	100	110	
		Orderable Option TPS3435xxH	180	200	220	
		Orderable Option TPS3435xxI	0.9	1	1.1	s
		Orderable Option TPS3435xxJ	1.26	1.4	1.54	
		Orderable Option TPS3435xxK	1.44	1.6	1.76	
		Orderable Option TPS3435xxL	9	10	11	
		Orderable Option TPS3435xxM	45	50	55	
		Orderable Option TPS3435xxN	90	100	110	

(1) Not production tested

6.7 Switching Characteristics

At $1.04V \leq V_{DD} \leq 6V$, $\overline{MR}$ = Open, $\overline{WDO}$ pull-up resistor ($R_{pull-up}$) = 100k Ω to VDD, output RESET / WDO load (C_{LOAD}) = 10pF and over operating free-air temperature range $-40^{\circ}C$ to $125^{\circ}C$, unless otherwise noted. VDD ramp rate $\leq 1V/\mu s$. Typical values are at $T_A = 25^{\circ}C$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{STRT}	Startup delay ⁽¹⁾				500	μs
t_{SD}	Watchdog startup delay	Orderable part number TPS3435xA, TPS3435xG		0		ms
		Orderable part number TPS3435xB, TPS3435xH	180	200	220	
		Orderable part number TPS3435xC, TPS3435xI	450	500	550	
		Orderable part number TPS3435xD, TPS3435xJ	0.9	1	1.1	s
		Orderable part number TPS3435xE, TPS3435xK	4.5	5	5.5	
		Orderable part number TPS3435xF, TPS3435xL	9	10	11	
t_{WDO}	Watchdog assert time delay	Orderable part number TPS3435xxxxB	1.6	2	2.4	ms
		Orderable part number TPS3435xxxxC	9	10	11	ms
		Orderable part number TPS3435xxxxD	22.5	25	27.5	ms
		Orderable part number TPS3435xxxxE	45	50	55	ms
		Orderable part number TPS3435xxxxF	90	100	110	ms
		Orderable part number TPS3435xxxxG	180	200	220	ms
		Orderable part number TPS3435xxxxH	0.9	1	1.1	s
		Orderable part number TPS3435xxxxI	9	10	11	s
t_{MR_WDO}	Propagation delay from $\overline{MR}$ low to WDO assertion	$V_{DD} \geq 1.25V$, $\overline{MR} = V_{\overline{MR_H}}$ to $V_{\overline{MR_L}}$		100		ns

(1) Specified by design parameter.

6.8 Timing Diagrams

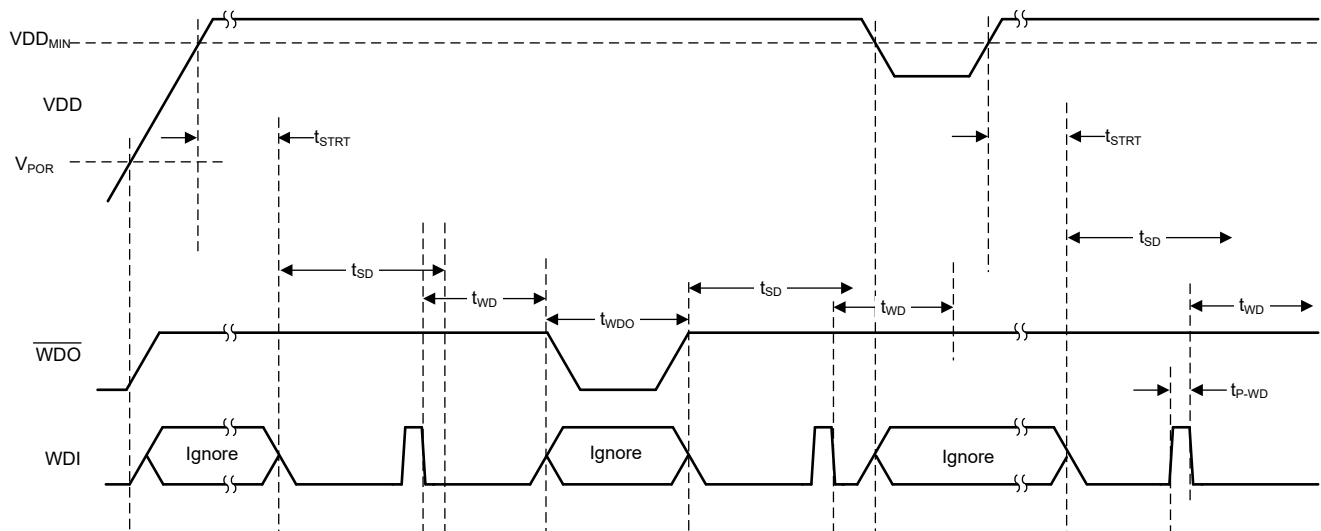


Figure 6-1. Functional Timing Diagram

6.9 Typical Characteristics

all curves are taken at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

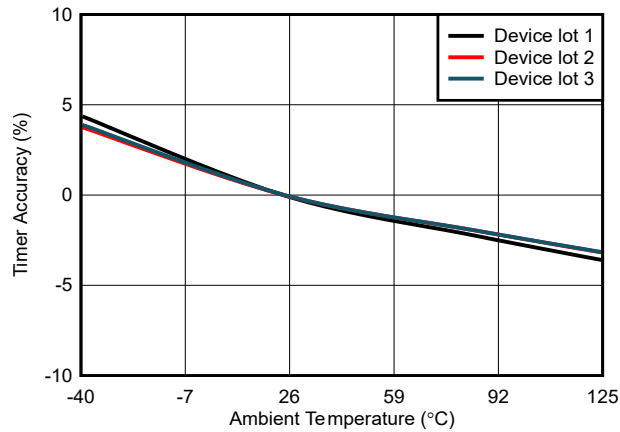


Figure 6-2. Timer Accuracy vs Temperature

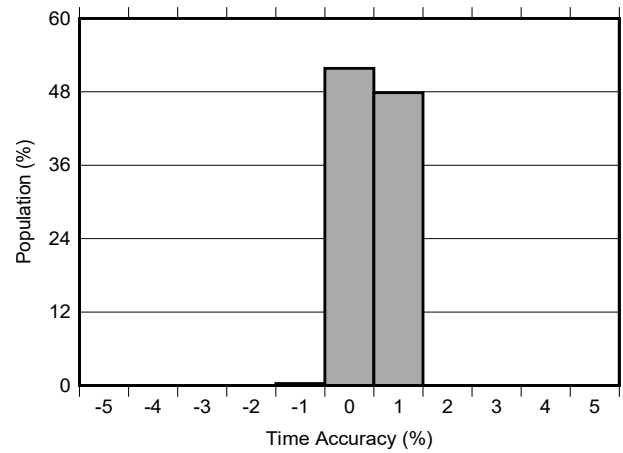


Figure 6-3. Timer Accuracy Histogram

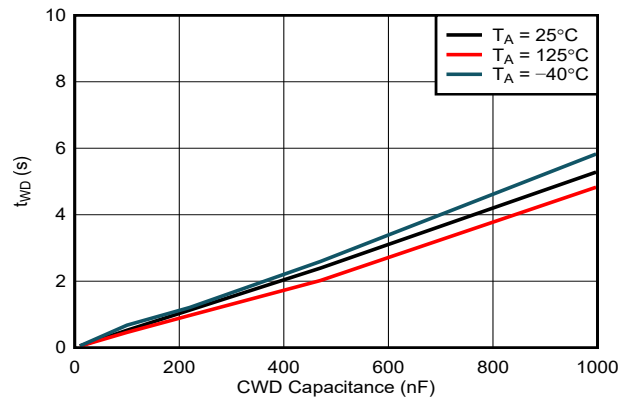


Figure 6-4. t_{WD} vs Capacitance

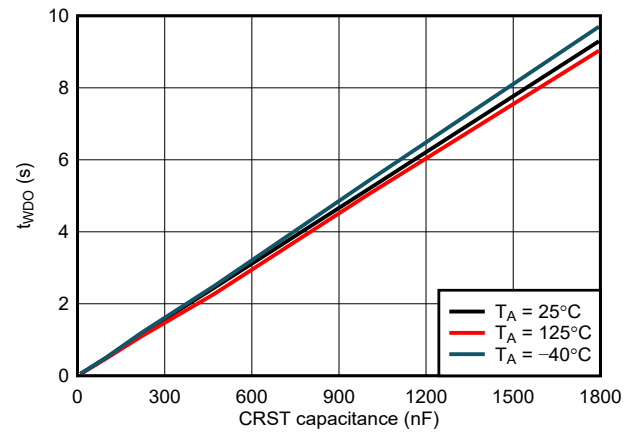


Figure 6-5. t_{WD0} vs Capacitance

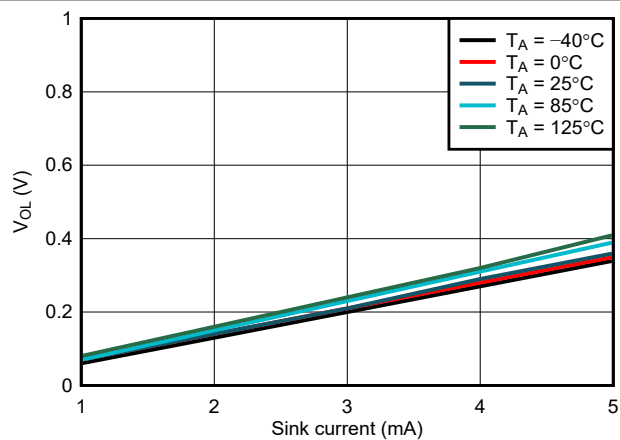


Figure 6-6. WDO V_{OL} vs I_{sink} , $V_{DD} = 1.5\text{V}$

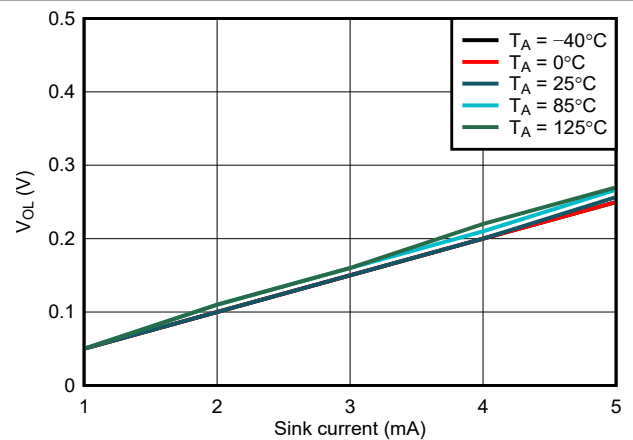


Figure 6-7. WDO V_{OL} vs I_{sink} , $V_{DD} = 3.3\text{V}$

6.9 Typical Characteristics (continued)

all curves are taken at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

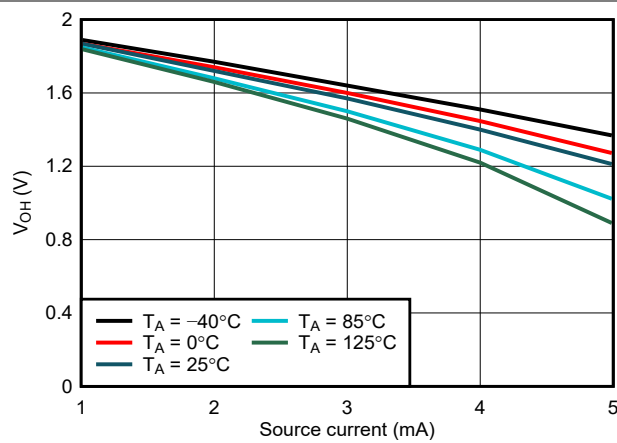


Figure 6-8. WDO V_{OH} vs I_{source} , $V_{DD} = 2.0\text{V}$

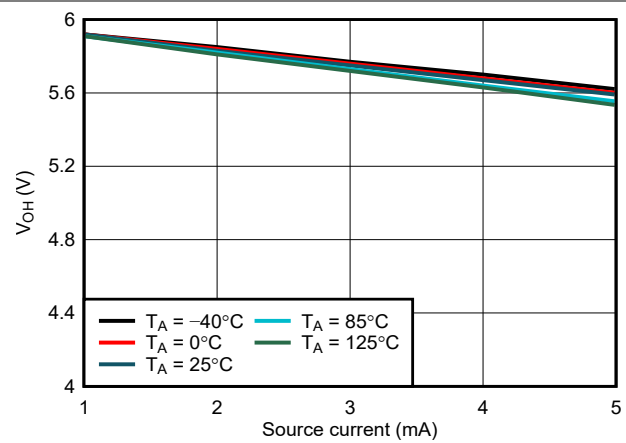


Figure 6-9. WDO V_{OH} vs I_{source} , $V_{DD} = 6.0\text{V}$

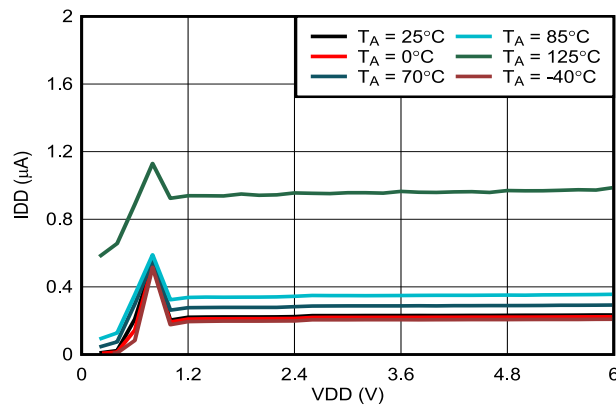


Figure 6-10. Supply Current vs Power-Supply Voltage

7 Detailed Description

7.1 Overview

The TPS3435-Q1 is a high-accuracy timeout watchdog timer device. The device family supports multiple features related to watchdog operation in a compact 8 pin SOT23 package. The devices are available in 3 different pinout configurations. Each pinout offers access to different features to meet the various application requirements. The device family is rated for AEC-Q100 applications.

7.2 Functional Block Diagrams

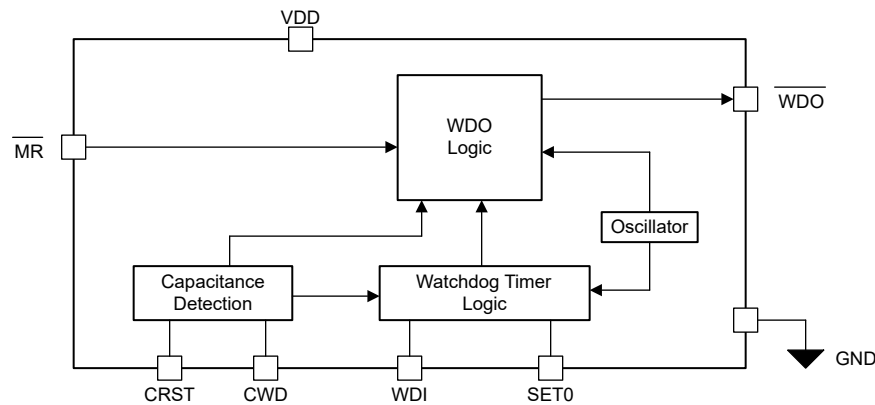


Figure 7-1. Pinout Option A

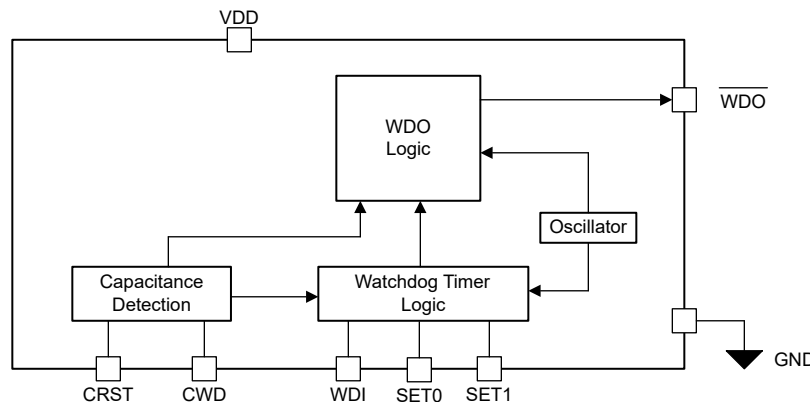


Figure 7-2. Pinout Option B

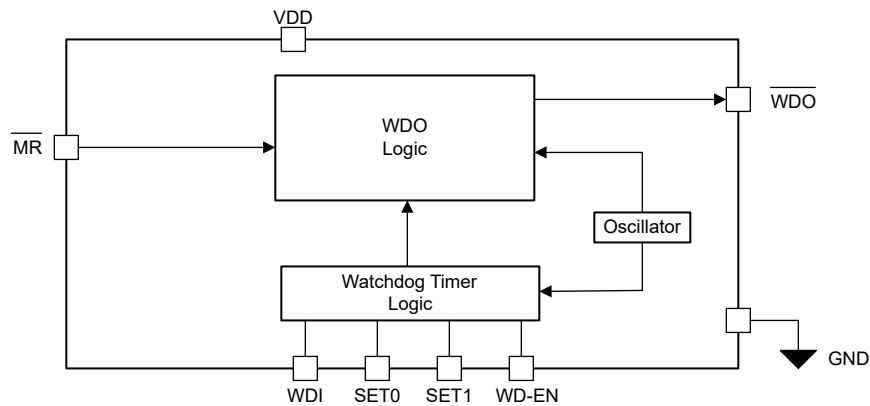


Figure 7-3. Pinout Option C

7.3 Feature Description

7.3.1 Timeout Watchdog Timer

The TPS3435-Q1 offers high precision timeout watchdog timer monitoring. The device is available in multiple pinout options A to C which support multiple features to meet ever expanding needs of various applications. Make sure a correct pinout is selected to meet the application needs.

The timeout watchdog is active when the VDD voltage is higher than the VDD_{MIN} , $\overline{MR}$ voltage is held higher than $0.7 \times VDD$ and watchdog is enabled. TPS3435-Q1 family offers various startup time delay options to make sure enough time is available for the host to complete boot operation. Please refer [Section 7.3.1.3](#) for additional details.

The timeout watchdog timer monitors the WDI pin for falling edge in the time frame defined by t_{WD} time period. Refer [Section 7.3.1.1](#) section to arrive at the relevant t_{WD} value needed for application. The timer value is reset when a valid falling edge is detected on WDI pin in the t_{WD} time duration. When a valid WDI transition is not detected in t_{WD} time, the device asserts WDO output. The WDO is asserted for time t_{WDO} . Refer [Section 7.3.3](#) to arrive at the relevant t_{WDO} value needed for application.

[Figure 7-4](#) shows the basic operation for timeout watchdog timer operation. The TPS3435-Q1 watchdog functionality supports multiple features. Details are available in following sub sections.

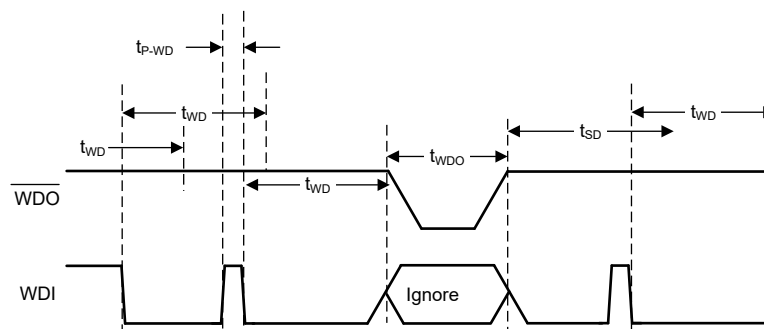


Figure 7-4. Timeout Watchdog Timer Operation

7.3.1.1 t_{WD} Timer

The t_{WD} timer for TPS3435-Q1 can be set using an external capacitor connected between CWD pin and GND pin. This feature is available with pinout options A or B. Applications which are space constrained or need timer values which meet offered timer options, can benefit when using pinout options C. The TPS3435-Q1 offers multiple fixed timer options ranging from 1ms up-to 100s.

The TPS3435-Q1, when using capacitance based timer, senses the capacitance value during the power up. The capacitor is charged and discharged with known internal current source for one cycle to sense the capacitance value. The sensed value is used to arrive at t_{WD} timer for the watchdog operation. This unique implementation helps reduce the continuous charge and discharge current for the capacitor, thus reducing overall current consumption. Continuous charge and discharge of capacitance creates wider dead time (no watchdog monitor functionality) when capacitor is discharging. The dead time is higher for high value of capacitance. The unique implementation of TPS3435-Q1 helps avoid the dead time as the capacitance is not continuously charging or discharging under normal operation. Make sure C_{CWD} is $< 200 \times C_{CRST}$ for accurate calibration of capacitance. [Equation 1](#) highlights the relationship between t_{WD} in second and CWD capacitance in farad. The t_{WD} timer is 20% accurate for the capacitor's typical value. Accuracy of the capacitance has additional impact on the t_{WD} time. Make sure the capacitance meets the recommended operating range. Capacitance outside the recommended range can lead to incorrect operation of the device.

$$t_{WD} \text{ (sec)} = 4.95 \times 10^6 \times C_{CWD} \text{ (F)} \quad (1)$$

The TPS3435-Q1 also offers wide selection of high accuracy fixed timer options starting from 1ms to 100sec including various industry standard values. The TPS3435-Q1 fixed time options are $\pm 10\%$ accurate for $t_{WD} \geq$

10ms. For $t_{WD} < 10\text{ms}$, the accuracy is $\pm 20\%$. t_{WD} value relevant to application can be identified from the orderable part number. Refer [Section 4](#) section to identify mapping of orderable part number to t_{WD} value.

The TPS3435-Q1 offers flexibility to change the t_{WD} value on the fly by controlling the logic levels on the SETx pins. [Section 7.3.1.4](#) section explains the advantages offered by this feature and the device behavior with various SETx pin combinations.

7.3.1.2 Watchdog Enable Disable Operation

The TPS3435-Q1 supports watchdog enable or disable functionality. This functionality is critical for different use cases as listed below.

- Disable watchdog during firmware update to avoid host RESET.
- Disable watchdog during software step-by-step debug operation.
- Disable watchdog when performing critical task to avoid watchdog error interrupt.
- Keep watchdog disabled until host boots up.

The TPS3435-Q1 supports watchdog enable or disable functionality through either WD-EN pin (pin configuration C) or SET[1:0] = 0b'01 (pin configuration B) logic combination. For a given pinout only one of these two methods is available for the user to disable watchdog operation.

For a pinout which offers a WD-EN pin, the watchdog enable disable functionality is controlled by the logic state of WD-EN pin. Drive WD-EN = 1 to enable the watchdog operation or drive WD-EN = 0 to disable the watchdog operation. The WD-EN pin can be toggled any time during the device operation. The [Figure 7-5](#) diagram shows timing behavior with WD-EN pin control.

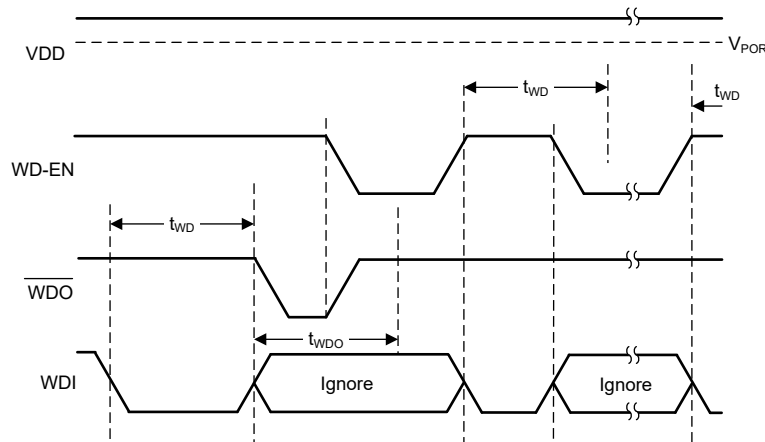


Figure 7-5. Watchdog Enable: WD-EN Pin Control

SET[1:0] = 0b'01 combination can be used to disable watchdog operation with a pinout which offers SET1 and SET0 pins, but does not include WD-EN pin. The SET pin logic states can be changed at any time during watchdog operation. Refer [Section 7.3.1.4](#) section for additional details regarding SET[1:0] pin behavior.

Pinout options A, B offer watchdog timer control using a capacitance connected between CWD and GND pin. A capacitance value higher than recommended or connect to GND leads to watchdog functionality getting disabled. Capacitance based disable operation overrides the other two options mentioned above. Changing capacitance on the fly does not enable or disable watchdog operation. A power supply recycle is needed to detect change in capacitance.

Ongoing watchdog frame is terminated when watchdog is disabled. WDO stays deasserted when watchdog operation is disabled. When enabled the device immediately enters t_{WD} frame and start watchdog monitoring operation.

7.3.1.3 t_{SD} Watchdog Start Up Delay

The TPS3435-Q1 supports watchdog startup delay feature. This feature is activated after power up or after WDO assert event. When t_{SD} frame is active, the device monitors the WDI pin but the WDO output is not asserted. This feature allows time for the host complete boot process before watchdog monitoring can take over. The start up delay helps avoid unexpected WDO assert events during boot. The t_{SD} time is predetermined based on the device part number selected. Refer [Section 4](#) section for details to map the part number to t_{SD} time. Pinout option A, B are available only in no delay or 10 sec start up delay options.

To exit t_{SD} frame, one of the following event must occur:

- The host provides a valid pulse transition on the WDI pin.
- Change in logic state of SET[1:0].
- Toggling of the WD_EN pin.

The device enters watchdog monitoring phase after the device exits the t_{SD} frame.

Failure to provide one of the exit condition within t_{SD} triggers the watchdog error by asserting the WDO output pin for t_D , this is observed in [Figure 7-6](#).

The t_{SD} frame is not initiated when the watchdog functionality is enabled using WD-EN pin or SET[1:0] pin combination as described in [Section 7.3.1.2](#) section.

[Figure 7-6](#) shows the operation for t_{SD} time frame.

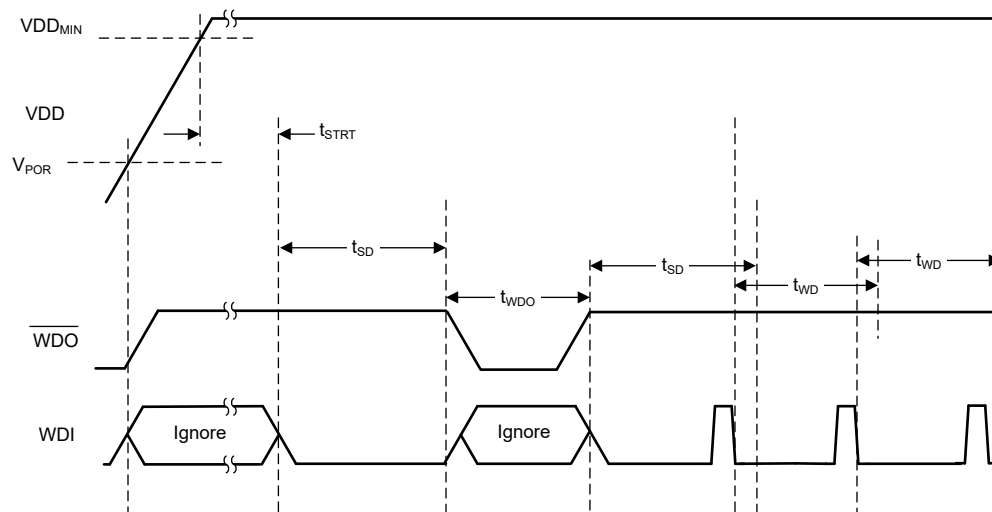


Figure 7-6. t_{SD} Frame Behavior

7.3.1.4 SET Pin Behavior

The TPS3435-Q1 offers one or two SET pins based on the pinout option selected. SET pins offer flexibility to the user to program the t_{WD} timer on the fly to meet various application requirements. Typical use cases where SET pin can be used are:

- Use wide timeout timer when host is in sleep mode, change to small timeout operation when host is operational. Watchdog can be used to wake up the host after long duration to perform the application related activities before going back to sleep.
- Change to wide timeout timer when performing system critical tasks to make sure the watchdog does not interrupt the critical task. Change timer to application specified interval after the critical task is complete.

The t_{WD} timer value for the device is combination of timer selection based on the CWD pin or fixed timer value along with SET pin logic level. The base t_{WD} timer value is decided based on the Watchdog Time selector in the [Section 4](#) section. The SET pin logic level is decoded during the device power up. The SET pin value can be changed any time during the operation. SETx pin change which leads to change of watchdog timer value or enable/disable state, terminates the ongoing watchdog frame immediately. SETx pins can be updated when

WDO output is asserted as well. The updated t_{WD} timer value is going be applied after output is deasserted and the t_{SD} timer is over or terminated.

For a pinout which offers only SET0 pin to the user, the t_{WD} multiplier value is decided based on the Watchdog Time Scaling selector in the [Section 4](#) section. [Table 7-1](#) showcases an example of the t_{WD} values for different SET0 logic levels when using Watchdog Time setting as option D = 10ms.

Table 7-1. t_{WD} Scaling with SET0 Pin Only (Pin Configuration A)

WATCHDOG TIME SCALING SELECTION	t_{WD}	
	SET0 = 0	SET0 = 1
A	10ms	20ms
B	10ms	40ms
C	10ms	80ms
D	10ms	160ms
E	10ms	320ms
F	10ms	640ms
G	10ms	1280ms

For pinouts which offer both SET0 & SET1 pins to the user, the t_{WD} multiplier value is decided based on the Watchdog Time Scaling selector in the [Section 4](#) section. Two SETx pins offer 3 different time scaling options. The SET[1:0] = 0b'01 combination disables the watchdog operation. [Table 7-2](#) showcases an example of the t_{WD} values for different SET[1:0] logic levels when using Watchdog Time setting as option G = 100ms. The package pin out selected does not offer WD-EN pin.

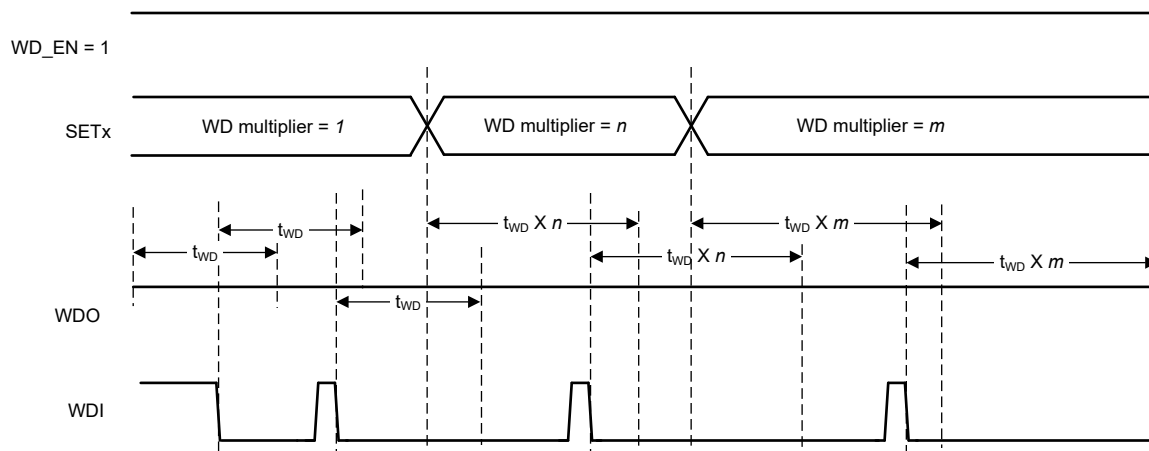
Table 7-2. t_{WD} Scaling with SET0 & SET1 Pins, WD-EN Pin Not Available (Pin Configuration B)

WATCHDOG TIME SCALING SELECTION	t_{WD}			
	SET[1:0] = 0b'00	SET[1:0] = 0b'01	SET[1:0] = 0b'10	SET[1:0] = 0b'11
A	100ms	Watchdog disable	200ms	400ms
B	100ms	Watchdog disable	400ms	800ms
C	100ms	Watchdog disable	800ms	1600ms
D	100ms	Watchdog disable	1600ms	3200ms
E	100ms	Watchdog disable	3200ms	6400ms
F	100ms	Watchdog disable	6400ms	12800ms
G	100ms	Watchdog disable	12800ms	25600ms

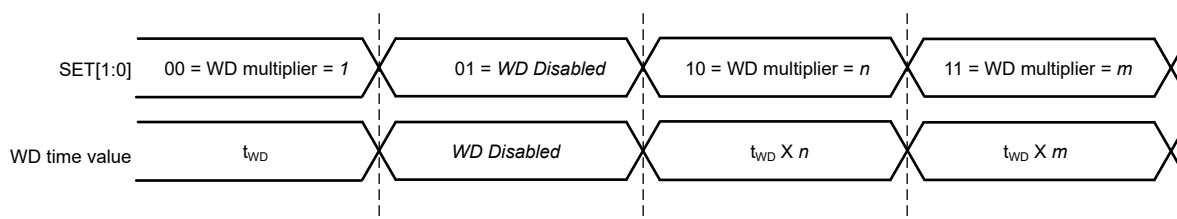
Selected pinout option can offer WD-EN pin along with SET[1:0] pins (Pin Configuration C). With this pinout, the WD-EN pin controls watchdog enable and disable operation. The SET[1:0] = 0b'01 combination operates as SET[1:0] = 0b'00.

Make sure the t_{WD} value with SETx multiplier does not exceed 640s. If a selection of timer and multiplier results in $t_{WD} > 640s$, the timer value is restricted to 640s.

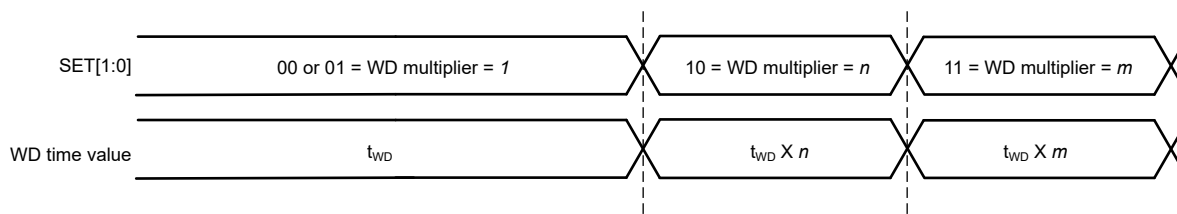
[Figure 7-7](#) to [Figure 7-9](#) diagrams show the timing behavior with respect to SETx status changes.

**Figure 7-7. Watchdog Behavior with SETx Pin Status**

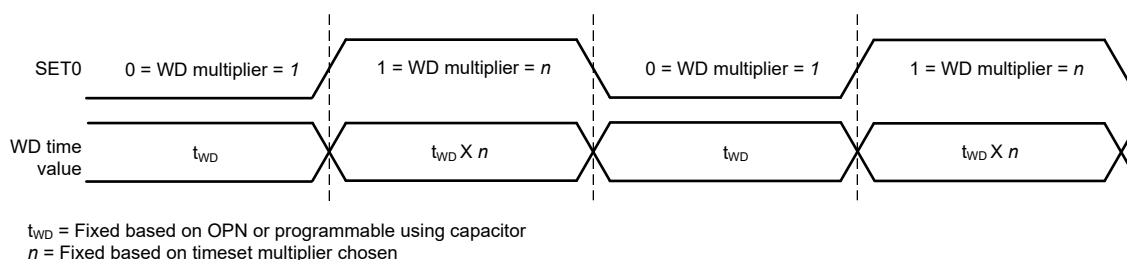
SET Pin (2 Pins) Operation; WD_EN Pin Not Available



SET Pin (2 Pins) Operation; WD_EN Available = 1



t_{WD} = Fixed based on OPN or programmable using capacitor
 n, m = Fixed based on timeset multiplier chosen

Figure 7-8. Watchdog Operation with 2 SET Pins

t_{WD} = Fixed based on OPN or programmable using capacitor
 n = Fixed based on timeset multiplier chosen

Figure 7-9. Watchdog Operation with 1 SET Pin

7.3.2 Manual RESET

The TPS3435-Q1 supports manual reset functionality using $\overline{\text{MR}}$ pin. $\overline{\text{MR}}$ pin when driven with voltage lower than $0.3 \times \text{VDD}$, asserts the WDO output. The $\overline{\text{MR}}$ pin has $100\text{k}\Omega$ pull up to VDD. The $\overline{\text{MR}}$ pin can be left floating. The internal pull up makes sure the output is not asserted due to $\overline{\text{MR}}$ pin trigger.

The output is deasserted after $\overline{\text{MR}}$ pin voltage rises above $0.7 \times \text{VDD}$ voltage. Refer [Figure 7-10](#) for more details.

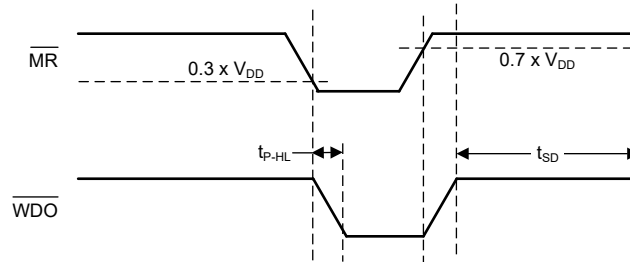


Figure 7-10. $\overline{\text{MR}}$ Pin Response

7.3.3 WDO Output

The TPS3435-Q1 device offers WDO output pin. WDO output is asserted when $\overline{\text{MR}}$ pin voltage is lower than 0.3 X VDD or watchdog timer error is detected.

The output is asserted for t_{WDO} time when any relevant events described above are detected, except for $\overline{MR}$ event. The time t_{WDO} can be programmed by connecting a capacitor between CRST pin and GND or the device asserts t_{WDO} for fixed time duration as selected by orderable part number. Refer [Section 4](#) section for all available options.

Equation 2 describes the relationship between capacitor value and the time t_{WDO} . Make sure the capacitance meets the recommended operating range. Capacitance outside the recommended range can lead to incorrect operation of the device.

$$t_{WDO} (\text{sec}) = 4.95 \times 10^6 \times C_{CRST} (F) \quad (2)$$

TPS3435-Q1 also offers a unique option of latched output. An orderable with latched output holds the output in asserted state indefinitely until the device is power cycled or the error condition is addressed. If the output is latched due to $\overline{\text{MR}}$ pin low voltage, the output latch is released when $\overline{\text{MR}}$ pin voltage rises above $0.7 \times V_{\text{DD}}$ level. If the output is latched due to watchdog timer error, the output latch is released when a WDI negative edge is detected or the device is shutdown and powered up again. [Figure 7-11](#) shows timing behavior of the device with latched output configuration.

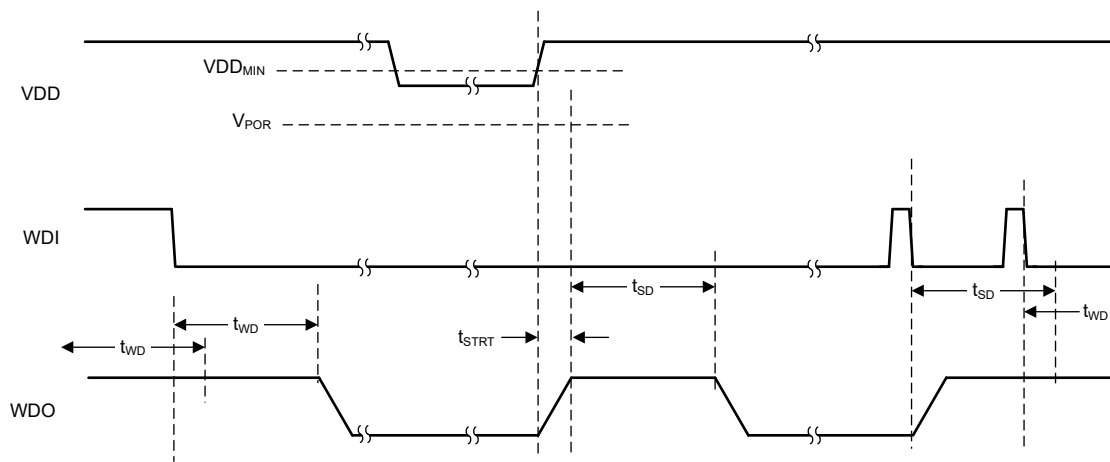


Figure 7-11. Output Latch Timing Behavior

7.4 Device Functional Modes

Table 7-3 summarizes the functional modes of the TPS3435-Q1.

Table 7-3. Device Functional Modes

VDD	WATCHDOG STATUS	WDI	WDO
$V_{DD} < V_{POR}$	Not Applicable	—	Undefined
$V_{POR} \leq V_{DD} < V_{DDmin}$	Not Applicable	Ignored	High
$V_{DD} \geq V_{DDmin}$	Disabled	Ignored	High
	Enabled	$t_{pulse}^1 < t_{WD(min)}$	High
	Enabled	$t_{pulse}^1 > t_{WD(max)}$	Low

(1) Where t_{pulse} is the time between falling edges on WDI.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The following sections describe in detail proper device implementation, depending on the final application requirements.

8.1.1 Output Assert Delay

The TPS3435-Q1 features two options for setting the output assert delay (t_{WDO}): using a fixed timing and programming the timing through an external capacitor.

8.1.1.1 Factory-Programmed Output Assert Delay Timing

Fixed output assert delay timings are available using pinout C. Using these timings enables a high-precision, 10% accurate output assert delay timing.

8.1.1.2 Adjustable Capacitor Timing

The TPS3435-Q1 also utilizes a programmable output assert delay, using a precision current source to charge an external capacitor upon device startup. The typical delay time resulting from a given external capacitance on the CRST pin can be calculated by Equation 3, where t_{WDO} is the output assert delay time in seconds and C_{CRST} is the capacitance in microfarads.

$$t_{WDO} \text{ (sec)} = 4.95 \times 10^6 \times C_{CRST} \text{ (F)} \quad (3)$$

Note that to minimize the difference between the calculated output assert delay time and the actual output assert delay time, use a high-quality ceramic dielectric COG, X5R, or X7R capacitor and minimize parasitic board capacitance around this pin. Table 8-1 lists the output assert delay time for typical capacitor values.

Table 8-1. Output Assert Delay Time for Common Capacitor Values

C_{CRST}	OUTPUT ASSERT DELAY TIME (t_{WDO})			UNIT
	MIN ⁽¹⁾	TYP	MAX ⁽¹⁾	
10nF	39.6	49.5	59.4	ms
100nF	396	495	594	ms
1μF	3960	4950	5940	ms

(1) Minimum and maximum values are calculated using capacitor's typical value.

8.1.2 Watchdog Timer Functionality

The TPS3435-Q1 features two options for setting the watchdog timer (t_{WD}): using a fixed timing and programming the timing through an external capacitor.

8.1.2.1 Factory-Programmed Timing Options

Fixed watchdog timeout options are available using pinout C. Using these timings enables a high-precision, 10% accurate watchdog timer t_{WD} .

8.1.2.2 Adjustable Capacitor Timing

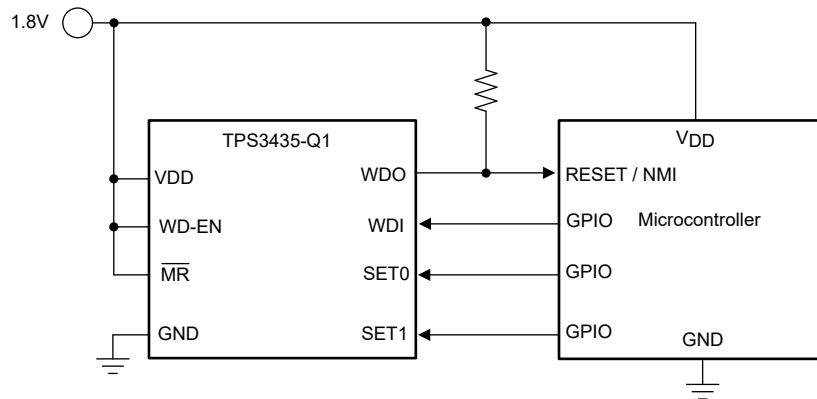
Adjustable t_{WD} timing is achievable by connecting a capacitor to the CWD pin. If this method is used, please consult Equation 1 for calculating typical t_{WD} values using the nominal capacitor value. Capacitor tolerances

cause the actual device timing to vary such that the minimum of t_{WD} can decrease and the maximum of t_{WD} can increase by the capacitor tolerance. For the most accurate timing, use ceramic capacitors with COG dielectric material.

8.2 Typical Applications

8.2.1 Design 1: Monitoring a Standard Microcontroller for Timeouts

This example application uses the TPS3435CDDBBDDFRQ1 to monitor a microcontroller to make sure the device is not stalled during operation.



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Figure 8-1. Microcontroller Watchdog Monitoring Circuit

8.2.1.1 Design Requirements

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Watchdog Timeout Period	Typical timeout period of 40ms	Typical timeout period of 40ms
Watchdog Output Assert Delay	Typical output assert of 2ms	Typical output assert of 2ms
Startup Delay	Minimum startup delay of 700ms	Minimum startup delay of 900ms
Output logic voltage	Open-drain	Open-drain
Maximum device current consumption	20μA	250nA typical, 3.0μA maximum ⁽¹⁾

(1) Only includes the current consumption of the TPS3435-Q1.

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Setting the Watchdog Timeout Period

The watchdog timeout design requirement can be met either by using a fixed-timeout version of the TPS3435-Q1 or by connecting a capacitor between the CWD pin and GND. The typical values can be met with preprogrammed fixed time options, hence a pinout offering fixed time options is selected. Please see the [Section 6.6](#) for a list of fixed timeouts. If using the CWD feature, please refer to [Section 7.3.1.1](#) for instructions on how to program the timeout period. In this application example, the 40ms timeout watchdog period is achieved by using watchdog time of 10ms (option D) and watchdog time scaling of 4 (option B). Connect SET[1:0] = 0b'10 to select watchdog time scaling of 4.

8.2.1.2.2 Setting Output Assert Delay

Please see the [Section 6.7](#) for a list of fixed timeouts. Timeout option B was chosen to meet the design requirement for a 2ms typical timeout.

8.2.1.2.3 Setting the Startup Delay

Startup delay option D is chosen, which offers a startup delay of 1s. This accounts for the minimum specification of 700ms.

8.2.1.2.4 Calculating the $\overline{WDO}$ Pullup Resistor

The TPS3435-Q1 uses an open-drain configuration for the $\overline{WDO}$ output, as shown in Figure 8-2. When the FET is off, the resistor pulls the drain of the transistor to VDD and when the FET is turned on, the FET pulls the output to ground, thus creating an effective resistor divider. The resistors in this divider must be chosen to make sure that V_{OL} is below the maximum value. To choose the proper pullup resistor, there are three key specifications to keep in mind: the pullup voltage (V_{PU}), the recommended maximum $\overline{WDO}$ pin current (I_{Sink}), and V_{OL} . The maximum V_{OL} is 0.3V, meaning that the effective resistor divider created must be able to bring the voltage on the reset pin below 0.3V with I_{Sink} kept below 2mA for $V_{DD} \geq 3V$ and 500 μ A for $V_{DD} = 1.5V$. For this example, with a $V_{PU} = V_{DD} = 1.5V$, a resistor must be chosen to keep I_{Sink} below 500 μ A because this value is the maximum consumption current allowed. To make sure this specification is met, a pullup resistor value of 10k Ω was selected, which sinks a maximum of 150 μ A when $\overline{WDO}$ is asserted.

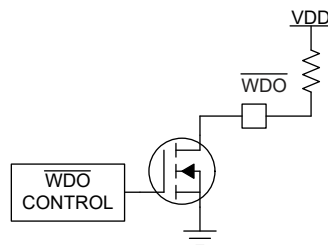


Figure 8-2. Open-Drain $\overline{WDO}$ Configuration

8.3 Power Supply Recommendations

This device is designed to operate from an input supply with a voltage range between 1.04V and 6V. An input supply capacitor is not required for this device; however, if the input supply is noisy, then good analog practice is to place a 0.1 μ F capacitor between the VDD pin and the GND pin.

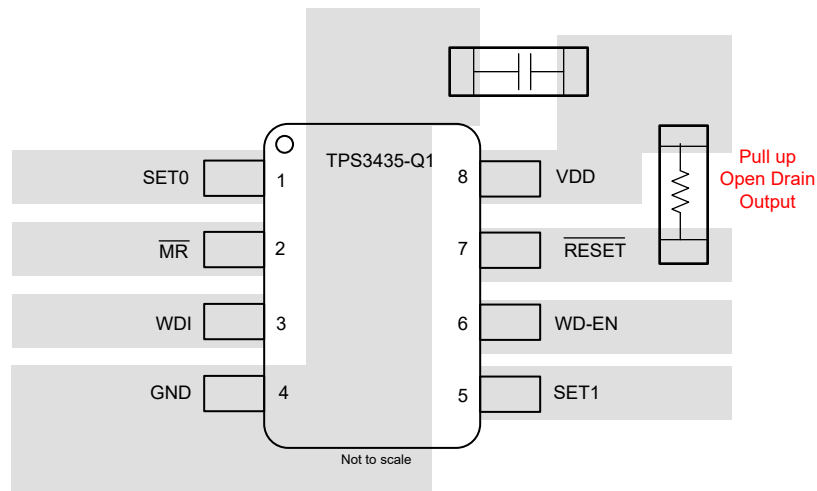
8.4 Layout

8.4.1 Layout Guidelines

Make sure that the connection to the VDD pin is low impedance. Good analog design practice recommends placing a 0.1 μ F ceramic capacitor as near as possible to the VDD pin. If a capacitor is not connected to the CRST pin, then minimize parasitic capacitance on this pin so the $\overline{WDO}$ delay time is not adversely affected.

- Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a 0.1 μ F ceramic capacitor as near as possible to the VDD pin.
- Place C_{CRST} capacitor as close as possible to the CRST pin.
- Place C_{CWD} capacitor as close as possible to the CWD pin.
- Place the pullup resistor on the $\overline{WDO}$ pin as close to the pin as possible.

8.4.2 Layout Example



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Figure 8-3. Typical Layout for the Pinout C of TPS3435-Q1

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2023) to Revision B (March 2025)	Page
• Added available device part table.....	3
• Added t _{SD} exit condition.....	18

Changes from Revision * (October 2022) to Revision A (June 2023)	Page
• Advance Information to Production Data release.....	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS3435AFACADDFRQ	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-45 to 125	NLHOH
TPS3435CAGBJDDFRQ	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	NLHOM
TPS3435CAKAGDDFRQ	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-45 to 125	NLHOJ
TPS3435CECAJDDFRQ	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	NLHOP

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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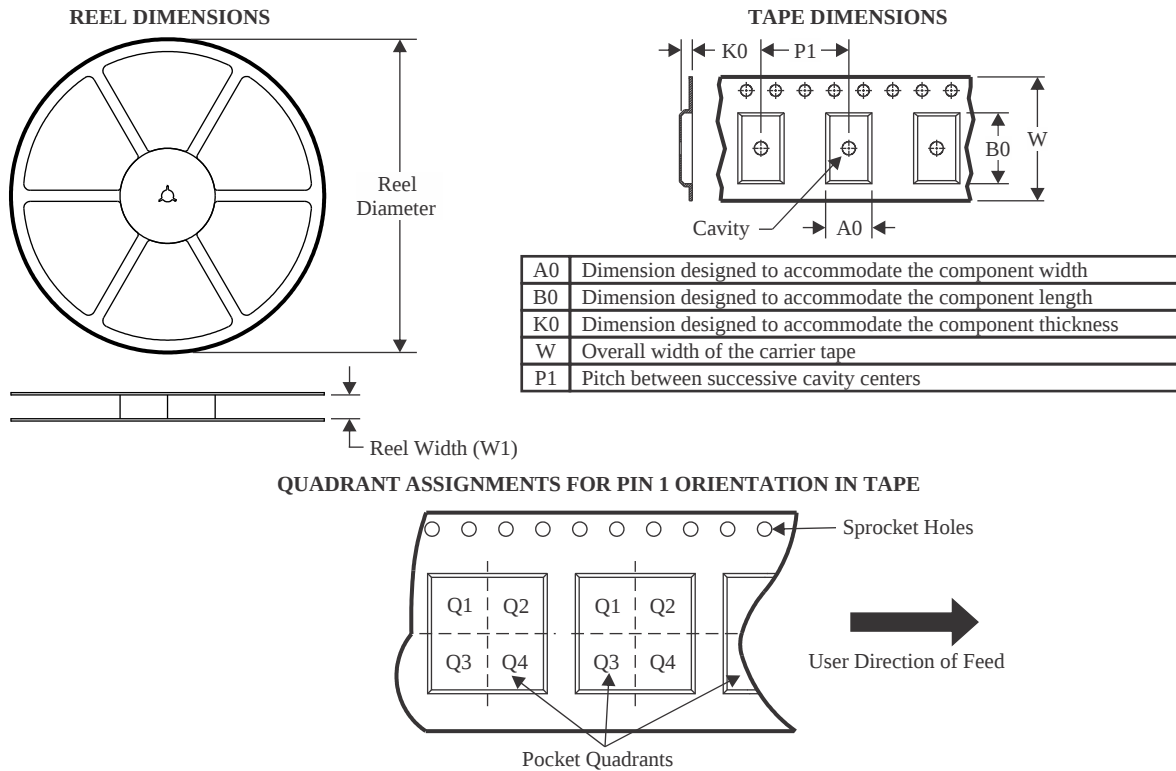
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OTHER QUALIFIED VERSIONS OF TPS3435-Q1 :

- Catalog : [TPS3435](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3435AFACADDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3435CAGBJDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3435CAKAGDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3435CECAJDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

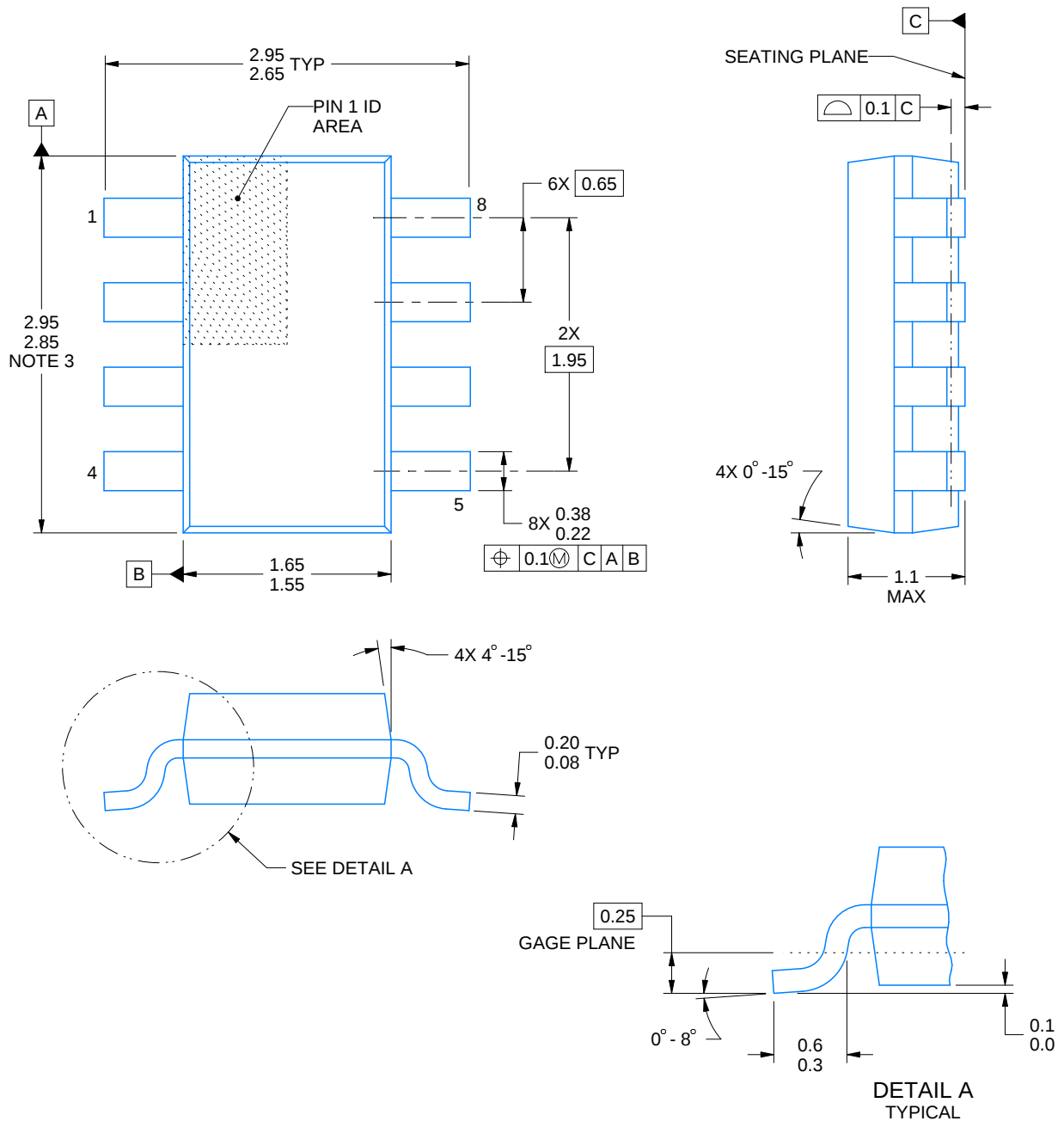


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3435AFACADDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TPS3435CAGBJDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TPS3435CAKAGDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TPS3435CECAJDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0

DDF0008A**PACKAGE OUTLINE****SOT-23-THIN - 1.1 mm max height**

PLASTIC SMALL OUTLINE



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NOTES:

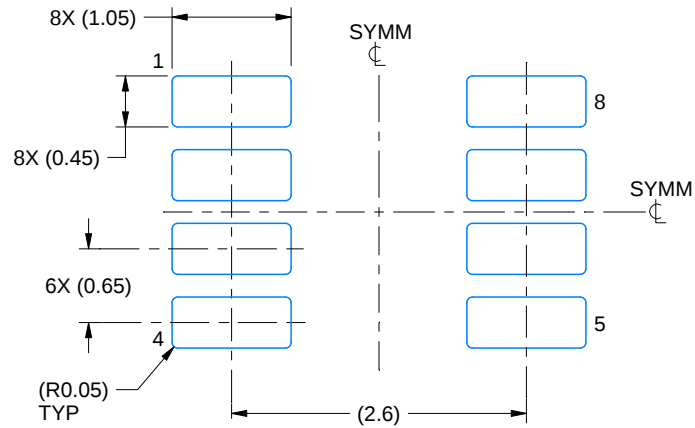
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT

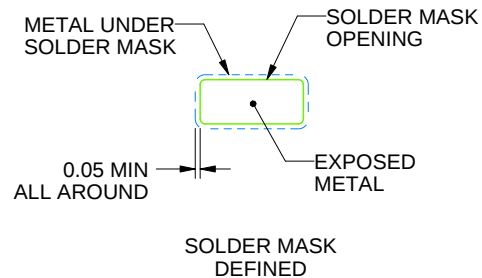
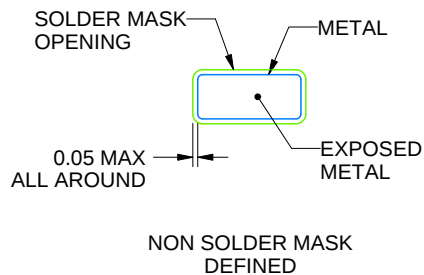
DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

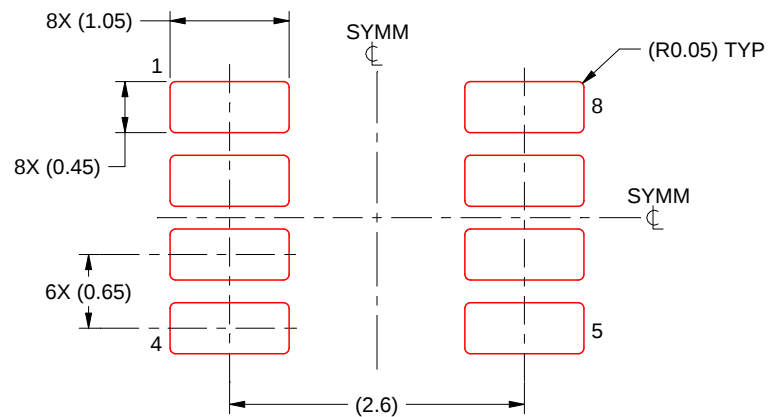
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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