采用 2x2 DRV 封装的 TPS6229x 1A 降压转换器

1 特性

- 高效率 - 高达 96%
- 高达 1000mA 的输出电流
- V_{IN} 范围为 2.3V 至 6.0V，支持具有扩展电压范围的锂离子电池
- 2.25MHz 固定频率运行
- 轻载电流下的省电模式
- PWM 模式下的输出电压精度为 ±1.5%
- 固定输出电压选项
- 静态电流典型值为 15μA
- 可实现最低压降的 100% 占空比
- 轻载时的电压定位
- 采用 2mm × 2mm × 0.8mm WSON (6) 封装 (DRV)

2 应用

- 移动电话、智能手机
- 无线 LAN
- 掌上电脑
- 低功耗 DSP 电源
- 便携式媒体播放器
- 负载点 (POL) 应用

3 说明

TPS6229x 器件是高效的同步降压直流/直流转换器，经优化可适用于电池供电的便携式 应用。这些器件采用单块锂离子电池提供高达 1000mA 的输出电流。

凭借 2.3V 至 6.0V 的输入电压范围，这些器件支持具有扩展电压范围的电池，非常适合为便携式 应用 （如手机和其他便携式设备）供电。

TPS6229x 器件在 2.25MHz 的固定开关频率下运行，在轻载电流情况下会进入省电模式，以便在整个负载电流范围内保持高效率。

省电模式经过优化，具有低输出电压纹波。对于低噪声应用，可通过将 MODE 引脚的电平拉高来强制这些器件进入固定频率脉宽调制 (PWM) 模式。在关断模式下，流耗减少至 1μA 以下。TPS6229x 器件允许使用小型电感器和电容器，可实现较小的解决方案尺寸。

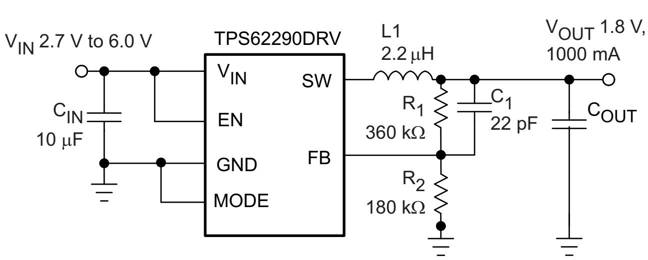
TPS6229x 器件在自然通风环境下的额定工作温度范围为 –40°C 至 85°C。这些器件采用 2mm × 2mm 6 引脚 WSON 封装 (DRV)。

器件信息(1)

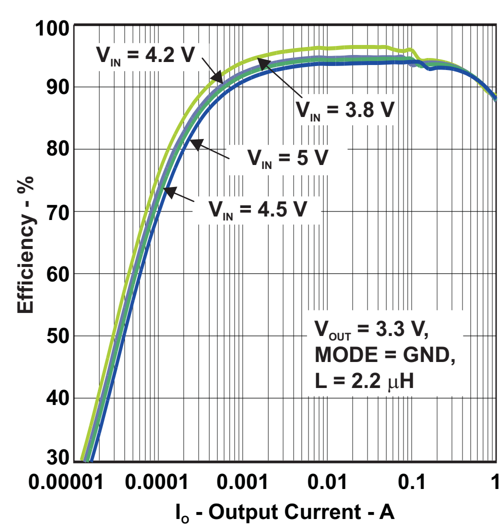
器件型号	封装	封装尺寸（标称值）
TPS6229x	SON (6)	2.00mm × 2.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型应用电路原理图



效率与输出电流间的关系



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision F (January 2016) to Revision G	Page
• Changed Equation 3 operator from × to + in correcting the $I_L$max formula.	12
• Added cross references to the Third-party Products disclaimer.	12

Changes from Revision E (September 2015) to Revision F	Page
• Added *Device Comparison Table*	3

Changes from Revision D (November 2009) to Revision E	Page
• 已添加 *引脚配置和功能* 部分、*ESD 额定值* 表、*特性* *说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分	1

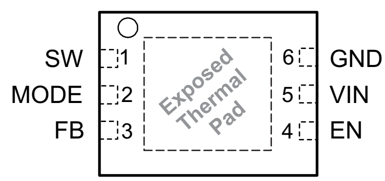
5 Device Comparison Table

PART NUMBER	OUTPUT VOLTAGE(1)	DEVICE MARKING(2)
TPS62290	Adjustable	BYN
TPS62291	3.3 V fixed	CFY
TPS62293	1.8 V fixed	CFD

(1) Contact TI for other fixed output voltage options
(2) For the most current package and ordering information, see *机械、封装和可订购信息*, or see the TI website at www.ti.com

6 Pin Configuration and Functions

DRV Package
6-PIN SON
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
EN	4	IN	This is the enable pin of the device. Pulling this pin to low forces the device into shutdown mode. Pulling this pin to high enables the device. This pin must be terminated.
FB	3	IN	Feedback pin for the internal regulation loop. Connect the external resistor divider to this pin. In case of fixed output voltage option, connect this pin directly to the output capacitor
GND	6	PWR	GND supply pin
MODE	2	IN	MODE pin = High forces the device to operate in fixed-frequency PWM mode. Mode pin = Low enables the power save mode with automatic transition from PFM mode to fixed-frequency PWM mode.
SW	1	OUT	This is the switch pin and is connected to the internal MOSFET switches. Connect the external inductor between this terminal and the output capacitor.
VIN	5	PWR	V_{IN} power supply pin.
Exposed Thermal Pad			Connect the exposed thermal pad to GND.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Input voltage range (2)	–0.3	7	V
	Voltage range at EN, MODE	–0.3	V_{IN} +0.3, ≤ 7	V
	Voltage at SW	–0.3	7	V
	Peak output current	Internally limited		A
T_J	Maximum operating junction temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Supply voltage	2.3		6	V
	Output voltage range for adjustable voltage	0.6		V_{IN}	V
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS6229x DRV (SON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	67.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	88.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Over full operating ambient temperature range, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply for condition V_{IN} = EN = 3.6 V. External components C_{IN} = 4.7 µF 0603, C_{OUT} = 10 µF 0603, L = 2.2 µH, refer to parameter measurement information.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage		2.3		6	V
I_{OUT}	Output current	V_{IN} 2.7 V to 6 V			1000	mA
		V_{IN} 2.5 V to 2.7 V			600	
		V_{IN} 2.3 V to 2.5 V			300	
I_Q	Operating quiescent current	I_{OUT} = 0 mA, PFM mode enabled (MODE = GND) device not switching, See (1)		15		µA
		I_{OUT} = 0 mA, switching with no load (MODE = V_{IN}) PWM operation, V_{OUT} = 1.8 V, V_{IN} = 3 V		3.8		mA
I_{SD}	Shutdown current	EN = GND		0.1	1	µA
UVLO	Undervoltage lockout threshold	Falling		1.85		V
		Rising		1.95		
ENABLE, MODE						
V_{IH}	High level input voltage, EN, MODE	2.3 V ≤ V_{IN} ≤ 6 V	1		V_{IN}	V
V_{IL}	Low level input voltage, EN, MODE	2.3 V ≤ V_{IN} ≤ 6 V	0		0.4	V
I_{IN}	Input bias current, EN, MODE	EN, MODE = GND or V_{IN}		0.01	1	µA
POWER SWITCH						
$R_{DS(on)}$	High side MOSFET on-resistance	V_{IN} = V_{GS} = 3.6 V, T_A = 25°C		240	480	mΩ
	Low side MOSFET on-resistance			185	380	
I_{LIMF}	Forward current limit MOSFET high-side and low side	V_{IN} = V_{GS} = 3.6 V	1.19	1.4	1.68	A
T_{SD}	Thermal shutdown	Increasing junction temperature		140		°C
	Thermal shutdown hysteresis	Decreasing junction temperature		20		
OSCILLATOR						
f_{SW}	Oscillator frequency	2.3 V ≤ V_{IN} ≤ 6 V	2.0	2.25	2.5	MHz
OUTPUT						
V_{OUT}	Adjustable output voltage range		0.6		V_I	V
V_{ref}	Reference voltage			600		mV
$V_{FB(PWM)}$	Feedback voltage PWM mode	MODE = V_{IN}, PWM operation, 2.3 V ≤ V_{IN} ≤ 6 V, See (2)	–1.5%	0%	1.5%	
$V_{FB(PFM)}$	Feedback voltage PFM mode	MODE = GND, device in PFM mode, +1% voltage positioning active, See (1)		1%		
	Load regulation			–0.5		%/A
$t_{Start\ Up}$	Start-up time	Time from active EN to reach 95% of V_{OUT}		500		µs
t_{Ramp}	V_{OUT} ramp-up time	Time to ramp from 5% to 95% of V_{OUT}		250		µs
I_{lkg}	Leakage current into SW pin	V_{IN} = 3.6 V, V_{IN} = V_{OUT} = V_{SW}, EN = GND, See (3)		0.1	1	µA

(1) In PFM mode, the internal reference voltage is set to typical 1.01 × V_{ref} . See the parameter measurement information.
(2) For V_{IN} = V_{OUT} + 1.0 V
(3) In fixed output voltage versions, the internal resistor divider network is disconnected from FB pin.

7.6 Typical Characteristics

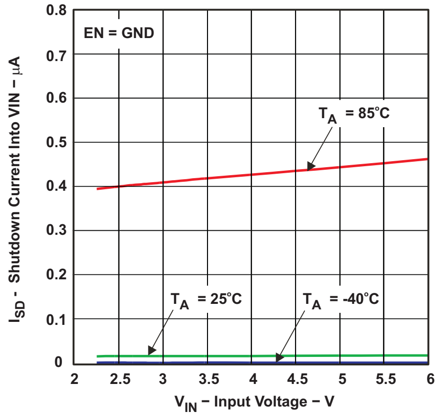


Figure 1. Shutdown Current Into VIN vs Input Voltage

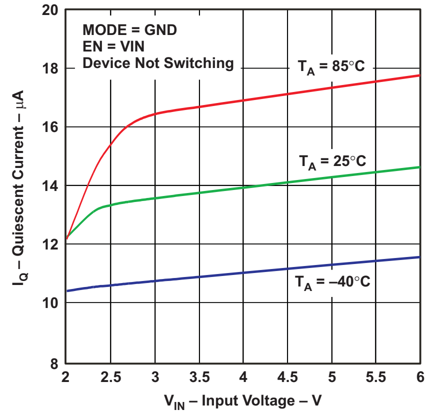


Figure 2. Quiescent Current vs Input Voltage

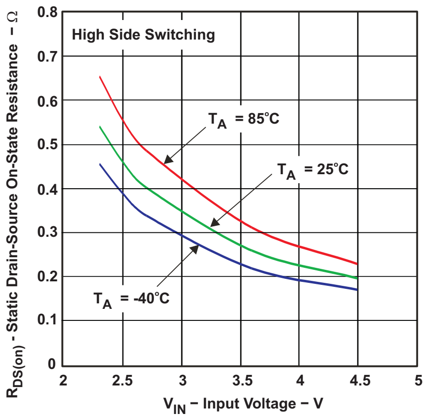


Figure 3. Static Drain-Source On-State Resistance vs Input Voltage

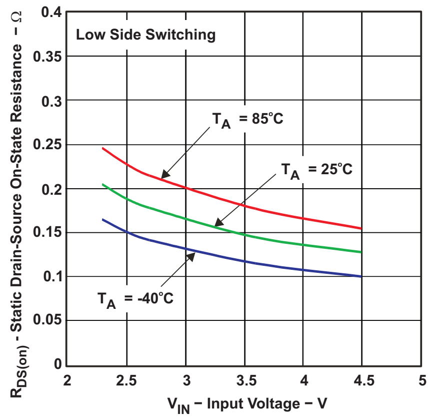


Figure 4. Static Drain-Source On-State Resistance vs Input Voltage

8 Detailed Description

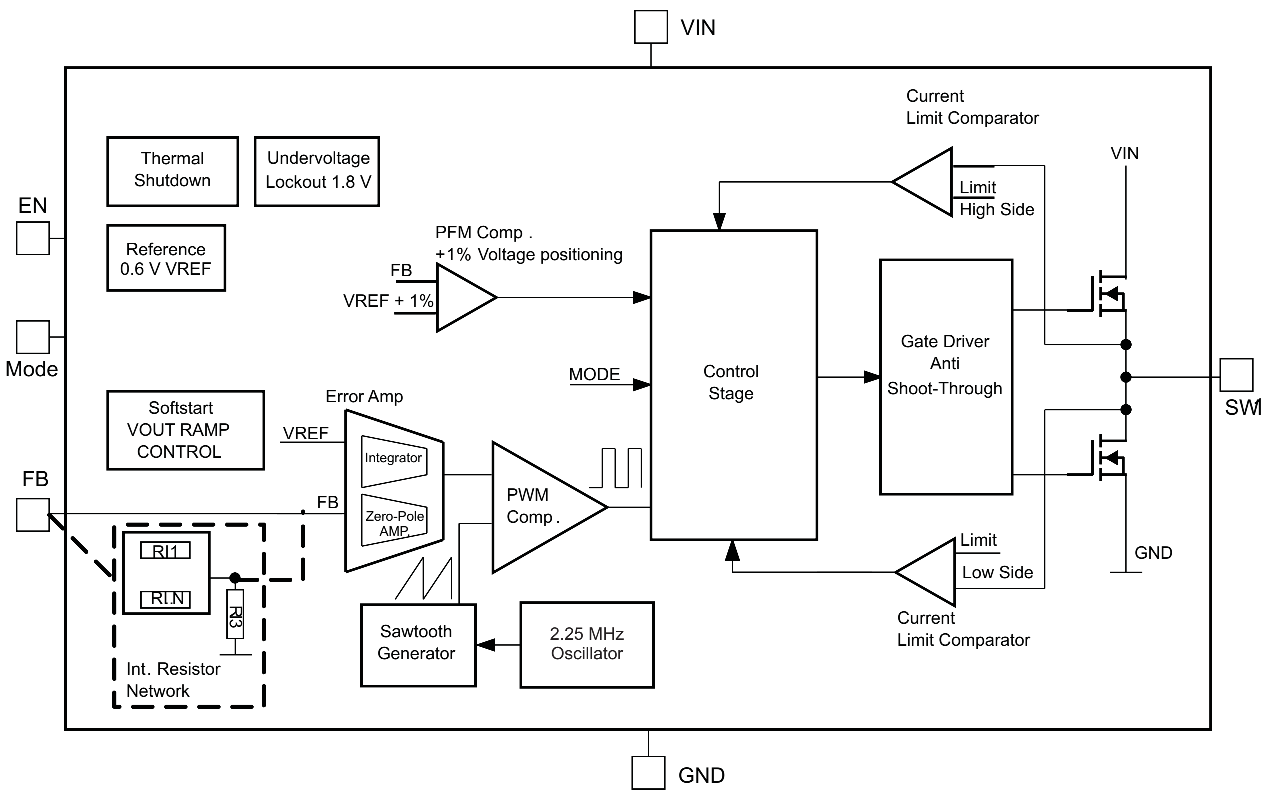
8.1 Overview

The TPS6229x step down converters operate with typically 2.25-MHz fixed frequency pulse width modulation (PWM) mode at moderate to heavy load currents. At light load currents, the converters can automatically enter power save mode and operate then in pulse frequency modulation (PFM) mode.

During PWM operation, the converters use a unique fast response voltage mode controller scheme with input voltage feed-forward to achieve good line and load regulation allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the high side MOSFET switch is turned on. The current flows now from the input capacitor via the high side MOSFET switch through the inductor to the output capacitor and load. During this phase, the current ramps up until the PWM comparator trips and the control logic will turn off the switch. The current limit comparator also turns off the switch in case the current limit of the high side MOSFET switch is exceeded. After a dead time preventing shoot through current, the low side MOSFET rectifier is turned on and the inductor current ramps down. The current flows now from the inductor to the output capacitor and to the load. It returns to the inductor through the low side MOSFET rectifier.

The next cycle is initiated by the clock signal again turning off the low side MOSFET rectifier and turning on the high side MOSFET switch.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Dynamic Voltage Positioning

This feature reduces the voltage undershoots/overshoots at load steps from light to heavy load and vice versa. It is active in power save mode and regulates the output voltage 1% higher than the nominal value. This provides more headroom for both the voltage drop at a load step, and the voltage increase at a load throw-off.

Feature Description (continued)

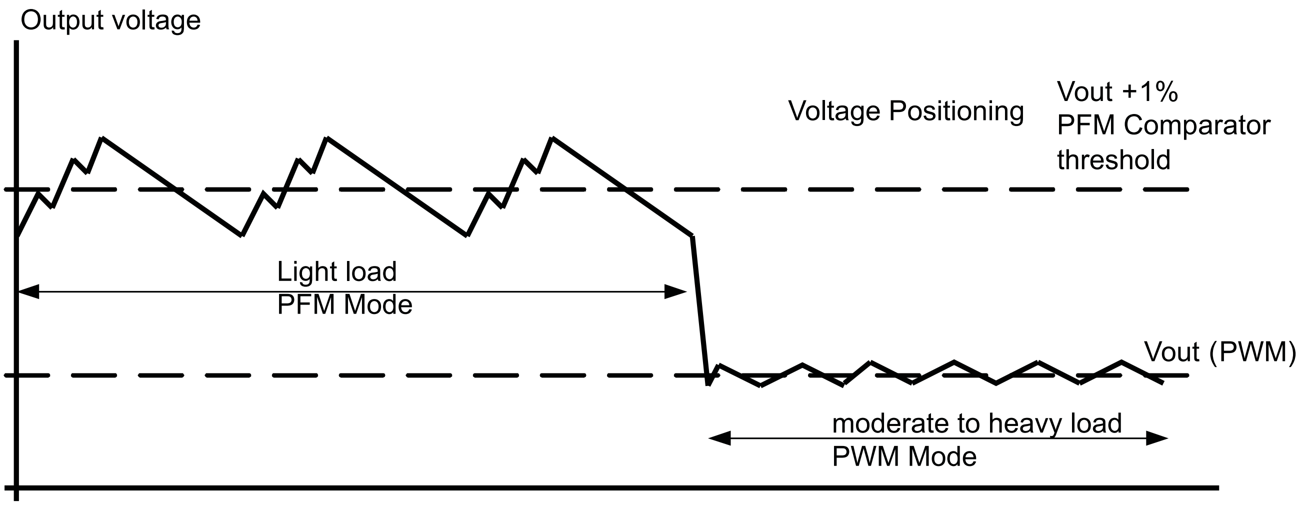


Figure 5. Power Save Mode Operation

8.3.2 Enable

The device is enabled by setting EN pin to high. During the start up time $t_{Start\ Up}$ the internal circuits are settled and the soft start circuit is activated. The EN input can be used to control power sequencing in a system with various DC/DC converters. The EN pin can be connected to the output of another converter, to drive the EN pin high and getting a sequencing of supply rails. With EN = GND, the device enters shutdown mode, in which all internal circuits are disabled. In fixed output voltage versions, the internal resistor divider network is disconnected from FB pin.

8.3.3 Mode Selection

The MODE pin allows mode selection between forced PWM mode and power save mode.

Connecting this pin to GND enables the power save mode with automatic transition between PWM and PFM mode. Pulling the MODE pin high forces the converter to operate in fixed frequency PWM mode even at light load currents. This allows simple filtering of the switching frequency for noise sensitive applications. In this mode, the efficiency is lower compared to the power save mode during light loads.

The condition of the MODE pin can be changed during operation and allows efficient power management by adjusting the operation mode of the converter to the specific system requirements.

8.3.4 Undervoltage Lockout

The undervoltage lockout circuit prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery and disables the output stage of the converter. The undervoltage lockout threshold is typically 1.85 V with falling V_{IN}.

8.3.5 Thermal Shutdown

As soon as the junction temperature, T_J, exceeds 140°C (typical) the device goes into thermal shutdown. In this mode, the high side and low side MOSFETs are turned-off. The device continues its operation when the junction temperature falls below the thermal shutdown hysteresis.

8.4 Device Functional Modes

8.4.1 Soft-Start

The TPS6229x has an internal soft start circuit that controls the ramp up of the output voltage. The output voltage ramps up from 5% to 95% of its nominal value within typical 250 µs. This limits the inrush current in the converter during ramp up and prevents possible input voltage drops when a battery or high impedance power source is used. The soft start circuit is enabled within the start up time $t_{Start\ Up}$.

8.4.2 Power Save Mode

The power save mode is enabled with MODE pin set to low level. If the load current decreases, the converter will enter power save mode operation automatically. During power save mode the converter skips switching and operates with reduced frequency in PFM mode with a minimum quiescent current to maintain high efficiency. The converter will position the output voltage typically +1% above the nominal output voltage. This voltage positioning feature minimizes voltage drops caused by a sudden load step.

The transition from PWM mode to PFM mode occurs once the inductor current in the low side MOSFET switch becomes zero, which indicates discontinuous conduction mode.

During the power save mode the output voltage is monitored with a PFM comparator. As the output voltage falls below the PFM comparator threshold of V_{OUT} nominal +1%, the device starts a PFM current pulse. The high side MOSFET switch will turn on and the inductor current ramps up. After the on-time expires, the switch is turned off and the low side MOSFET switch is turned on until the inductor current becomes zero.

The converter effectively delivers a current to the output capacitor and the load. If the load is below the delivered current, the output voltage will rise. If the output voltage is equal or higher than the PFM comparator threshold, the device stops switching and enters a sleep mode with typical 15 µA current consumption.

If the output voltage is still below the PFM comparator threshold, a sequence of further PFM current pulses are generated until the PFM comparator threshold is reached. The converter starts switching again once the output voltage drops below the PFM comparator threshold.

With a fast single threshold comparator, the output voltage ripple during PFM mode operation can be kept small. The PFM pulse is time controlled, which allows to modify the charge transferred to the output capacitor by the value of the inductor. The resulting PFM output voltage ripple and PFM frequency depend in first order on the size of the output capacitor and the inductor value. Increasing output capacitor values and inductor values will minimize the output ripple. The PFM frequency decreases with smaller inductor values and increases with larger values.

The PFM mode is left and PWM mode entered in case the output current can not longer be supported in PFM mode. The power save mode can be disabled through the MODE pin set to high. The converter will then operate in fixed frequency PWM mode.

8.4.3 100% Duty Cycle Low Dropout Operation

The device starts to enter 100% duty cycle mode once the input voltage comes close to the nominal output voltage. In order to maintain the output voltage, the high side MOSFET switch is turned on 100% for one or more cycles.

With further decreasing V_{IN} the high side MOSFET switch is turned on completely. In this case, the converter offers a low input-to-output voltage difference. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range.

The minimum input voltage to maintain regulation depends on the load current and output voltage, and can be calculated as:

$$V_{IN}min = V_{OUT}max + (I_{OUT}max \times (R_{DS(on)}max + R_L)) \tag{1}$$

where

- $I_{OUT}max$ = Maximum output current plus inductor ripple current
- $R_{DS(on)}max$ = Maximum P-channel switch $R_{DS(on)}$
- R_L = DC resistance of the inductor
- $V_{OUT}max$ = Nominal output voltage plus maximum output voltage tolerance

Device Functional Modes (continued)

8.4.4 Short-Circuit Protection

The high side and low side MOSFET switches are short-circuit protected with maximum switch current equal to I_{LIMF}. The current in the switches is monitored by current limit comparators. Once the current in the high side MOSFET switch exceeds the threshold of its current limit comparator, it turns off and the low side MOSFET switch is activated to ramp down the current in the inductor and high side MOSFET switch. The high side MOSFET switch can only turn on again, once the current in the low side MOSFET switch has decreased below the threshold of its current limit comparator.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS6229x devices are high-efficiency synchronous step-down DC/DC converters featuring power save mode or 2.25-MHz fixed frequency operation.

9.2 Typical Application

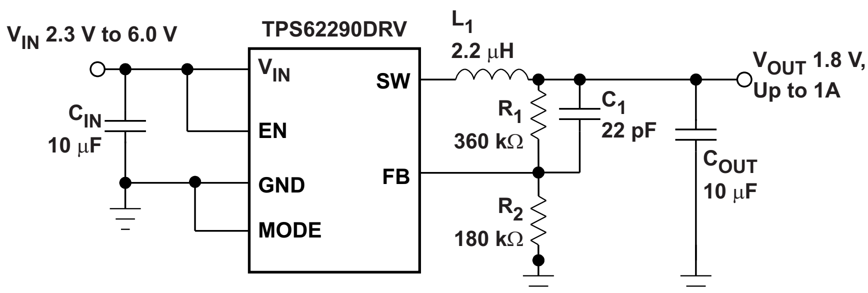


Figure 6. TPS62290DRV Adjustable 1.8 V

9.2.1 Design Requirements

The design guideline provides a component selection to operate the device within the recommended operating condition.

Table 1 shows the list of components for the Application Characterstic Curves.

Table 1. List of Components

COMPONENT REFERENCE	PART NUMBER	MANUFACTURER(1)	VALUE
C_{IN}	GRM188R60J106M	Murata	10 µF, 6.3 V. X5R Ceramic
C_{OUT}	GRM188R60J106M	Murata	10 µF, 6.3 V. X5R Ceramic
C_1		Murata	22 pF, COG Ceramic
L_1	LPS3015	Coilcraft	2.2 µH, 110 mΩ
R_1, R_2	Values depending on the programmed output voltage		

(1) See Third-party Products disclaimer

9.2.2 Detailed Design Procedure

9.2.2.1 Output Voltage Setting

The output voltage can be calculated to:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right)$$ with an internal reference voltage V_{REF} typical 0.6 V.

To minimize the current through the feedback divider network, R_2 should be 180 kΩ or 360 kΩ. The sum of R_1 and R_2 should not exceed ~1MΩ, to keep the network robust against noise.

An external feed forward capacitor C_1 is required for optimum load transient response. The value of C_1 should be in the range between 22 pF and 33 pF.

Route the FB line away from noise sources, such as the inductor or the SW line.

9.2.2.2 Output Filter Design (Inductor and Output Capacitor)

The TPS6229x is designed to operate with inductors in the range of 1.5 µH to 4.7 µH and with output capacitors in the range of 4.7 µF to 22 µF. The part is optimized for operation with a 2.2-µH inductor and 10-µF output capacitor.

Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. For stable operation, the L and C values of the output filter may not fall below 1-µH effective inductance and 3.5-µF effective capacitance.

9.2.2.2.1 Inductor Selection

The inductor value has a direct effect on the ripple current. The selected inductor has to be rated for its DC resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_{IN} or V_{OUT}.

The inductor selection has also impact on the output voltage ripple in PFM mode. Higher inductor values will lead to lower output voltage ripple and higher PFM frequency, lower inductor values will lead to a higher output voltage ripple but lower PFM frequency.

Equation 2 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 3. This is recommended because during heavy load transient the inductor current will rise above the calculated value.

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \tag{2}$$

$$I_{Lmax} = I_{OUTmax} + \frac{\Delta I_L}{2}$$

where

- f = Switching frequency (2.25 MHz typical)
- L = Inductor value
- ΔI_L = Peak-to-peak inductor ripple current
- I_{Lmax} = Maximum inductor current (3)

A more conservative approach is to select the inductor current rating just for the maximum switch current of the corresponding converter.

Accepting larger values of ripple current allows the use of low inductance values, but results in higher output voltage ripple, greater core losses, and lower output current capability.

The total losses of the coil have a strong impact on the efficiency of the DC/DC conversion and consist of both the losses in the DC resistance $R_{(DC)}$) and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

Table 2. List of Inductors

DIMENSIONS [mm^3]	INDUCTOR TYPE	SUPPLIER[1]
3 × 3 × 1.5	LPS3015	Coilcraft
3 x 3 x 1.5	LQH3NPN2R2NM0	MURATA
3.2 x 2.6 x 1.2	MIPSA3226D2R2	FDK

(1) See Third-party Products disclaimer

9.2.2.2.2 Output Capacitor Selection

The advanced fast-response voltage mode control scheme of the TPS6229x allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies.

At nominal load current, the device operates in PWM mode and the RMS ripple current is calculated as:

$$I_{RMSC_{OUT}} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \left(\frac{1}{2 \times \sqrt{3}} \right) \quad (4)$$

At nominal load current, the device operates in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta V_{OUT} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \left(\frac{1}{8 \times Cout \times f} + ESR \right) \quad (5)$$

At light load currents the converter operates in power save mode and the output voltage ripple is dependent on the output capacitor and inductor value. Larger output capacitor and inductor values minimize the voltage ripple in PFM mode and tighten DC output accuracy in PFM mode.

9.2.2.2.3 Input Capacitor Selection

The buck converter has a natural pulsating input current; therefore, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. For most applications, a 10-µF ceramic capacitor is recommended. The input capacitor can be increased without any limit for better input voltage filtering.

Take care when using only small ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output or V_{IN} step on the input can induce ringing at the V_{IN} pin. The ringing can couple to the output and be mistaken as loop instability or could even damage the part by exceeding the maximum ratings.

Table 3. List of Capacitor

CAPACITANCE	TYPE	SIZE	SUPPLIER(1)
10 µF	GRM188R60J106M69D	0603 1.6 × 0.8 × 0.8 mm^3	Murata

(1) See Third-party Products disclaimer

9.2.3 Application Curves

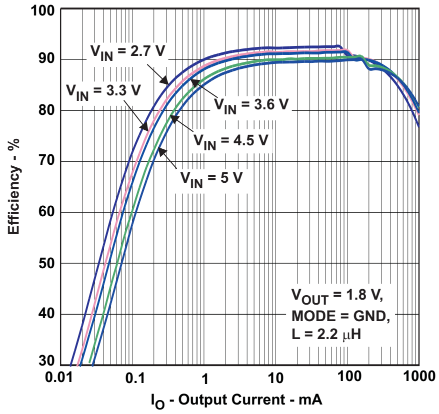


Figure 7. Efficiency (Power Save Mode) vs Output Current, V_{OUT} = 1.8 V

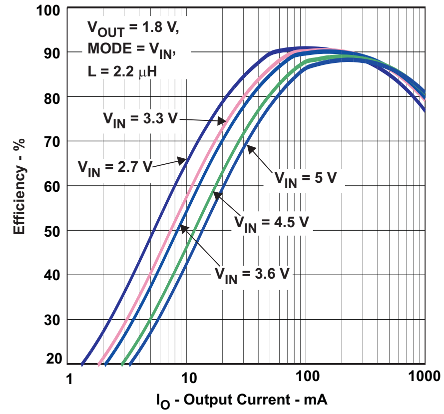


Figure 8. Efficiency (Forced PWM Mode) vs Output Current, V_{OUT} = 1.8 V

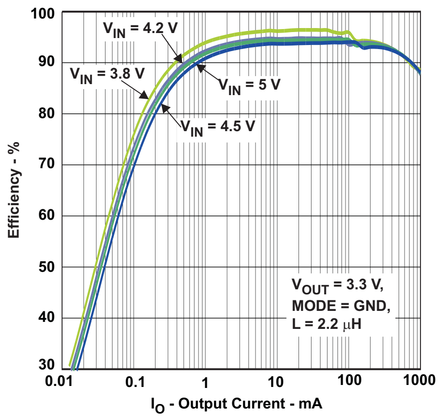


Figure 9. Efficiency (Power Save Mode) vs Output Current, V_{OUT} = 3.3 V

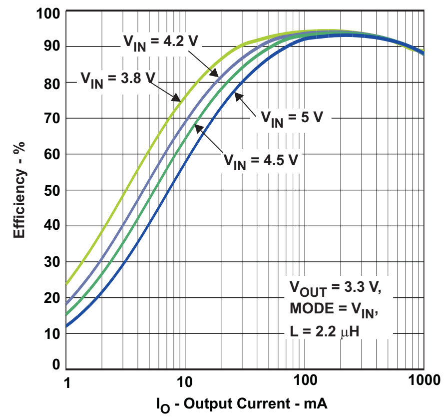


Figure 10. Efficiency (Forced PWM Mode) vs Output Current, V_{OUT} = 3.3 V

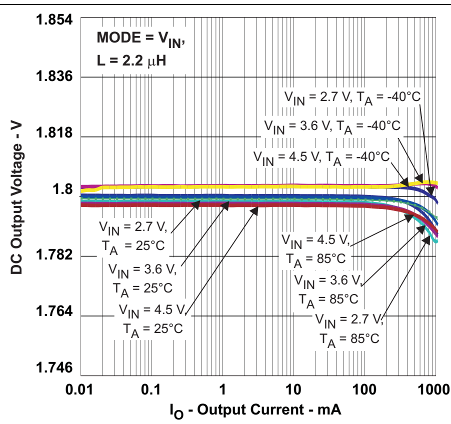


Figure 11. Output Voltage Accuracy (1.8-V Forced PWM Mode) vs Output Current

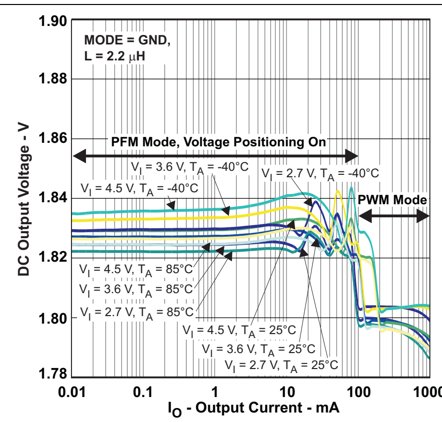


Figure 12. Output Voltage Accuracy (1.8-V Power Save Mode) vs Output Current

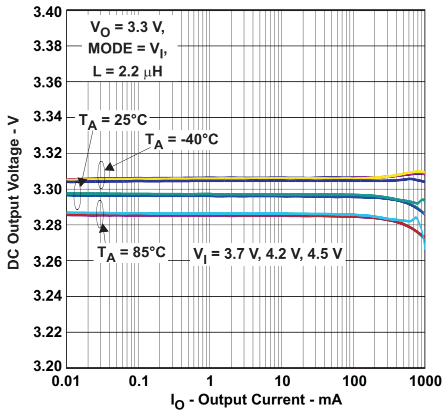


Figure 13. Output Voltage Accuracy 3.3-V Forced PWM Mode vs Output Current

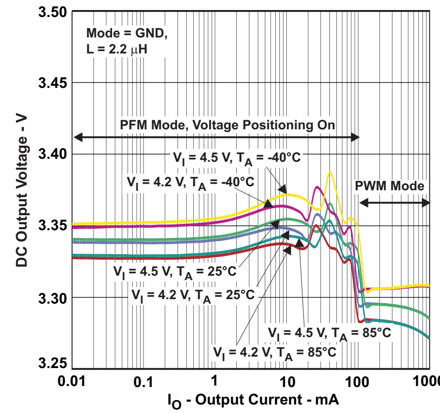


Figure 14. Output Voltage Accuracy 3.3-V Power Save Mode vs Output Current

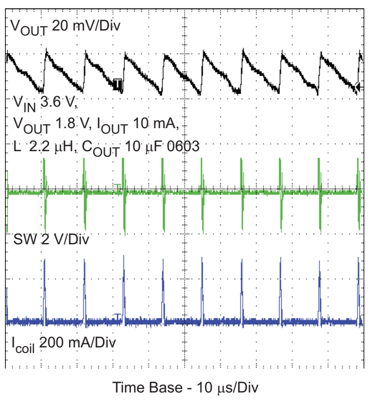


Figure 15. Typical Operation vs PFM Mode

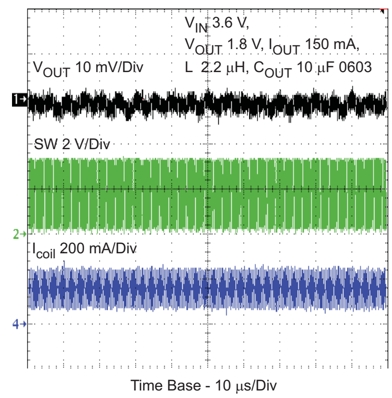


Figure 16. Typical Operation vs PWM Mode

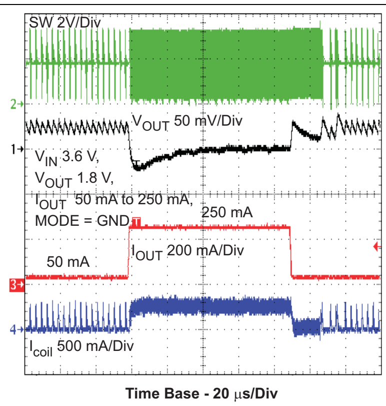


Figure 17. PFM Load Transient

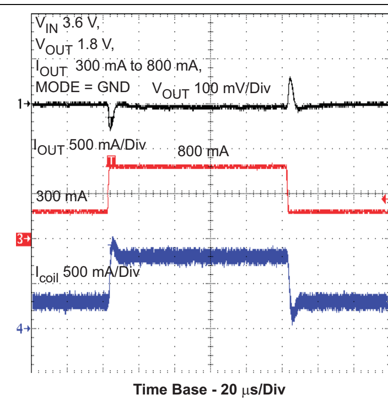


Figure 18. PFM Line Transient

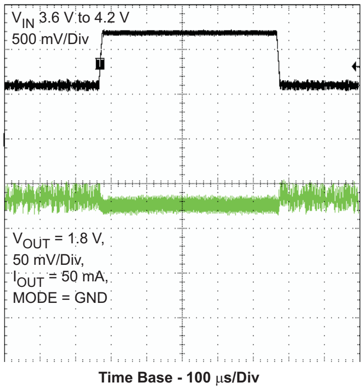


Figure 19. PWM Load Transient

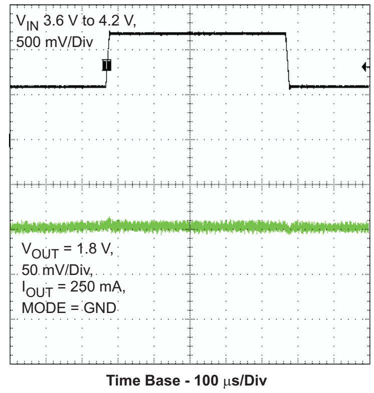


Figure 20. PWM Line Transient

9.3 System Examples

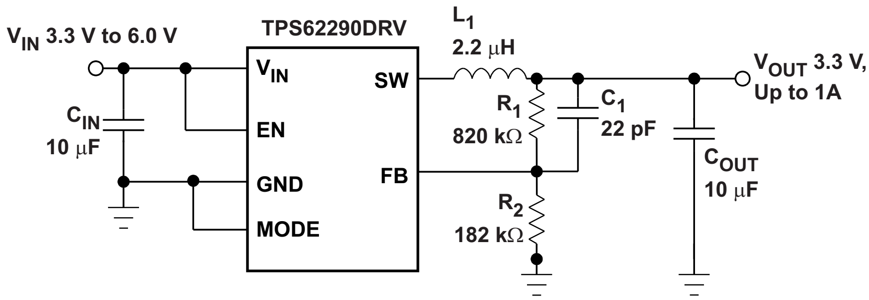


Figure 21. TPS62290DRV Adjustable 3.3 V

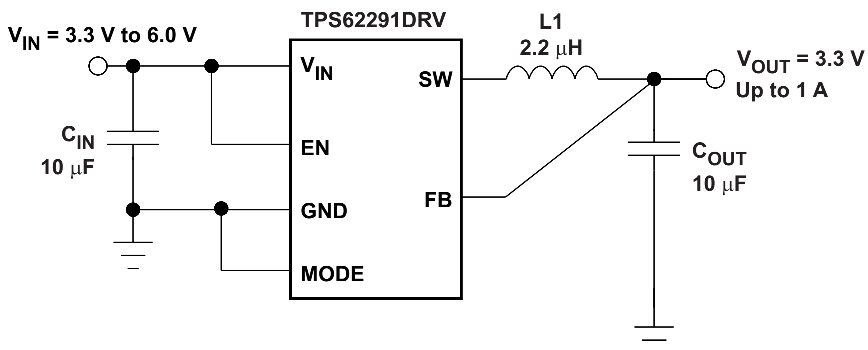


Figure 22. TPS62291DRV Fixed 3.3 V

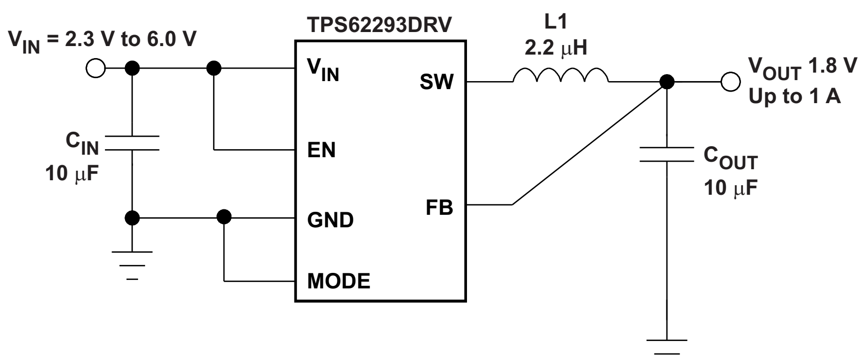


Figure 23. TPS62291DRV Fixed 1.8 V

10 Power Supply Recommendations

The TPS6229x devices have no special requirements for its input power supply. The input power supply's output current needs to be rated according to the supply voltage, output voltage and output current of the TPS6229x.

11 Layout

11.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design. Proper function of the device demands careful attention to PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, stability issues as well as EMI problems. It is critical to provide a low inductance, impedance ground path. Therefore, use wide and short traces for the main current paths. The input capacitor should be placed as close as possible to the IC pins as well as the inductor and output capacitor.

Connect the GND pin of the device to the exposed thermal pad of the PCB and use this pad as a star point. Use a common power GND node and a different node for the signal GND to minimize the effects of ground noise. Connect these ground nodes together to the exposed thermal pad (star point) underneath the IC. Keep the common path to the GND pin, which returns the small signal components and the high current of the output capacitors as short as possible to avoid ground noise. The FB line should be connected right to the output capacitor and routed away from noisy components and traces (for example, SW line).

11.2 Layout Example

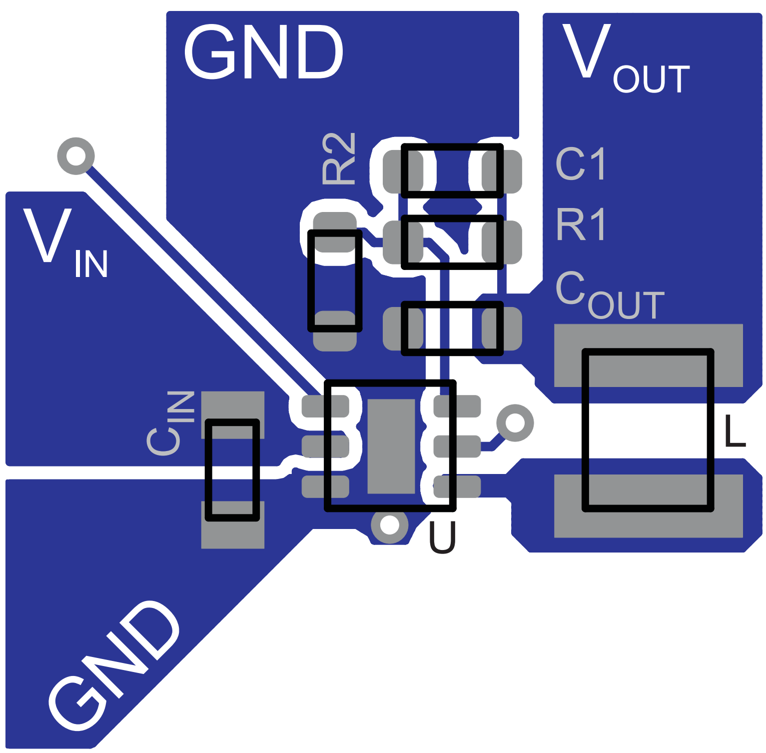


Figure 24. Layout Diagram

12 器件和文档支持

12.1 器件支持

12.1.1 Third-Party Products Disclaimer

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12.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件以及申请样片或购买产品的快速访问链接。

表 **4.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具和软件	支持和社区
TPS62290	单击此处	单击此处	单击此处	单击此处	单击此处
TPS62291	单击此处	单击此处	单击此处	单击此处	单击此处
TPS62293	单击此处	单击此处	单击此处	单击此处	单击此处

12.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.6 术语表

SLYZ022 — *TI* 术语表。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请参阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS62290DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BYN
TPS62290DRVT	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BYN
TPS62291DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-1-260C-UNLIM	-40 to 85	CFY
TPS62291DRVT	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU | NIPDAU	Level-1-260C-UNLIM	-40 to 85	CFY
TPS62293DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-1-260C-UNLIM	-40 to 85	CFD
TPS62293DRVT	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CFD

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS62290, TPS62293 :

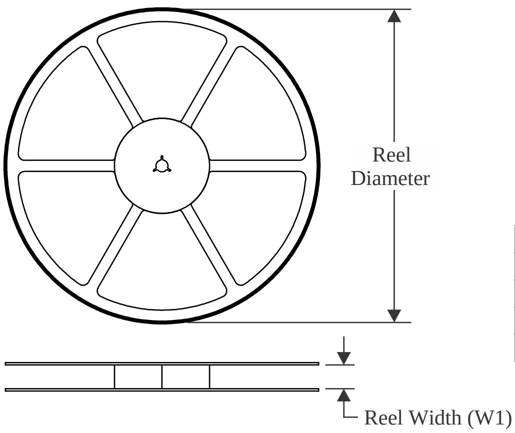
- Automotive : TPS62290-Q1, TPS62293-Q1

NOTE: Qualified Version Definitions:

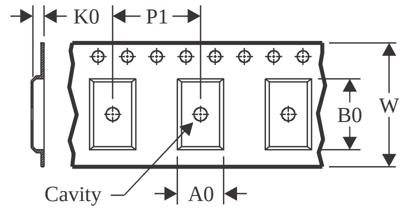
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

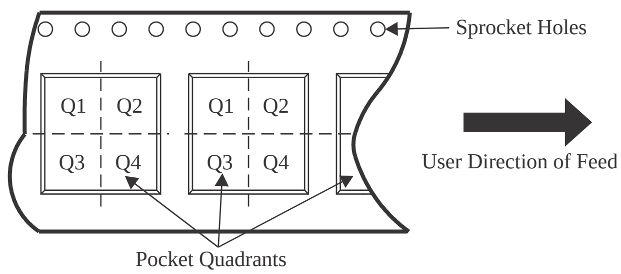


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

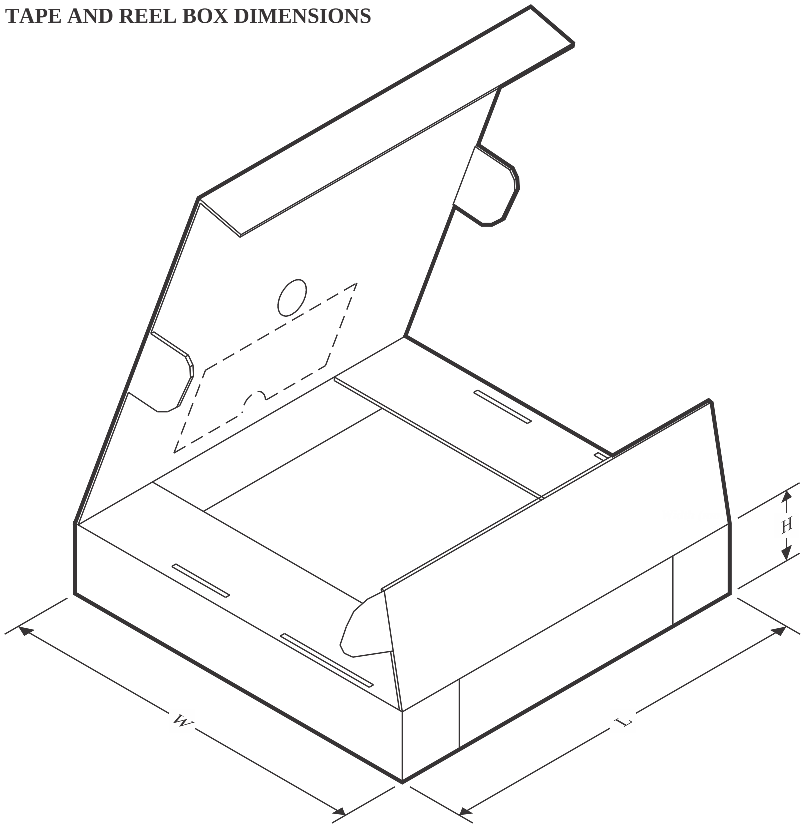
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

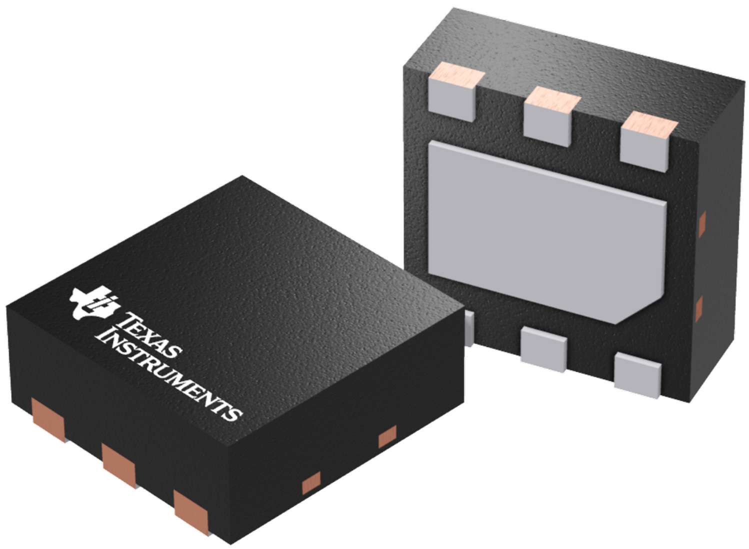
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62290DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62290DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62290DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS62291DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62291DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62293DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62293DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

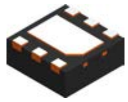


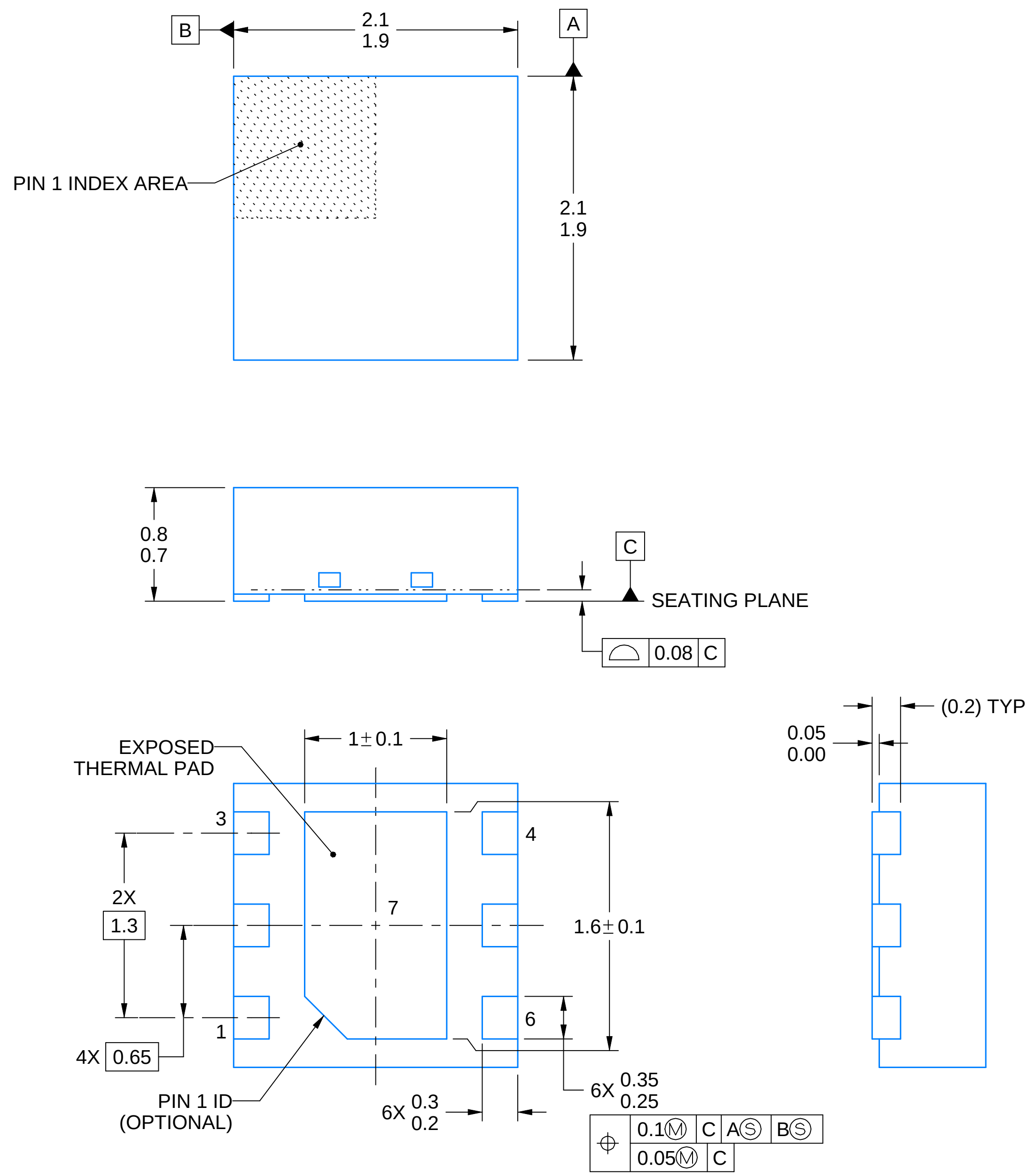
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62290DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TPS62290DRVT	WSON	DRV	6	250	210.0	185.0	35.0
TPS62290DRVT	WSON	DRV	6	250	200.0	183.0	25.0
TPS62291DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TPS62291DRVT	WSON	DRV	6	250	210.0	185.0	35.0
TPS62293DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TPS62293DRVT	WSON	DRV	6	250	200.0	183.0	25.0



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

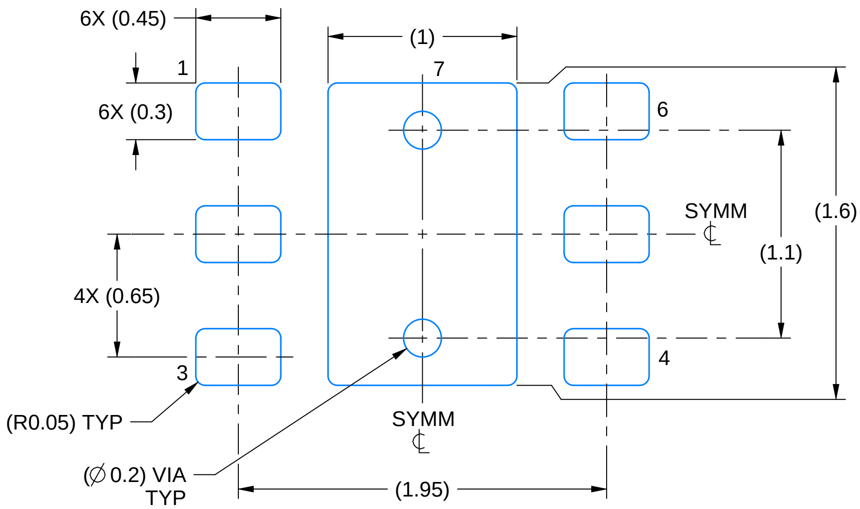




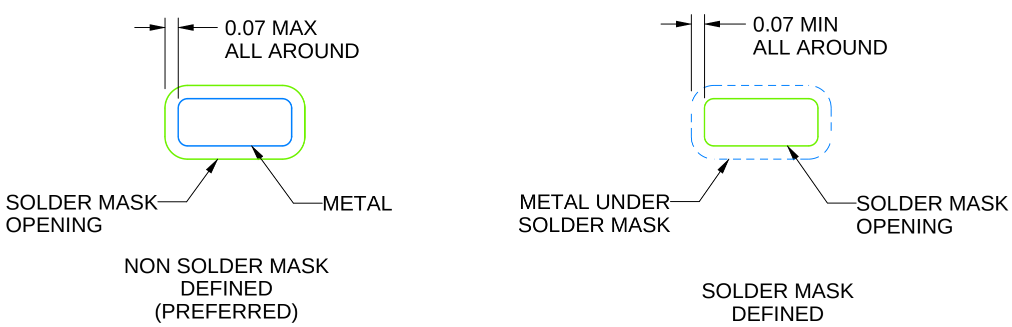
4222173/B 04/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:25X

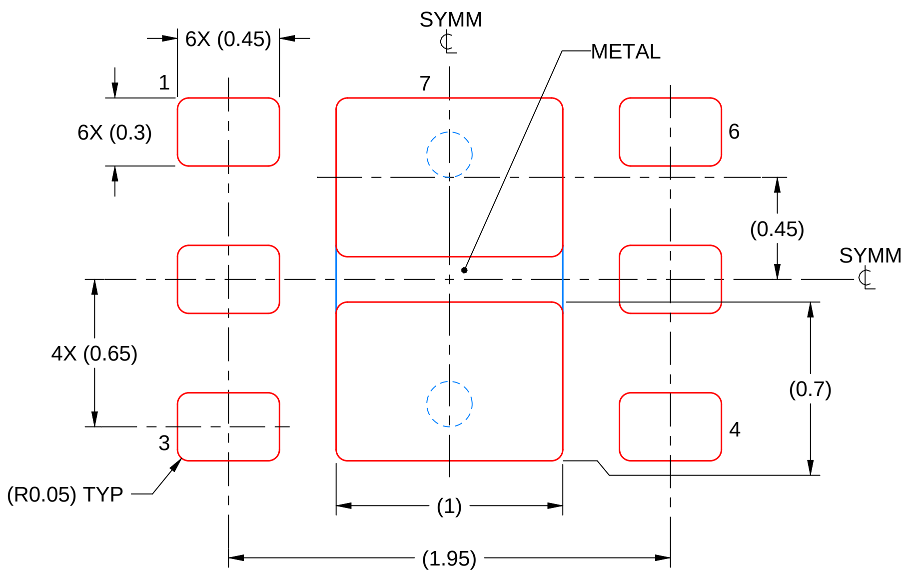


SOLDER MASK DETAILS

4222173/B 04/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



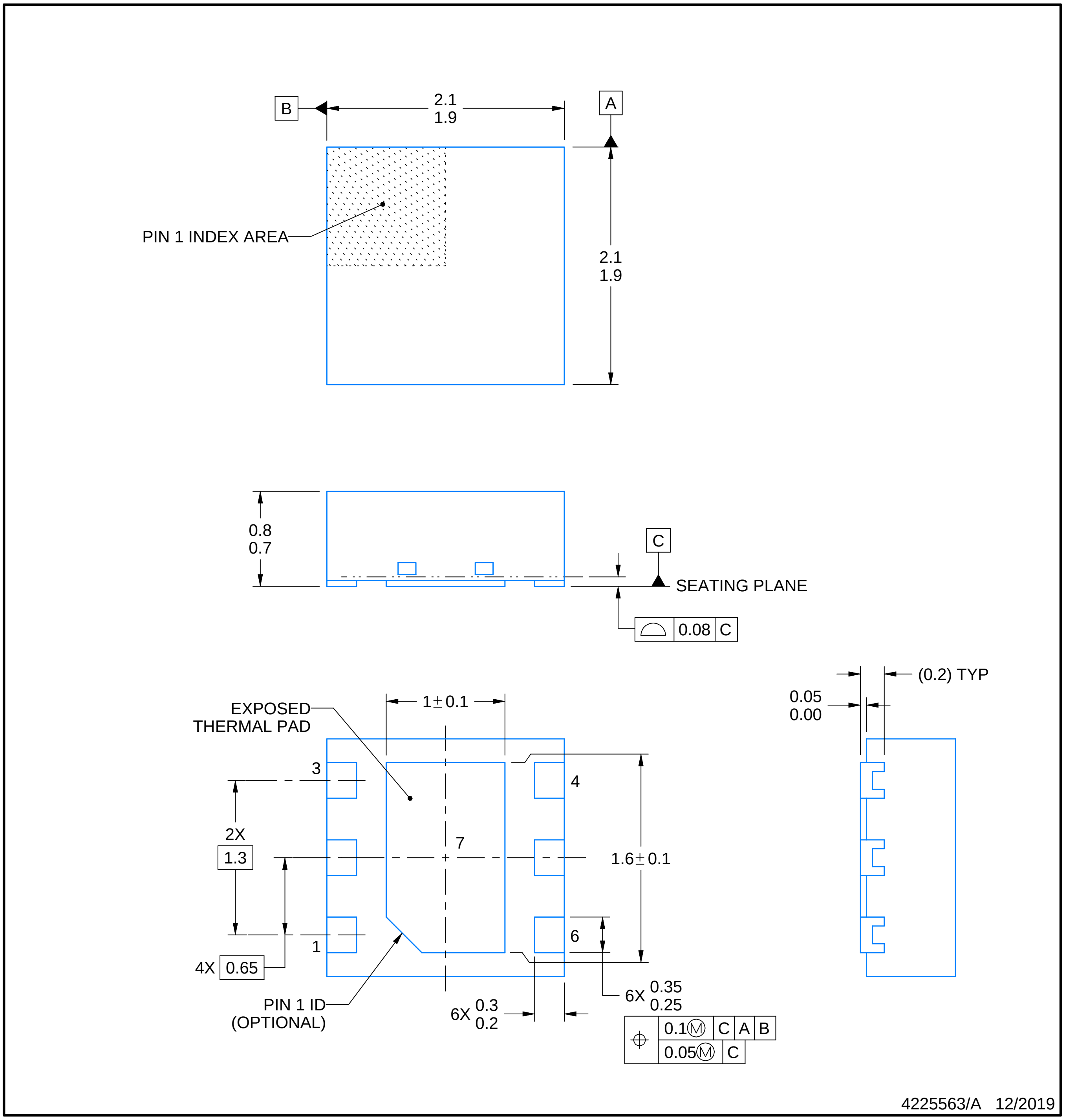
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/B 04/2018

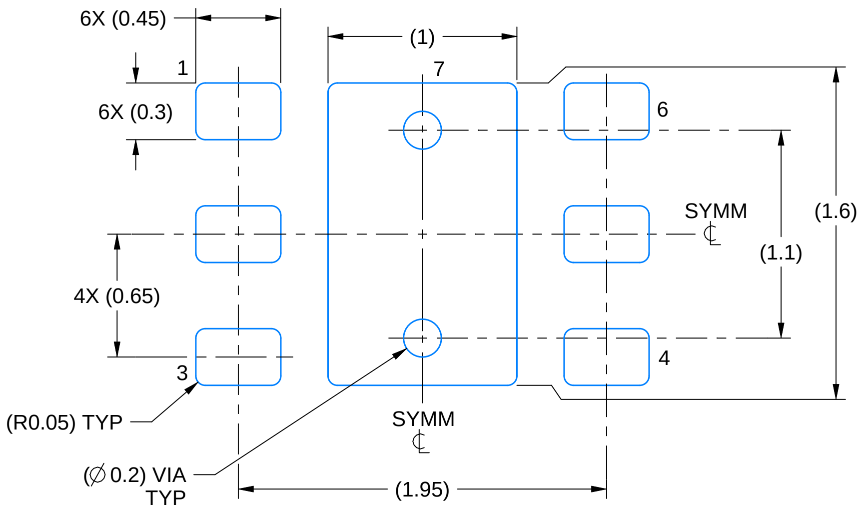
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

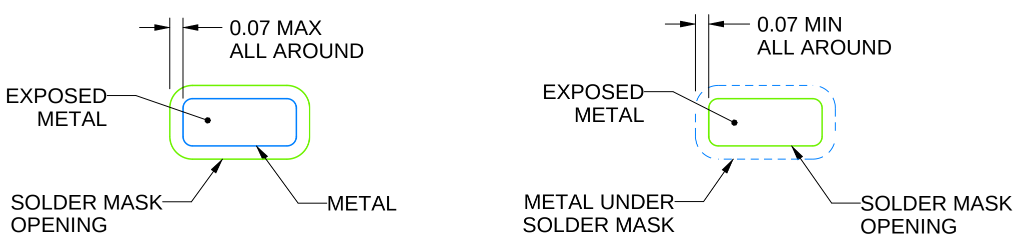


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X



NON SOLDER MASK
DEFINED
(PREFERRED)

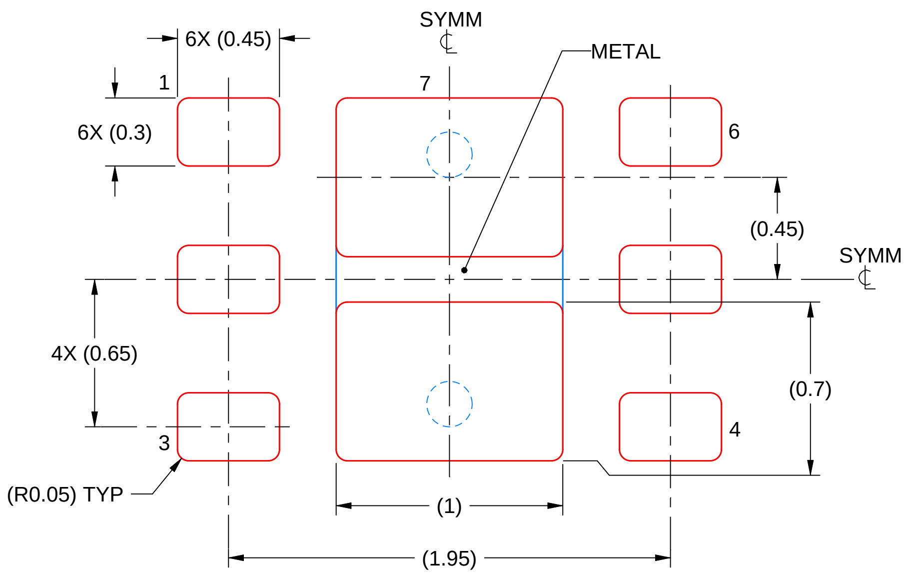
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4225563/A 12/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4225563/A 12/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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