

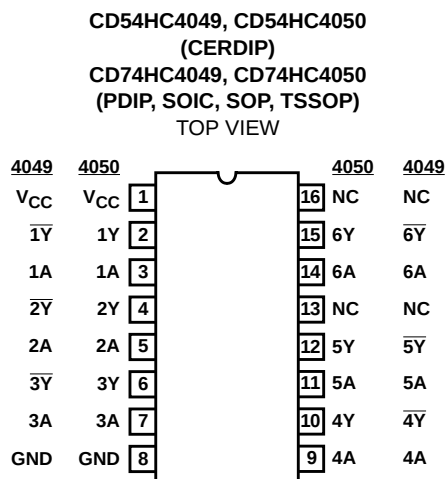
February 1998 - Revised February 2005

High-Speed CMOS Logic Hex Buffers, Inverting and Non-Inverting

Features

- Typical Propagation Delay: 6ns at $V_{CC} = 5V$, $C_L = 15pF$, $T_A = 25^\circ C$
- High-to-Low Voltage Level Converter for up to $V_I = 16V$
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . $-55^\circ C$ to $125^\circ C$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$

Pinout



Description

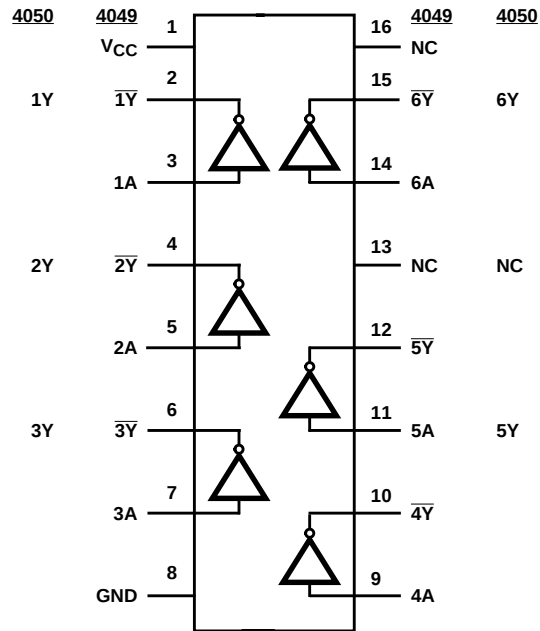
The 'HC4049 and 'HC4050 are fabricated with high-speed silicon gate technology. They have a modified input protection structure that enables these parts to be used as logic level translators which convert high-level logic to a low-level logic while operating off the low-level logic supply. For example, 15-V input pulse levels can be down-converted to 0-V to 5-V logic levels. The modified input protection structure protects the input from negative electrostatic discharge. These parts also can be used as simple buffers or inverters without level translation. The 'HC4049 and 'HC4050 are enhanced versions of equivalent CMOS types.

Ordering Information

PART NUMBER	TEMP. RANGE ($^\circ C$)	PACKAGE
CD54HC4049F3A	-55 to 125	16 Ld CERDIP
CD54HC4050F3A	-55 to 125	16 Ld CERDIP
CD74HC4049E	-55 to 125	16 Ld PDIP
CD74HC4049M	-55 to 125	16 Ld SOIC
CD74HCT4050MT	-55 to 125	16 Ld SOIC
CD74HC4049M96	-55 to 125	16 Ld SOIC
CD74HC4049NSR	-55 to 125	16 Ld SOP
CD74HC4049PW	-55 to 125	16 Ld TSSOP
CD74HC4049PWR	-55 to 125	16 Ld TSSOP
CD74HC4049PWT	-55 to 125	16 Ld TSSOP
CD74HC4050E	-55 to 125	16 Ld PDIP
CD74HC4050M	-55 to 125	16 Ld SOIC
CD74HC4050MT	-55 to 125	16 Ld SOIC
CD74HC4050M96	-55 to 125	16 Ld SOIC
CD74HC4050NSR	-55 to 125	16 Ld SOP
CD74HC4050PW	-55 to 125	16 Ld TSSOP
CD74HC4050PWR	-55 to 125	16 Ld TSSOP
CD74HC4050PWT	-55 to 125	16 Ld TSSOP

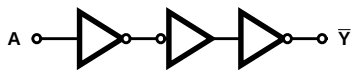
NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

Functional Diagram

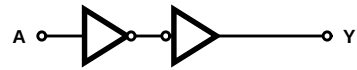


Logic Diagrams

HC4049



HC4050



CD54HC4049, CD74HC4049, CD54HC4050, CD74HC4050

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} -0.5V to 7V
 Input Voltage Range -0.5V to 16V
 DC Input Diode Current, I_{IK}
 For $V_I < -0.5V$ -20mA
 DC Output Diode Current, I_{OK}
 For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ $\pm 20mA$
 DC Output Source or Sink Current per Output Pin, I_O
 For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ $\pm 25mA$
 DC V_{CC} or Ground Current, I_{CC} or I_{GND} $\pm 50mA$

Operating Conditions

Temperature Range (T_A) -55°C to 125°C
 Supply Voltage Range, V_{CC}
 HC Types 2V to 6V
 HCT Types 4.5V to 5.5V
 DC Input Voltage, V_I 0V to 15V
 DC Output Voltage, V_O 0V to V_{CC}
 Input Rise and Fall Time
 2V 1000ns (Max)
 4.5V 500ns (Max)
 6V 400ns (Max)

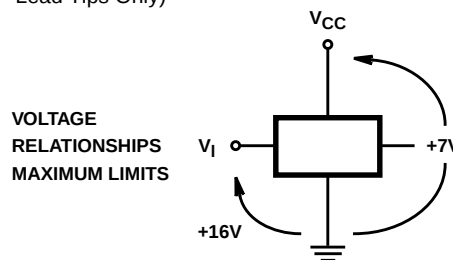
CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

Thermal Information

Package Thermal Impedance, θ_{JA} (see Note 1):
 E (PDIP) Package 67°C/W
 M (SOIC) Package 73°C/W
 NS (SOP) Package 64°C/W
 PW (TSSOP) Package 108°C/W
 Maximum Junction Temperature (Hermetic Package or Die) ... 175°C
 Maximum Junction Temperature (Plastic Package) 150°C
 Maximum Storage Temperature Range -65°C to 150°C
 Maximum Lead Temperature (Soldering 10s) 300°C
 (SOIC - Lead Tips Only)



DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C			−40°C TO 85°C		−55°C TO 125°C		UNITS
		V _I (V)	I _O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
High Level Input Voltage	V _{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V _{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	−0.02	2	1.9	-	-	1.9	-	1.9	-	V
			−0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			−0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			−4	4.5	3.98	-	-	3.84	-	3.7	-	V
			−5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I _I	V _{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	μA
		15	-	6	-	-	±0.5	-	±5	-	±5	

CD54HC4049, CD74HC4049, CD54HC4050, CD74HC4050

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V _I (V)	I _O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Quiescent Device Current	I _{CC}	V _{CC} or GND	0	6	-	-	2	-	20	-	40	μA

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay, nA to nȳ HC4049 nA to nY HC4050	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	85	-	105	-	130	ns
			4.5	-	-	17	-	21	-	26	ns
			6	-	-	14	-	18	-	22	ns
		C _L = 15pF	5	-	6	-	-	-	-	-	ns
Transition Times (Figure 1)	t _{TLH} , t _{THL}	C _L = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	C _I	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 2, 3)	C _{PD}	-	5	-	35	-	-	-	-	-	pF

NOTES:

- C_{PD} is used to determine the dynamic power consumption, per gate.
- P_D = V_{CC}² f_i (C_{PD} + C_L) where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuit and Waveform

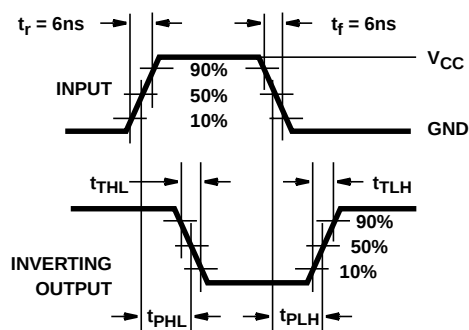


FIGURE 1. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-8681901EA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8681901EA CD54HC4049F3A
5962-8682001EA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8682001EA CD54HC4050F3A
CD54HC4049F3A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8681901EA CD54HC4049F3A
CD54HC4050F3A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8682001EA CD54HC4050F3A
CD74HC4049E	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC4049E
CD74HC4049M	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HC4049M
CD74HC4049M96	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4049M
CD74HC4049MT	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HC4049M
CD74HC4049NS	Obsolete	Production	SOP (NS) 16	-	-	Call TI	Call TI	-	HC4049M
CD74HC4049NSR	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4049M
CD74HC4049PW	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-55 to 125	HJ4049
CD74HC4049PWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4049
CD74HC4050E	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC4050E
CD74HC4050M	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HC4050M
CD74HC4050M96	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4050M
CD74HC4050MT	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HC4050M
CD74HC4050NSR	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4050M
CD74HC4050PW	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-55 to 125	HJ4050
CD74HC4050PWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4050
CD74HC4050PWRG4	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4050
CD74HC4050PWT	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-55 to 125	HJ4050

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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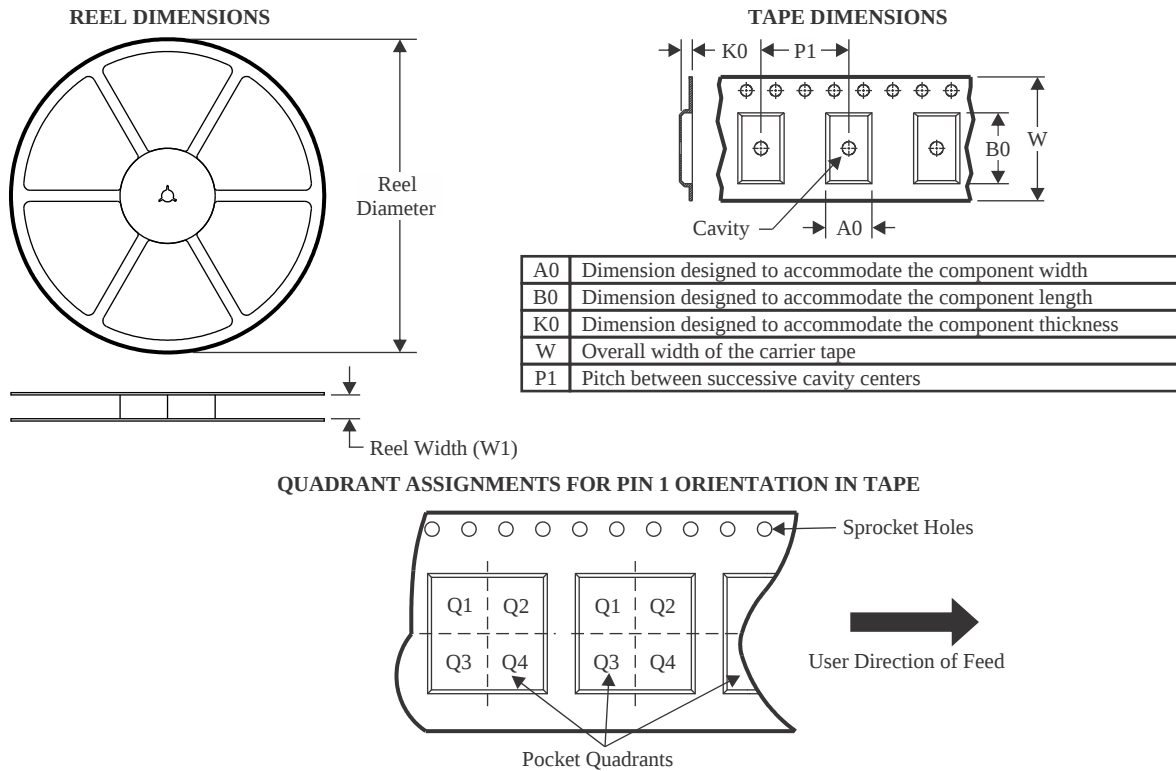
OTHER QUALIFIED VERSIONS OF CD54HC4049, CD54HC4050, CD74HC4049, CD74HC4050 :

- Catalog : [CD74HC4049](#), [CD74HC4050](#)
- Military : [CD54HC4049](#), [CD54HC4050](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4049M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4049NSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD74HC4049PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4050M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4050NSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD74HC4050PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4049M96	SOIC	D	16	2500	353.0	353.0	32.0
CD74HC4049NSR	SOP	NS	16	2000	356.0	356.0	35.0
CD74HC4049PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
CD74HC4050M96	SOIC	D	16	2500	353.0	353.0	32.0
CD74HC4050NSR	SOP	NS	16	2000	356.0	356.0	35.0
CD74HC4050PWR	TSSOP	PW	16	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74HC4049E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4049E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4049EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4049EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4050E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4050E	N	PDIP	16	25	506	13.97	11230	4.32

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