AM26LV31 低压、高速四路差分线路驱动器

1 特性

- 开关频率高达 32MHz
- 由 3.3V 单电源供电运行
- 传播延迟时间：8ns（典型值）
- 脉冲偏移时间：500ps（典型值）
- 高输出驱动电流：±30 mA
- 受控上升和下降时间：3ns（典型值）
- 100Ω 负载时的差分输出电压：1.5V（典型值）
- 超低功耗
  - 直流，0.3mW（最大值）
  - 所有通道 32MHz（空载），385mW（典型值）
- 支持 5V 逻辑输入及 3.3V 电源
- 针对 AM26C31、AM26LS31 和 MB571 的低压引脚对引脚兼容替换产品
- 在断电情况下具有高输出阻抗
- 驱动器输出短路保护电路
- 封装选项包括小巧 (D, NS) 塑料封装

2 应用

- 电机控制：无刷直流和有刷直流
- 现场变送器：温度传感器和压力传感器
- 采用 Modbus 的温度传感器或控制器

3 说明

AM26LV31C 和 AM26LV31I 是具有三态输出的 BiCMOS 四路差分线路驱动器。它们与 TIA/EIA-422-B 和 ITU Recommendation V.11 驱动器类似，但电源电压范围较小。

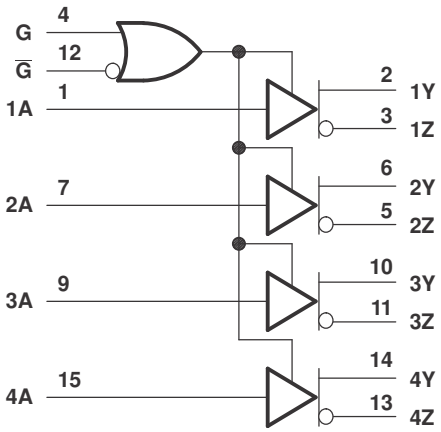
这些器件经过优化，可在高达 32MHz 的开关速率下实现平衡总线传输。输出端可提供非常高的电流，从而驱动双绞线传输线路等平衡线路，并在关断情况下提供高阻抗。四个驱动器均具有使能功能，该功能提供了两种可选输入：有源高电平使能输入和有源低电平使能输入。AM26LV31C 和 AM26LV31I 使用德州仪器 (TI) 专有 LinIMPACT-C60™ 技术进行设计，有助于在不影响速度的情况下实现超低功耗。这些器件会在与 AM26LV32 四路线路接收器配合使用时提供最佳的性能。

AM26LV31C 的额定工作温度范围为 0°C 至 70°C。AM26LV31I 的额定工作温度范围为 -45°C 至 85°C。

封装信息

器件型号	封装(1)	封装尺寸(2)
AM26LV31C	SOIC (D) 16	9.9mm x 6mm
AM26LV31I	SOIC (D) 16	9.9mm x 6mm
	SO (NS) 16	10.2mm x 7.8mm

(1) 有关更多信息，请参阅节 11。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



逻辑图（正逻辑）

Table of Contents

4 Pin Configuration and Functions

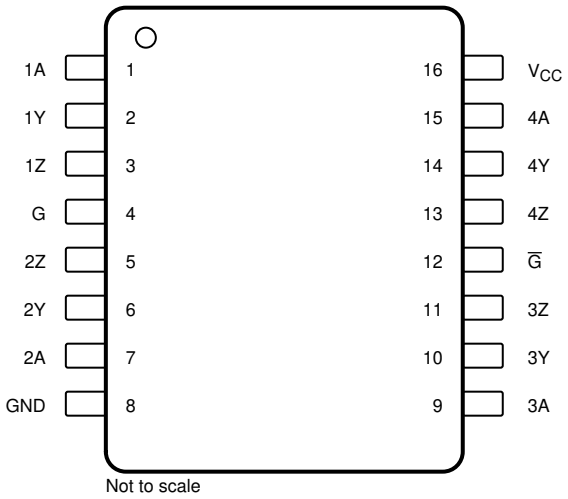


图 4-1. D or NS Package, SOIC 16 Pins (Top View)

表 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	1A	I	Driver 1 input
2	1Y	O	Driver 1 output
3	1Z	O	Driver 1 inverted output
4	G	I	Active high enable
5	2Z	O	Driver 2 inverted output
6	2Y	O	Driver 2 output
7	2A	I	Driver 2 input
8	GND	—	Ground pin
9	3A	I	Driver 3 input
10	3Y	O	Driver 3 output
11	3Z	O	Driver 3 inverted output
12	$\overline{G}$	I	Active low enable
13	4Z	O	Driver 4 inverted output
14	4Y	O	Driver 4 output
15	4A	I	Driver 4 input
16	V_{CC}	—	Power pin

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage range, V_{CC} (2)	–0.3	6	V
Input voltage range, V_I	–0.3	6	V
Output voltage range, V_O	–0.3	6	V
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. .
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				–30	mA
I_{OL}	Low-level output current				30	mA
T_A	Operating free-air temperature	AM26LV31C	0		70	°C
		AM26LV31I	–45		85	°C

5.4 Thermal Information

THERMAL METRIC(1)		D (SOIC) 16 PINS	NS (SO) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.6	88.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.5	46.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.2	50.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.4	13.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.8	50.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over recommended operating supply-voltage and free-air temperature ranges (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = 18mA				–1.5	V
V_{OH}	High-level output voltage	V_{IH} = 2V,	I_{OH} = –12mA	1.85	2.3		V
V_{OL}	Low-level output voltage	V_{IL} = 0.8V,	I_{OH} = 12mA		0.8	1.05	V
$\|V_{OD}\|$	Differential output voltage(2)	R_L = 100Ω		0.95	1.5		V
V_{OC}	Common-mode output voltage			1.3	1.55	1.9	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage(2)					±0.2	V
I_O	Output current with power off	V_O = –0.25V or 6V,	V_{CC} = 0			±100	μA
I_{OZ}	Off-state (high-impedance state) output current	V_O = –0.25V or 6V,	G = 0.8V or $\overline{G}$ = 2V			±100	μA
I_H	High-level input current	V_{CC} = 0 or 3V,	V_I = 5.5V			10	μA
I_L	Low-level input current	V_{CC} = 3.6V,	V_I = 0			–10	μA
I_{OS}	Short-circuit output current	V_{CC} = 3.6V,	V_O = 0			–200	mA
I_{CC}	Supply current (all drivers)	V_I = V_{CC} or GND,	No load			100	μA
C_{pd}	Power-dissipation capacitance (all drivers)(3)	No load			160		pF

(1) All typical values are at V_{CC} = 3.3V, T_A = 25°C.
(2) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
(3) C_{pd} determines the no-load dynamic current consumption. $I_S = C_{pd} \times V_{CC} \times f + I_{CC}$

5.6 Switching Characteristics

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	See 图 6-2		4	8	20	ns
t_{PHL}	Propagation delay time, high- to low-level output			4	8	20	ns
t_t	Transition time (t_r or t_f)				3		ns
SR	Slew rate, single-ended output voltage	See Note (2) and 图 6-2			0.3	1	V/ns
t_{PZH}	Output-enable time to high level	See 图 6-3			10	20	ns
t_{PZL}	Output-enable time to low level	See 图 6-4			10	20	ns
t_{PHZ}	Output-disable time from high level	See 图 6-3			10	20	ns
t_{PLZ}	Output-disable time from low level	See 图 6-4			10	20	ns
$t_{sk(p)}$	Pulse skew	f = 32MHz,	See Note (3)		0.5	3	ns
$t_{sk(o)}$	Skew limit	f = 32MHz				3	ns
$t_{sk(lim)}$	Skew limit (device to device)	f = 32 MHz,	See Note (4)			3	ns

(1) All typical values are at V_{CC} = 3.3V, T_A = 25°C
(2) Slew rate is defined by 方程式 1
(3) Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
(4) Skew limit (device to device) is the maximum difference in propagation delay times between any two channels of any two devices.

$$SR = \frac{90\%\,(V_{OH} - V_{OL}) - 10\%\,(V_{OH} - V_{OL})}{t_f}$$, the differential slew rate of V_{CC} is 2 x SR. (1)

5.7 Typical Characteristics

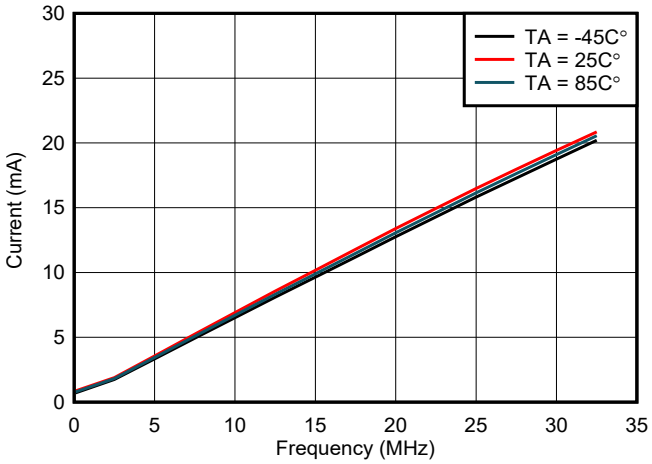


图 5-1. Current vs Frequency

6 Parameter Measurement Information

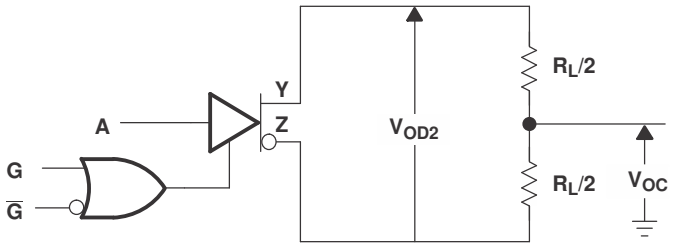
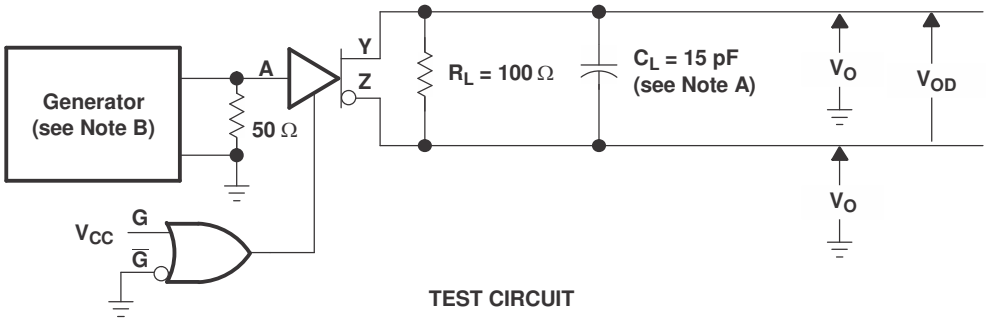
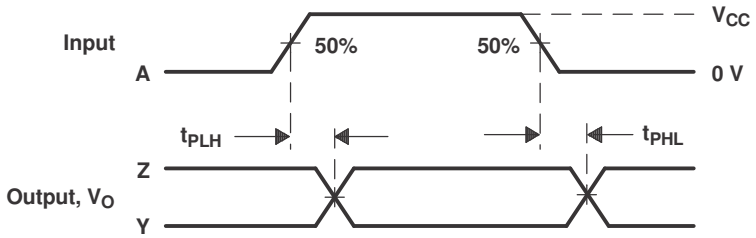


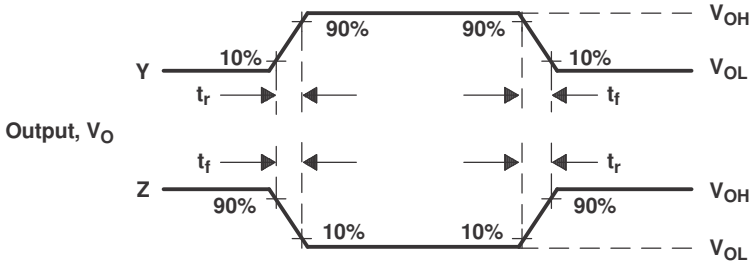
图 6-1. Differential and Common-Mode Output Voltages



TEST CIRCUIT



PROPAGATION DELAY TIMES

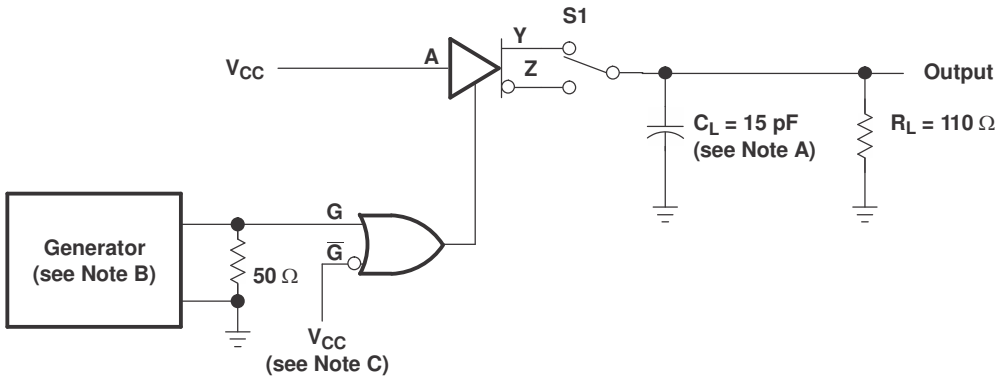


RISE AND FALL TIMES

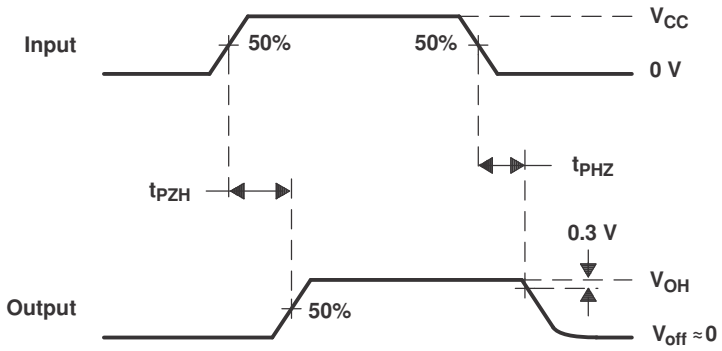
A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR = 10MHz, Z_O = 50 Ω , 50%v duty cycle, t_r and t_f ≤ 10ns.

图 6-2. Test Circuit and Voltage Waveforms, t_{PHL} and t_{PLH}



TEST CIRCUIT



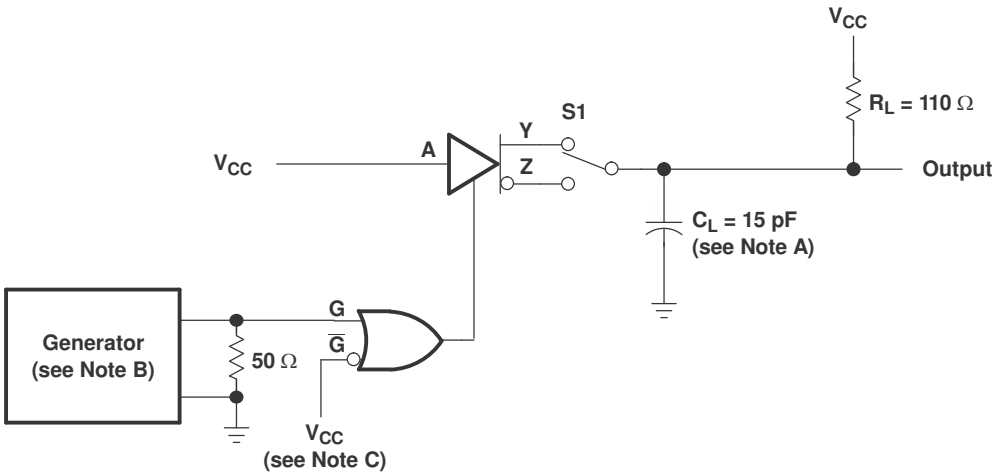
VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

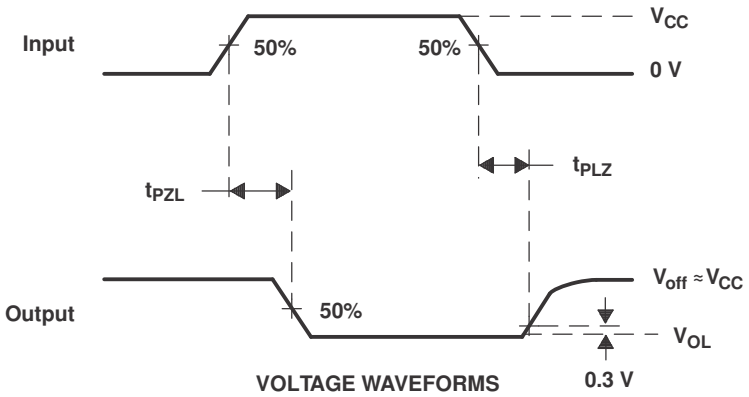
B. The input pulse is supplied by a generator having the following characteristics: PRR = 1MHz, Z_O = 50 Ω, 50%v duty cycle, t_r and t_f (10% to 90%) ⩽ 2ns.

C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform to $\overline{G}$.

图 6-3. Test Circuit and Voltage Waveforms, t_{PZH} and t_{PHZ}



TEST CIRCUIT



VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR = 1MHz, Z_O = 50 Ω, 50%v duty cycle, t_r and t_f (10% to 90%) ≤ 2ns.

C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform to $\overline{G}$.

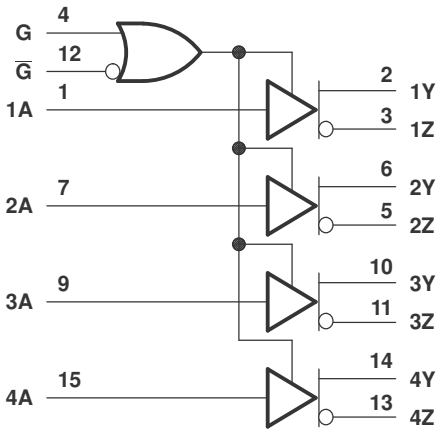
图 6-4. Test Circuit and Voltage Waveforms, t_{PZL} and t_{PLZ}

7 Detailed Description

7.1 Overview

The AM26LV31C and AM26LV31I are BiCMOS quadruple differential line drivers with 3-state outputs. The devices are designed to be similar to TIA/EIA-422-B and ITU Recommendation V.11 drivers with a single 3.3-V power supply. The drivers also integrate active-high and active-low enables for precise device control.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Active high and active low

The devices can be configured using the G and G logic inputs to select transmitter output. A logic high on the G pin or a logic low on the G pin enables the device to operate. These pins are simply a way to configure the logic to match that of the receiving or transmitting controller or microprocessor.

7.3.2 Operates from a 3.3-V Supply with up to 5-V Logic

While the transmitters operate from a single 3.3-V rail, the logic can operate off the same rail or another 5-V rail, making designs much more flexible to communicate to controllers.

7.3.3 High Speed Transmission

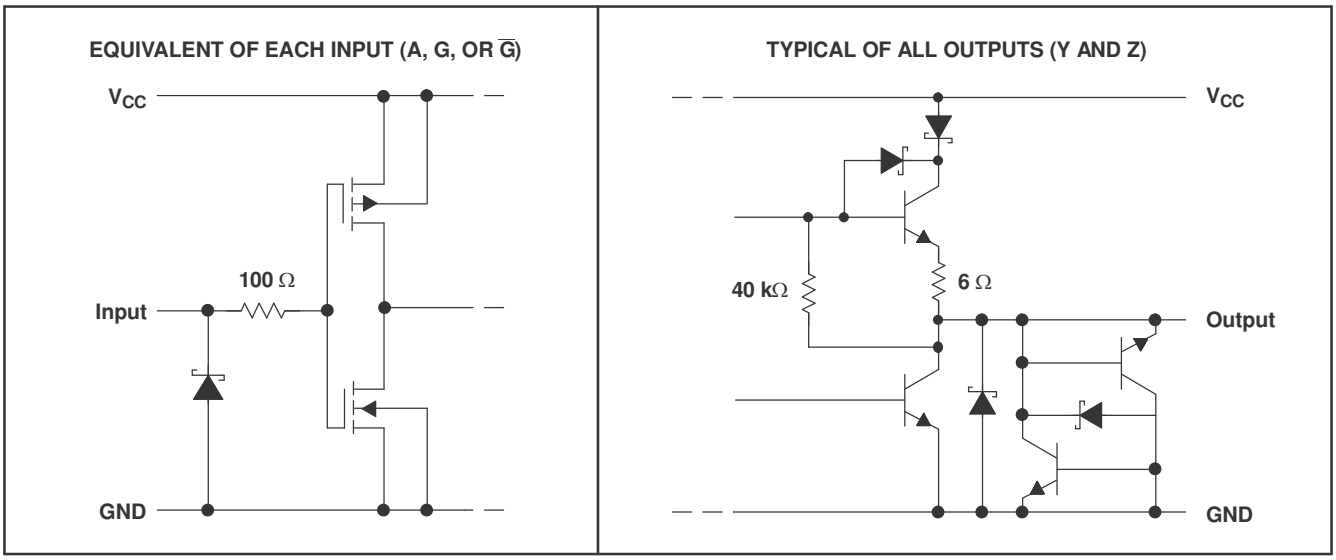
The AM26LV31C and AM26LV31I are optimized for balanced-bus transmission at switching rates up to 32 MHz. The devices are designed using Texas Instruments proprietary LinIMPACT-C60™ technology, facilitating ultra-low power consumption without sacrificing speed.

7.4 Device Functional Modes

表 7-1. Function Table(1)

INPUT A	ENABLES G	ENABLES $\overline{G}$	OUTPUTS Y	OUTPUTS Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)



ll resistor values are nominal.

图 7-1. Schematic (Each Driver)

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

When designing a system that uses drivers, receivers, and transceivers, proper cable termination is essential for highly reliable applications with reduced reflections in the transmission line. If termination is used, it can be placed at the end of the cable near the last receiver. Factors to consider when determining the type of termination usually are performance requirements of the application and the ever-present factor, cost. The different types of termination techniques discussed are unterminated lines, parallel termination, AC termination, and multipoint termination. For laboratory experiments, 100 feet of 100-Ω, 24-AWG, twisted-pair cable (Bertek) was used. A single driver and receiver, TI AM26LV31C and AM26LV32C, respectively, were tested at room temperature with a 3.3-V supply voltage. The first plot shows output waveforms from the driver at the start of the cable (A/B); the second plot shows input waveforms to the receiver at the far end of the cable (Y).

8.2 Typical Application

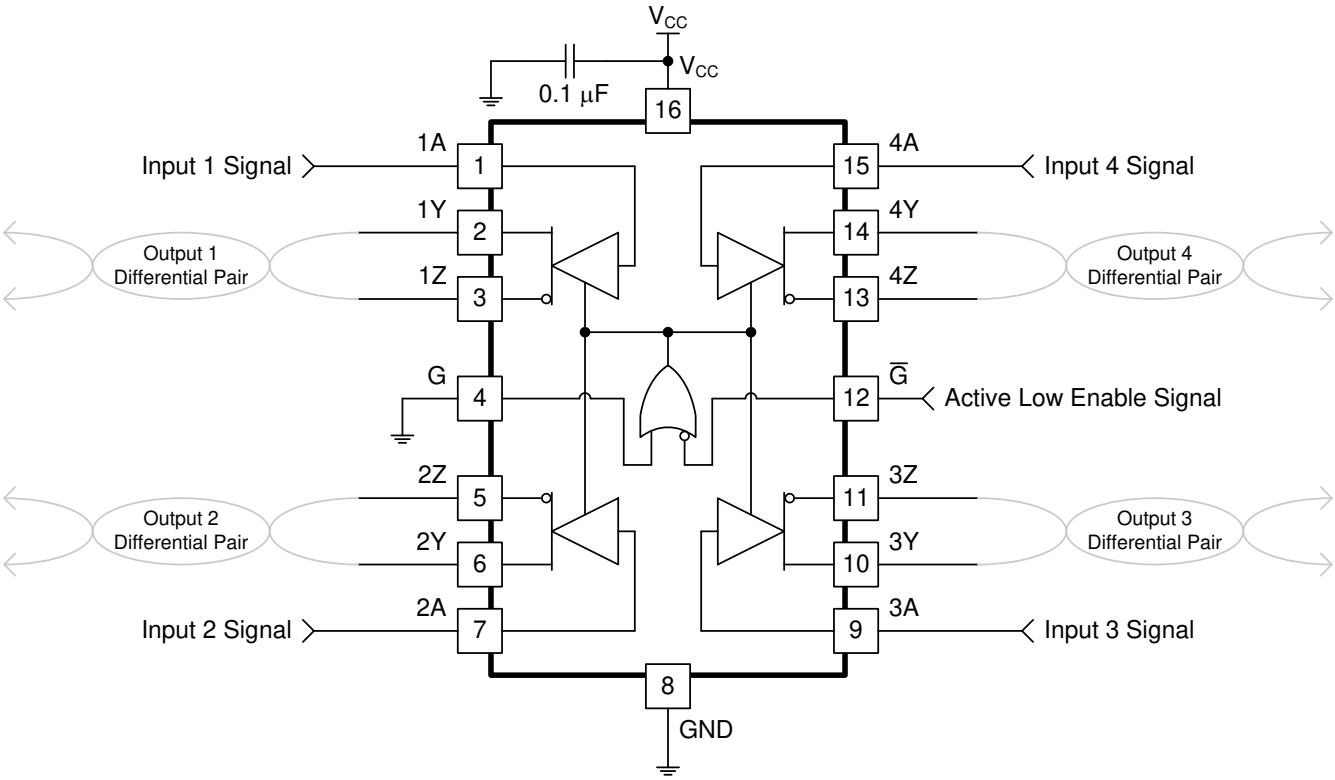


图 8-1. Differential Terminated Configuration With All Channels and Active Low Enable Used

8.2.1 Design Requirements

Resistor and capacitor (if used) termination values are shown for each laboratory experiment, but vary from system to system. For example, the termination resistor, RT, must be within 20% of the characteristic impedance, Zo, of the cable and can vary from about 80 Ω to 120 Ω.

This example requires the following:

- 3.3-V power source
- RS-485 bus operating at 32 MHz or less
- Connector that ensures the correct polarity for port pins

8.2.2 Detailed Design Procedure

Ensure values in Absolute Maximum Ratings are not exceeded. Supply voltage, V_{IH}, and V_{IL} must comply with Recommended Operating Conditions.

Place the device close to bus connector to keep traces (stub) short to prevent adding reflections to the bus line. If desired, add external fail-safe biasing to ensure 200 mV on the A-B port, if the drive is in high impedance state (see Failsafe in RS-485 data buses).

8.2.3 Application Curves

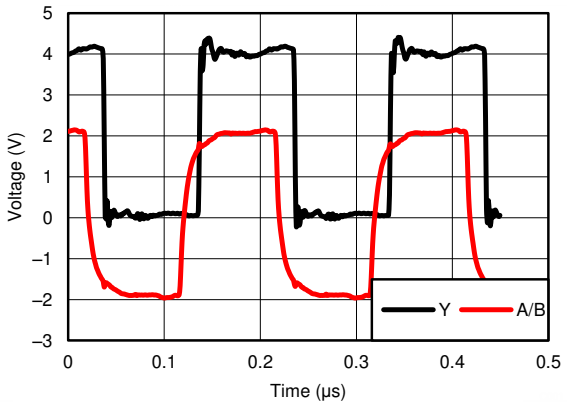


图 8-2. Differential 120-Ω Terminated Output Waveforms (Cat 5E Cable)

8.3 Power Supply Recommendations

Place a 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies.

8.4 Layout

8.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry. Connect low-ESR, 0.1-µF ceramic bypass capacitors between supply pin and ground, placed as close to the device as possible.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.

- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

8.4.2 Layout Example

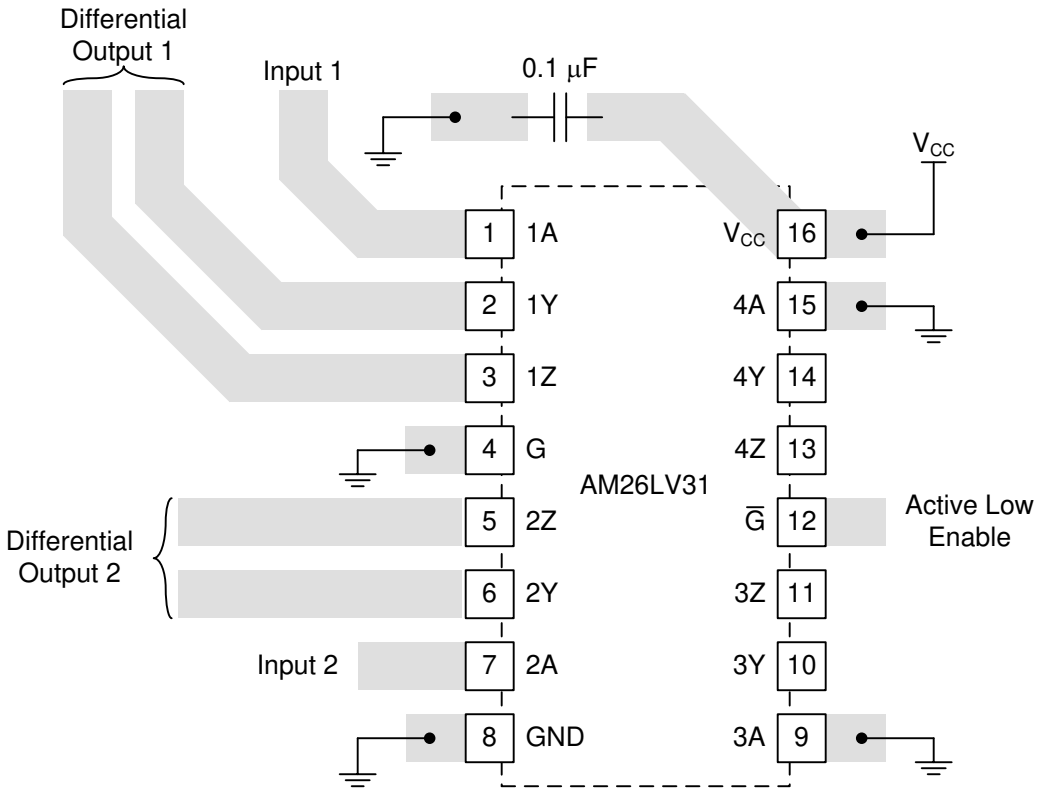


图 8-3. Trace Layout on PCB and Recommendations

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

9.4 Trademarks

LinIMPACT-C60™ is a trademark of Texas Instruments.
TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision H (April 2018) to Revision I (April 2024)	Page
• 将“器件信息”更改为*封装信息* 表	1
• Changed the *Thermal Information* table values	4
• Changed 图 5-1	6
• Changed the Note B in 图 6-2	7

Changes from Revision G (May 2005) to Revision H (April 2018)	Page
• 添加了*器件信息* 表、*ESD 等级* 表、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分	1
• Changed the t_{PLH} and t_{PHL} MAX value From: 12 ns To: 20 ns in the *Switching Characteristics*	5
• Changed the $t_{sk(p)}$ and $t_{sk(o)}$ MAX value From: 1.5 ns To: 3 ns in the *Switching Characteristics*	5

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AM26LV31CD	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	0 to 70	AM26LV31C
AM26LV31CDR	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	0 to 70	AM26LV31C
AM26LV31CDRG4	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	0 to 70	AM26LV31C
AM26LV31CNSR	Obsolete	Production	SOP (NS) | 16	-	-	Call TI	Call TI	0 to 70	26LV31
AM26LV31ID	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-45 to 85	AM26LV31I
AM26LV31IDR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-45 to 85	AM26LV31I
AM26LV31INSR	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-45 to 85	26LV31I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

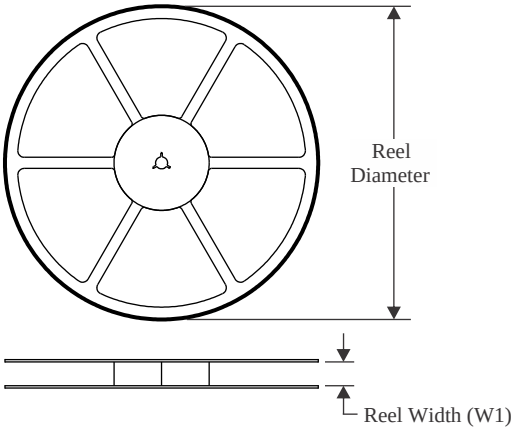
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

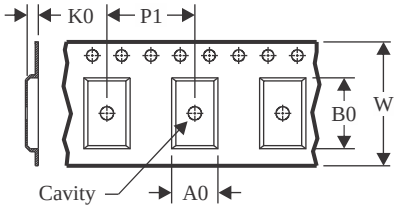
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

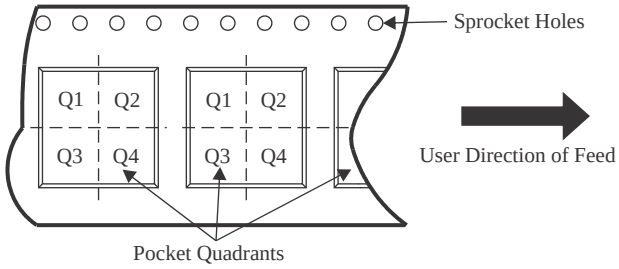


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

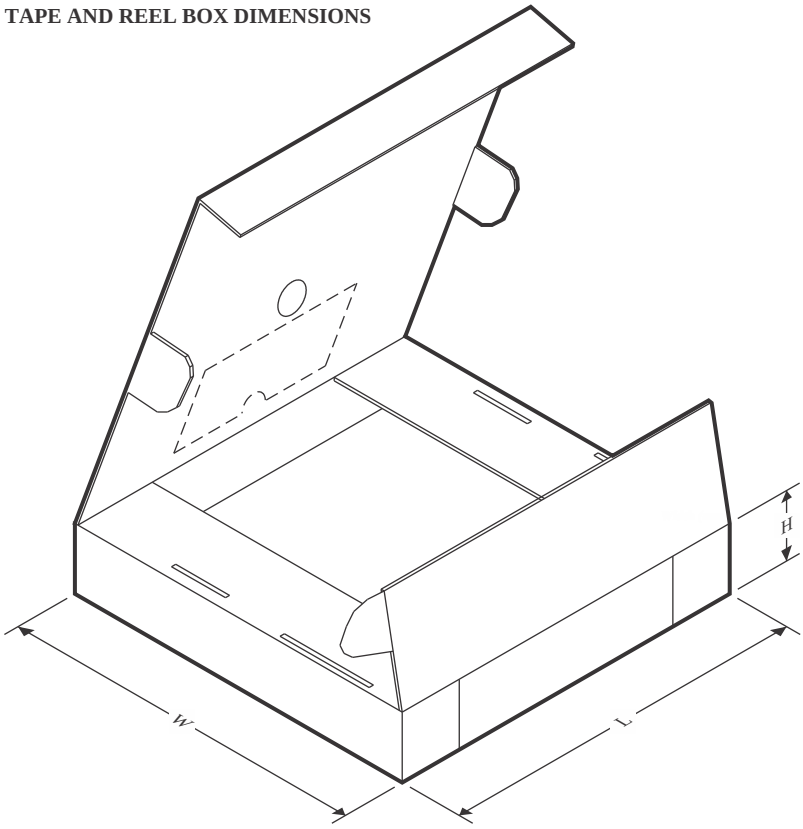
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

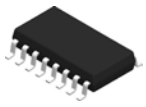
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AM26LV31IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26LV31IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26LV31INSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
AM26LV31INSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AM26LV31IDR	SOIC	D	16	2500	353.0	353.0	32.0
AM26LV31IDR	SOIC	D	16	2500	340.5	336.1	32.0
AM26LV31INSR	SOP	NS	16	2000	353.0	353.0	32.0
AM26LV31INSR	SOP	NS	16	2000	356.0	356.0	35.0

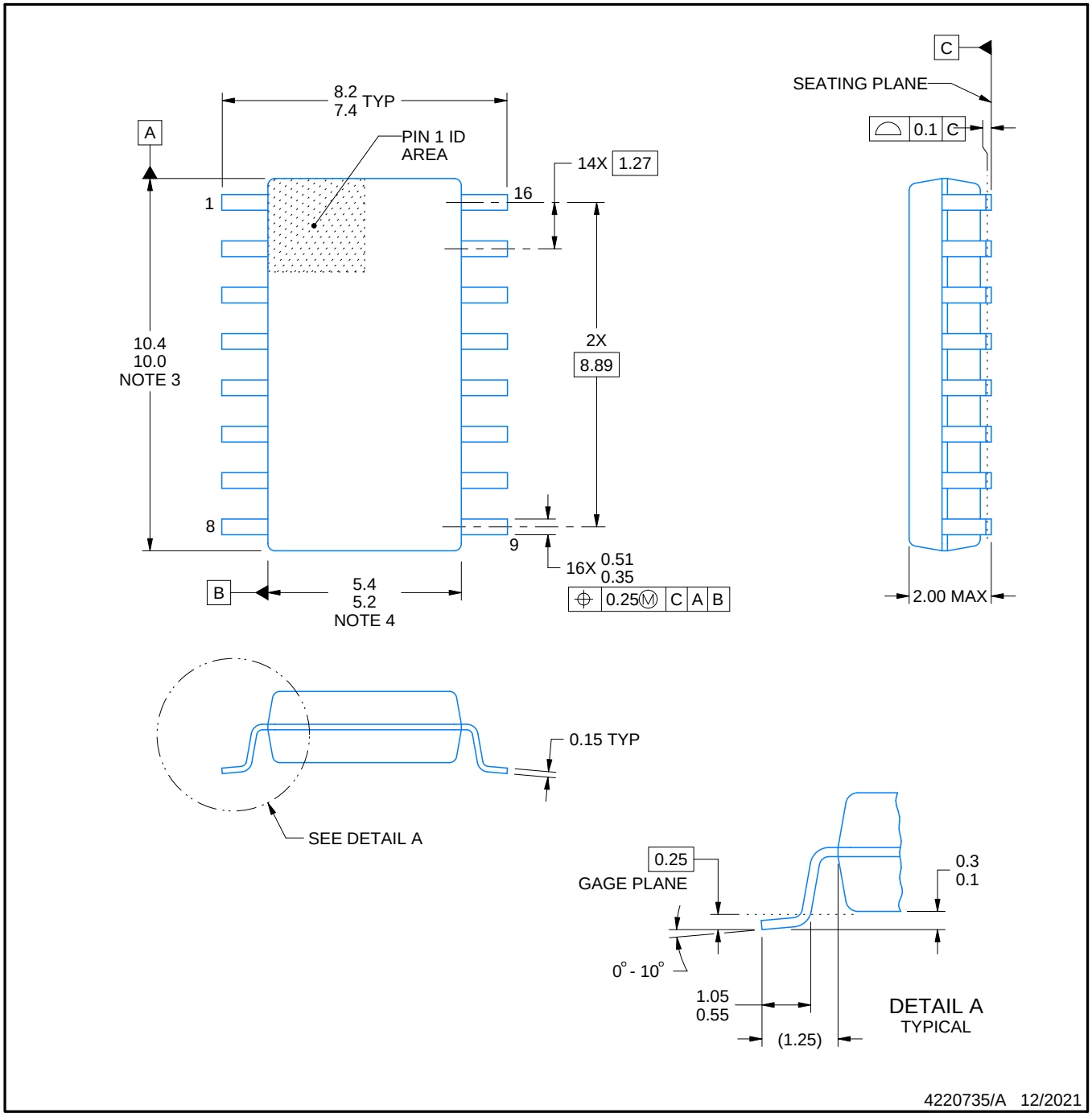


PACKAGE OUTLINE

NS0016A

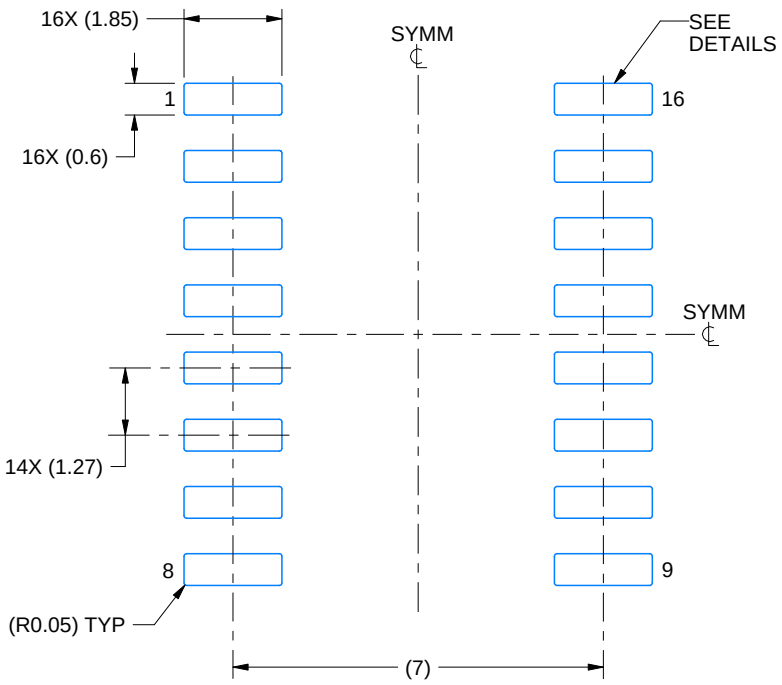
SOP - 2.00 mm max height

SOP

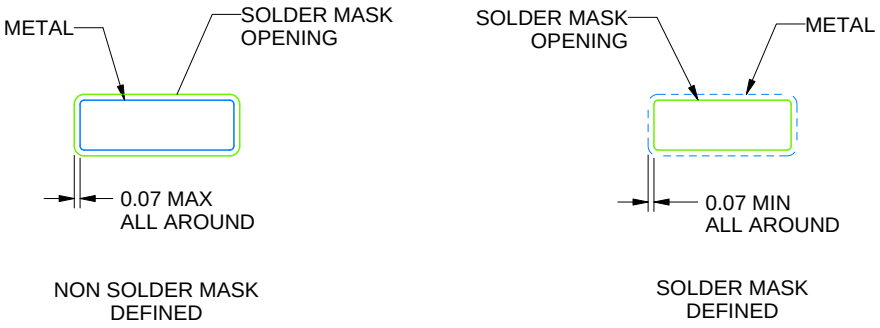


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

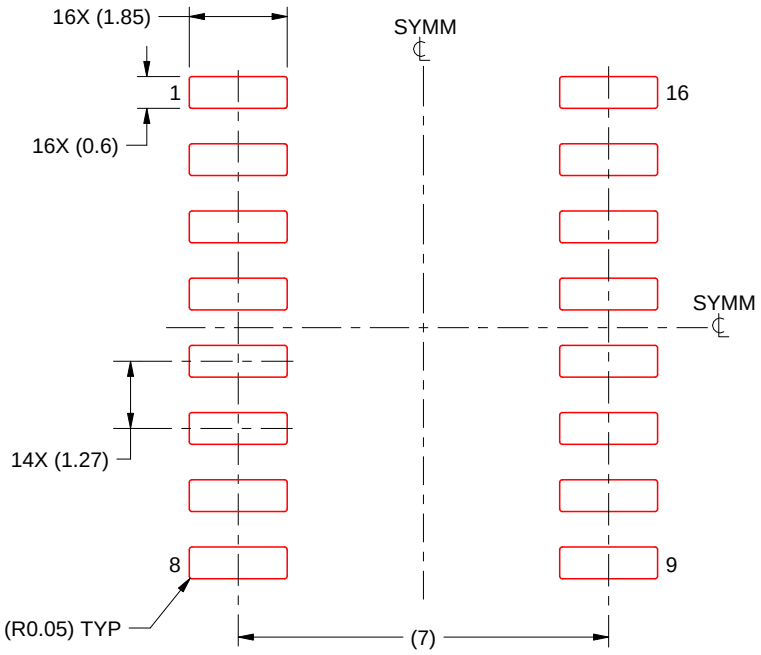
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



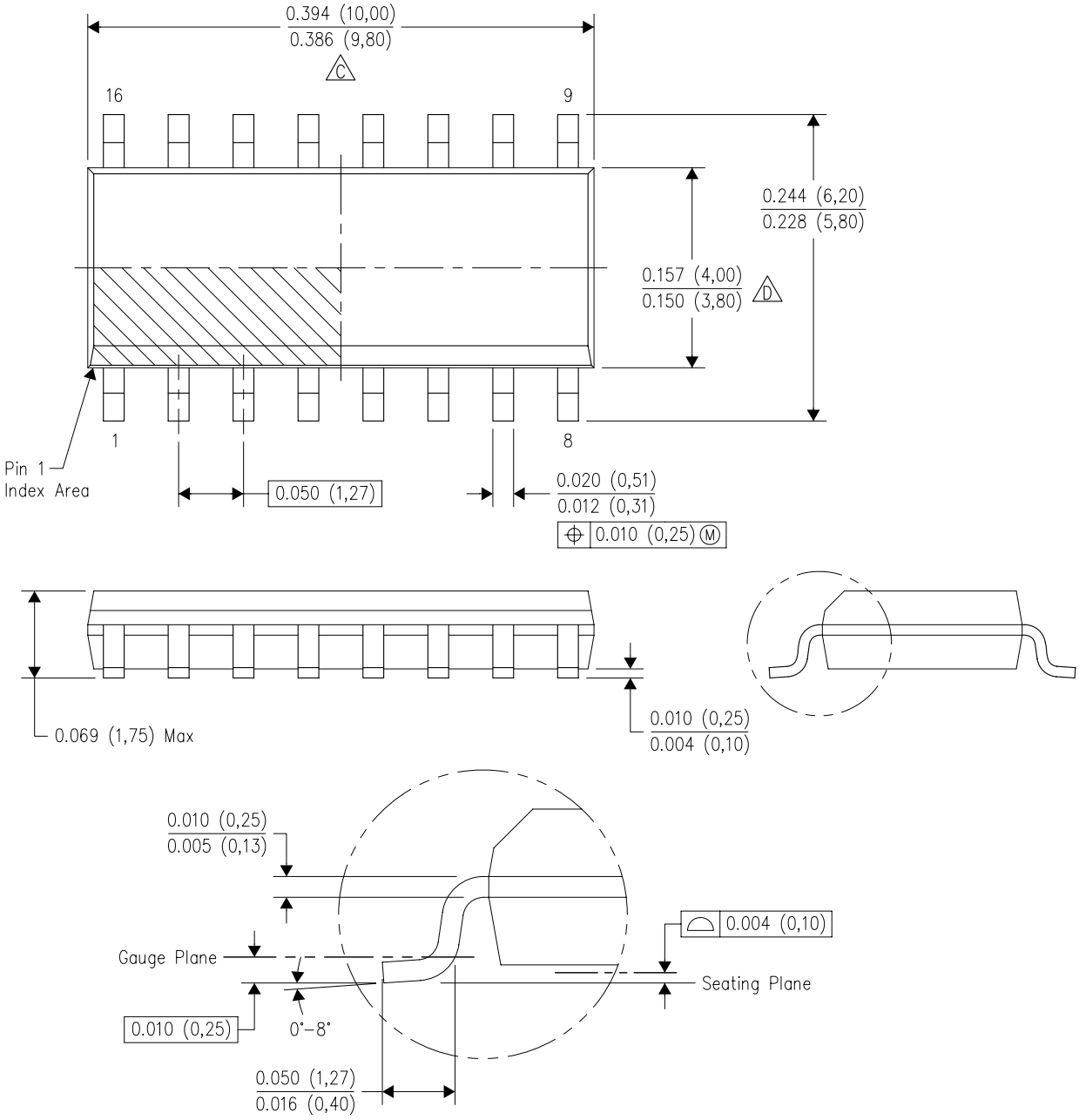
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

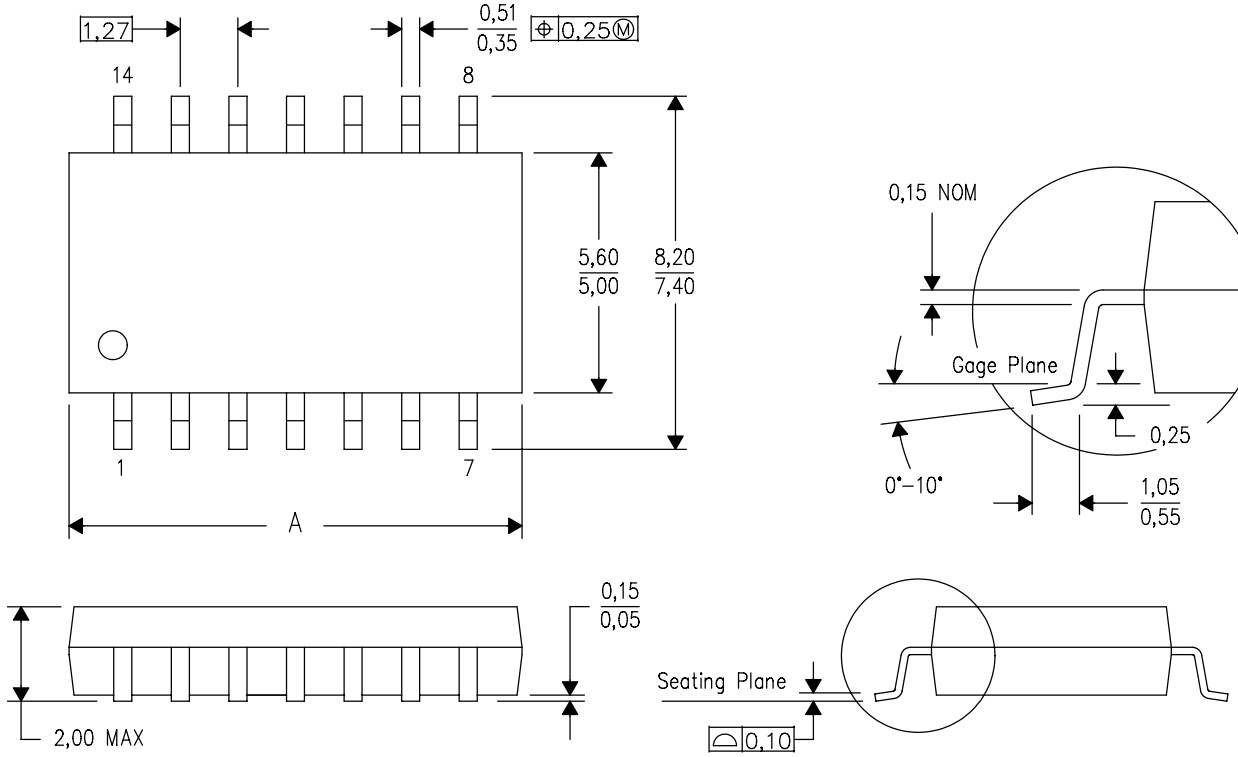


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。 严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265