

SNx4ACT04 六路反相器

1 特性

- V_{CC} 工作范围为 4.5V 至 5.5V
- 输入电压高达 5.5V
- t_{pd} 最大值为 8.5ns (5V 时)
- 输入兼容 TTL 电压

2 应用

- 同步反相时钟输入
- 对开关进行去抖
- 对数字信号进行反相

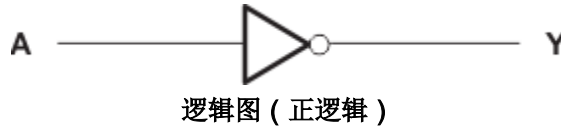
3 说明

‘ACT04 器件包含六个独立的逆变器。这些器件执行布尔函数 $Y = \overline{A}$ 。

器件信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾	本体尺寸 ⁽³⁾
SN54ACT04	J (CDIP, 14)	19.56mm × 7.9mm	19.56mm × 6.67mm
	W (CFP, 14)	9.21mm × 9.02mm	9.21mm × 6.3mm
	FK (LCCC, 20)	8.89mm × 8.89mm	8.89mm × 8.89mm
SN74ACT04	BQA (WQFN, 14)	3mm × 2.5mm	3mm × 2.5mm
	DB (SSOP, 14)	6.2mm × 7.8mm	6.2mm × 5.3mm
	D (SOIC, 14)	8.65mm × 6mm	8.65mm × 3.9mm
	N (PDIP, 14)	19.3mm × 6.35mm	19.3mm × 9.4mm
	NS (SOP, 14)	10.2mm × 7.8mm	10.3mm × 5.3mm
	PW (TSSOP, 14)	5mm × 6.4mm	5mm × 4.4mm

- (1) 有关更多信息，请参阅节 11。
(2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。
(3) 本体尺寸 (长 × 宽) 为标称值，不包括引脚。



逻辑图 (正逻辑)



Table of Contents

1 特性	1	7.2 Feature Description.....	8
2 应用	1	7.3 Device Functional Modes.....	8
3 说明	1	8 应用信息免责声明	9
4 Pin Configuration and Functions	3	8.1 Power Supply Recommendations.....	9
5 Specifications	5	8.2 Layout.....	9
5.1 Absolute Maximum Ratings.....	5	9 Device and Documentation Support	10
5.2 ESD Ratings.....	5	9.1 Documentation Support.....	10
5.3 Recommended Operating Conditions.....	5	9.2 接收文档更新通知.....	10
5.4 Thermal Information.....	5	9.3 支持资源.....	10
5.5 Electrical Characteristics.....	6	9.4 Trademarks.....	10
5.6 Switching Characteristics.....	6	9.5 静电放电警告.....	10
5.7 Operating Characteristics.....	6	9.6 术语表.....	10
6 Parameter Measurement Information	7	10 Revision History	10
7 Detailed Description	8	11 Mechanical, Packaging, and Orderable Information	11
7.1 Functional Block Diagram.....	8		

4 Pin Configuration and Functions

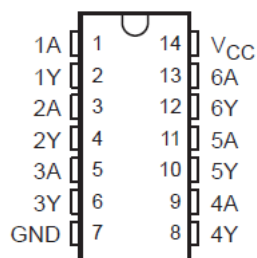


图 4-1. SN54ACT04 J or W Package; SN74ACT04 D, DB, N, NS, or PW Package (Top View)

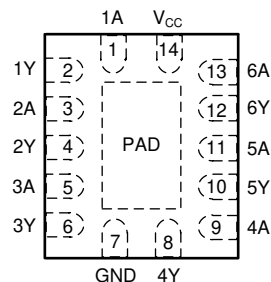


图 4-2. BQA Package, 14-Pin WQFN (Top View)

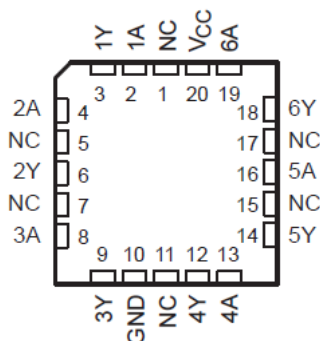


图 4-3. SN54ACT04 FK Package (Top View)

表 4-1. Pin Functions

PIN			I/O ⁽¹⁾	DESCRIPTION
NAME	BQA, D, DB, N, NS, PW, J, or W	FK		
1A	1	2	Input	Channel 1, Input A
1Y	2	3	Output	Channel 1, Output Y
2A	3	4	Input	Channel 2, Input A
2Y	4	6	Output	Channel 2, Output Y
3A	5	8	Input	Channel 3, Input A
3Y	6	9	Output	Channel 3, Output Y
GND	7	10	—	Ground
4Y	8	12	Output	Channel 4, Output Y
4A	9	13	Input	Channel 4, Input A
5Y	10	14	Output	Channel 5, Output Y
5A	11	16	Input	Channel 5, Input A
6Y	12	18	Output	Channel 6, Output Y
6A	13	19	Input	Channel 6, Input A
V _{CC}	14	20	—	Positive Supply

表 4-1. Pin Functions (续)

PIN			I/O ⁽¹⁾	DESCRIPTION
NAME	BQA, D, DB, N, NS, PW, J, or W	FK		
NC		1, 5, 7, 11, 15, 17	—	Not internally connected
Thermal pad			—	Connect the GND pin to the exposed thermal pad for correct operation. Connect the thermal pad to any internal PCB ground plane using multiple vias for good thermal performance.

(1) I = input, O = output, P = power, FB = feedback, GND = ground, N/A = not applicable

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	- 0.5	7	V
V_I	Input voltage range ⁽¹⁾	- 0.5	$V_{CC} + 0.5$	V
V_O	Output voltage range ⁽¹⁾	- 0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$ or $V_I > V_{CC}$		±20 mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20 mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±50 mA
	Continuous current through V_{CC} or GND			±200 mA
T_{stg}	Storage temperature range	- 60	150	°C

(1) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±300

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

		SN54ACT04		SN74ACT04		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		- 24		- 24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		8		8	ns/V
T_A	Operating free-air temperature	- 55	125	- 40	85	°C

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SNx4ACT04						UNIT
		BQA (WQFN)	D (SOIC)	DB (SSOP)	N (PDIP)	NS (SOP)	PW (TSSOP)	
		14 PINS						
R _{θJA}	Junction-to-ambient thermal resistance	85.4	89.9	96	80	76	148	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54ACT04		SN74ACT04		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = - 50 µA	4.5 V	4.4	4.49		4.4		4.4		V
		5.5 V	5.4	5.49		5.4		5.4		
	I _{OH} = - 24 mA	4.5 V	3.86			3.7		3.76		
		5.5 V	4.86			4.7		4.76		
	I _{OH} = - 50 mA ⁽¹⁾	5.5 V				3.85				
	I _{OH} = - 75 mA ⁽¹⁾	5.5 V						3.85		
V _{OL}	I _{OL} = 50 µA	4.5 V		0.001	0.1		0.1		0.1	V
		5.5 V		0.001	0.1		0.1		0.1	
	I _{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I _{OL} = 50 mA ⁽¹⁾	5.5 V					1.65			
	I _{OL} = 75 mA ⁽¹⁾	5.5 V							1.65	
I _I	V _I = V _{CC} or GND	5.5 V			±0.1		±1		±1	µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			2		40		20	µA
ΔI _{CC} ⁽²⁾	One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V		0.6			1.6		1.5	mA
C _i	V _I = V _{CC} or GND	5 V		4.5						pF

(1) Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

(2) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

5.6 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see 图 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			SN54ACT04		SN74ACT04		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	Y	1	6	8.5	1	9	1	9	ns
t _{PHL}			1	5.5	8	1	8.5	1	8.5	

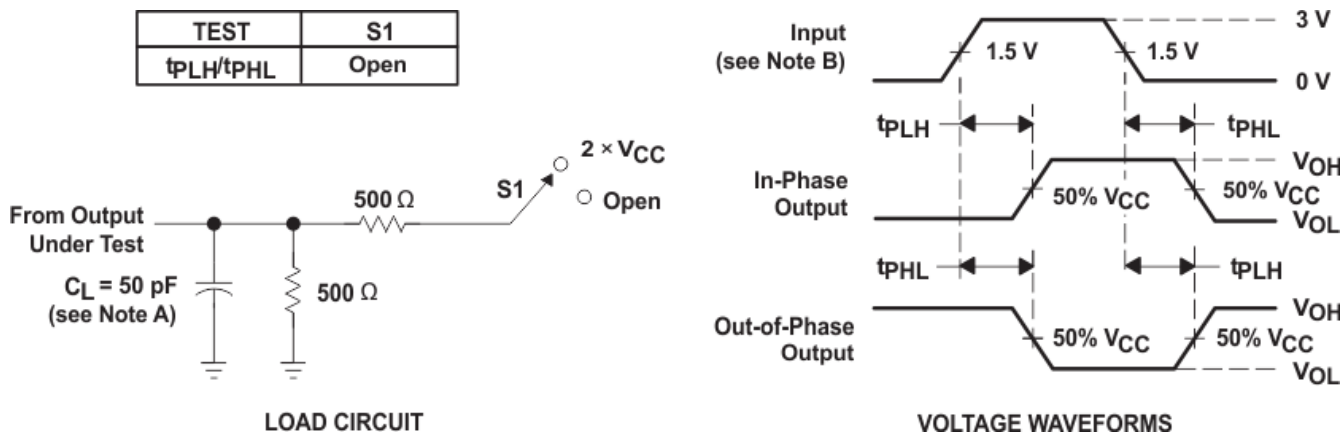
5.7 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C _{pd}	Power dissipation capacitance	C _L = 50 pF	f = 1 MHz	45	pF

6 Parameter Measurement Information

6.1

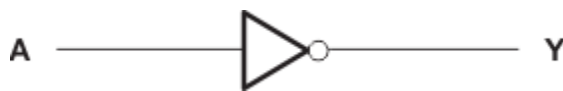


- A. C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\ \text{MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\ \text{ns}$, $t_f \leq 2.5\ \text{ns}$.
- C. The outputs are measured one at a time with one input transition per measurement.

图 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Functional Block Diagram



Logic Diagram (Positive Logic)

7.2 Feature Description

The SNx4ACT04 devices have an operating V_{CC} range from 4.5 V to 5.5 V.

7.3 Device Functional Modes

Function Table lists the function modes of the SNx4ACT04.

Function Table
(Each Inverter)

INPUT	OUTPUT
A	Y
H	L
L	H

8 应用信息免责声明

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [节 5.3](#).

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended; if there are multiple V_{CC} pins, then 0.01 μF or 0.022 μF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and a 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

8.2 Layout

8.2.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. [Layout Diagram](#) specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the IOs, so they cannot float when disabled.

8.2.1.1 Layout Example

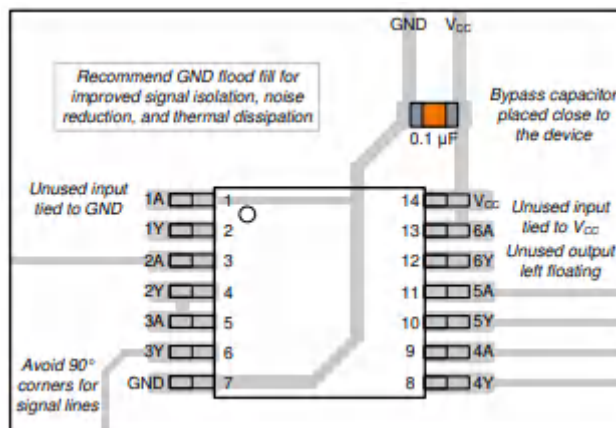


图 8-1. Layout Diagram

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 9-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54ACT04	Click here	Click here	Click here	Click here	Click here
SN74ACT04	Click here	Click here	Click here	Click here	Click here

9.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](#) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的[使用条款](#)。

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

9.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision E (August 2024) to Revision F (November 2024) Page

- 向 **器件信息** 表、**引脚配置和功能** 部分以及 **热性能信息** 表中添加了 BQA 封装..... **1**
- 向 **器件信息** 表中添加了 J、W 和 FK 封装..... **1**

Changes from Revision D (January 2023) to Revision E (August 2024) Page

- 向 **器件信息** 表中添加了封装尺寸和 N 封装信息..... **1**
- Updated R_{θJA} values: D = 86 to 89.9, PW = 113 to 148, all values in °C/W..... **5**

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-89734012A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 89734012A SNJ54ACT 04FK
5962-8973401CA	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8973401CA SNJ54ACT04J
5962-8973401DA	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8973401DA SNJ54ACT04W
5962-8973401VCA	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8973401VC A SNV54ACT04J
5962-8973401VDA	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8973401VD A SNV54ACT04W
SN74ACT04BQAR	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AD04
SN74ACT04D	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	-40 to 85	ACT04
SN74ACT04DBR	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD04
SN74ACT04DR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT04
SN74ACT04N	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74ACT04N
SN74ACT04NSR	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT04
SN74ACT04PW	Obsolete	Production	TSSOP (PW) 14	-	-	Call TI	Call TI	-40 to 85	AD04
SN74ACT04PWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	AD04
SN74ACT04PWR1G4	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD04
SNJ54ACT04FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 89734012A SNJ54ACT 04FK
SNJ54ACT04J	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8973401CA SNJ54ACT04J
SNJ54ACT04W	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8973401DA SNJ54ACT04W

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54ACT04, SN54ACT04-SP, SN74ACT04 :

- Catalog : [SN74ACT04](#), [SN54ACT04](#)
- Automotive : [SN74ACT04-Q1](#), [SN74ACT04-Q1](#)
- Enhanced Product : [SN74ACT04-EP](#), [SN74ACT04-EP](#)
- Military : [SN54ACT04](#)
- Space : [SN54ACT04-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

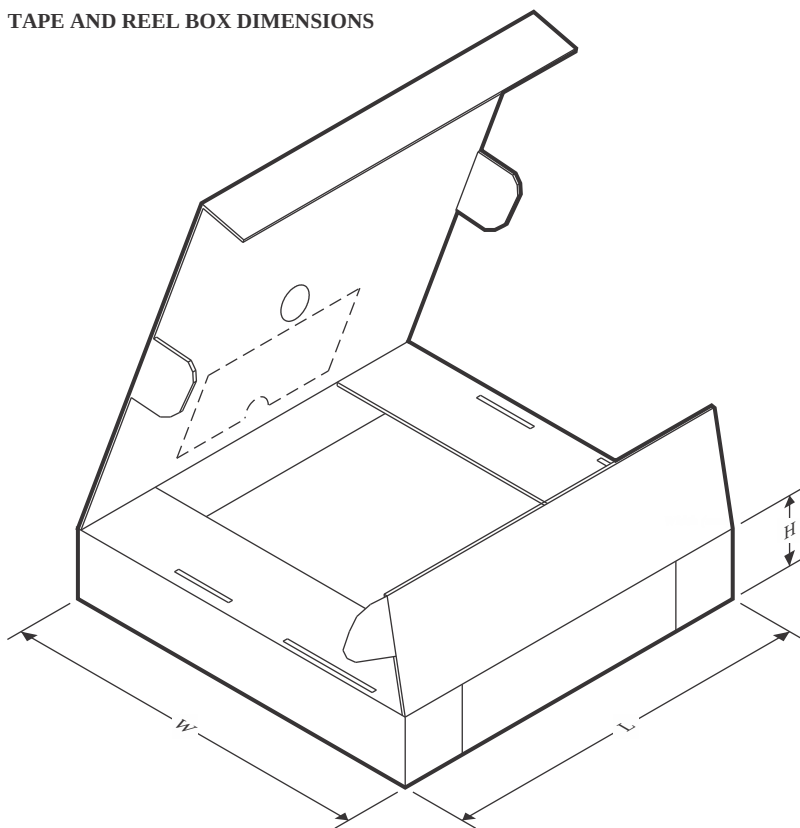
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ACT04BQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74ACT04DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74ACT04DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74ACT04DR	SOIC	D	14	2500	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
SN74ACT04DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74ACT04DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74ACT04NSR	SOP	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74ACT04PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74ACT04PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74ACT04PWR1G4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74ACT04PWR1G4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ACT04BQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74ACT04DBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74ACT04DR	SOIC	D	14	2500	356.0	356.0	35.0
SN74ACT04DR	SOIC	D	14	2500	340.5	336.1	32.0
SN74ACT04DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74ACT04DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74ACT04NSR	SOP	NS	14	2000	356.0	356.0	35.0
SN74ACT04PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74ACT04PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74ACT04PWR1G4	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74ACT04PWR1G4	TSSOP	PW	14	2000	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-89734012A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-8973401DA	W	CFP	14	25	506.98	26.16	6220	NA
5962-8973401VDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74ACT04N	N	PDIP	14	25	506	13.97	11230	4.32
SN74ACT04N	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54ACT04FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ACT04W	W	CFP	14	25	506.98	26.16	6220	NA

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

BQA 14

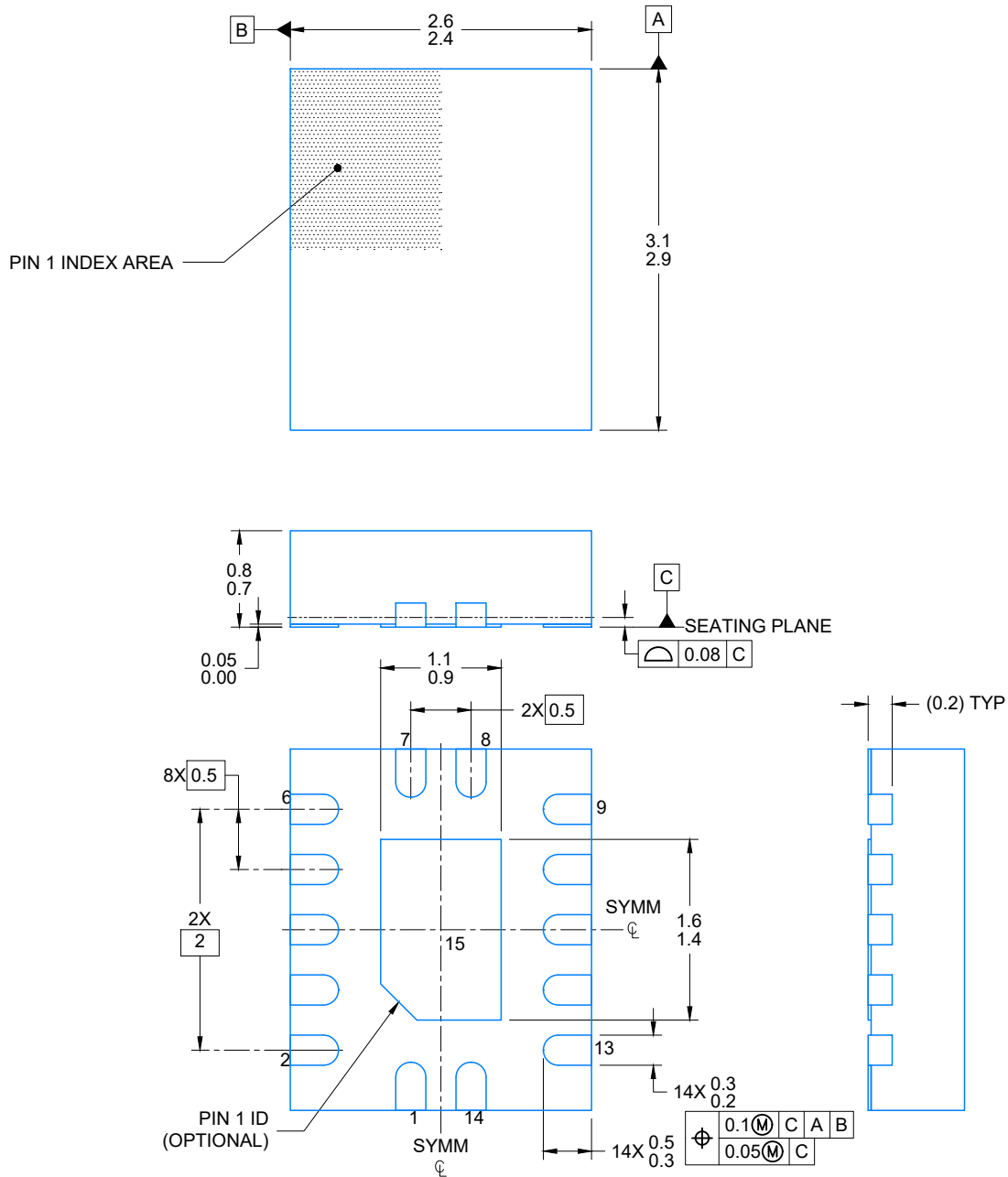
WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.





4224636/A 11/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
 88% PRINTED COVERAGE BY AREA
 SCALE: 20X

4224636/A 11/2018

NOTES: (continued)

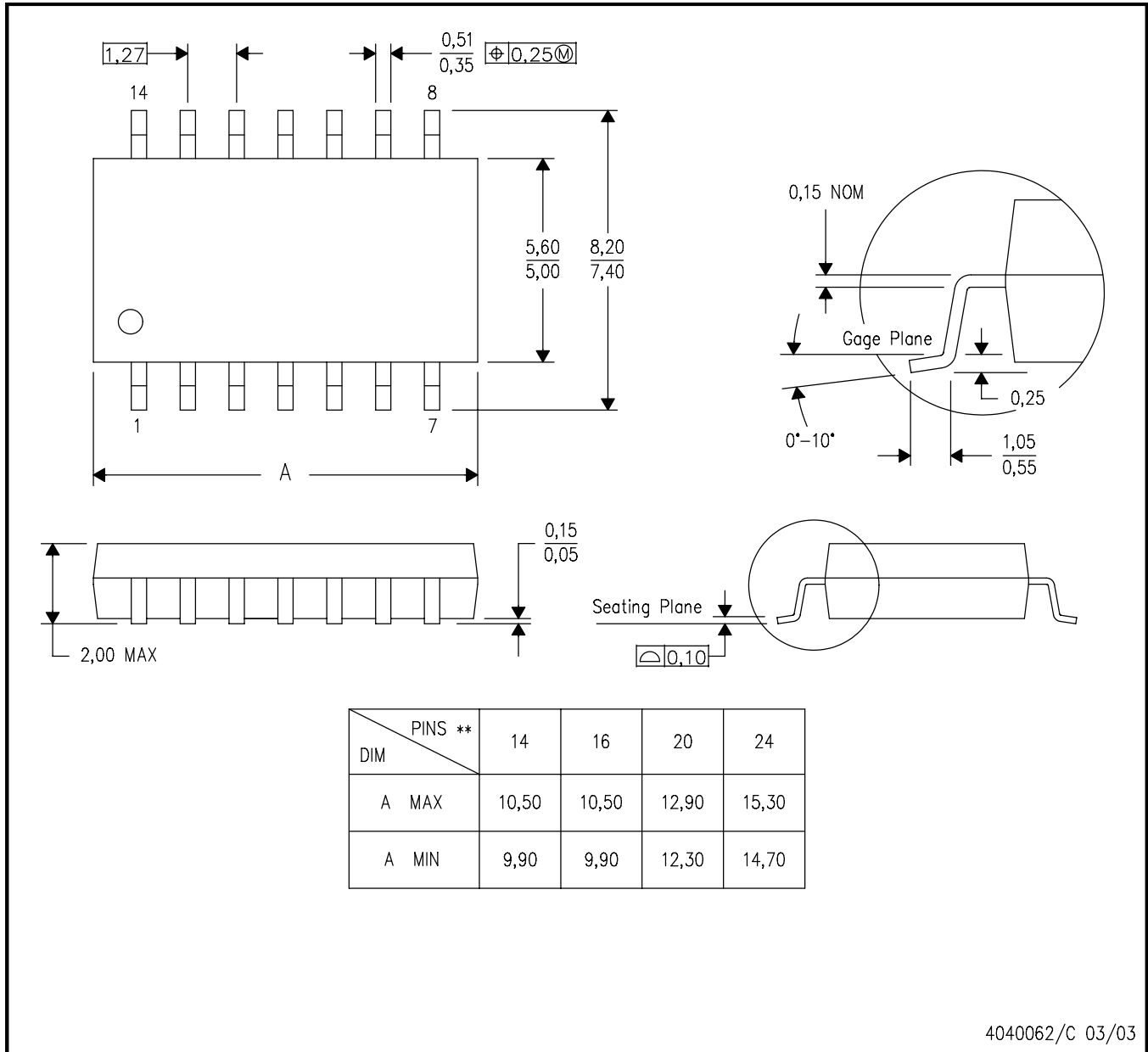
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK





4220762/A 05/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

J 14

GENERIC PACKAGE VIEW

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

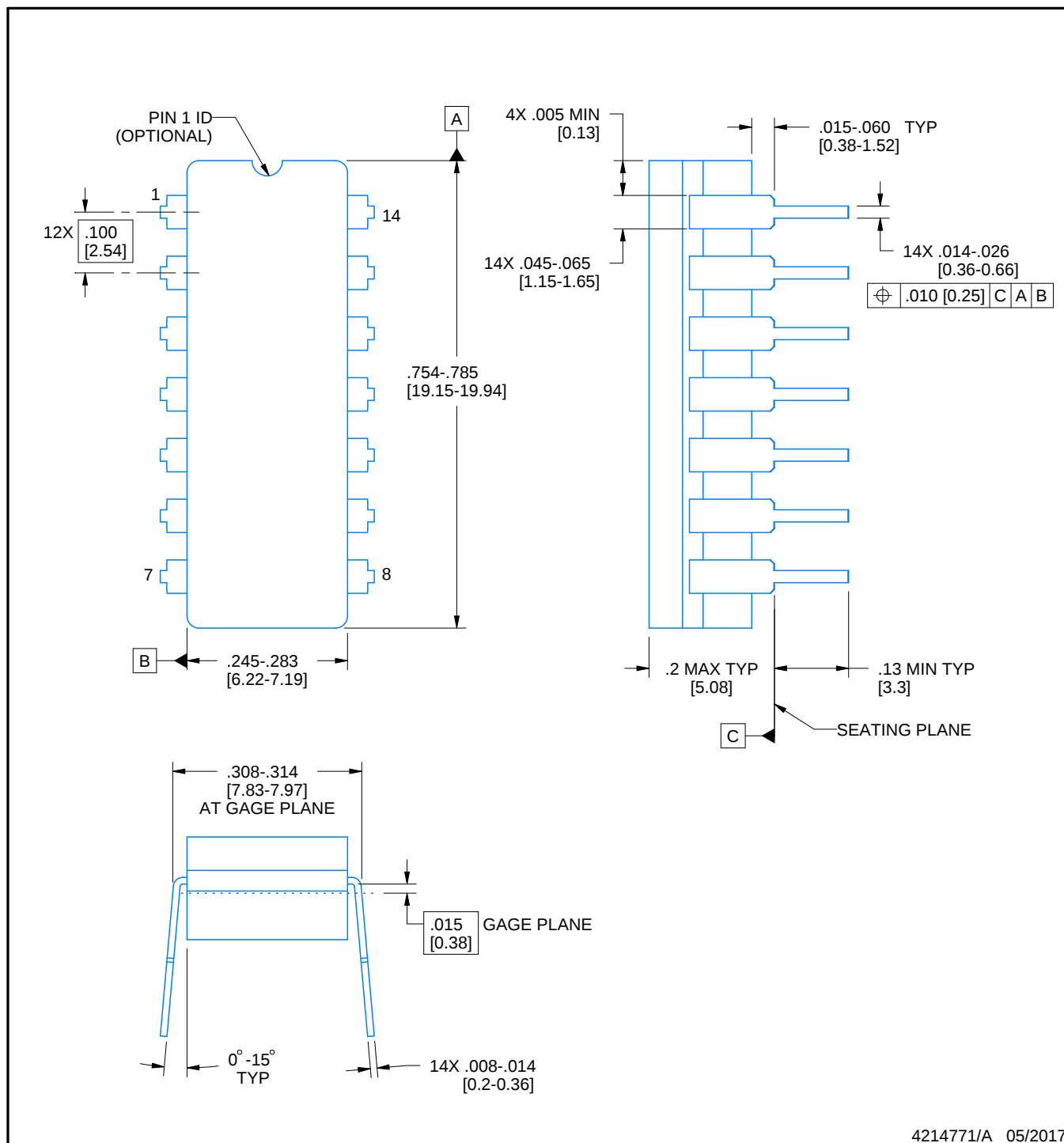


J0014A

PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

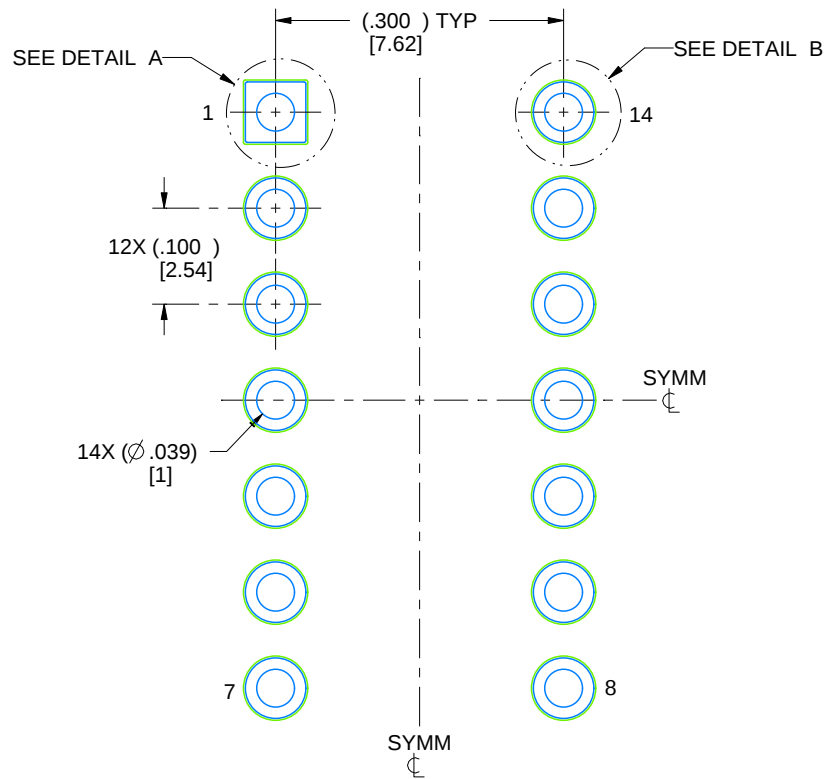
NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

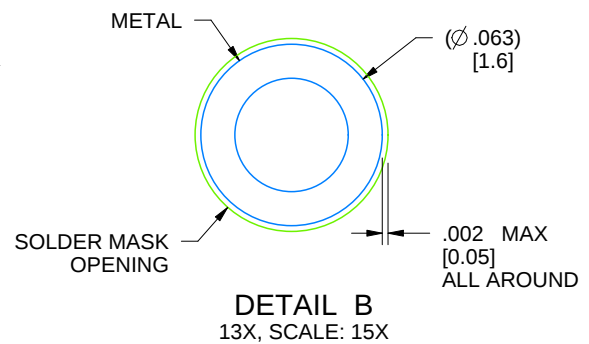
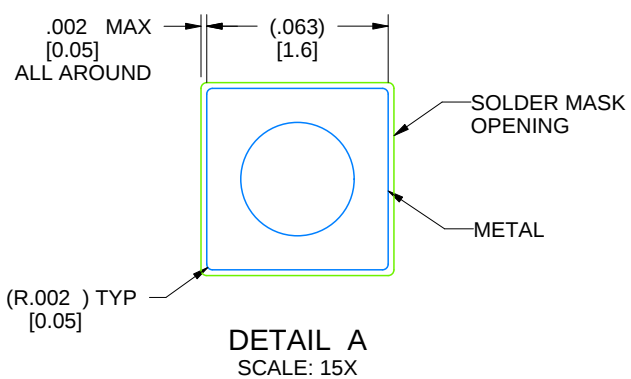
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

PW0014A

PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

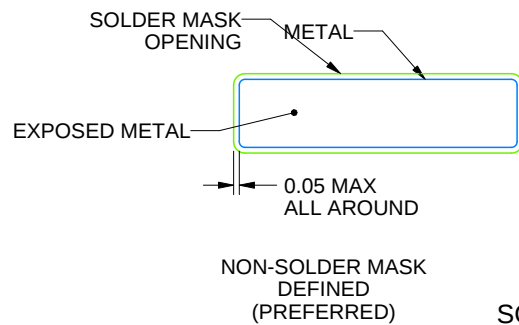
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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