

适用于 USB Type-C 和 HDMI 2.0 的 ESD122 2 通道 ESD 保护二极管

1 特性

- IEC 61000-4-2 4 级静电放电 (ESD) 保护
 - $\pm 17\text{kV}$ 接触放电
 - $\pm 17\text{kV}$ 气隙放电
- 可承受超过 1 万次 ESD 冲击而不出现任何性能下降的情况, 符合 IEC 61000-4-2 4 级 (接触) 标准
- IEC 61000-4-4 瞬态放电 (EFT) 保护
 - 80A (5/50ns)
- IEC 61000-4-5 浪涌保护
 - 2.5A (8/20 μs)
- 低 IO 电容
 - IO 之间 0.1pF (典型)
 - IO 接地 0.2pF (典型)
- 直流击穿电压: 5.1V (最小值)
- 超低泄漏电流: 10nA (最大值)
- 低 ESD 钳位电压: 在 5A TLP 下为 8.4V
- 支持超过 10Gbps 的高速接口
- 工业温度范围: -40°C 至 $+125^{\circ}\text{C}$
- Type-C 友好型双通道直通布线封装
- 引脚适合对称差分高速信号路由
- 两种不同的封装选项
 - 0402 封装, 0.6mm $\times$ 1mm, 0.34mm 间距
 - 0502 封装, 0.6mm $\times$ 1.32mm, 0.5mm 间距

2 应用

- 终端设备
 - 手机和平板电脑
 - 便携式计算机和台式机
 - 机顶盒
 - 电视和监视器
 - 服务器
- 接口
 - USB Type-C
 - HDMI 2.0/1.4
 - USB 3.1 第 2 代/第 1 代, USB 3.0 和 USB 2.0
 - Thunderbolt-1 和 Thunderbolt-2
 - 显示端口 1.3
 - PCI Express 3.0 总线接口
 - 串口硬盘 (SATA)

3 说明

ESD122 是一种双向 TVS ESD 保护二极管阵列, 用于 USB Type-C 和 HDMI 2.0 电路保护。ESD122 的额定消散接触 ESD 冲击能力达到了 IEC 61000-4-2 国际标准所规定的最高水平 (17kV 接触放电, 17kV 气隙放电)。

该器件具有每通道和引脚一个低 IO 电容, 以适应对称差分高速信号路由, 使其成为保护高达 10Gbps 的高速接口 (如 USB 3.1 第 2 代和 HDMI 2.0) 的理想选择。低动态电阻和低钳位电压确保系统级抗瞬变事件保护。

此外, ESD122 是面向 USB Type-C Tx/Rx 线路的理想 ESD 解决方案。由于 USB Type-C 连接器有两层, 所以使用 4 通道 ESD 器件需要 VIA 来降级信号完整性。使用 4 个 ESD122 (2 通道) 器件可最大限度减少 VIA 的数量并简化电路板布局。

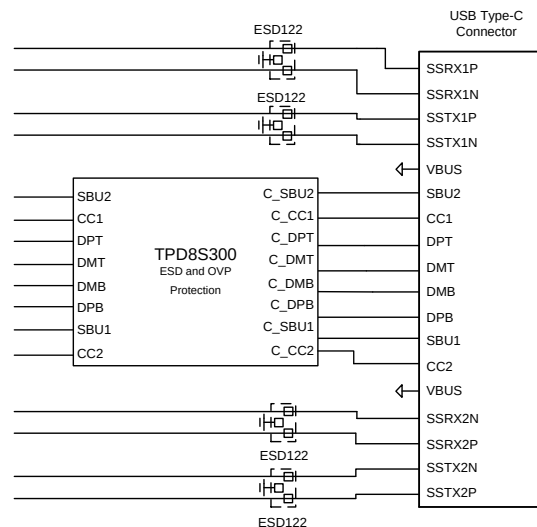
在两个简便的直通布线封装中提供了 ESD122。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
ESD122	X2SON (3)	(DMX) 0.60mm $\times$ 1.00mm
		(DMY) 0.60mm $\times$ 1.32mm

(1) 如需了解所有可用封装, 请参阅产品说明书末尾的可订购产品附录。

USB Type-C 应用示例



目录

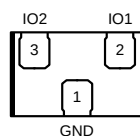
1	特性	1	7.4	Device Functional Modes.....	9
2	应用	1	8	Application and Implementation	10
3	说明	1	8.1	Application Information.....	10
4	修订历史记录	2	8.2	Typical Applications	10
5	Pin Configuration and Functions	3	9	Power Supply Recommendations	14
6	Specifications	4	10	Layout	14
6.1	Absolute Maximum Ratings	4	10.1	Layout Guidelines	14
6.2	ESD Ratings—JEDEC Specification.....	4	10.2	Layout Examples.....	14
6.3	ESD Ratings—IEC Specification	4	11	器件和文档支持	16
6.4	Recommended Operating Conditions.....	4	11.1	文档支持	16
6.5	Thermal Information	4	11.2	接收文档更新通知	16
6.6	Electrical Characteristics.....	5	11.3	社区资源.....	16
6.7	Typical Characteristics	6	11.4	商标.....	16
7	Detailed Description	8	11.5	静电放电警告	16
7.1	Overview	8	11.6	术语表	16
7.2	Functional Block Diagram	8	12	机械、封装和可订购信息	16
7.3	Feature Description.....	8			

4 修订历史记录

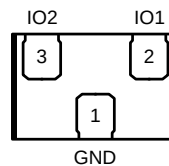
Changes from Original (June 2017) to Revision A	Page
• Changed V_{BRF} From: MIN = 5.1, MAX = 7 To: MIN = 5 and MAX = 7.9	5
• Changed V_{BRR} From: MIN = -7, MAX = -5.1 To: MIN = -7.9 and MAX = -5	5

5 Pin Configuration and Functions

**DMX Package
3-Pin X2SON
Top View**



**DMY Package
3-Pin X2SON
Top View**



Pin Functions

PIN			I/O	DESCRIPTION
NAME	DMX NO.	DMY NO.		
GND	1	1	—	Ground
IO1	2	2	I	ESD protected channel
IO2	3	3	I	ESD protected channel

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Electrical fast transient	IEC 61000-4-4 (5/50 ns) at 25°C		80	A
Peak pulse	IEC 61000-4-5 Power (t_p - 8/20 μ s) at 25°C		20	W
	IEC 61000-4-5 Current (t_p - 8/20 μ s) at 25°C		2.5	A
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	DMD storage temperature	–65	155	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings—JEDEC Specification

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	
		±2500	
		±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings—IEC Specification

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	V
		IEC 61000-4-2 air-gap discharge	
		±17000	
		±17000	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IO}	Input pin voltage	–3.6	3.6	V
T_A	Operating free-air temperature	–40	125	°C

6.5 Thermal Information

THERMAL METRIC ⁽¹⁾		ESD122		UNIT
		DMX (X2SON)	DMY (X2SON)	
		3 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	617.8	717.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	286.2	300.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	455.1	526	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	99.3	113.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	453.4	523.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{RWM}	Reverse stand-off voltage	I _{IO} < 10 nA	–3.6		3.6	V
V _{BRF}	Breakdown voltage, any IO pin to GND ⁽¹⁾	I _{IO} = 1 mA, T _A = 25°C	5		7.9	V
V _{BRR}	Breakdown voltage, GND to any IO pin ⁽¹⁾	I _{IO} = 1 mA, T _A = 25°C	–7.9		–5	V
V _{HOLD}	Holding voltage ⁽²⁾	I _{IO} = 1 mA		5.9		V
V _{CLAMP}	Clamping voltage	I _{PP} = 1 A, TLP, from IO to GND, T _A = 25°C		6.4		V
		I _{PP} = 5 A, TLP, from IO to GND, T _A = 25°C		8.4		
		I _{PP} = 1 A, TLP, from GND to IO, T _A = 25°C		6.4		
		I _{PP} = 5 A, TLP, from GND to IO, T _A = 25°C		8.4		
I _{LEAK}	Leakage current, any IO to GND	V _{IO} = ±2.5 V			10	nA
R _{DYN}	Dynamic resistance	IO to GND, Measured between TLP I _{PP} of 10 A and 20 A, T _A = 25°C		0.5		Ω
		GND to IO, Measured between TLP I _{PP} of 10 A and 20 A, T _A = 25°C		0.5		
C _L	Line capacitance	V _{IO} = 0 V, f = 1 MHz, IO to GND, T _A = 25°C		0.2	0.27	pF
ΔC _L	Variation of line capacitance	Difference between the capacitance of the two IO pins measured with respect to ground, V _{IO} = 0 V, f = 1 MHz, T _A = 25°C, GND = 0 V			0.01	pF
C _{CROSS}	Channel to channel capacitance	Capacitance from one IO to another IO, V _{IO} = 0 V, f = 1 MHz, T _A = 25°C, GND = 0 V		0.1	0.14	pF

(1) V_{BRF} and V_{BRR} are defined as the voltage obtained at 1 mA when sweeping the voltage up, before the device latches into the snapback state.

(2) V_{HOLD} is defined as the voltage when 1 mA is applied, after the device has successfully latched into the snapback state.

6.7 Typical Characteristics

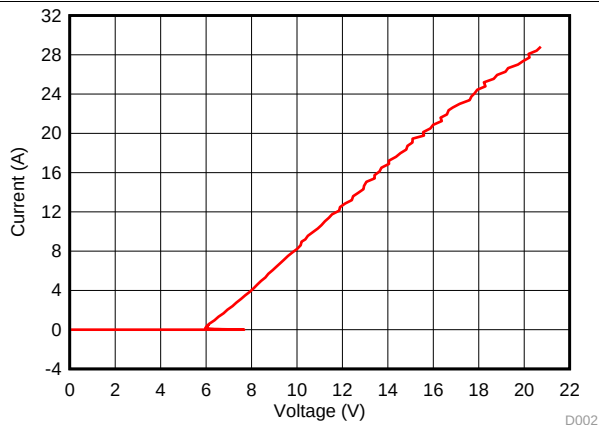


Figure 1. Positive TLP Curve, IO Pin to GND

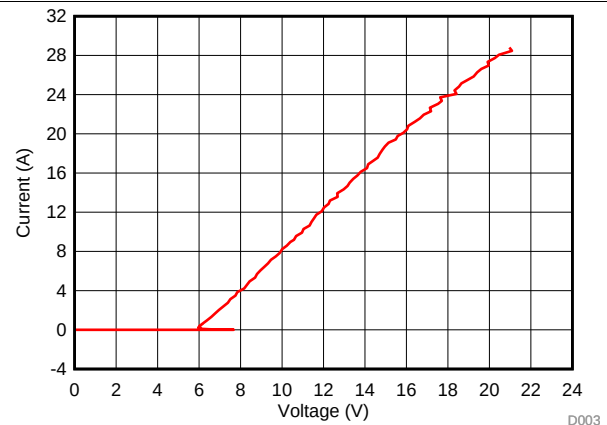


Figure 2. Negative TLP Curve, IO Pin to GND (Plotted as Positive TLP Curve GND to IO)

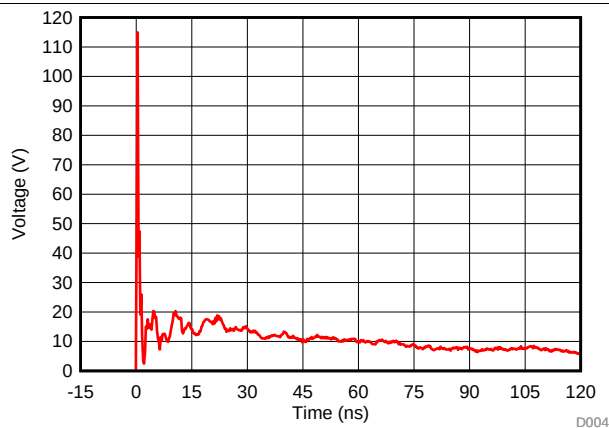


Figure 3. 8-kV IEC 61000-4-2 Waveform, IO Pin to GND

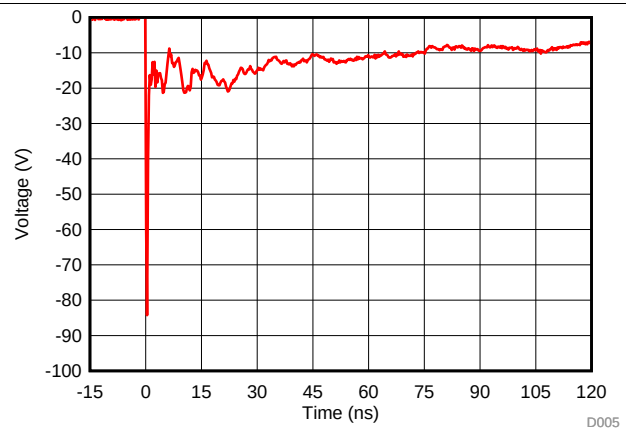


Figure 4. -8-kV IEC 61000-4-2 Waveform, IO Pin to GND

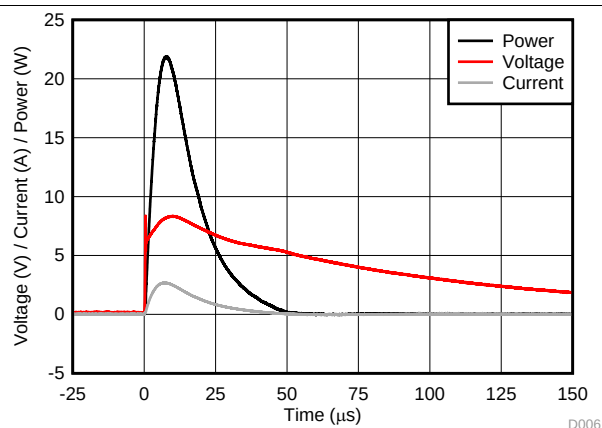


Figure 5. IEC 61000-4-5 Surge Curve ($t_p = 8/20\mu s$), IO Pin to GND

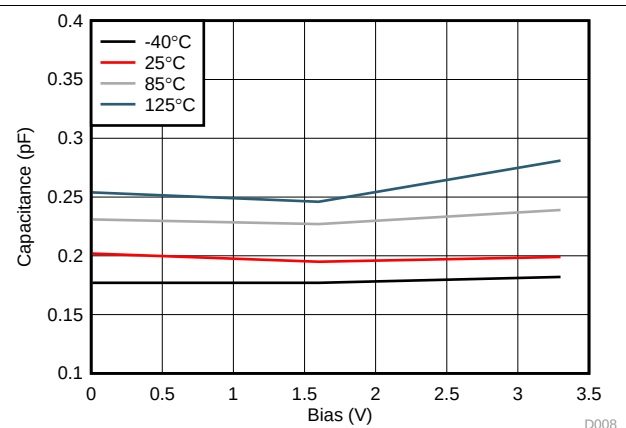


Figure 6. Capacitance vs Bias Voltage at Multiple Temperatures, IO Pin to GND

Typical Characteristics (continued)

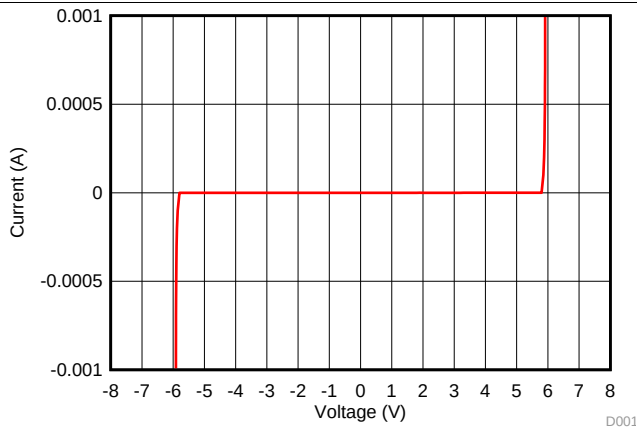


Figure 7. DC Voltage Sweep I-V Curve, IO Pin to GND

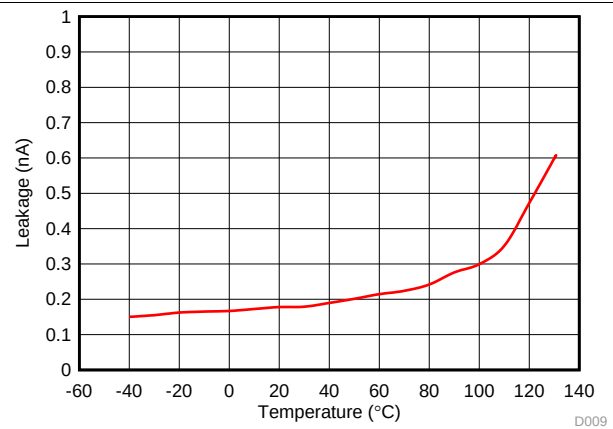


Figure 8. Leakage Current vs Temperature, IO Pin to GND, at 2.5 V Bias

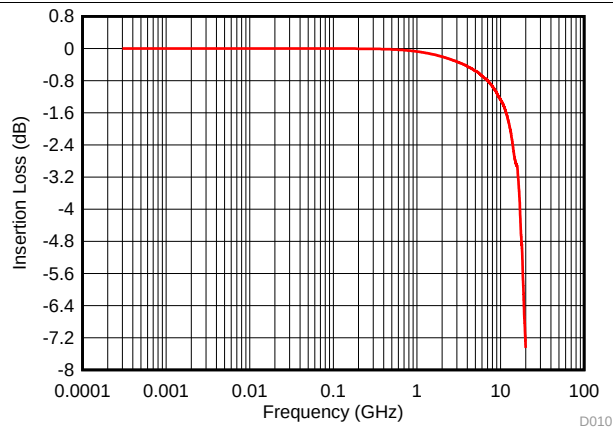


Figure 9. Insertion Loss

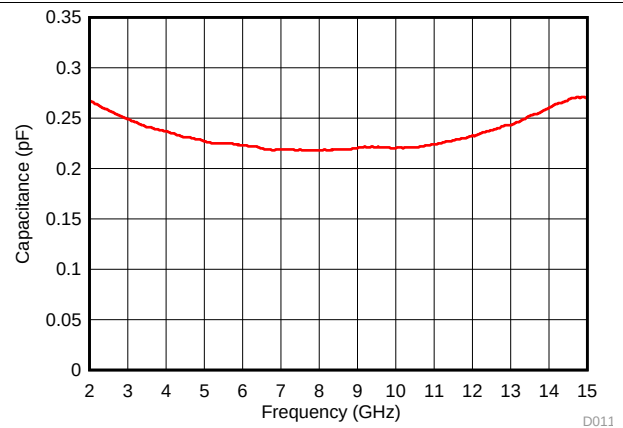


Figure 10. Capacitance vs Frequency

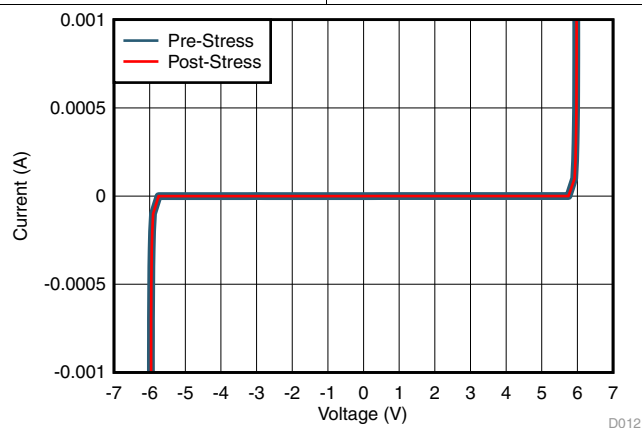


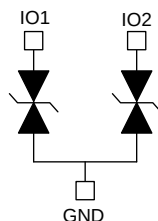
Figure 11. DC Voltage Sweep I-V Curve, IO Pin to GND, Pre and Post 10,000 Repetitive ESD Strikes per IEC 61000-4-2 Level 4 (Contact)

7 Detailed Description

7.1 Overview

The ESD122 is a bidirectional ESD Protection Diode with ultra-low capacitance. This device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 International Standard. The ultra-low capacitance makes this device ideal for protecting any super high-speed signal pins. Additionally, the ESD122 has two identical protection channels with a symmetrical pin-out that is suited for the differential high-speed signal lines.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 IEC 61000-4-2 ESD Protection

The I/O pins can withstand ESD events up to ± 17 -kV contact and air gap. An ESD-surge clamp diverts the current to ground.

7.3.2 IEC 61000-4-4 EFT Protection

The I/O pins can withstand an electrical fast transient burst of up to 80 A (5/50-ns waveform, 4 kV with 50- Ω impedance). An ESD-surge clamp diverts the current to ground.

7.3.3 IEC 61000-4-5 Surge Protection

The I/O pins can withstand surge events up to 2.5 A and 20 W (8/20- μ s waveform). An ESD-surge clamp diverts this current to ground.

7.3.4 IO Capacitance

The capacitance between each I/O pin to ground is very small and supports data rates up to 10 Gbps.

7.3.5 DC Breakdown Voltage

The DC breakdown voltage of each I/O pin is a minimum of ± 5.1 V. This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of ± 3.6 V.

7.3.6 Ultra Low Leakage Current

The I/O pins feature an ultra-low leakage current of 10 nA (maximum) with a bias of ± 2.5 V.

7.3.7 Low ESD Clamping Voltage

The I/O pins feature an ESD clamp that is capable of clamping the voltage to 8.4 V ($I_{PP-TLP} = 5$ A).

7.3.8 Supports High Speed Interfaces

This device is capable of supporting high speed interfaces up to 10 Gbps such as USB 3.1 Gen2 and Gen1, USB 3.0, USB 2.0, Thunderbolt-1, Thunderbolt-2, PCI express 3.0, Display Port 1.3, HDMI 2.0, and HDMI 1.4, because of the extremely low IO capacitance.

7.3.9 Industrial Temperature Range

This device features an industrial operating range of -40°C to $+125^{\circ}\text{C}$.

Feature Description (continued)

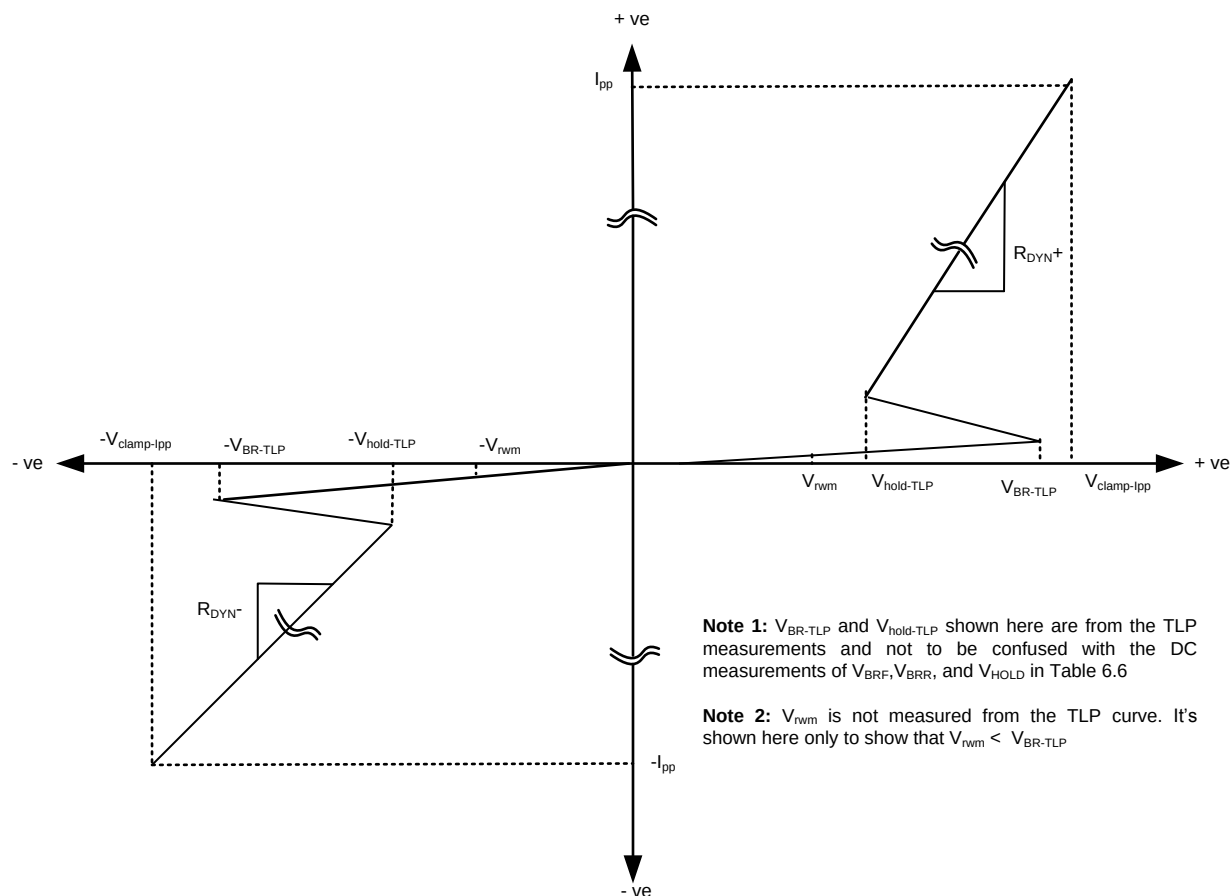
7.3.10 Easy Flow-Through Routing Package

The layout of this device makes it simple and easy to add protection to an existing layout. 2-channel setup provides easy, flexible routing and good matching between the channels.

7.4 Device Functional Modes

The ESD122 is a passive circuit that triggers when voltages are above V_{BRF} or below V_{BRR} . During ESD events, voltages as high as ± 17 kV (contact) can be directed to ground via the internal diode network. When the voltages on the protected line fall below the trigger levels of ESD122 (usually within 10s of nano-seconds) the device reverts to passive.

Figure 12 shows typical TLP behavior of bi-directional ESD device.



**Figure 12. Generic TLP I-V Curve for a Bi-Directional ESD Device
for the Illustration of V_{rwm} , V_{BR} , V_{hold} and V_{clamp}**

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The ESD122 is a diode type TVS which is used to provide a path to ground for dissipating ESD events on high-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP} , to a safe level for the protected IC.

8.2 Typical Applications

8.2.1 USB 3.1 Gen 2 Application

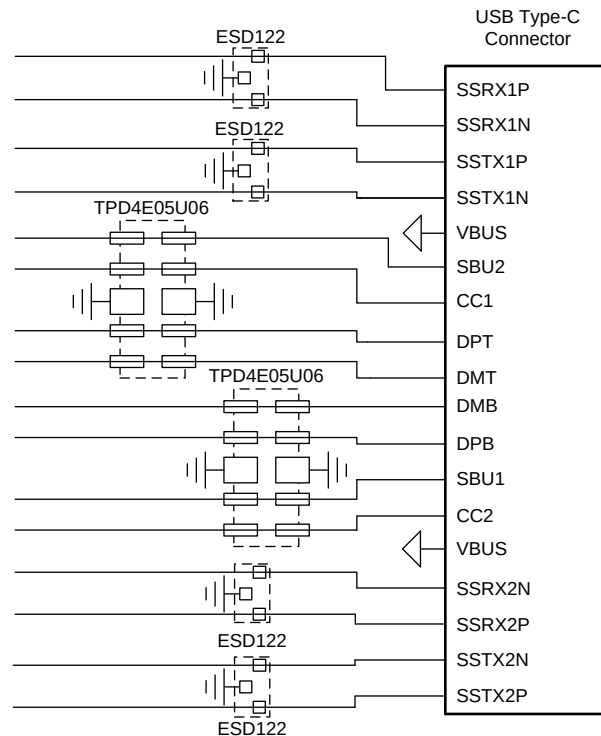


Figure 13. Typical Application

8.2.1.1 Design Requirements

For this design example, four ESD122 devices and two TPD4E05U06 devices are being used in a USB 3.1 Gen 2 Type-C application. This provides a complete ESD protection scheme.

Given the application, the parameters listed in [Table 1](#) are known.

Typical Applications (continued)

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on Type C SuperSpeed+ lines	0 V to 3.6 V
Operating frequency on Type C USB 3.1 Gen 2 SuperSpeed+ lines	5 GHz
Signal range on CC, SBU, and DP/DM lines	0 V to 5 V
Operating frequency on CC, SBU, and DP/DM lines	up to 480 MHz

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Signal Range

The ESD122 supports signal ranges between -3.6 V and 3.6 V , which supports the SuperSpeed+ pairs on the USB Type-C application. The TPD4E05U06 supports signal ranges between 0 V and 5.5 V , which supports the CC, SBU, and DP/DM lines.

8.2.1.2.2 Operating Frequency

The ESD122 has a 0.27 pF (maximum) capacitance, which supports the USB 3.1 Gen 2 Type-C rate of 10 Gbps with sufficient capacitance margin. The TPD4E05U06 has a 0.5 pF (typical) capacitance, which easily supports the CC, SBU, and DP/DM data rates. The ESD122 has 2 identical protection channels for the differential HDMI high-speed signal lines. The symmetrical pin out of the device with a ground pin between the two differential signal pins makes it suitable for this application.

8.2.1.3 Application Curves

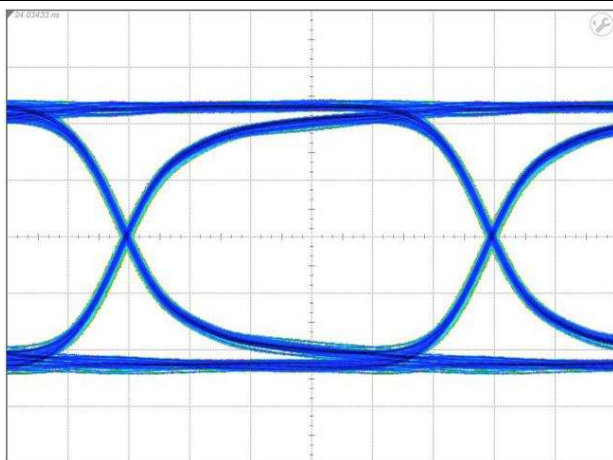


Figure 14. USB3.1 Gen2 10-Gbps Eye Diagram Without ESD122

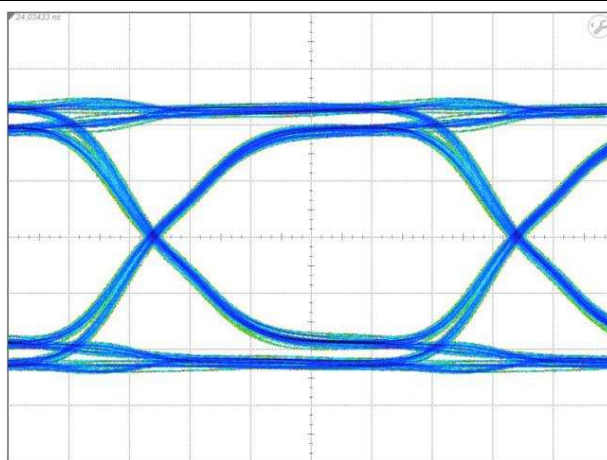
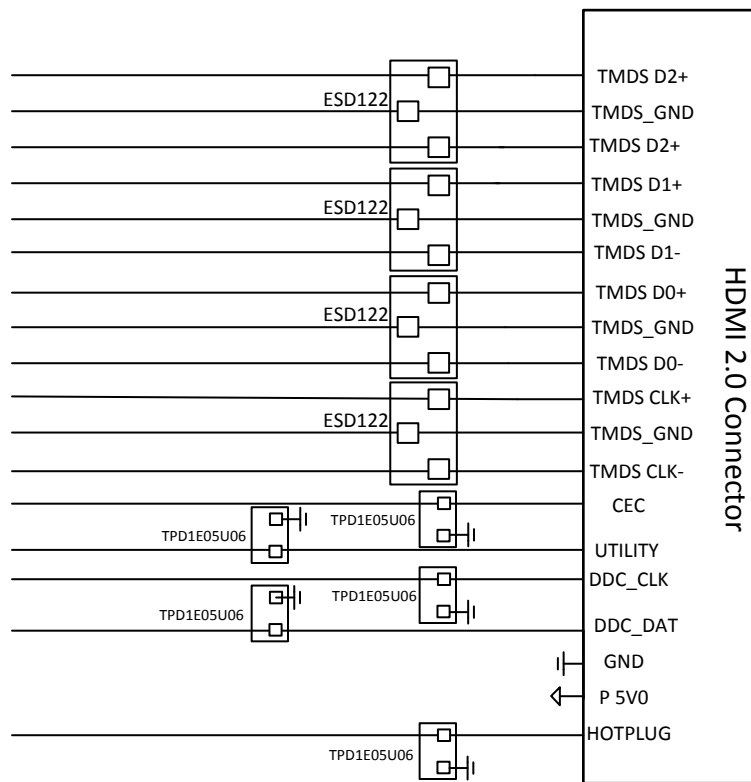


Figure 15. : USB3.1 Gen2 10-Gbps Eye Diagram With ESD122

8.2.2 HDMI 2.0 Application



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Figure 16. HDMI 2.0 Schematic

8.2.2.1 Design Requirements

For this design example, the four ESD122 devices for the HDMI 2.0 high-speed lines, and four TPD1E05U06 devices on the control lines HDMI 2.0 control lines. This provides a complete port protection scheme.

Given the HDMI 2.0 application, the parameters listed in [Table 2](#) are known.

Table 2. Design Parameters

DESIGN PARAMETER	VALUE
Signal voltage range on the high-speed pins	0 V to 3.3 V
Signal voltage range on the control pins	0 V to 5 V
Max operating frequency of high-speed lines	3 GHz

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 Signal Range

The ESD122 supports signal ranges between -3.6 V and 3.6 V , which supports the high-speed lines on the HDMI 2.0 application. The TPD1E05U06 supports signal ranges between 0 V and 5.5 V , which supports the HDMI control lines.

8.2.2.2.2 Operating Frequency

The ESD122 has a 0.27 pF (maximum) capacitance, which supports the HDMI 2.0 rate of 6 Gbps with sufficient capacitance margin. The TPD1E05U06 has a 0.42 pF (typical) capacitance, which easily supports the control lines. The ESD122 has 2 identical protection channels for the differential HDMI high-speed signal lines. The symmetrical pin out of the device with a ground pin between the two differential signal pins makes it suitable for this application.

8.2.2.3 Application Curves

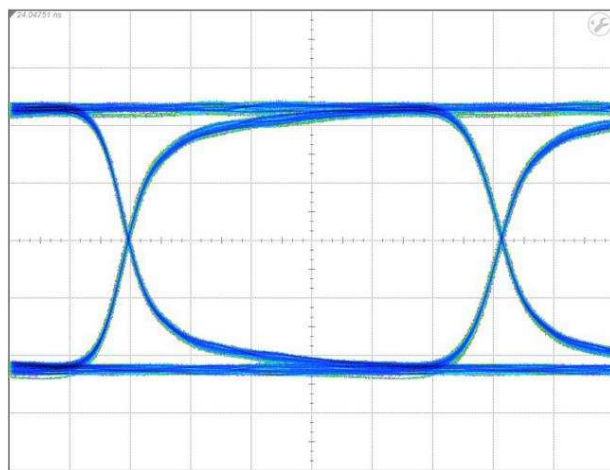


Figure 17. HDMI 2.0 6-Gbps Eye Diagram Without ESD122

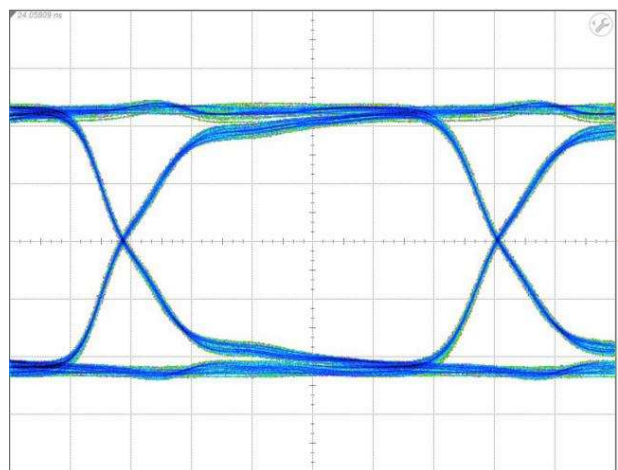


Figure 18. HDMI 2.0 6-Gbps Eye Diagram With ESD122

9 Power Supply Recommendations

This device is a passive ESD device so there is no need to power it. Take care not to violate the recommended I/O specification (–3.6 V to 3.6 V) to ensure the device functions properly.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
 - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
 - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible. Use as few vias as possible for 10-Gbps application.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
 - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Examples

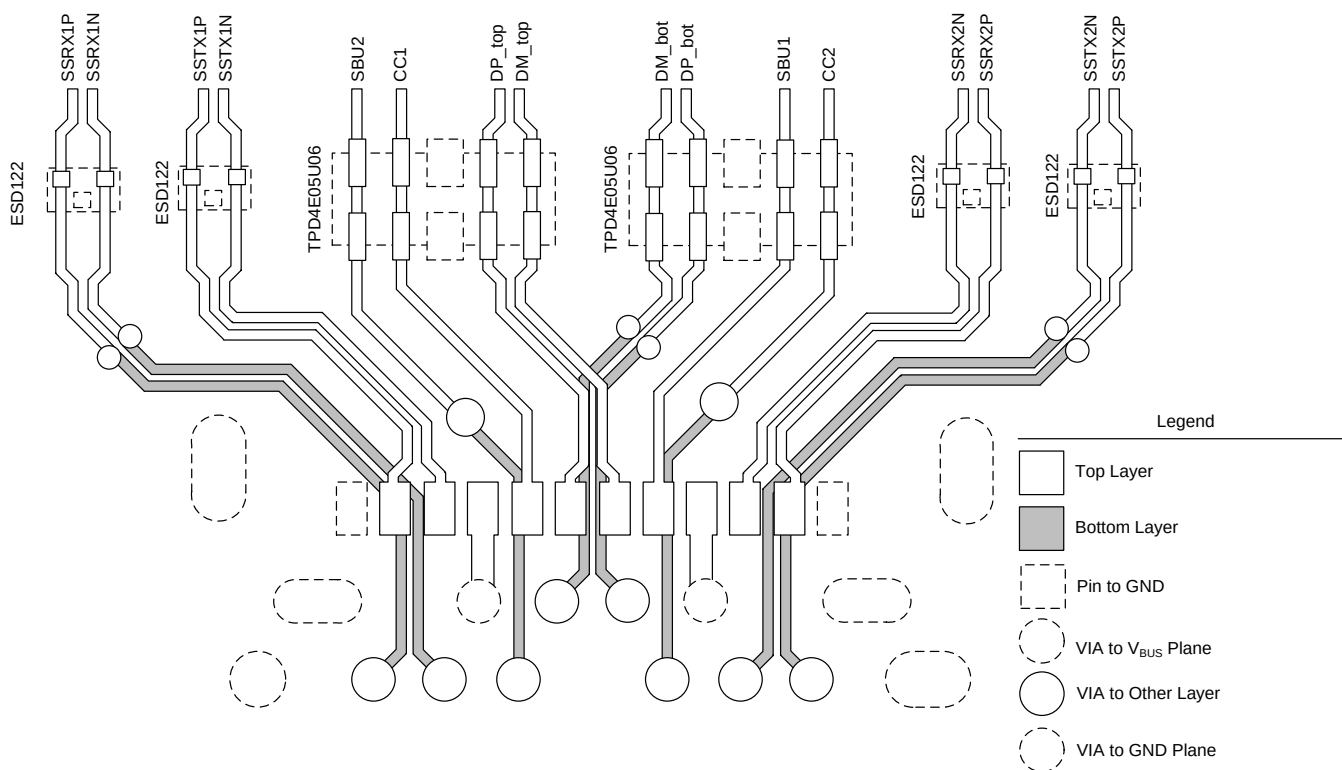


Figure 19. USB 3.1 Gen 2 SuperSpeed Lines Protected by ESD122

Layout Examples (continued)

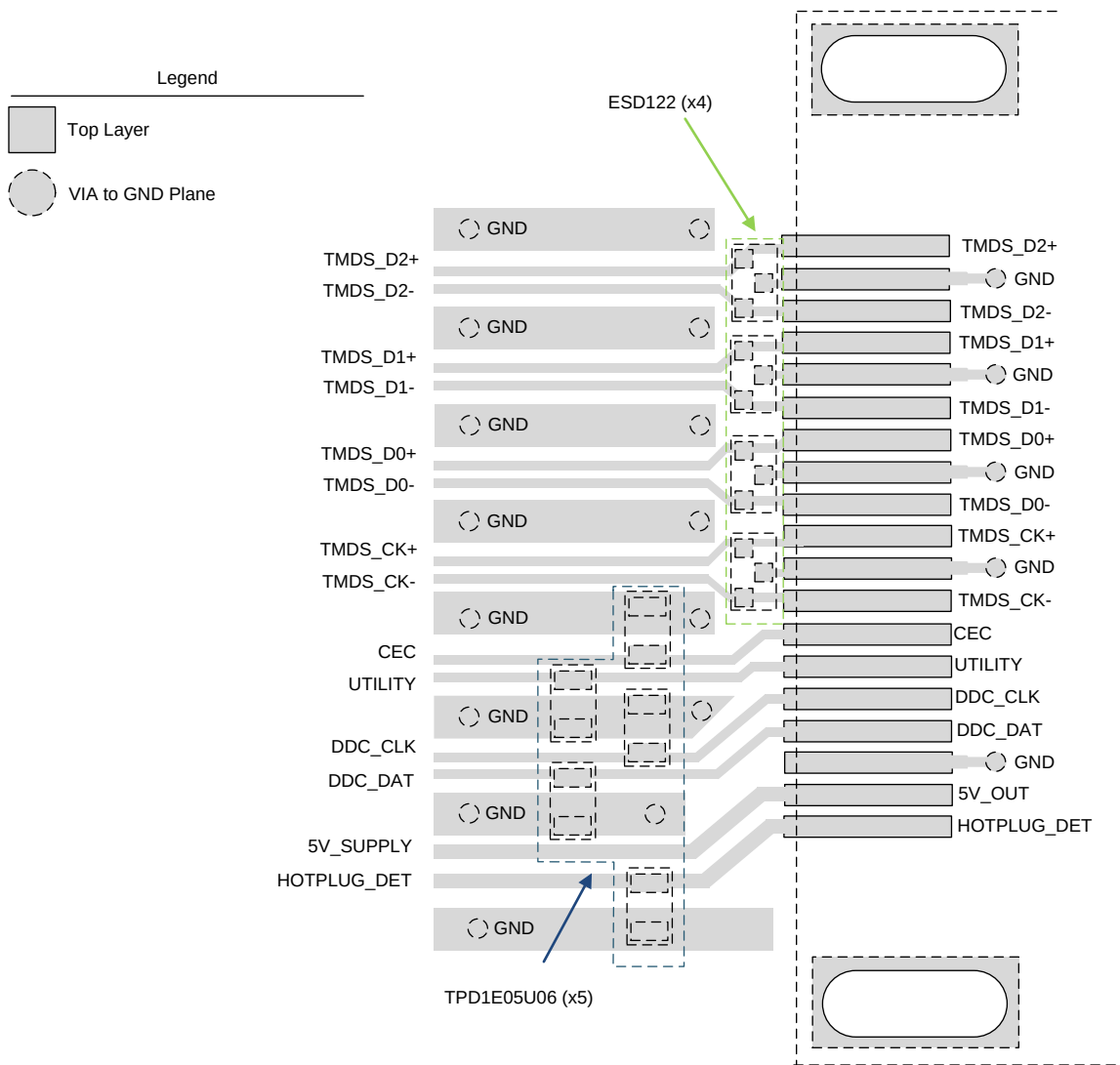


Figure 20. HDMI2 Layout

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

请参阅如下相关文档：

[ESD122 评估模块](#)

11.2 接收文档更新通知

如需接收文档更新通知，请访问 [Ti.com.cn](http://ti.com.cn) 上的器件产品文件夹。单击右上角的 [通知我](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

TI E2E™ 在线社区 **TI 的工程师对工程师 (E2E) 社区**。此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 **TI 参考设计支持** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

11.4 商标

E2E is a trademark of Texas Instruments.

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11.5 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 术语表

[SLYZ022](#) — TI 术语表。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ESD122DMXR	Active	Production	X2SON (DMX) 3	10000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	6U
ESD122DMYR	Active	Production	X2SON (DMY) 3	10000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	6V

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

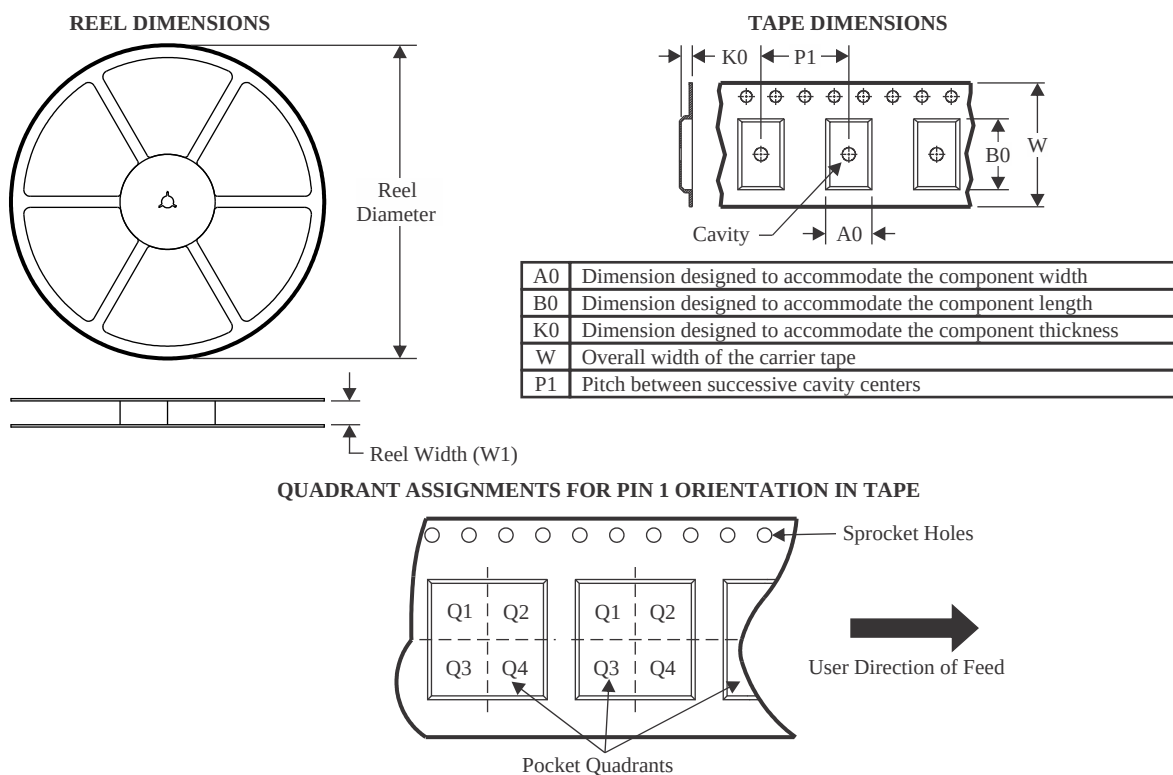
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

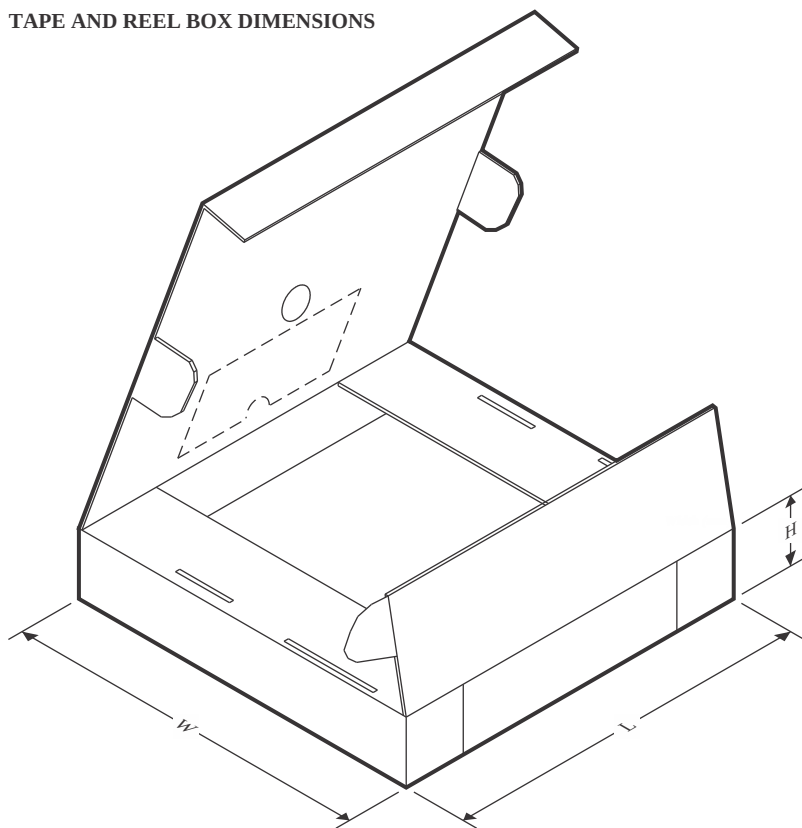
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD122DMXR	X2SON	DMX	3	10000	180.0	9.5	0.72	1.12	0.43	2.0	8.0	Q1
ESD122DMYR	X2SON	DMY	3	10000	180.0	9.5	0.72	1.42	0.43	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD122DMXR	X2SON	DMX	3	10000	189.0	185.0	36.0
ESD122DMYR	X2SON	DMY	3	10000	189.0	185.0	36.0



DMY0003A

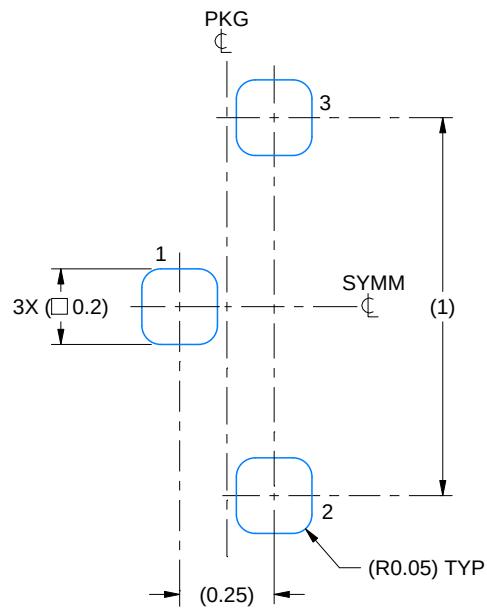
- 
- TEXAS
INSTRUMENTS
www.ti.com

EXAMPLE BOARD LAYOUT

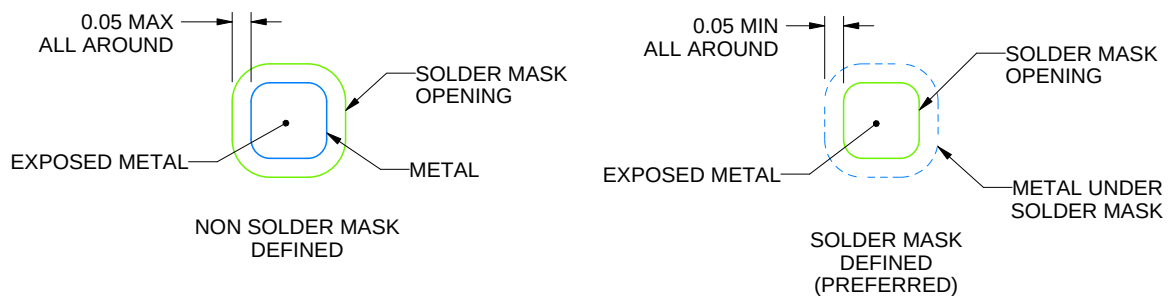
DMY0003A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X



SOLDER MASK DETAILS

4223464/A 01/2017

NOTES: (continued)

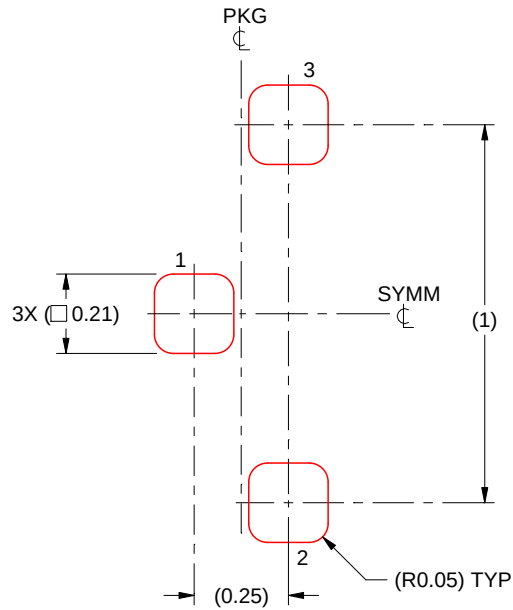
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271)

EXAMPLE STENCIL DESIGN

DMY0003A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

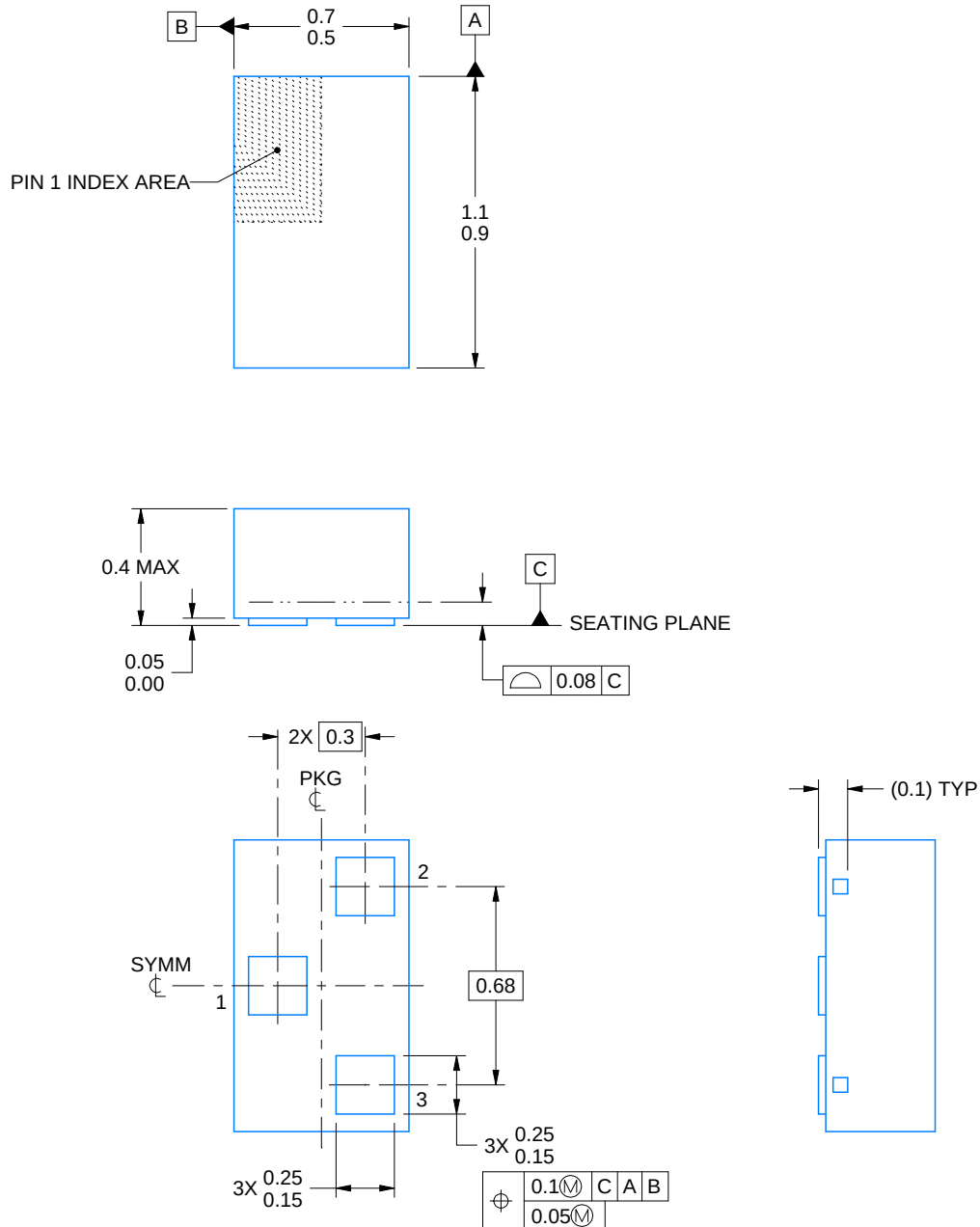


SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE: 50X

4223464/A 01/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



4223380/A 10/2016

NOTES:

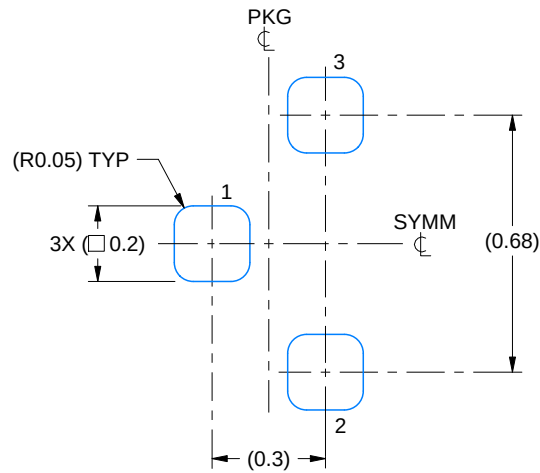
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

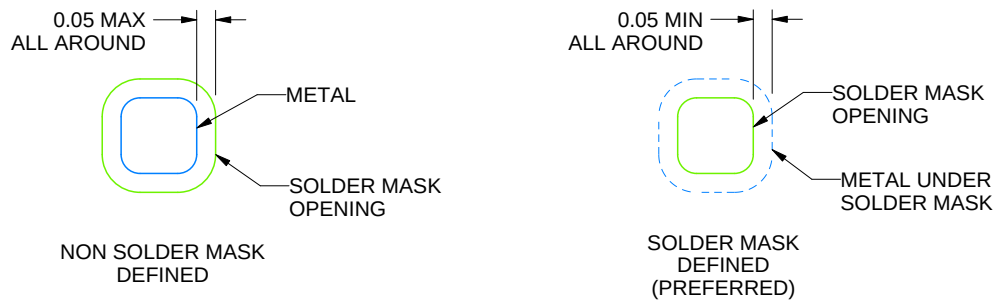
DMX0003A

X2SON - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:50X



SOLDER MASK DETAILS

4223380/A 10/2016

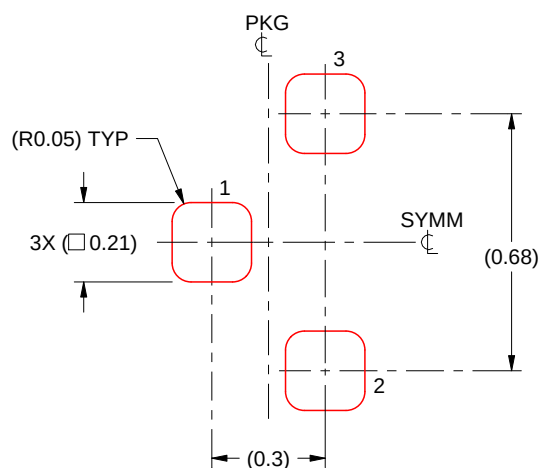
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).

DMX0003A

X2SON - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:50X

4223380/A 10/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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