SN74LVC1G38 Single 2-Input NAND Gate With Open-Drain Output

1 Features

- Latch-up performance exceeds 100 mA Per JESD 78, Class II
- ESD protection exceeds JESD 22
  - 2000-V Human-body model (A114-A)
  - 200-V Machine model (A115-A)
  - 1000-V Charged-device model (C101)
- Available in the Texas Instruments NanoStar™ and NanoFree™ Packages
- Supports 5-V V_{CC} operation
- Inputs accept voltages to 5.5 V
- Supports down translation to V_{CC}
- Maximum t_{pd} of 4.5 ns at 3.3 V
- Low power consumption, 10-µA maximum I_{CC}
- ±24-mA Output drive at 3.3 V
- I_{off} Supports partial-power-down mode and back-drive protection

2 Applications

- AV receivers
- Blu-ray players and home theaters
- DVD recorders and players
- Desktop or notebook PCs
- Digital radio or internet radio players
- Digital video cameras (DVC)
- Embedded PCs
- GPS: personal navigation devices
- Mobile internet devices
- Network projector front-ends
- Portable media players
- Pro audio mixers
- Smoke detectors
- Solid dtate drive (SSD): enterprise
- High-definition (HDTV)
- Tablets: enterprise
- Audio docks: portable
- DLP front projection systems
- DVR and DVS
- Digital picture frame (DPF)
- Digital still cameras

3 Description

The SN74LVC1G38 device is designed for 1.65-V to 5.5-V V_{CC} operation.

This device is a single two-input NAND buffer gate with open-drain output. It performs the Boolean function $Y = \overline{A \times B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device which prevents damage to the device.

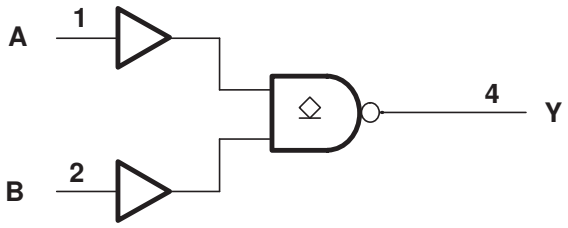
NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

Device Information(1)

DEVICE NAME	PACKAGE	BODY SIZE (NOM)
SN74LVC1G38DBV	SOT-23 (5)	2.90 mm × 1.60 mm
SN74LVC1G38DCK	SC70 (5)	2.00 mm × 1.25 mm
SN74LVC1G38DRY	SON (6)	1.45 mm × 1.00 mm
SN74LVC1G38DSF	SON (6)	1.00 mm × 1.00 mm
SN74LVC1G38YZP	DSBGA (5)	0.89 mm × 1.39 mm
SN74LVC1G38DPW	X2SON (5)	0.80 mm × 0.80 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (October) to Revision G — **Page**

- Changed the T_A high-end temp from +1255°C to +125°C in the Test Conditions field of the Electrical Characteristics table. ... 6

Changes from Revision E (August 2017) to Revision F — **Page**

- Added values for DPW (X2SON) package in *Thermal Information* table. ... 5

Changes from Revision D (December 2013) to Revision E — **Page**

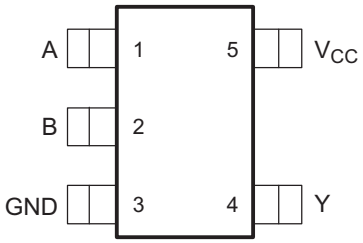
- Added DPW (X2SON) package ... 1
- Added *Applications*, *Device Information* table, *Pin Configuration and Functions* section, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Detailed Description* section, *Application and Implementation* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Added Maximum junction temperature, T_J ... 4
- Changed values in the Thermal Information table to align with JEDEC standards ... 5

Changes from Revision C (March 2011) to Revision D — **Page**

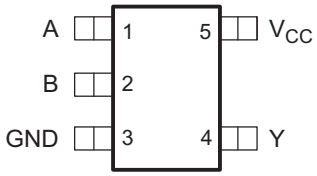
- Updated document to new TI data sheet format. ... 1
- Updated I_{off} in Features. ... 1
- Added ESD warning. ... 1
- Updated operating temperature range. ... 5

5 Pin Configuration and Functions

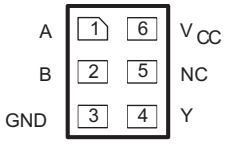
DBV Package
5-Pin SOT-23
Top View



DCK Package
5-Pin SC70
Top View

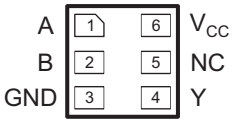


DRY Package
6-Pin SON
Top View



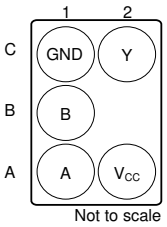
NC – No internal connection.

DSF Package
6-Pin SON
Top View



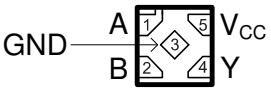
See mechanical drawings for dimensions

YZP Package
5-Pin DSBGA
Bottom View



Not to scale

DPW Package
5-Pin X2SON
Top View



Pin Functions

PIN				I/O	DESCRIPTION
NAME	DBV, DCK, DPW	DRY, DSF	YZP		
A	1	1, 5	A1	I	Logic Input A
B	2	2	B1	I	Logic Input B
GND	3	3	C1	—	Ground
NC	—	5	—	—	No Internal Connection
Y	4	4	C2	O	Output Y
V_{CC}	5	6	A2	—	Positive Supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	6.5	V
V_I	Input voltage(2)		–0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	6.5	V
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_J	Maximum junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	1000	
		Machine Model (MM), A115-A	200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 3 V to 3.6 V	2		
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 3 V to 3.6 V		0.8	
		V_{CC} = 4.5 V to 5.5 V		0.3 × V_{CC}	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	5.5	V
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 3 V		16	
				24	
		V_{CC} = 4.5 V		32	
Δt/Δv	Input transition rise and fall rate	V_{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	ns/V
		V_{CC} = 3.3 V ± 0.3 V		10	
		V_{CC} = 5 V ± 0.5 V		5	
T_A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*.

6.4 Thermal Information

THERMAL METRIC(1)		SN74LVC1G38						UNIT
		DBV (SOT-23)	DCK (SC70)	DRY (SON)	DSF (SON)	YZP (DSBGA)	DPW (X2SON)	
		5 PINS	5 PINS	6 PINS	6 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	247.2	276.1	366.9	406.2	146.2	511.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	154.5	178.9	253.8	201.0	1.4	241.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	86.8	70.9	227.5	256.9	39.3	374.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	58.0	47.0	75.8	35.2	0.7	45.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	86.4	69.3	227.7	256.6	39.8	373.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	168.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{OL}		I_{OL} = 100 µA	T_A = –40°C to +85°C	1.65 V to 5.5 V			0.1	V
			T_A = –40°C to +125°C					
		I_{OL} = 4 mA	T_A = –40°C to +85°C	1.65 V			0.45	
			T_A = –40°C to +125°C					
		I_{OL} = 8 mA	T_A = –40°C to +85°C	2.3 V			0.3	
			T_A = –40°C to +125°C					
		I_{OL} = 16 mA	T_A = –40°C to +85°C	3 V			0.4	
			T_A = –40°C to +125°C					
		I_{OL} = 24 mA	T_A = –40°C to +85°C				0.55	
			T_A = –40°C to +125°C					
		I_{OL} = 32 mA	T_A = –40°C to +85°C	4.5 V			0.55	
			T_A = –40°C to +125°C					
I_I	A or B inputs	V_I = 5.5 V or GND	T_A = –40°C to +85°C	1.65 V to 5.5 V			±1	µA
			T_A = –40°C to +125°C					
I_{off}		V_I or V_O = 5.5 V	T_A = –40°C to +85°C	0			±10	µA
			T_A = –40°C to +125°C					
I_{CC}		V_I = 5.5 V or GND, I_O = 0	T_A = –40°C to +85°C	1.65 V to 5.5 V			10	µA
			T_A = –40°C to +125°C					
ΔI_{CC}		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	T_A = –40°C to +85°C	3 V to 5.5 V			500	µA
			T_A = –40°C to +125°C					
C_i		V_I = V_{CC} or GND		3.3 V		3.5		pF
C_o		V_O = V_{CC} or GND		3.3 V		4.5		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

6.6 Switching Characteristics, C_L = 15 pF

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	MAX	UNIT
t_{pd}	A or B	Y	T_A = –40°C to +85°C	V_{CC} = 1.8 V ± 0.15 V	2.9	7.4	ns
				V_{CC} = 2.5 V ± 0.2 V	1.7	3.8	
				V_{CC} = 3.3 V ± 0.3 V	1.5	4.9	
				V_{CC} = 5 V ± 0.5 V	0.9	2.4	

6.7 Switching Characteristics, C_L = 30 pF or 50 pF, –40°C to +85°C

over recommended operating free-air temperature range, C_L = 30 pF or 50 pF (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	MAX	UNIT
t_{pd}	A or B	Y	T_A = –40°C to +85°C	V_{CC} = 1.8 V ± 0.15 V	2.8	10	ns
				V_{CC} = 2.5 V ± 0.2 V	1.6	6	
				V_{CC} = 3.3 V ± 0.3 V	1.4	4.5	
				V_{CC} = 5 V ± 0.5 V	1	3.9	

6.8 Switching Characteristics, C_L = 30 pF or 50 pF, –40°C to +125°C

over recommended operating free-air temperature range, C_L = 30 pF or 50 pF (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	MAX	UNIT
t_{pd}	A or B	Y	T_A = –40°C to +125°C	V_{CC} = 1.8 V ± 0.15 V	2.8	11	ns
				V_{CC} = 2.5 V ± 0.2 V	1.6	6.5	
				V_{CC} = 3.3 V ± 0.3 V	1.4	5	
				V_{CC} = 5 V ± 0.5 V	1	4.4	

6.9 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	f = 10 MHz	V_{CC} = 1.8 V	3	pF
			V_{CC} = 2.5 V	3	
			V_{CC} = 3.3 V	4	
			V_{CC} = 5 V	6	

6.10 Typical Characteristics

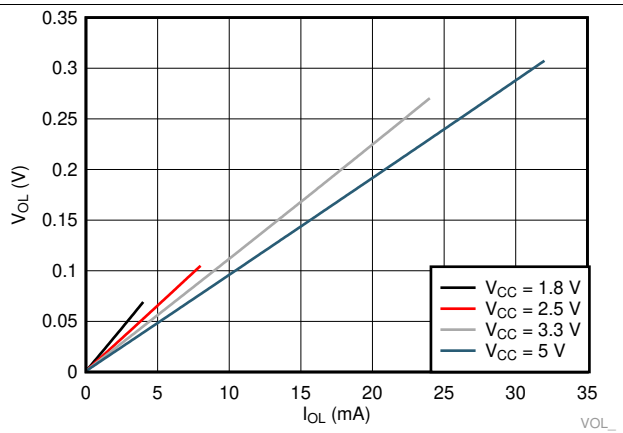
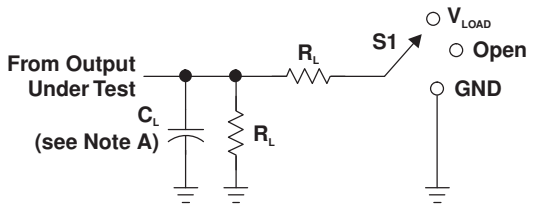


Figure 1. Typical I_{OL} vs. V_{OL} (T_A = 25°C)

7 Parameter Measurement Information

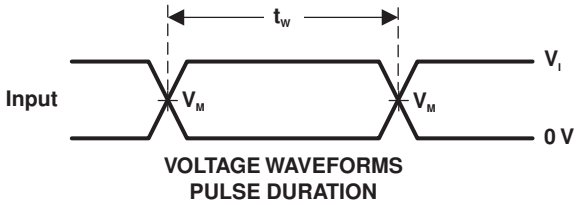
(Open Drain)



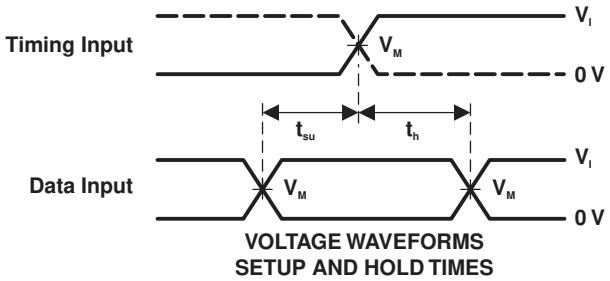
LOAD CIRCUIT

TEST	S1
t_{PZL} (see Notes E and F)	V_{LOAD}
t_{PLZ} (see Notes E and G)	V_{LOAD}
t_{PHZ}/t_{PZH}	V_{LOAD}

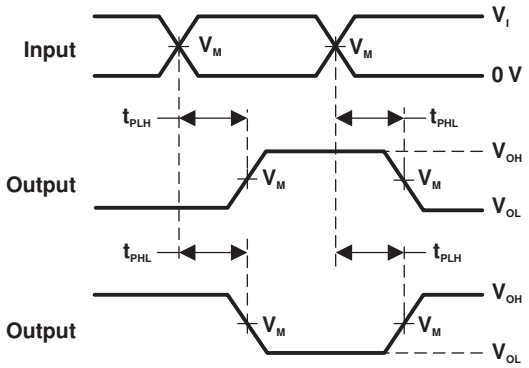
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	1 MΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	1 MΩ	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	15 pF	1 MΩ	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	1 MΩ	0.3 V



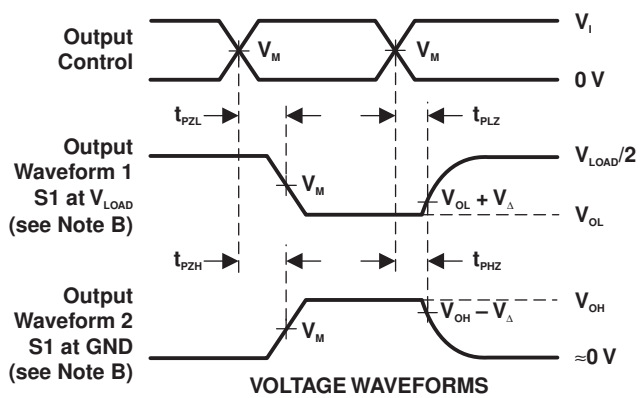
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



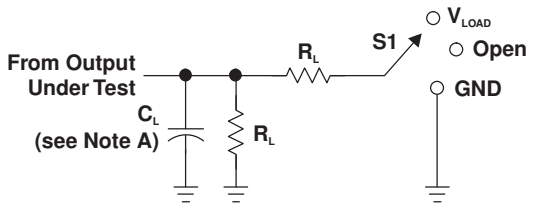
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators have the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. Because this device has open-drain outputs, t_{PLZ} and t_{PZL} are the same as t_{PD}.
F. t_{PZL} is measured at V_M.
G. t_{PLZ} is measured at V_{OL} + V_Δ.
H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

Parameter Measurement Information (continued)

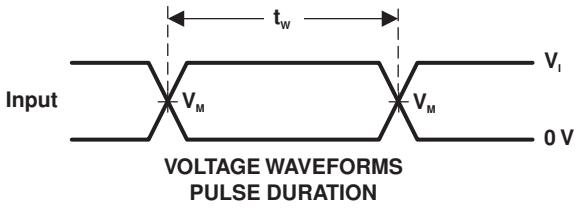
(Open Drain)



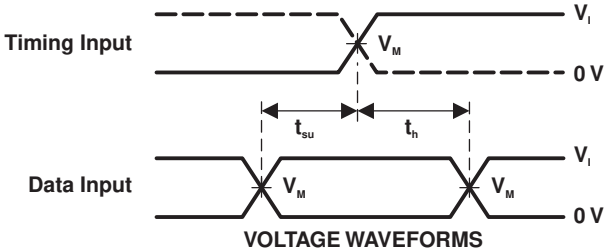
LOAD CIRCUIT

TEST	S1
t_{PZL} (see Notes E and F)	V_{LOAD}
t_{PLZ} (see Notes E and G)	V_{LOAD}
t_{PHZ}/t_{PZH}	V_{LOAD}

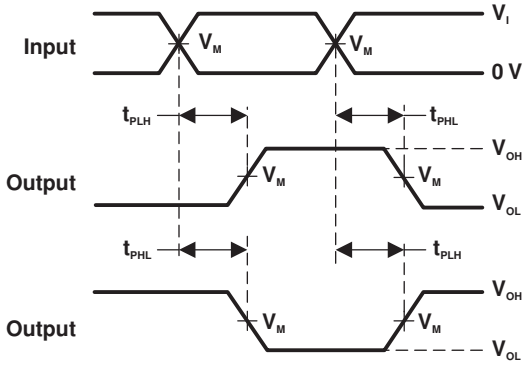
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V



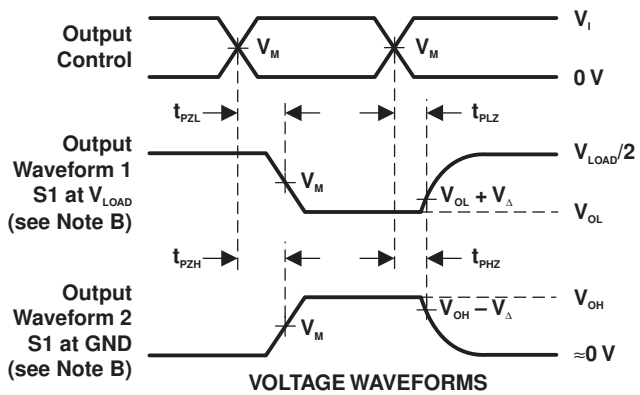
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators have the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. Because this device has open-drain outputs, t_{PLZ} and t_{PZL} are the same as t_{PD}.
F. t_{PZL} is measured at V_M.
G. t_{PLZ} is measured at V_{OL} + V_Δ.
H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74LVC1G38 device is a single two-input NAND gate with open-drain outputs designed for 1.65-V to 5.5-V Vcc operation. It performs the Boolean function $Y = \overline{A \times B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device which prevents damage to the device.

8.2 Functional Block Diagram

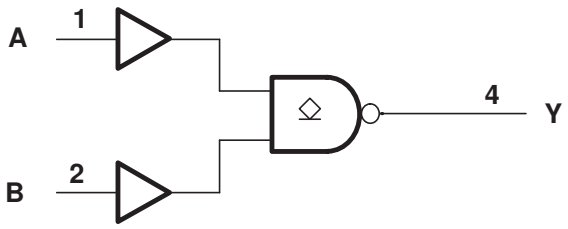


Figure 4. Logic Diagram (Positive Logic)

8.3 Feature Description

8.3.1 High-Drive Open-Drain Output

The open-drain output allows the device to sink current when the output is LOW and maintains a high impedance state when the output is HIGH. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the power output of the device to be limited to avoid thermal runaway and damage due to over-current. The electrical and thermal limits defined the in the *Absolute Maximum Ratings* must be followed at all times.

8.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using ohm's law (R = V ÷ I).

Signals applied to the inputs need to have fast edge rates, as defined by $\Delta t/\Delta v$ in *Recommended Operating Conditions* to avoid excessive currents and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

Feature Description (continued)

8.3.3 Clamp Diodes

The inputs and outputs to this device have negative clamping diodes.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

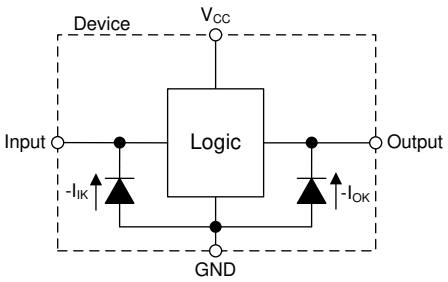


Figure 5. Electrical Placement of Clamping Diodes for Each Input and Output

8.3.4 Partial Power Down (I_{off})

The inputs and outputs for this device enter a high impedance state when the supply voltage is 0 V. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the .

8.3.5 Over-Voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the *Absolute Maximum Ratings*.

8.3.6 Up Translation and Down Translation Capable Outputs

Outputs of this device can be driven above the supply voltage so long as they remain below the maximum output voltage value specified in the *Absolute Maximum Ratings*. When the device is not actively driving LOW, the output is in the high impedance state. If a pull-up resistor is connected from the output to a power supply (of any valid value), the output will be driven by this supply, and therefore can have a voltage that is either higher or lower than the V_{CC} supply of the device. An application of this device performing up-translation is depicted in *Application and Implementation*, where additional design details are provided.

8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74LVC1G38 device.

Table 1. Function Table

INPUTS		OUTPUT
A	B	Y
L	L	Hi-Z
L	H	Hi-Z
H	L	Hi-Z
H	H	L

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Open-drain devices are intrinsically capable of voltage translation. In this application, a 1.8-V logic signal is inverted and up-translated to 5 V at the output when the EN signal input is driven high by a 3.3-V signal. The output is held at 5 V in this scenario when the output of the device is in the high impedance state.

9.2 Typical Application

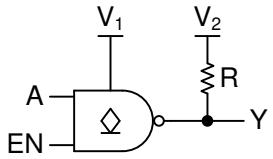


Figure 6. Gated Voltage Translating Inverter Schematic Using SN74LVC1G38

9.2.1 Design Requirements

The supply voltage at V_1 must be set to provide input thresholds for the signals A and EN. This device uses CMOS technology and has an open-drain output. Outputs of open-drain devices can be tied directly together to produce a wired-OR configuration. This device has high current drive that will create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - Rise time and fall time specs. See ($\Delta t/\Delta V$) in the *Recommended Operating Conditions* table.
   - Specified high and low levels. See (VIH and VIL) in the *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant allowing them to go as high as (VI max) in the *Recommended Operating Conditions* table at any valid VCC.
2. Recommended Output Conditions
   - Load currents should not exceed (IO max). These limits are located in the *Absolute Maximum Ratings* table.
   - Outputs can be pulled above VCC for up-translation applications as long as the maximum output voltage in the *Absolute Maximum Ratings* table is observed.

9.2.3 Application Curve

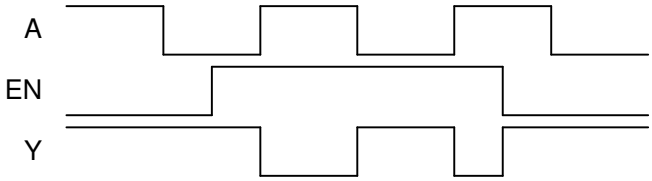


Figure 7. Application Timing Diagram

10 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

The V_{CC} pin should have a good bypass capacitor to prevent power disturbance. It is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 8 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or V_{CC}, whichever makes more sense or is more convenient.

Even low data rate digital signals can have high frequency signal components due to fast edge rates. When a printed-circuit board (PCB) trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 9 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

11.2 Layout Example

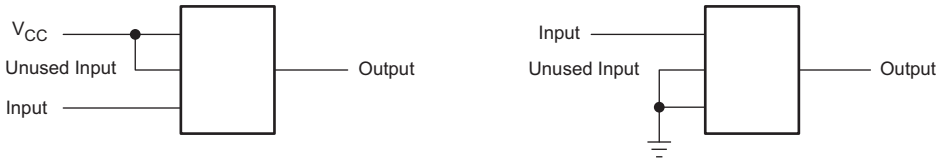


Figure 8. Proper multi-gate input termination diagram

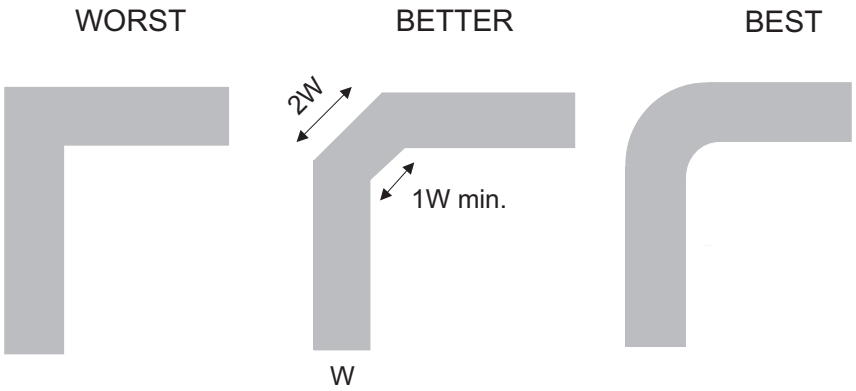


Figure 9. Trace Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Designing and Manufacturing with TI's X2SON Packages* Application Note
- Texas Instruments, *How to Select Little Logic* Application Note
- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* Application Note.
- Texas Instruments, *Understanding and Interpreting Standard-Logic Data Sheets* Application Note
- Texas Instruments, *Introduction to Logic* Application Note
- Texas Instruments, *Signal Switch Data Book* User's Guide
- Texas Instruments, *LVC and LV Low-Voltage CMOS Logic Data Book* User's Guide
- Texas Instruments, *Low-Voltage Logic (LVC) Designer's Guide* User's Guide

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

NanoStar, NanoFree, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC1G38DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN | NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C385, C38F, C38J, C38R) (C38H, C38P, C38S)
SN74LVC1G38DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C385 C38S
SN74LVC1G38DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU | SN | NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C385, C38J, C38R) (C38H, C38S)
SN74LVC1G38DBVTG4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C385 C38S
SN74LVC1G38DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN | NIPDAU	Level-1-260C-UNLIM	-40 to 125	(D75, D7F, D7J, D7R) (D7H, D7P, D7S)
SN74LVC1G38DCKRG4	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D75 D7S
SN74LVC1G38DCKT	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU | SN | NIPDAU	Level-1-260C-UNLIM	-40 to 125	(D75, D7J, D7R) (D7H, D7S)
SN74LVC1G38DPWR	Active	Production	X2SON (DPW) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BP
SN74LVC1G38DRYR	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	D7
SN74LVC1G38DSFR	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	D7

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

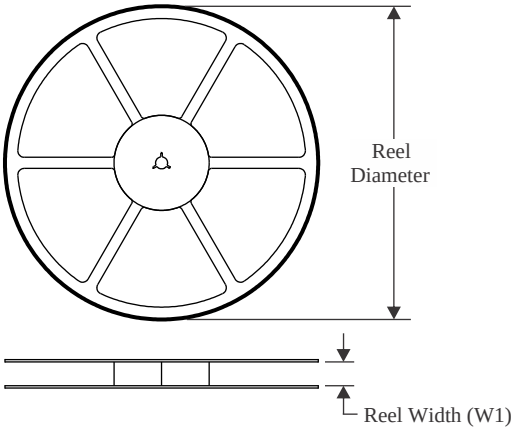
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

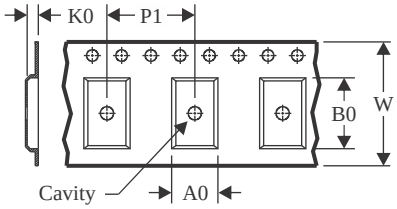
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

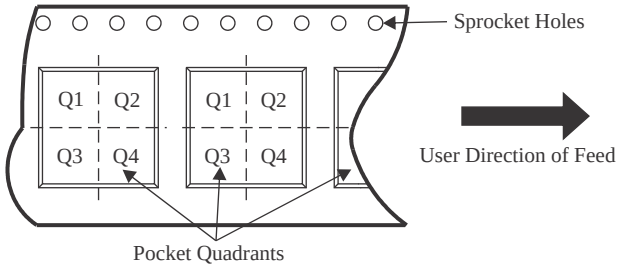


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

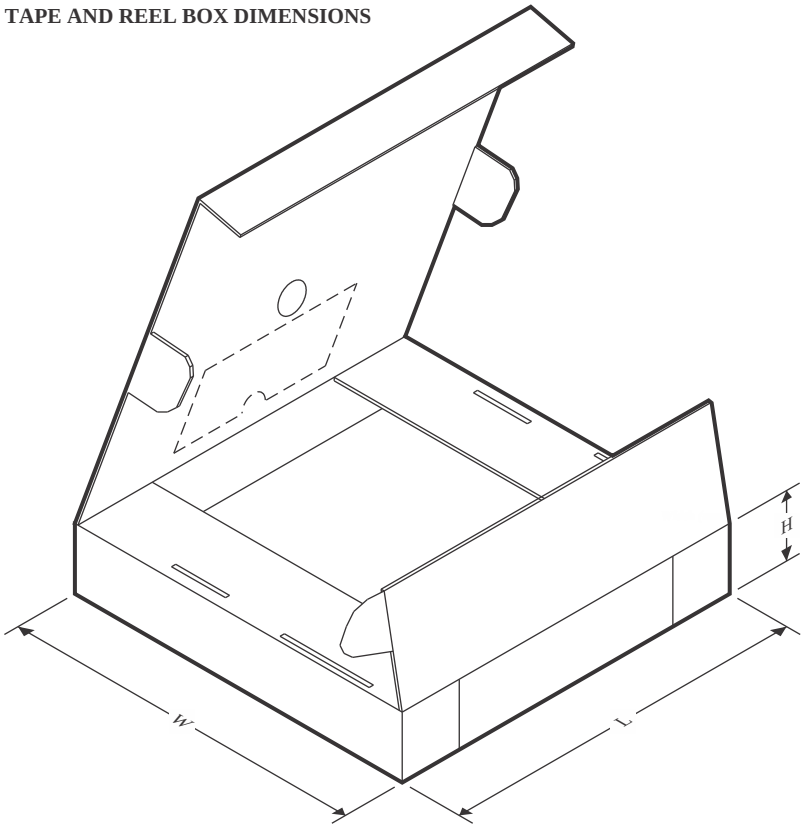
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G38DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G38DBVRG4	SOT-23	DBV	5	3000	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74LVC1G38DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G38DBVTG4	SOT-23	DBV	5	250	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74LVC1G38DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
SN74LVC1G38DCKRG4	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G38DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G38DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G38DCKT	SC70	DCK	5	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74LVC1G38DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q3
SN74LVC1G38DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC1G38DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G38DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74LVC1G38DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G38DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
SN74LVC1G38DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G38DCKR	SC70	DCK	5	3000	210.0	185.0	35.0
SN74LVC1G38DCKRG4	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G38DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G38DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G38DCKT	SC70	DCK	5	250	202.0	201.0	28.0
SN74LVC1G38DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
SN74LVC1G38DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G38DSFR	SON	DSF	6	5000	184.0	184.0	19.0

GENERIC PACKAGE VIEW

DPW 5 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

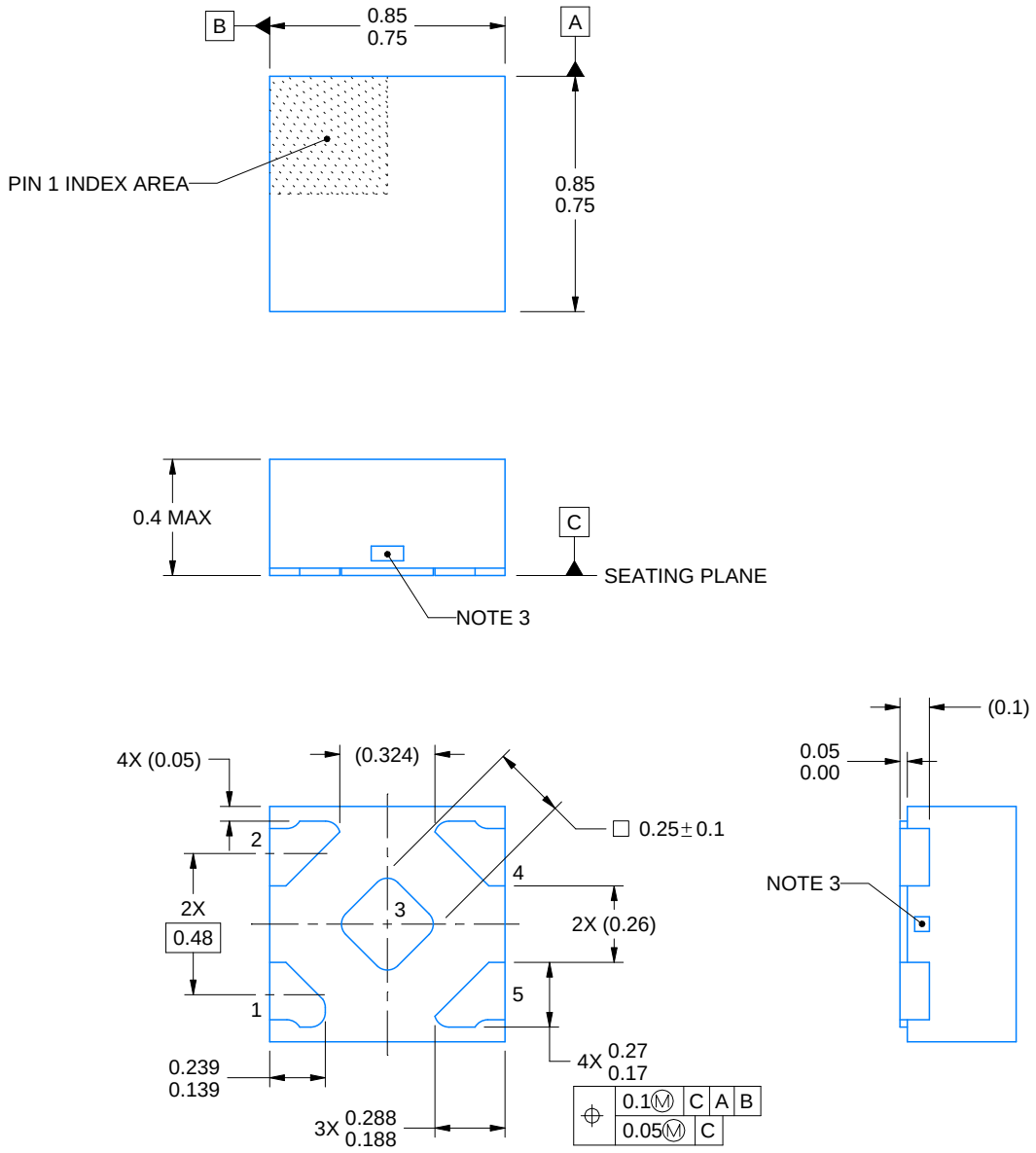
4211218-3/D

PACKAGE OUTLINE

DPW0005A

X2SON - 0.4 mm max height

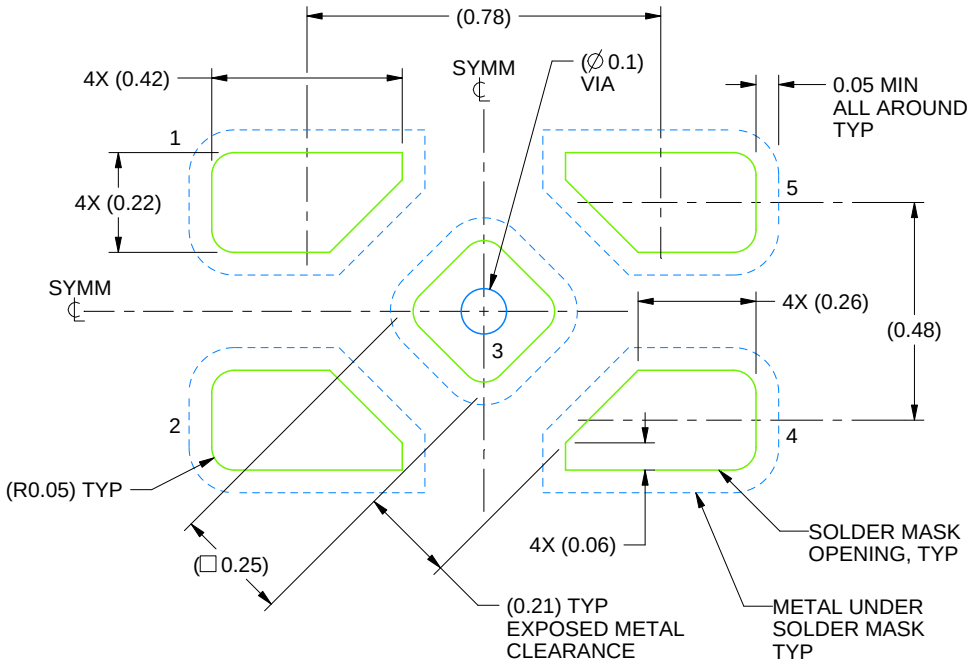
PLASTIC SMALL OUTLINE - NO LEAD



4223102/D 03/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/D 03/2022

NOTES: (continued)

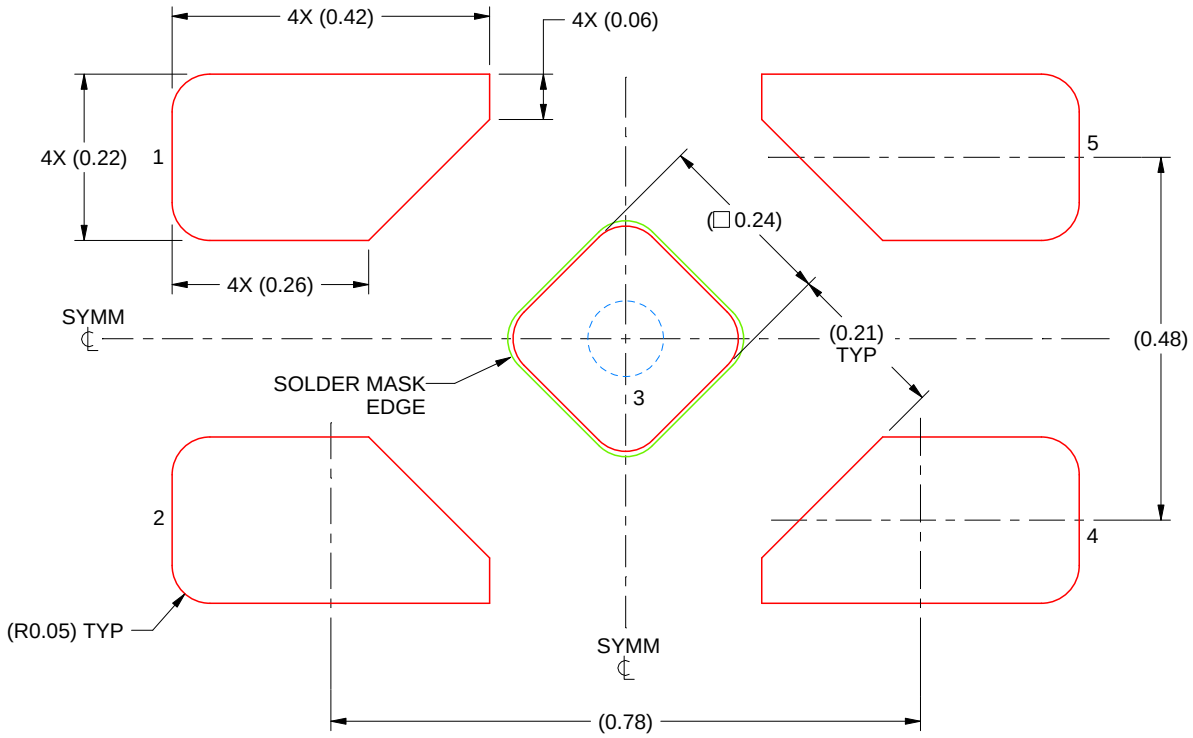
4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

4223102/D 03/2022

NOTES: (continued)

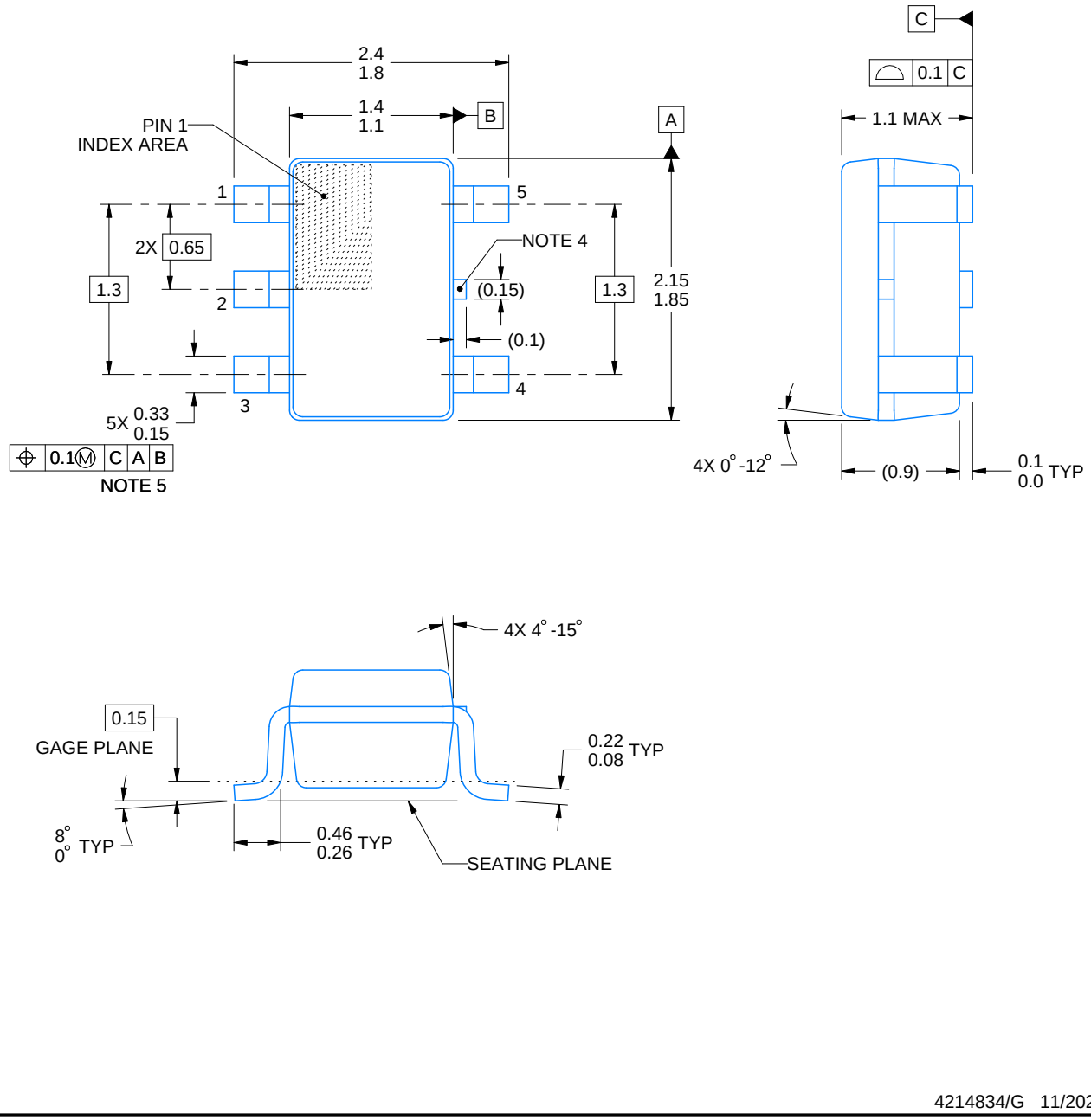
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

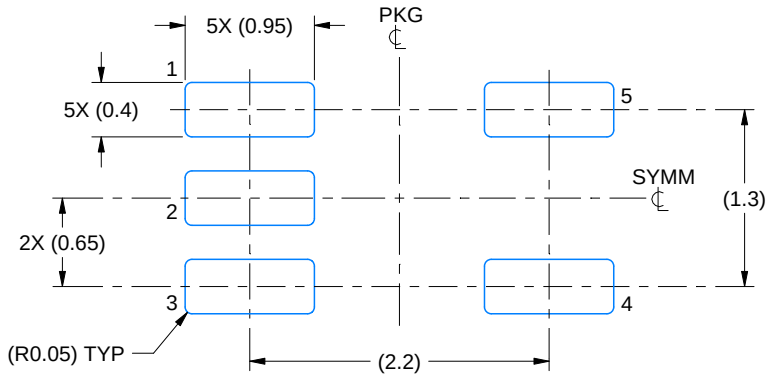
SMALL OUTLINE TRANSISTOR



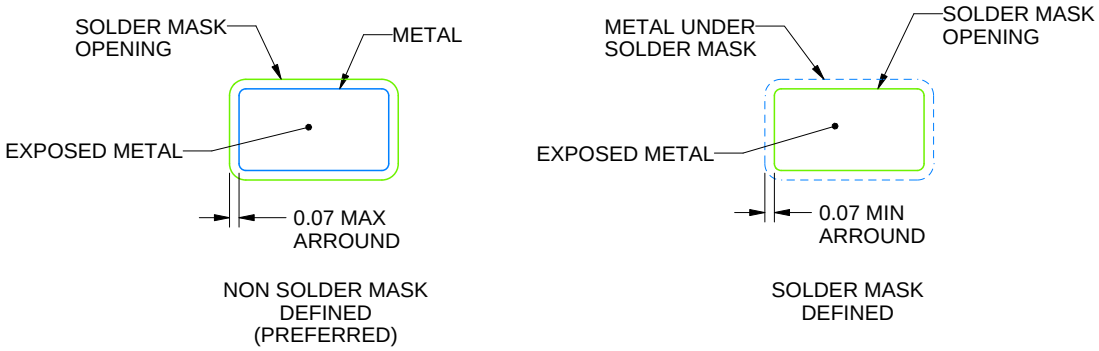
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

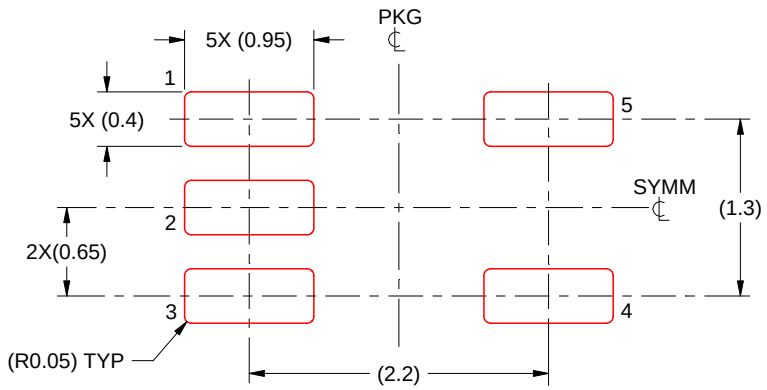


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

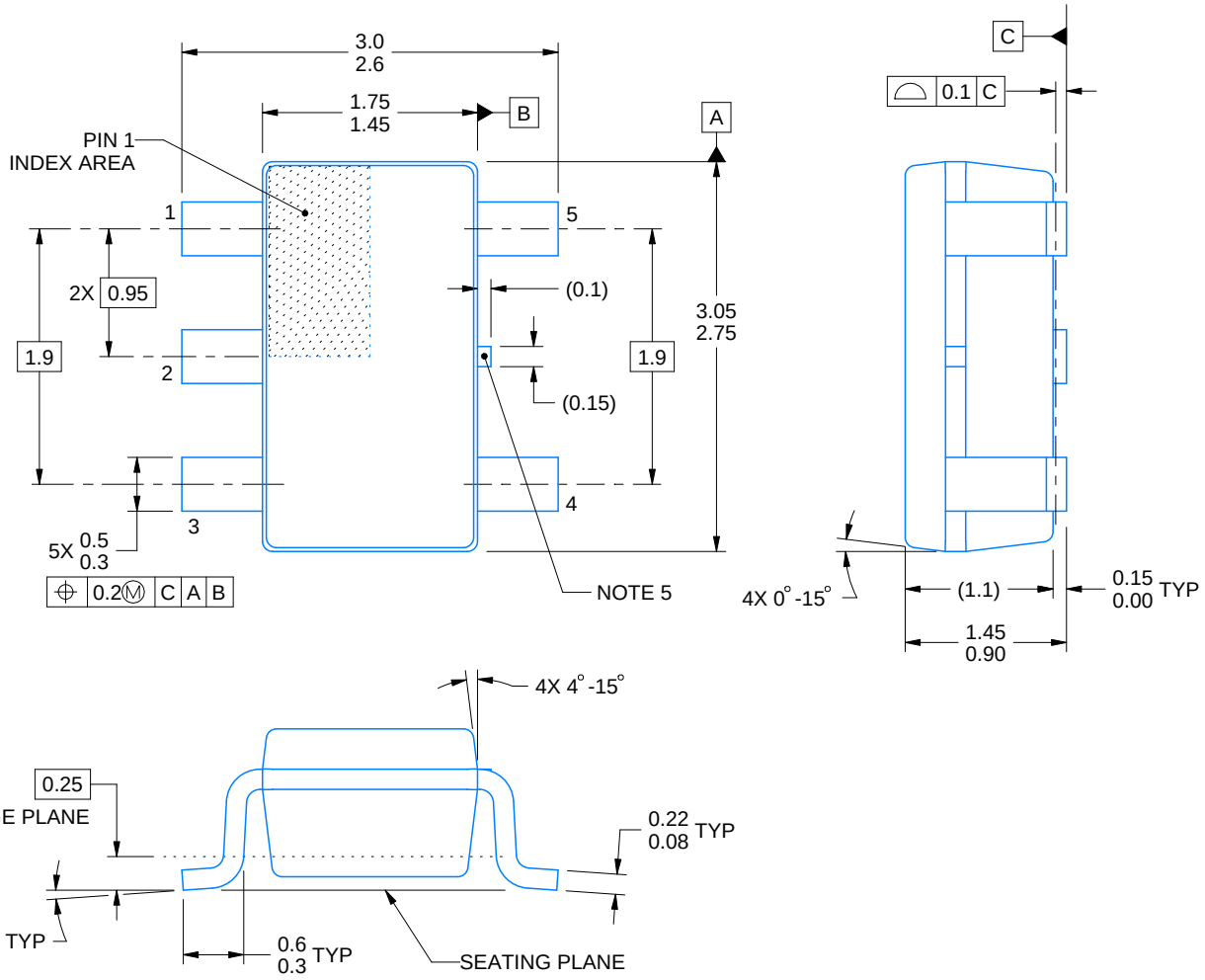
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

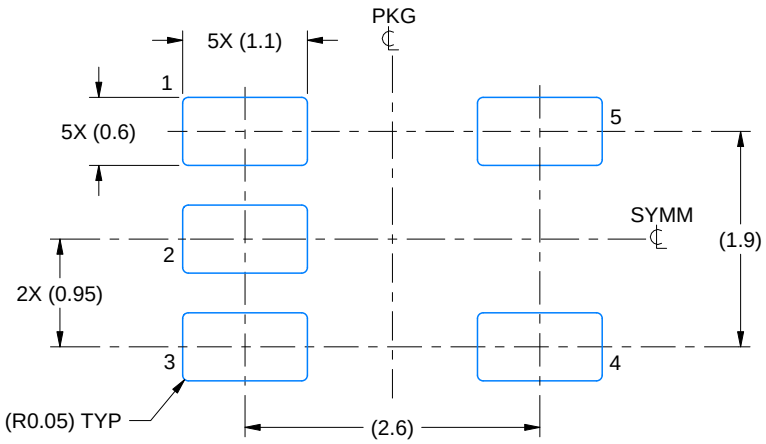
SMALL OUTLINE TRANSISTOR



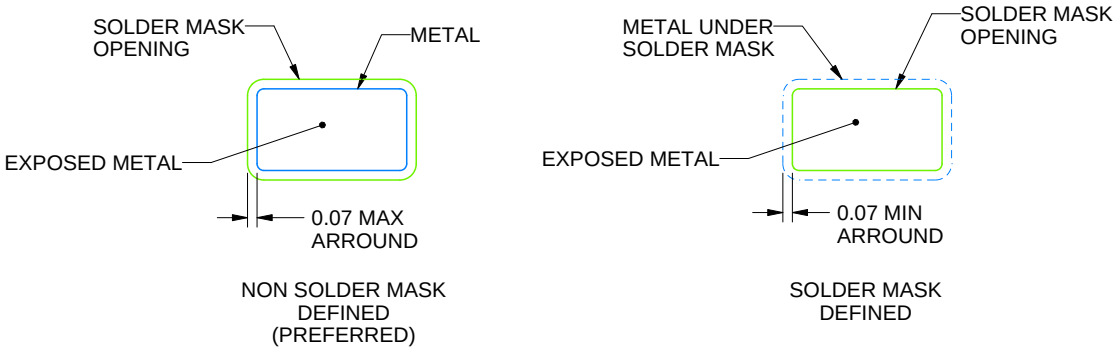
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

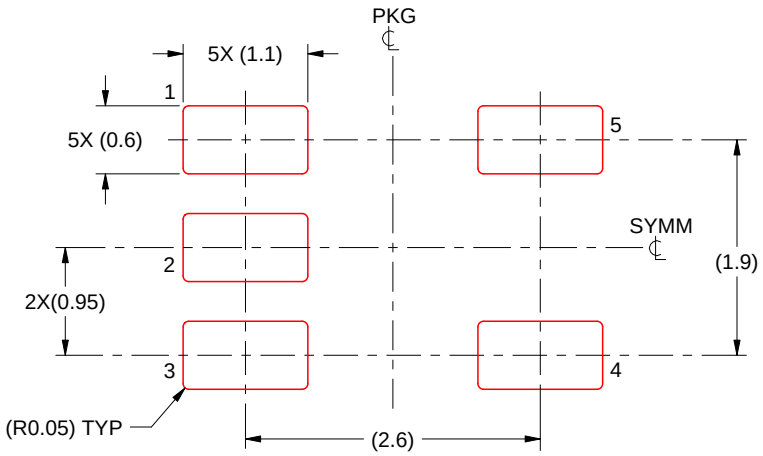


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

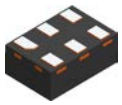
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DRY 6 USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

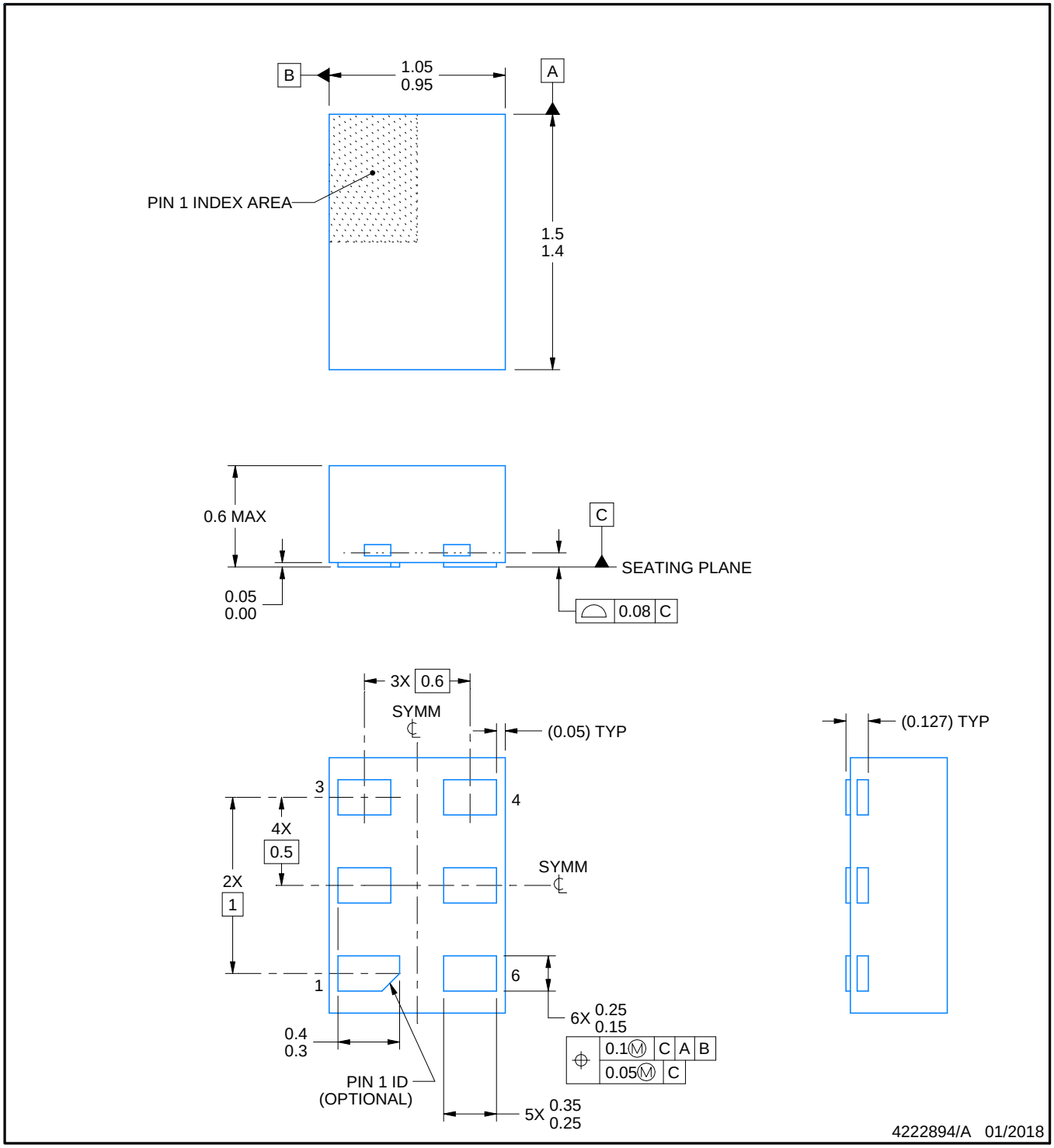
DRY0006A



PACKAGE OUTLINE

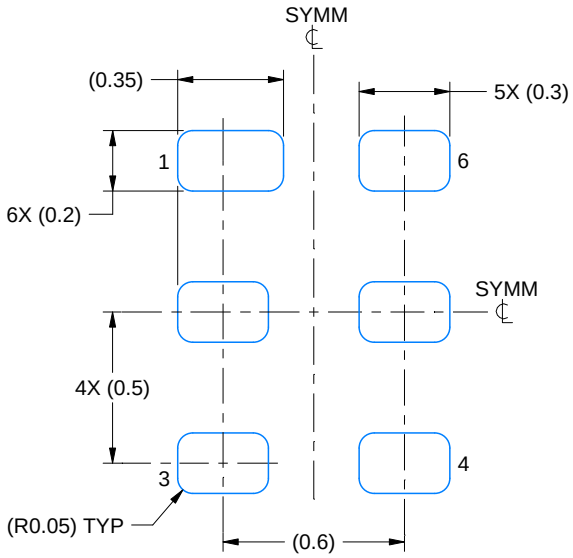
USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

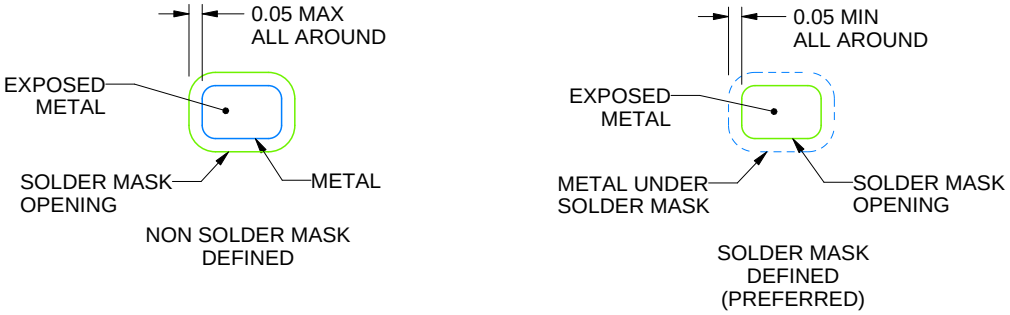


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

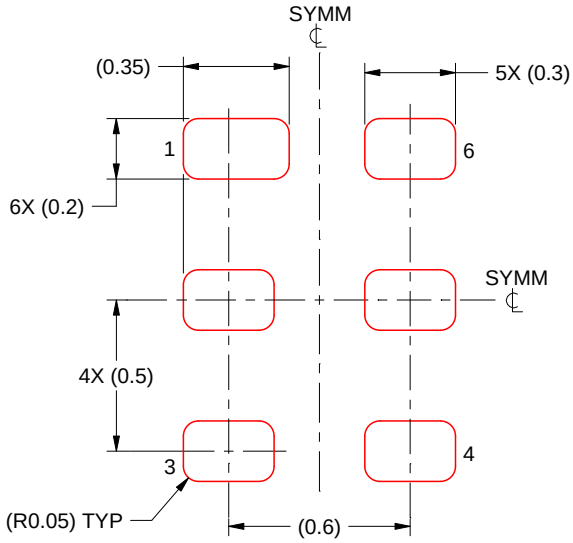
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

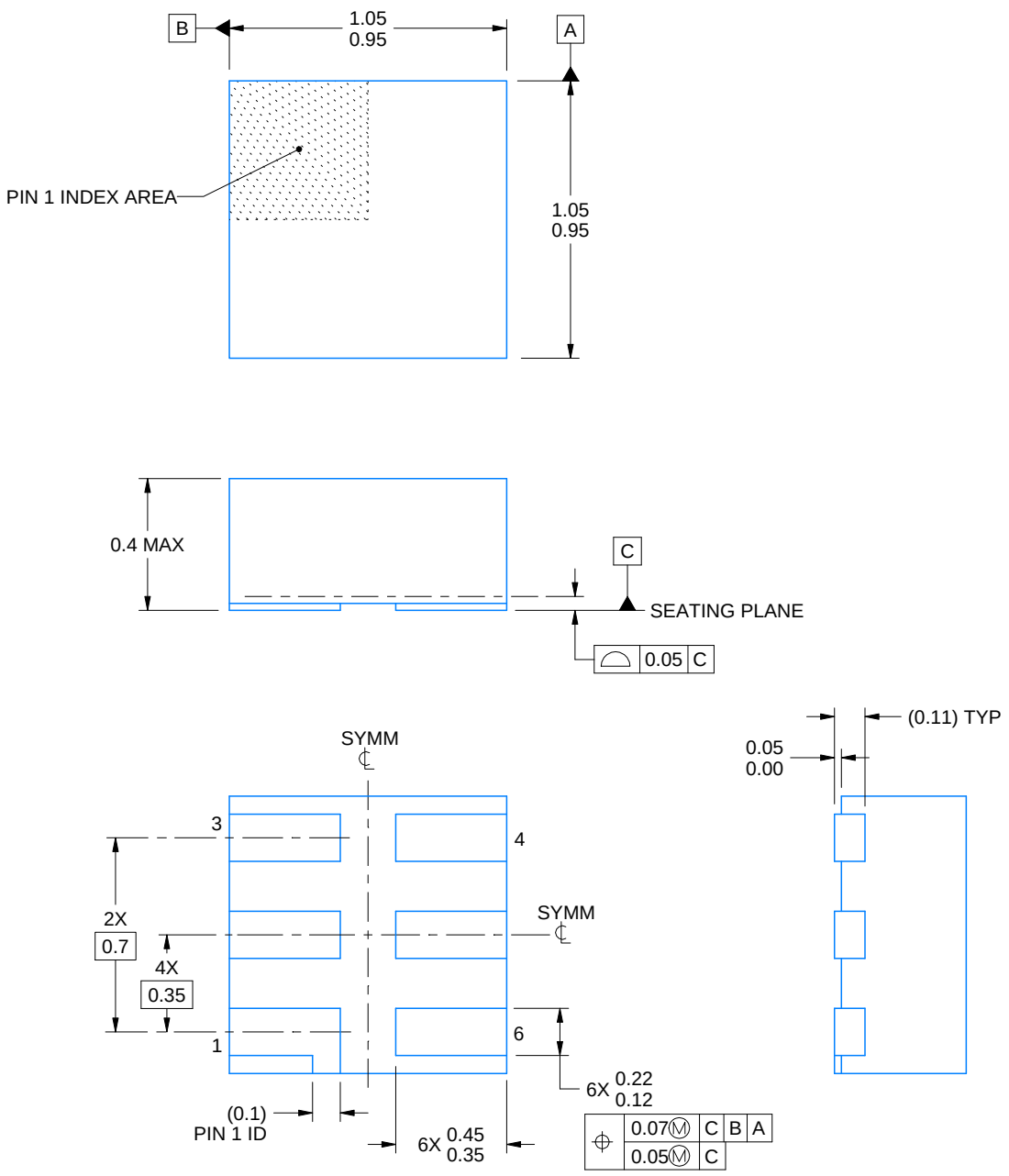
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DSF0006A

X2SON - 0.4 mm max height

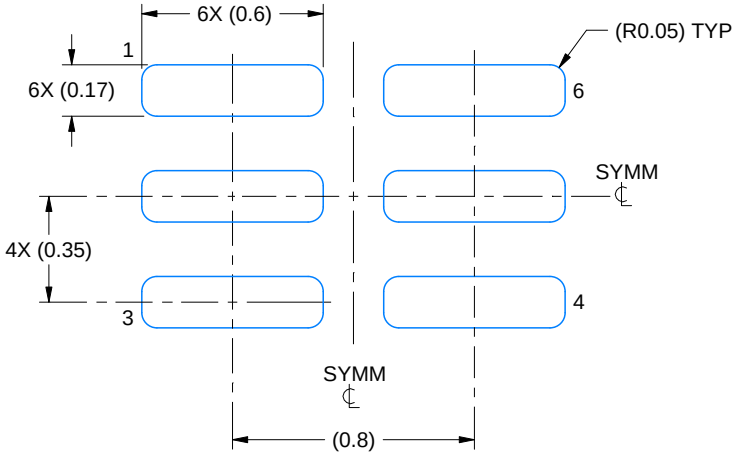
PLASTIC SMALL OUTLINE - NO LEAD



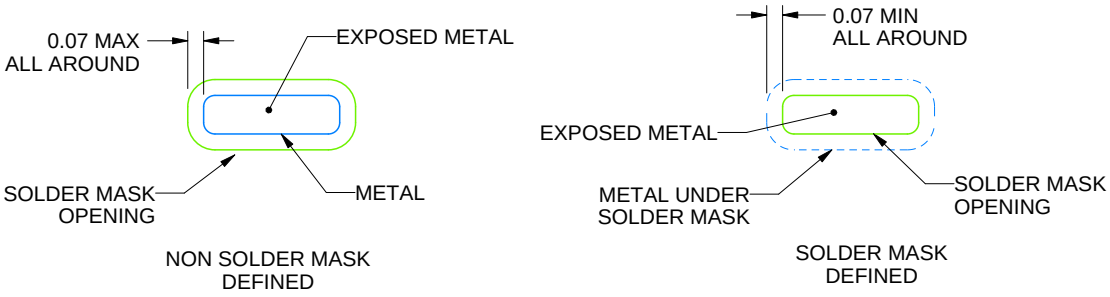
4220597/B 06/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

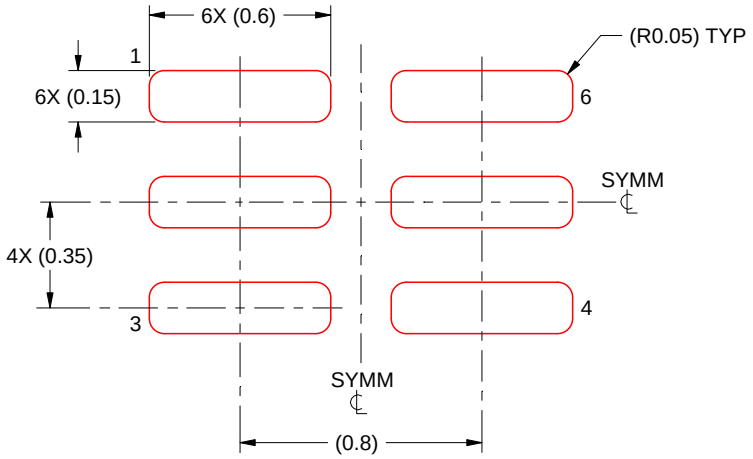
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/B 06/2022

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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