TPS7A7001 具有使能端的极低输入、极低压降 2A 稳压器

1 特性

- 输入电压低至 1.425V
- 2A 时的最大压降为 380mV
- 可调输出从 0.5V 开始
- 保护：电流限制和热关断
- 启用引脚
- 关断模式下静态电流 1μA
- 全工业温度范围
- 采用完全符合 RoHS 标准的小外形尺寸 (SO)-8 封装

2 应用

- 电信和网卡
- 主板和外设卡
- 工业应用
- 无线基础设施
- 机顶盒
- 医疗设备
- 笔记本电脑
- 电池供电系统

3 说明

TPS7A7001 是一款高性能、正电压、低压降 (LDO) 稳压器，专为 要求 在高达 2A 的电流下拥有超低输入电压和超低压降的应用而设计。该器件支持低至 1.425V 的单输入电压，输出电压最低可通过编程设定为 0.5V。输出电压可使用外部分压器进行设置。

TPS7A7001 具有 超低压降，非常 适用于 V_{OUT} 与 V_{IN} 极为接近的应用。此外，TPS7A7001 还具有使能引脚以便在关断模式下进一步降低功率耗散。TPS7A7001 在线路、负载和温度变化时提供出色的稳压功能。

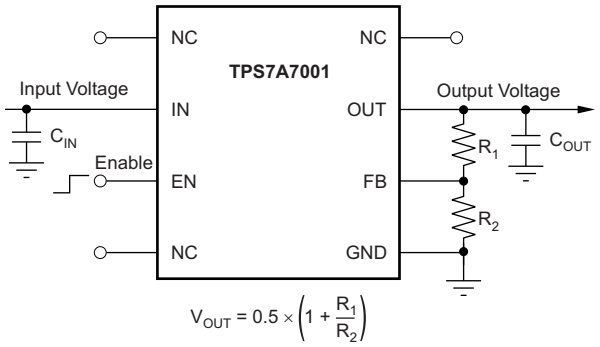
TPS7A7001 提供 8 引脚小型 PowerPAD™封装选项。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS7A7001	SO PowerPAD (8)	3.90mm x 4.89mm

(1) 要了解所有可用封装，请参见数据表末尾的封装选项附录。

典型应用



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision E (August 2015) to Revision F — **Page**

- Changed "operating free-air" to "junction" in *Absolute Maximum Ratings* table condition line ... 5
- Changed OUT pin max voltage from 7 to V_{IN} + 0.3 V or 7 V, whichever is smaller, in *Absolute Maximum Ratings* table (moved OUT from first row to second row) ... 5
- Deleted T_A, ambient temperature range, from *Recommended Operating Conditions* table ... 5
- Changed C_{OUT} max value from 47 µF to 200 µF in *Recommended Operating Conditions* table ... 5
- Added note (2) to *Recommended Operating Conditions* table regarding C_{OUT} max value ... 5
- Added feedforward capacitance to *Recommended Operating Conditions* table ... 5
- Deleted redundant notes 2 to 7 in the *Thermal Information* table; all information from deleted notes available in application report shown in note (1) ... 5
- Changed note (1) in *Electrical Characteristics*; deleted initial reference to R_1 and updated R_2 resistor range ... 6
- Changed *Output Capacitor (OUT)* section; reworded for clarity ... 10

Changes from Revision D (September 2013) to Revision E — **Page**

- 添加了 *ESD 额定值表*，*特性 描述*部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分。 ... 1

Changes from Revision C (January 2013) to Revision D — **Page**

- Added new text to *Internal Current Limit* section ... 8

Changes from Revision B (July 2012) to Revision C — **Page**

- Deleted maximum value for Output Current Limit parameter in *Electrical Characteristics* table ... 6

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Changes from Revision A (June 2012) to Revision B **Page**

- Changed Output Voltage, I_{LIM} parameter test conditions in *Electrical Characteristics* table 6

Changes from Original (January 2012) to Revision A **Page**

- 更改了*可调输出*特性着重号 1
- 已更改*说明*部分第一段中输出电压的最小值 1
- Changed *Electrical Characteristics* condition line 6
- Changed *Output Voltage Accuracy* parameter in *Electrical Characteristics* 6
- Changed test conditions for *Dropout Voltage* parameter in *Electrical Characteristics* 6
- Changed note (1) in *Electrical Characteristics* 6
- Added new note (4) to *Electrical Characteristics* 6

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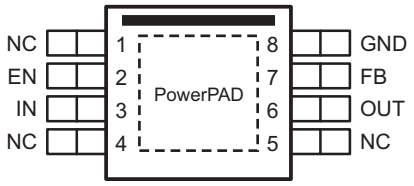
5 Pin Configuration and Functions

DDA Package
8-Pin SO PowerPAD
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	2	I	Enable input. Pulling this pin below 0.5 V turns the regulator off. Connect to V_{IN} if not being used.
FB	7	I	This pin is the output voltage feedback input through voltage dividers. See the Table 2 for more details.
GND	8	–	Ground pin
IN	3	I	Unregulated supply voltage pin. It is recommended to connect an input capacitor to this pin.
NC	1, 4, 5	–	Not internally connected. The NC pins are not connected to any electrical node. It is recommended to connect the NC pins to large-area planes.
OUT	6	O	Regulated output pin. A 4.7-µF or larger capacitor of any type is required for stability.
PowerPAD			TI strongly recommends connecting the thermal pad to a large-area ground plane. If an electrically floating, dedicated thermal plane is available, the thermal pad can also be connected to it.

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6 Specifications

6.1 Absolute Maximum Ratings

over junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	IN	–0.3	7	V
	EN, FB, OUT	–0.3	V_{IN} + 0.3(2)	
Current	OUT		Internally limited	A
Temperature	Operating virtual junction, T_J	–55	150	°C
	Storage, T_{stg}	–55	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The absolute maximum rating is V_{IN} + 0.3 V or 7.0 V, whichever is smaller.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	1.425		6.5	V
V_{EN}	Enable pin voltage	0		V_{IN}	V
C_{IN}	Input capacitor	1		10	µF
C_{OUT}	Output capacitor(1)(2)	4.7	10	200	µF
C_{FB}	Feedforward capacitance	0		100	nF
I_{OUT}	Output current	0		2	A
T_J	Junction temperature	–40		125	°C

(1) See Figure 1 and Figure 2 for additional output capacitor ESR requirements.
(2) For output capacitors larger than 47 µF, a feedforward capacitor of at least 220 pF must be used.

6.4 Thermal Information

THERMAL METRIC(1)		TPS7A7001 DDA (SO PowerPAD) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	29.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

Over the full operating temperature range (see *Recommended Operating Conditions*), V_{EN} = 1.1 V, $V_{FB} = V_{OUT}$(1), 1.425 V ≤ V_{IN} ≤ 6.5 V, 10 µA ≤ I_{OUT} ≤ 2 A, C_{OUT} = 10 µF (unless otherwise noted). Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE						
I_{GND}	GND pin current (small)	V_{IN} = 3.3 V, 50-Ω load resistor between OUT and GND			3	mA
	GND pin current (shutdown)	V_{IN} = 6.5 V, V_{EN} = 0 V			5	µA
OUTPUT VOLTAGE						
V_{OUT}	Output voltage accuracy(2)(3)	$V_{IN} = V_{OUT}$ + 0.5 V(4), I_{OUT} = 10 mA	–2%		2%	
		V_{IN} = 1.8 V, I_{OUT} = 0.8 A, 0°C ≤ $T_J = T_A$ ≤ +85°C	–2%		2%	
		I_{OUT} = 10 mA	–3%		3%	
$\Delta V_{O(\Delta VI)}$	Line regulation	I_{OUT} = 10 mA		0.2	0.4	%/V
$\Delta V_{O(\Delta IO)}$	Load regulation(3)	10 mA ≤ I_{OUT} ≤ 2 A		0.25	0.75	%/A
V_{DO}	Dropout voltage (5)	I_{OUT} = 1.0 A, 0.5 V ≤ V_{OUT} ≤ 5.0 V			200	mV
		I_{OUT} = 1.5 A, 0.5 V ≤ V_{OUT} ≤ 5.0 V			300	
		I_{OUT} = 2.0 A, 0.5 V ≤ V_{OUT} ≤ 5.0 V			380	
I_{LIM}	Output current limit	V_{IN} = 1.425 V, V_{OUT} = 0.9 × $V_{OUT(NOM)}$	2.1			A
FEEDBACK						
V_{REF}	Reference voltage accuracy	V_{IN} = 3.3 V, $V_{FB} = V_{OUT}$, I_{OUT} = 10 mA	0.490	0.500	0.510	V
I_{FB}	FB pin current	V_{FB} = 0.5 V			1	µA
ENABLE						
I_{EN}	EN pin current	V_{EN} = 0 V, V_{IN} = 3.3 V			0.2	µA
VIL_{EN}	EN pin input low (disable)	V_{IN} = 3.3 V	0		0.5	V
VIH_{EN}	EN pin input high (enable)	V_{IN} = 3.3 V	1.1		V_{IN}	V
TEMPERATURE						
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		160		°C
		Reset, temperature decreasing		140		°C

(1) When setting V_{OUT} to a value other than 0.5 V, connect R_2 to the FB pin using 27-kΩ ≤ R_2 ≤ 33-kΩ resistors. See Functional Block Diagram for details of R_1 and R_2.
(2) Accuracy does not include error on feedback resistors R_1 and R_2.
(3) TPS7A7001 is not tested at V_{OUT} = 0.5 V, 2.3 V ≤ V_{IN} ≤ 6.5 V, and 500 mA ≤ I_{OUT} ≤ 2 A because the power dissipation is higher than the maximum rating of the package. Also, this accuracy specification does not apply to any application condition that exceeds the power dissipation limit of the package.
(4) $V_{IN} = V_{OUT}$ + 0.5 V or 1.425 V, whichever is greater.
(5) $V_{DO} = V_{IN} - V_{OUT}$ with V_{FB} = GND configuration.

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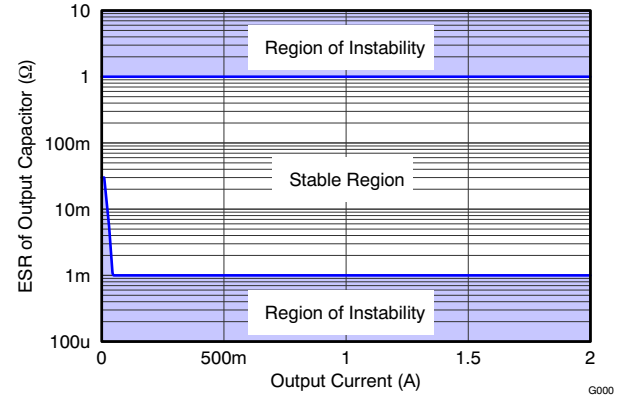
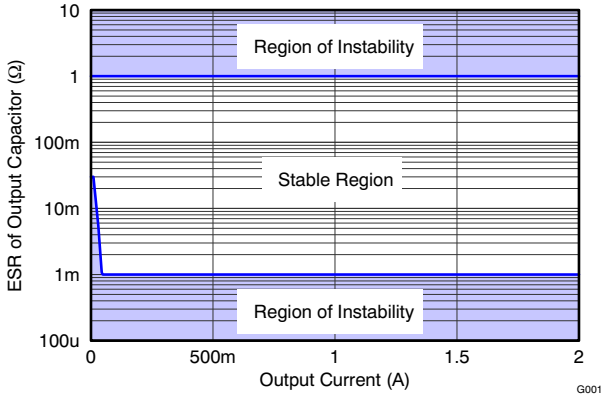
6.6 Typical Characteristics

for all fixed voltage versions and an adjustable version at T_J = 25°C, V_{EN} = V_{IN}, C_{IN} = 10 µF, C_{OUT} = 10 µF, and using the component values in Table 2 (unless otherwise noted)



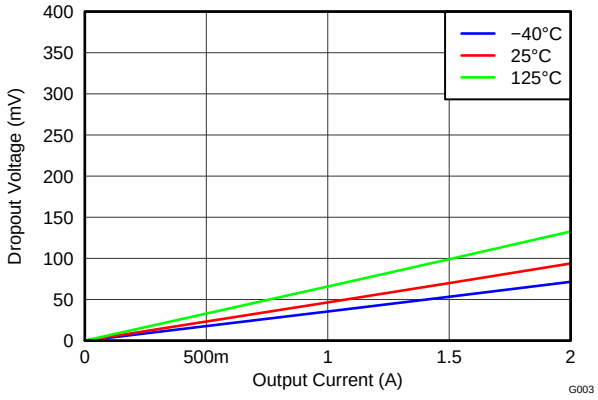
C_{OUT} = 10 µF

Figure 1. Stability Curve



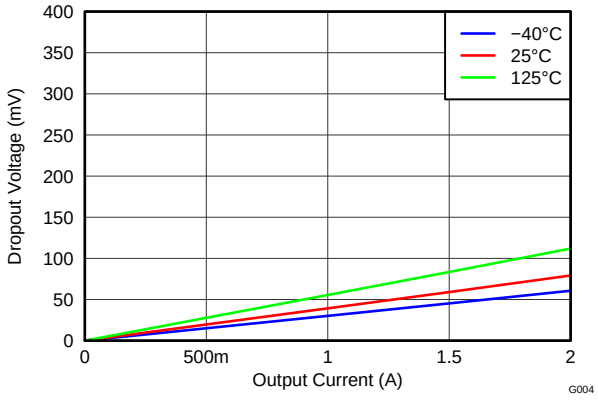
C_{OUT} = 100 µF

Figure 2. Stability Curve



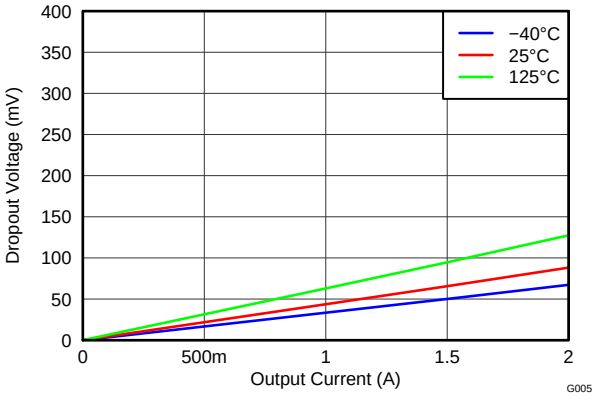
V_{OUT} = 3.3 V

Figure 3. Dropout Voltage vs Output Current



V_{OUT} = 1.6 V

Figure 4. Dropout Voltage vs Output Current



V_{OUT} = 1.4 V

Figure 5. Dropout Voltage vs Output Current

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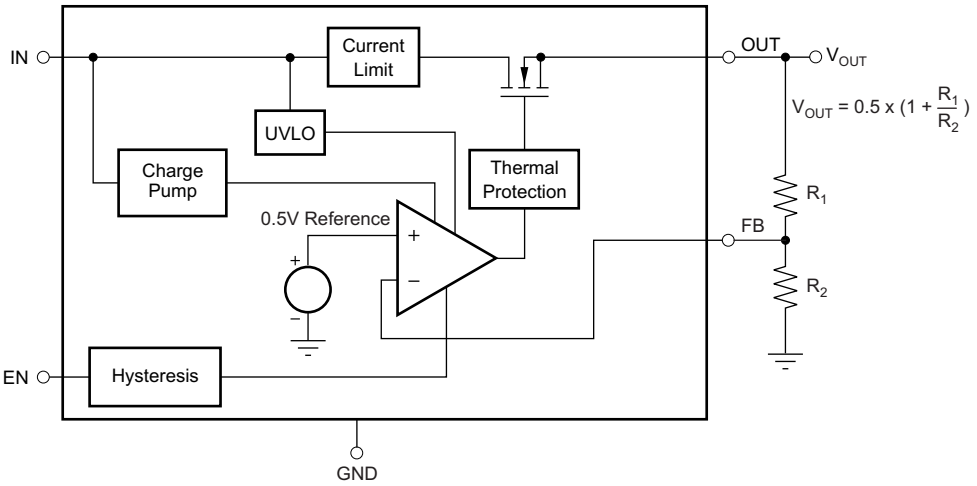
7 Detailed Description

7.1 Overview

The TPS7A7001 offers a high current supply with very low dropout voltage. The TPS7A7001 is designed to minimize the required component count for a simple, small-size, and low-cost solution.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable (EN)

The enable pin (EN) is an active high logic input. When it is logic low, the device turns off and its consumption current is less than 1 µA. When it is logic high, the device turns on. The EN pin is required to be connected to a logic high or logic low level.

When the enable function is not required, connect EN to VIN.

7.3.2 Internal Current Limit

The TPS7A7001 internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, the device should not be operated in a current limit state for extended periods of time.

Powering on the device with the enable pin, or increasing the input voltage above the minimum operating voltage while a low-impedance short exists on the output of the device, may result in a sequence of high-current pulses from the input to the output of the device. The energy consumed by the device is minimal during these events; therefore, there is no failure risk. Additional input capacitance helps to mitigate the load transient requirement of the upstream supply during these events.

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7.4 Device Functional Modes

Table 1 provides a quick comparison between the normal, dropout, and disabled modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	EN	I_{OUT}	T_J
Normal	$V_{IN} > V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$
Dropout	$V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$
Disabled	—	$V_{EN} < V_{EN(LO)}$	—	$T_J > T_{SD}$

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$).
- The enable voltage has previously exceeded the enable rising threshold voltage and not yet decreased below the enable falling threshold.
- The output current is less than the current limit ($I_{OUT} < I_{CL}$).
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$).

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass device is in a triode state and no longer controls the current through the LDO. Line or load transients in dropout can result in large output-voltage deviations.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Input Capacitor (IN)

Although an input capacitor is not required for stability, it is recommended to connect a 1-µF to 10-µF low equivalent series resistance (ESR) capacitor across IN and GND near the device.

8.1.2 Output Capacitor (OUT)

The TPS7A7001 is stable with standard ceramic capacitors with capacitance values from 4.7 µF to 47 µF without a feedforward capacitor. For output capacitors from 47 µF to 200 µF, a feedforward capacitor of at least 220 pF must be used. The TPS7A7001 is evaluated using an X5R-type, 10-µF ceramic capacitor. X5R- and X7R-type capacitors are recommended because of minimal variation in value and ESR over temperature. Maximum ESR must be less than 1 Ω.

As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude, but increases duration of the transient response.

8.1.3 Feedback Resistors (FB)

The voltage on the FB pin sets the output voltage and is determined by the values of R_1 and R_2. The values of R_1 and R_2 can be calculated for any voltage using the formula given in Equation 1:

$$V_{OUT} = 0.5 \times \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

Table 2 shows the recommended resistor values for the best performance of the TPS7A7001. If the values in Table 2 are not used, keep the value of R2 between 27 kΩ and 33 kΩ. In Table 2, E96 series resistors are used. For the actual design, pay attention to any resistor error factors.

Table 2. Sample Resistor Values for Common Output Voltages

V_{OUT}	R_1	R_2
1.0 V	30.1 kΩ	30.1 kΩ
1.2 V	42.2 kΩ	30.1 kΩ
1.5 V	60.4 kΩ	30.1 kΩ
1.8 V	78.7 kΩ	30.1 kΩ
2.5 V	121 kΩ	30.1 kΩ
3.0 V	150 kΩ	30.1 kΩ
3.3 V	169 kΩ	30.1 kΩ
5.0 V	274 kΩ	30.1 kΩ

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8.2 Typical Application

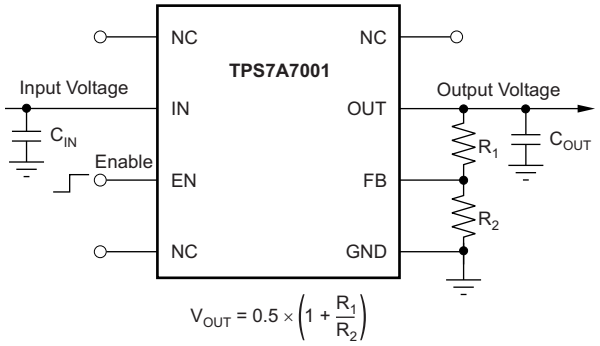


Figure 6. Typical Application

8.2.1 Design Requirements

Table 3 lists the design parameters.

Table 3. Design Parameters

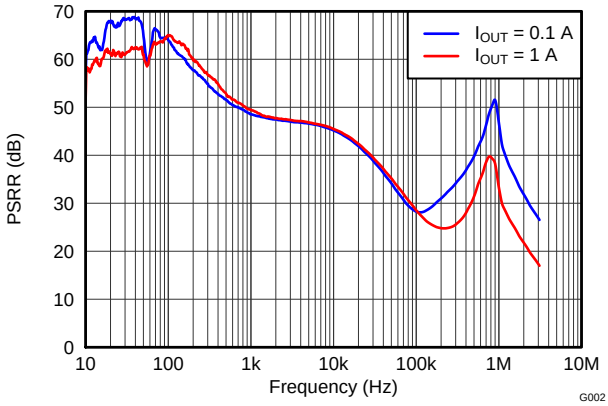
PARAMETER	DESIGN REQUIREMENT
Input voltage	3.3 V
Output voltage	2.5 V
Maximum output current	1.2 A

8.2.2 Detailed Design Procedure

Select the desired device based on the output voltage.

Provide an input supply with adequate headroom to account for dropout and output current to account for the GND terminal current, and power the load.

8.2.3 Application Curve



V_{IN} = 5.0 V, V_{OUT} = 3.3 V

Figure 7. Power-Supply Ripple Rejection vs Frequency

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9 Power Supply Recommendations

These devices are designed to operate from an input voltage supply range between 1.425 V and 6.5 V. The input voltage range provides adequate headroom in order for the device to have a regulated output. This input supply is well regulated and stable. If the input supply is noisy, additional input capacitors with low ESR help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

10.1.1 Board Layout Recommendation to Improve PSRR and Noise Performance

To improve ac measurements like PSRR, output noise, and transient response, use the board design shown in the layout example of Figure 8.

10.2 Layout Example

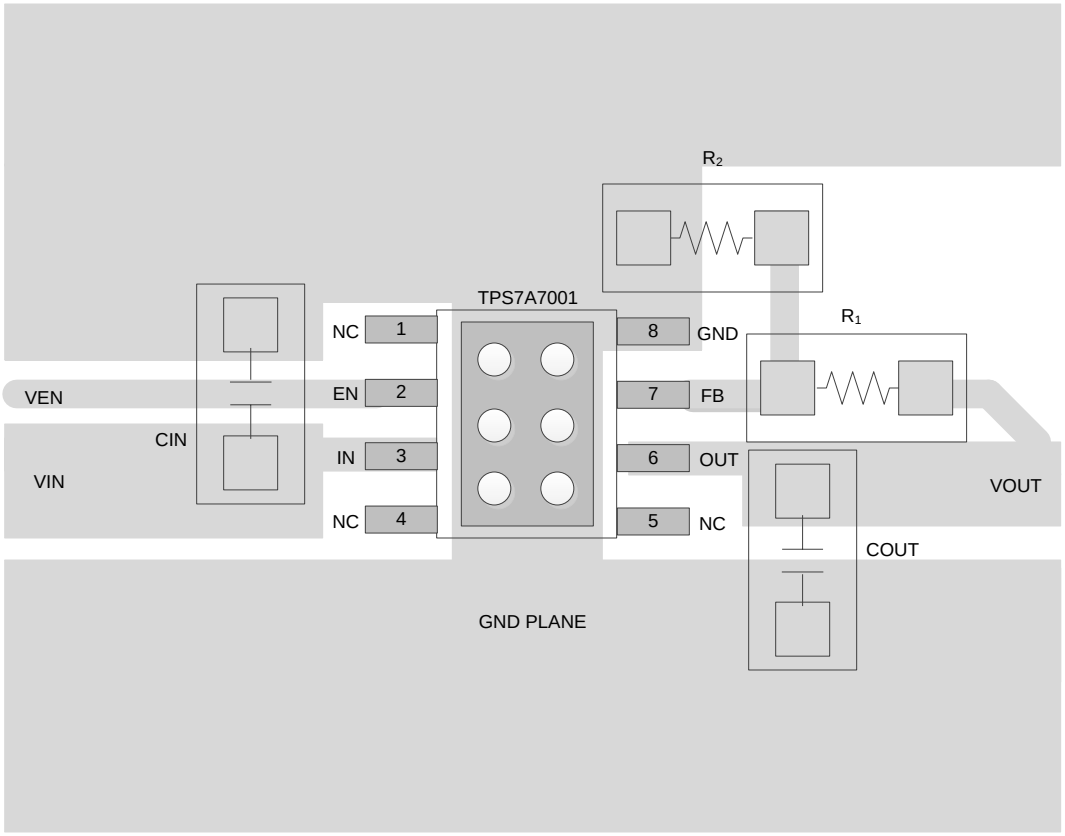

Figure 8. Layout Example

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10.3 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is re-enabled.

The internal protection circuitry of the TPS7A7001 is designed to protect against overload conditions. The protection circuitry is not intended to replace proper heat sinking. Continuously running the TPS7A7001 into thermal shutdown degrades device reliability.

10.4 Power Dissipation

Power dissipation (P_D) of the device depends on the input voltage and load conditions and is calculated using Equation 2:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

In order to minimize power dissipation and achieve greater efficiency, use the lowest possible input voltage necessary to achieve the required output voltage regulation

On the SO (DDA) package, the primary conduction path for heat is through the exposed pad to the printed circuit board (PCB). The pad can be connected to ground or left floating; however, attach the pad to an appropriate amount of copper PCB area to prevent the device from overheating. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device, and is calculated using Equation 3:

$$R_{\theta JA} = \left(\frac{+125°C - T_A}{P_D} \right) \quad (3)$$

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11 器件和文档支持

11.1 器件支持

11.1.1 器件命名规则

产品(1)	说明
TPS7A7001**yyyz**	YYY 为封装标识符。 Z 为封装数量。

(1) 要获得最新的封装和订货信息，请参阅本文档末尾的封装选项附录，或者访问器件产品文件夹，此文件夹位于www.ti.com内。

11.2 文档支持

11.2.1 相关文档

相关文档如下：

- *TI LDO 应用手册的主题索引*
- *半导体和集成电路 (IC) 封装热度量*

11.3 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

11.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 商标

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11.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7A7001DDA	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	QVH
TPS7A7001DDA.B	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QVH
TPS7A7001DDAR	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	QVH
TPS7A7001DDAR.B	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QVH

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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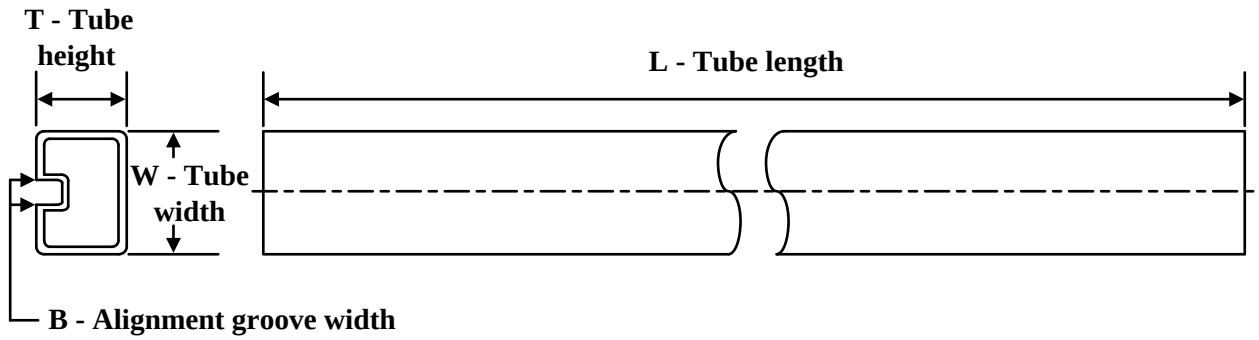
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TUBE

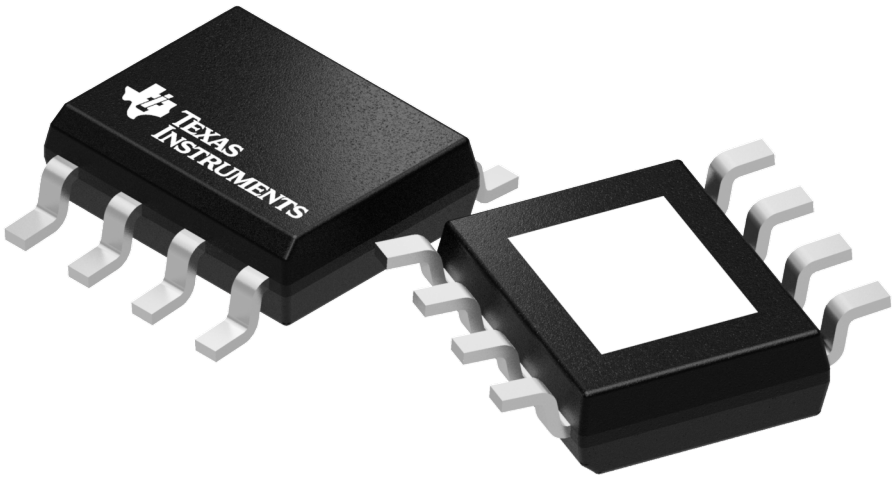


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS7A7001DDA	DDA	HSOIC	8	75	517	7.87	635	4.25
TPS7A7001DDA	DDA	HSOIC	8	75	507	8	3940	4.32
TPS7A7001DDA.B	DDA	HSOIC	8	75	507	8	3940	4.32
TPS7A7001DDA.B	DDA	HSOIC	8	75	517	7.87	635	4.25

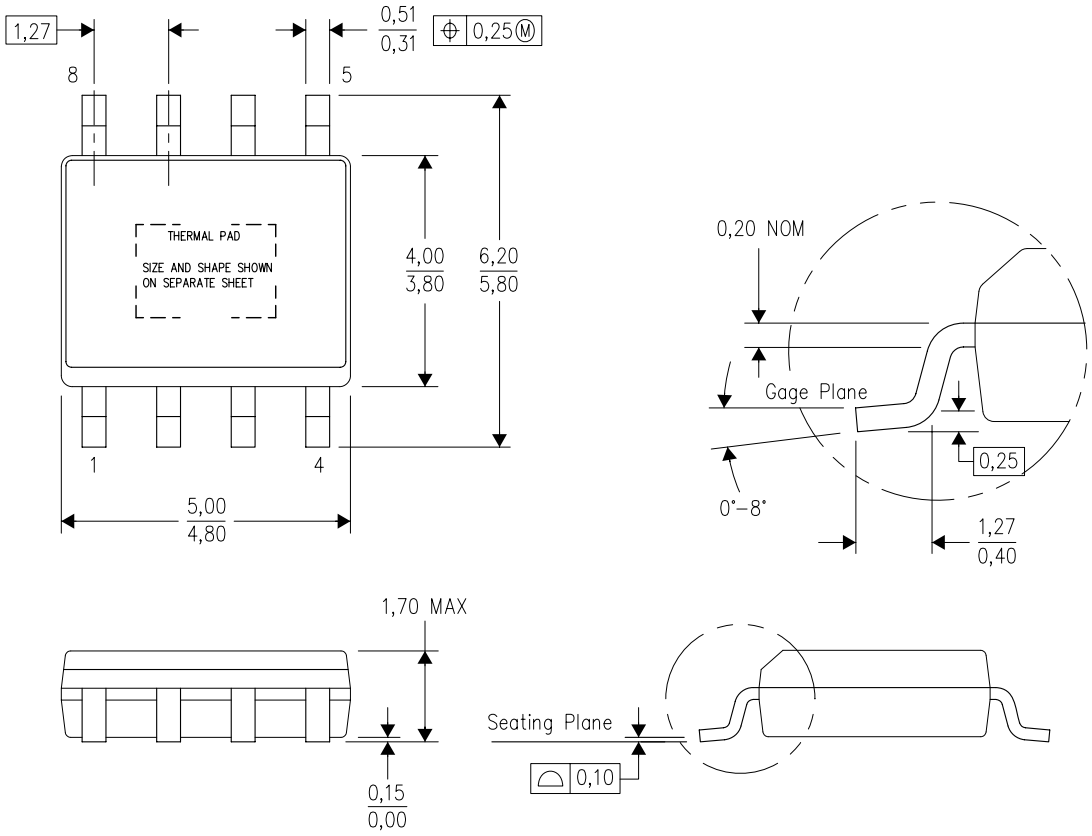
DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

PowerPAD is a trademark of Texas Instruments.

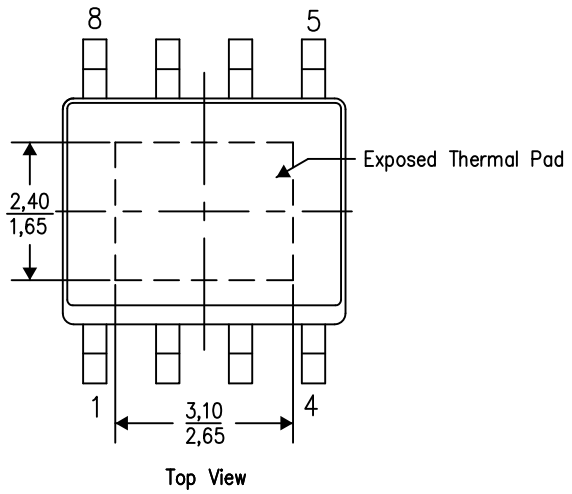
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206322–6/L 05/12

NOTE: A. All linear dimensions are in millimeters

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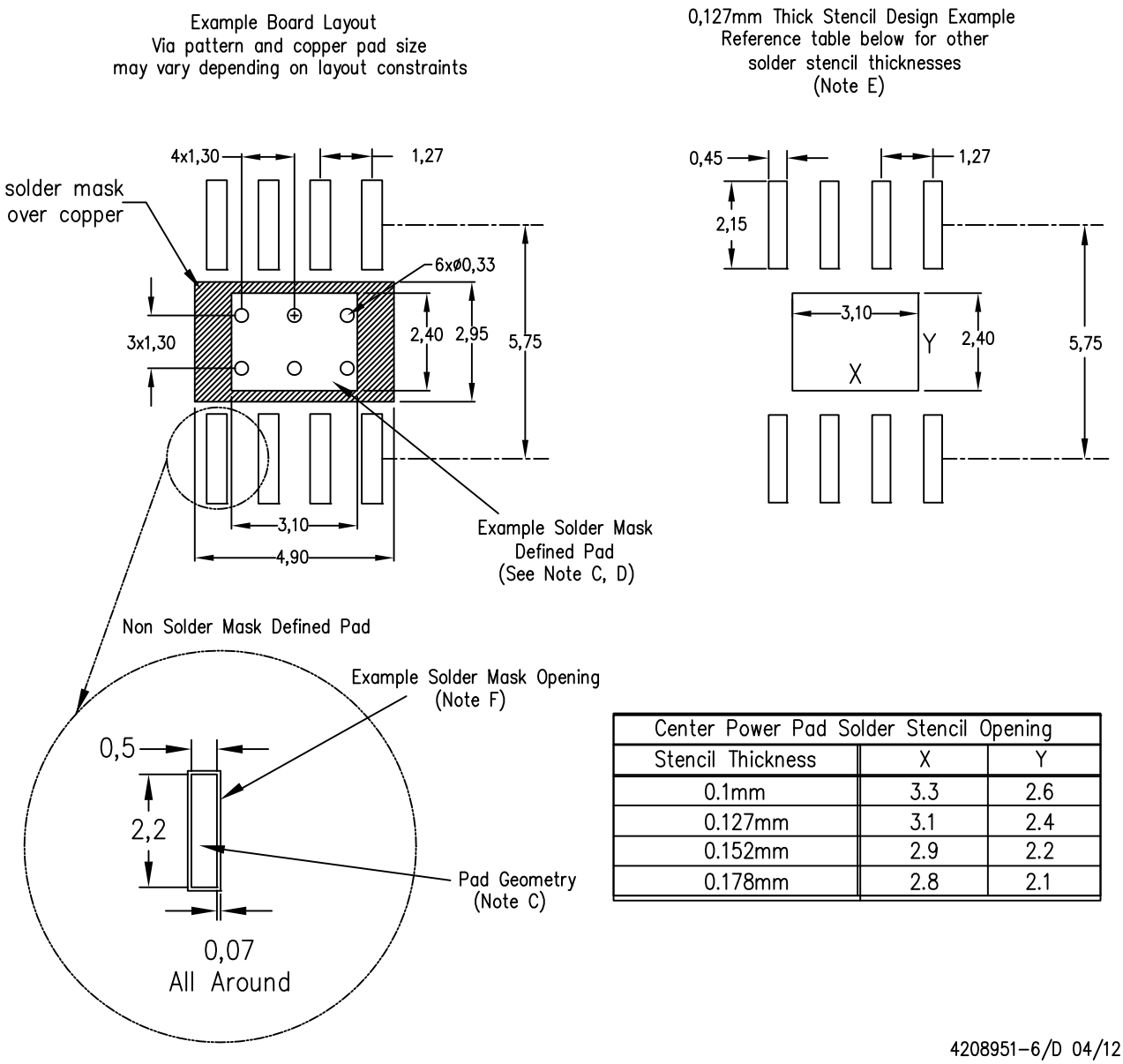
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.3	2.6
0.127mm	3.1	2.4
0.152mm	2.9	2.2
0.178mm	2.8	2.1

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

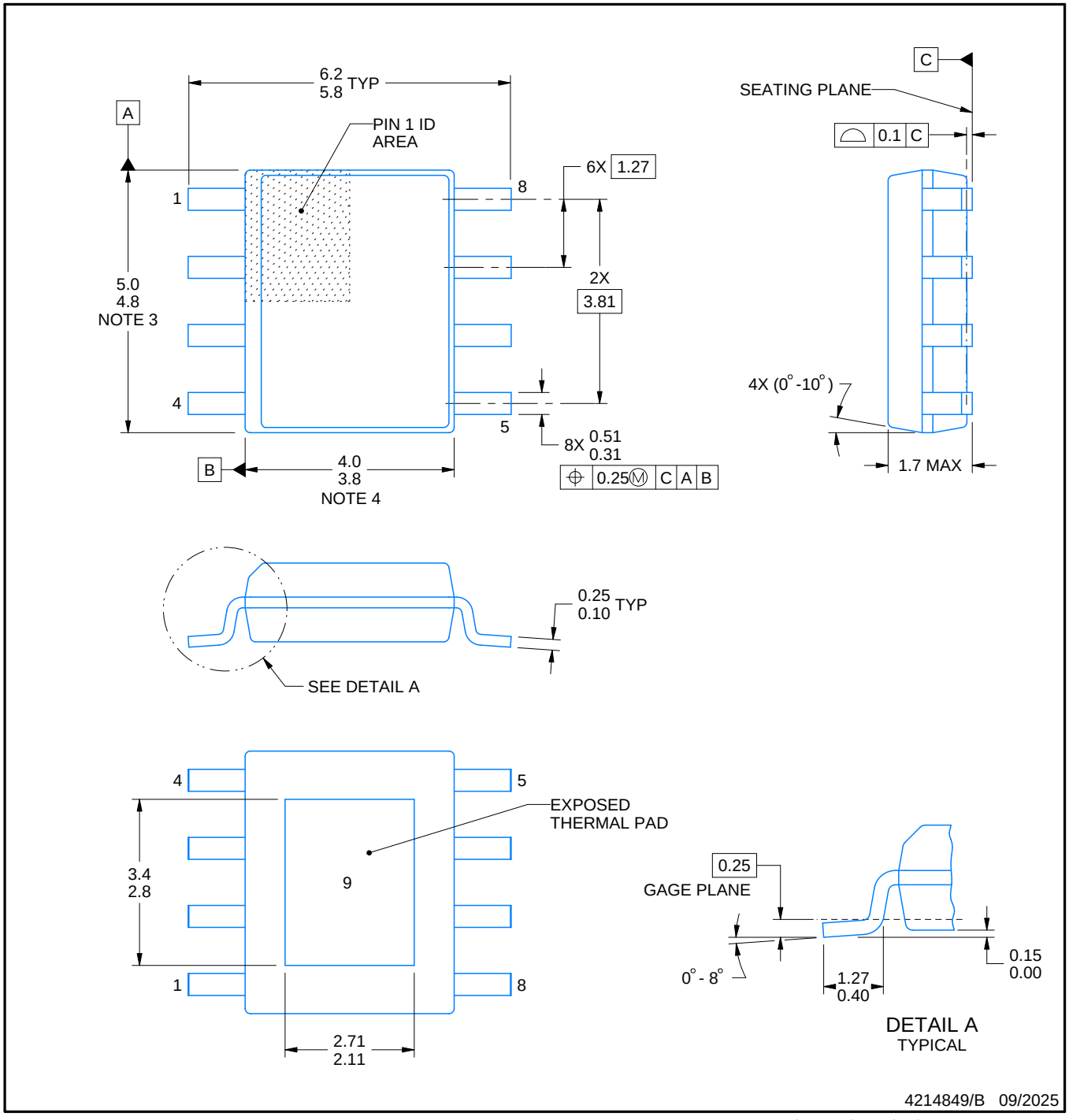
PowerPAD is a trademark of Texas Instruments.

PACKAGE OUTLINE

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

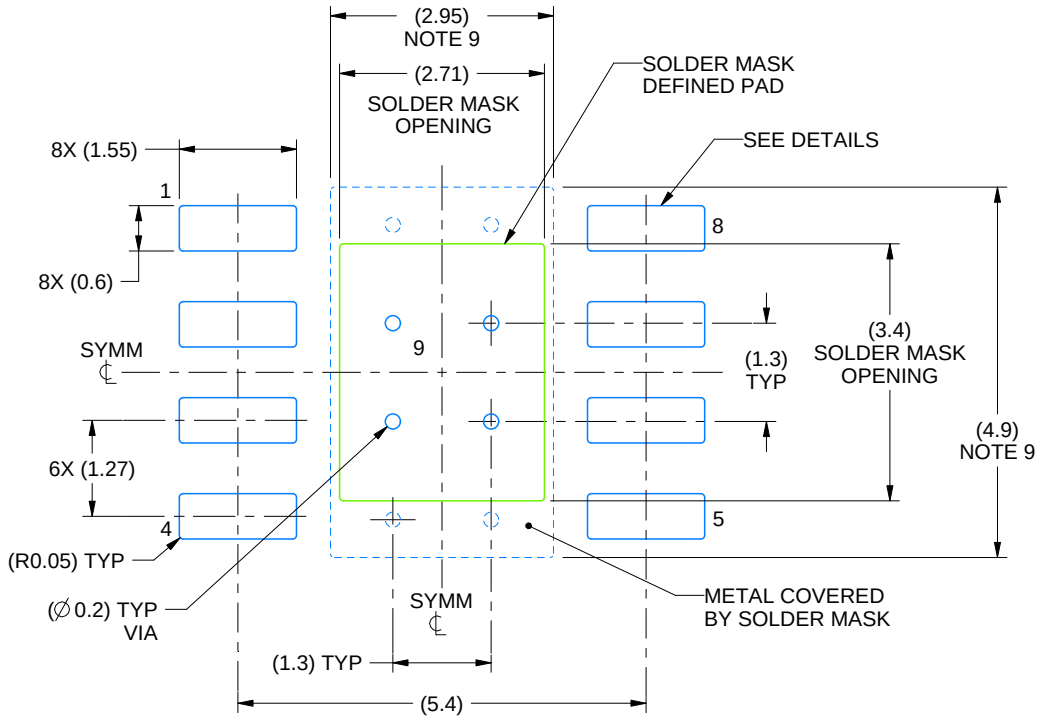
PLASTIC SMALL OUTLINE



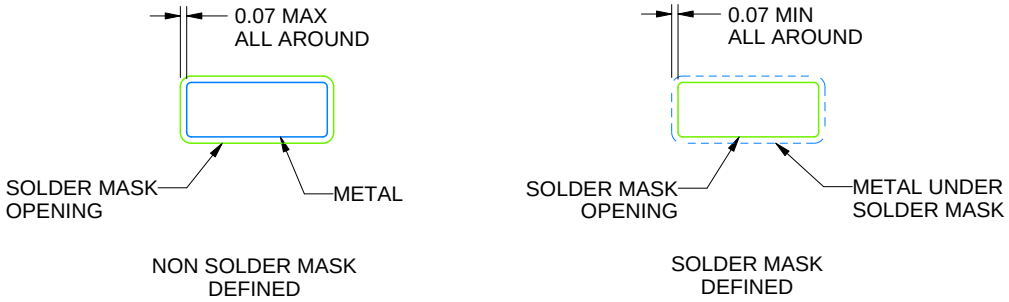
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
PADS 1-8

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NOTES: (continued)

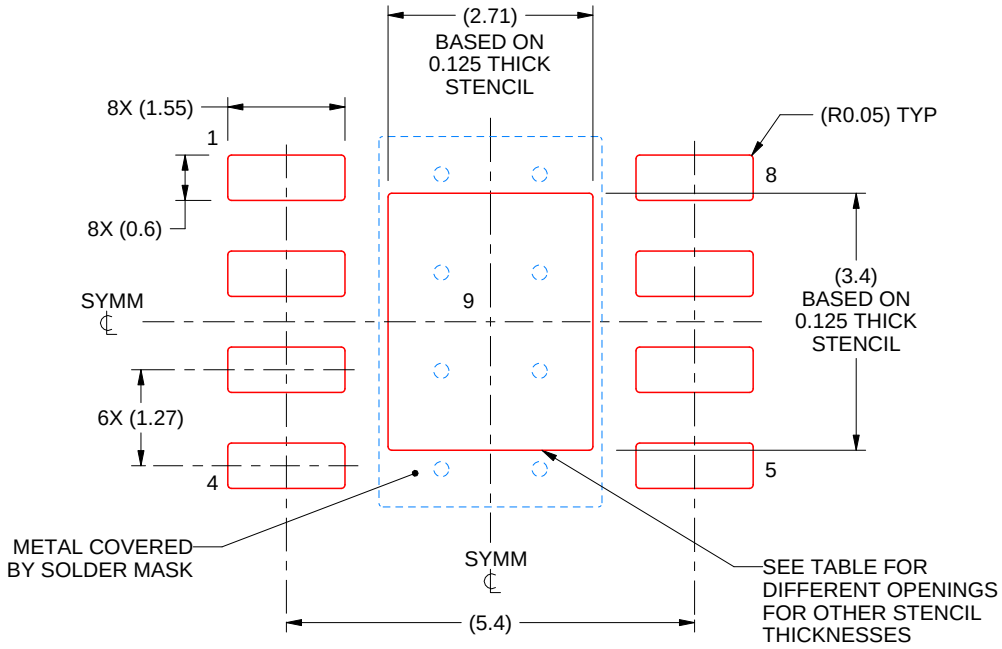
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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