

TPS7B82-Q1 汽车类 300mA、高压、超低 I_Q 低压降稳压器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准：
 - 温度等级 1： $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$
 - 温度等级 0： $-40^{\circ}\text{C} \leq T_A \leq 150^{\circ}\text{C}$
- 工作结温范围：
 - 1 级： $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$
 - 0 级： $-40^{\circ}\text{C} \leq T_J \leq 165^{\circ}\text{C}$
- 低静态电流 I_Q ：
 - 关断模式下 I_Q 为 300nA
 - 轻负载时典型值为 2.7 μA
 - 轻负载时最大值为 5 μA
- 3V 至 40V 宽 V_{IN} 输入电压范围，瞬态电压高达 45V
- 最大输出电流：300mA
- 输出电压精度为 2%
- 最大压降电压：对于固定 5V 输出版本，200mA 负载电流下为 700mV
- 与低 ESR (0.001 Ω 至 5 Ω) 陶瓷输出稳定电容器 (1 μF 至 200 μF) 搭配使用时可保持稳定
- 2.5V、3.3V 和 5V 固定输出电压
- 封装：
 - 8 引脚 HVSSOP， $R_{\theta JA} = 63.9^{\circ}\text{C/W}$
 - 6 引脚 WSON， $R_{\theta JA} = 72.8^{\circ}\text{C/W}$
 - 5 引脚 TO-252， $R_{\theta JA} = 31.1^{\circ}\text{C/W}$
 - 14 引脚 HTSSOP， $R_{\theta JA} = 52.0^{\circ}\text{C/W}$

2 应用

- 汽车音响主机
- 远程信息处理控制单元
- 大灯
- 车身控制模块
- 逆变器和电机控制

3 说明

在汽车电池连接应用中，低静态电流 (I_Q) 对于省电和延长电池寿命而言至关重要。对于始终开启的系统，必须要实现超低 I_Q 。

TPS7B82-Q1 是一款旨在在 3V 至 40V (45V 负载突降保护) 宽输入电压范围内运行的低压降线性稳压器。TPS7B82-Q1 的工作电压低至 3V，因此可在冷启动以及启动和停止情况下继续工作。该器件在轻负载时的典型静态电流仅为 2.7 μA ，是用于为待机系统中的微控制器 (MCU) 和 CAN/LIN 收发器供电的理想解决方案。

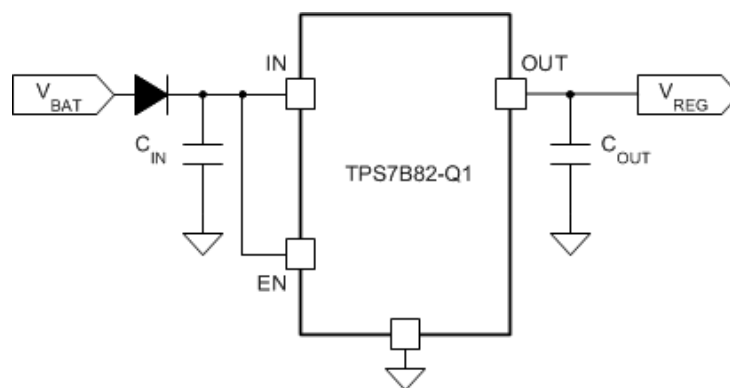
这些器件具有集成的短路和过流保护功能。该器件可在 -40°C 至 $+125^{\circ}\text{C}$ 的环境温度下运行，结温范围为 -40°C 至 $+150^{\circ}\text{C}$ 。此外，该器件采用了热传导封装，即使整个器件散热较多，也能实现持久运行。由于这些特性，该器件旨在用作各种汽车应用的电源。

封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾
TPS7B82-Q1	DGN (HVSSOP, 8)	3 mm × 4.9 mm
	DRV (WSON, 6)	2mm × 2mm
	KVU (TO-252, 5)	6.6 mm × 10.11 mm
	PWP (HTSSOP, 14)	5mm × 6.4mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

(2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。



典型应用原理图



Table of Contents

1 特性	1	7.3 Feature Description.....	11
2 应用	1	7.4 Device Functional Modes.....	12
3 说明	1	8 Application and Implementation	13
4 Revision History	2	8.1 Application Information.....	13
5 Pin Configuration and Functions	3	8.2 Typical Application.....	13
6 Specifications	4	8.3 Power Supply Recommendations.....	14
6.1 Absolute Maximum Ratings.....	4	8.4 Layout.....	15
6.2 ESD Ratings.....	4	9 Device and Documentation Support	16
6.3 Recommended Operating Conditions.....	4	9.1 接收文档更新通知.....	16
6.4 Thermal Information.....	5	9.2 支持资源.....	16
6.5 Electrical Characteristics: Grade 1 Options.....	5	9.3 Trademarks.....	16
6.6 Electrical Characteristics: Grade 0 Options.....	6	9.4 静电放电警告.....	16
6.7 Typical Characteristics.....	8	9.5 术语表.....	16
7 Detailed Description	11	10 Mechanical, Packaging, and Orderable Information	16
7.1 Overview.....	11		
7.2 Functional Block Diagram.....	11		

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision I (August 2021) to Revision J (August 2023)	Page
• Changed V_{OUT} parameter test conditions in <i>Electrical Characteristics</i> table.....	5

Changes from Revision H (March 2021) to Revision I (August 2021)	Page
• Changed I_Q parameter maximum specifications from $3.5\ \mu A$ to $5\ \mu A$ and from $4.5\ \mu A$ to $6.5\ \mu A$ in the <i>Electrical Characteristics: Grade 0 Options</i> table.....	6
• Changed $V_{(Load-Reg)}$ parameter maximum specification from $10\ mV$ to $20\ mV$ in the <i>Electrical Characteristics: Grade 0 Options</i> table.....	6
• Changed V_{OUT} parameter test condition from $40\ V$ to $14\ V$ in the <i>Electrical Characteristics: Grade 0 Options</i> table.....	6

5 Pin Configuration and Functions

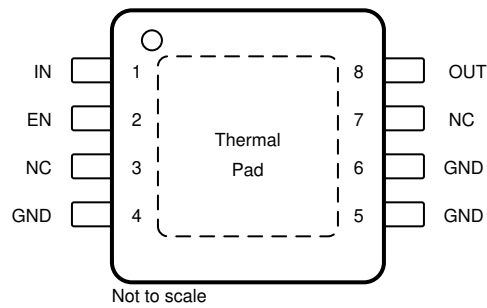


图 5-1. DGN Package, 8-Pin HVSSOP (Top View)

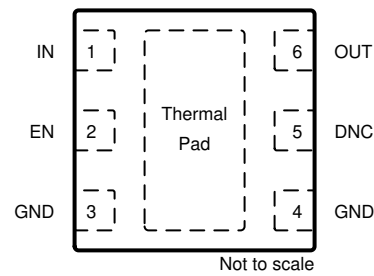


图 5-2. DRV Package, 6-Pin WSON (Top View)

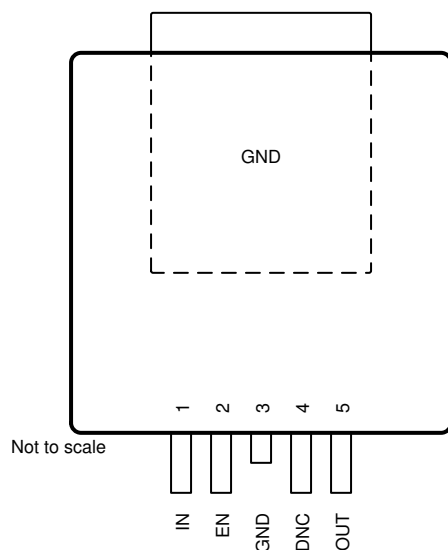


图 5-3. KVU Package, 5-Pin TO-252 (Top View)

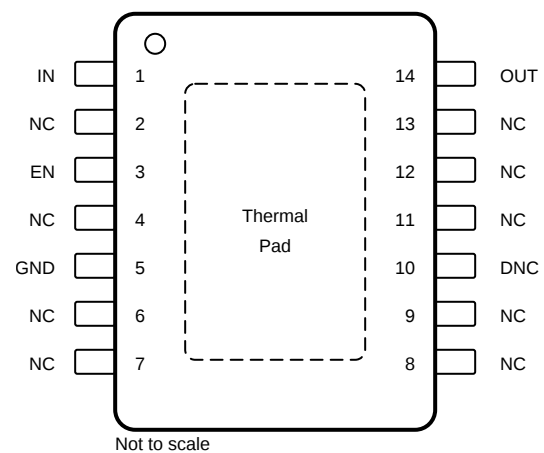


图 5-4. PWP Package, 14-Pin HTSSOP (Top View)

表 5-1. Pin Functions

PIN					TYPE	DESCRIPTION
NAME	NO.					
	DGN	DRV	KVU	PWP		
DNC	—	5	4	10	—	Do not connect to a biased voltage. Tie this pin to ground or leave floating.
EN	2	2	2	3	I	Enable input pin
GND	4, 5, 6	3,4	3, TAB	5	—	Ground reference
IN	1	1	1	1	I	Input power-supply pin
NC	3, 7	—	—	2, 4, 6, 7, 8, 9, 11, 12, 13	—	Not internally connected
OUT	8	6	5	14	O	Regulated output voltage pin
Thermal pad					—	Connect the thermal pad to a large-area GND plane for improved thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)^{(1) (2)}

		MIN	MAX	UNIT
V _{IN}	Unregulated input ⁽³⁾	– 0.3	45	V
V _{EN}	Enable input ⁽³⁾	– 0.3	V _{IN}	V
V _{OUT}	Regulated output	– 0.3	7	V
T _J	Junction temperature (grade 1)	– 40	150	°C
	Junction temperature (grade 0)	– 40	165	
T _{stg}	Storage temperature range	– 40	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND.
- (3) Absolute maximum voltage, withstand 45 V for 200 ms.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾ HBM ESD classification level H2	±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD classification level C3B	±750	
		Other pins	±500	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{IN}	Unregulated input voltage	3	40	V
V _{EN}	Enable input voltage	0	V _{IN}	V
C _{OUT}	Output capacitor requirements ⁽¹⁾	1	200	μF
ESR	Output capacitor ESR requirements ⁽²⁾	0.001	5	Ω
T _A	Ambient temperature (grade 1)	– 40	125	°C
	Ambient temperature (grade 0)	– 40	150	
T _J	Junction temperature (grade 1)	– 40	150	°C
	Junction temperature (grade 0)	– 40	165	

- (1) The output capacitance range specified in the table is the effective value.
- (2) Relevant equivalent series resistance (ESR) value at f = 10 kHz.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS7B82-Q1				UNIT
		DGN (HVSSOP)	DRV (WSON)	KVU (TO-252)	PWP (HTSSOP)	
		8 PINS	6 PINS	5 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63.9	72.8	31.1	52.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.2	85.8	39.9	48.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.6	37.4	9.9	28.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.8	2.7	4.2	2.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.3	37.3	9.9	28.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	12.1	13.8	2.8	10.7	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application note](#).

6.5 Electrical Characteristics: Grade 1 Options

$V_{IN} = 14\text{V}$, 10- μF ceramic output capacitor, grade 1 options, $T_J = -40^\circ\text{C}$ to $+150^\circ\text{C}$, over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND CURRENT (IN)							
V _{IN}	Input voltage			V _{OUT(NOM)} + V _(Dropout)		40	V
I _(SD)	Shutdown current	EN = 0 V		0.3		1	μ A
I _(Q)	Quiescent current	V _{IN} = 6 V to 40 V, EN ≥ 2 V, I _{OUT} = 0 mA	DRV and KVV packages	1.9		3.5	μ A
			DGN package	1.9		5	
		V _{IN} = 6 V to 40 V, EN ≥ 2 V, I _{OUT} = 0.2 mA	DRV and KVV packages	2.7		4.5	
			DGN package	2.7		6.5	
V _(IN, UVLO)	V _{IN} undervoltage detection	Ramp V _{IN} down until the output turns OFF				2.7	V
		Hysteresis				200	mV
ENABLE INPUT (EN)							
V _{IL}	Logic-input low level					0.7	V
V _{IH}	Logic-input high level			2			V
REGULATED OUTPUT (OUT)							
V _{OUT}	Regulated output	V _{IN} = V _{OUT} + V _(Dropout) to 40 V, I _{OUT} = 1 mA to 300 mA	DRV, KVV packages	- 1.5%		1.5%	
			DGN package for V _{OUT} = 5.0 V	- 1.5%		1.5%	
			DGN package for V _{OUT} = 2.5 V and 3.3 V	- 2%		2%	
V _(Line-Reg)	Line regulation	V _{IN} = 6 V to 40 V, I _{OUT} = 10 mA				10	mV
V _(Load-Reg)	Load regulation	V _{IN} = 14 V, I _{OUT} = 1 mA to 300 mA	DRV and KVV packages			10	mV
			DGN package			20	

6.5 Electrical Characteristics: Grade 1 Options (continued)

$V_{IN} = 14\text{-V}$, 10- μF ceramic output capacitor, grade 1 options, $T_J = -40^\circ\text{C}$ to $+150^\circ\text{C}$, over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V _(Dropout)	Dropout voltage ⁽¹⁾	V _{OUT(NOM)} = 5 V	I _{OUT} = 300 mA	DRV and KVVU packages	630	1170	mV	
				DGN package	1000			
			I _{OUT} = 200 mA	DRV and KVVU packages	420	780		
				DGN package	400	700		
			I _{OUT} = 100 mA	DRV and KVVU packages	210	390		
				DGN package	200	350		
		V _{OUT} = 3.3 V	I _{OUT} = 300 mA	DRV and KVVU packages	730	1350		
				DGN package	1250			
			I _{OUT} = 200 mA	DRV and KVVU packages	475	900		
				DGN package	850			
			I _{OUT} = 100 mA			450		
I _{OUT}	Output current	V _{OUT} in regulation			0	300	mA	
I _(CL)	Output current limit	V _{OUT} short to 90% × V _{OUT}			310	510	690	mA
PSRR	Power-supply ripple rejection	V _(Ripple) = 0.5 V _{PP} , I _{OUT} = 10 mA, frequency = 100 Hz, C _{OUT} = 2.2 μF			60		dB	
OPERATING TEMPERATURE RANGE								
T _(SD)	Junction shutdown temperature				175		°C	
T _(HYST)	Hysteresis of thermal shutdown				20		°C	

(1) Dropout is not valid for the 2.5-V output because of the minimum input voltage limits.

6.6 Electrical Characteristics: Grade 0 Options

$V_{IN} = 14\text{-V}$, 10- μF ceramic output capacitor, grade 0 options (PWP package), $T_J = -40^\circ\text{C}$ to $+165^\circ\text{C}$, over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND CURRENT (IN)							
V _{IN}	Input voltage			V _{OUT(NOM)} + V _(Dropout)		40	V
I _(SD)	Shutdown current	EN = 0 V		0.3		1	μA
I _(Q)	Quiescent current	V _{IN} = 6 V to 40 V, EN ≥ 2 V, I _{OUT} = 0 mA		1.9		5	
		V _{IN} = 6 V to 40 V, EN ≥ 2 V, I _{OUT} = 0.2 mA		2.7		6.5	μA
V _(IN, UVLO)	V _{IN} undervoltage detection	Ramp V _{IN} down until the output turns OFF				2.7	V
		Hysteresis		200			mV
ENABLE INPUT (EN)							
V _{IL}	Logic-input low level					0.7	V
V _{IH}	Logic-input high level			2			V
REGULATED OUTPUT (OUT)							
V _{OUT}	Regulated output	V _{IN} = V _{OUT} + V _(Dropout) to 14 V, I _{OUT} = 1 mA to 300 mA		- 1.5%		1.5%	

6.6 Electrical Characteristics: Grade 0 Options (continued)

$V_{IN} = 14\text{-V}$, 10- μF ceramic output capacitor, grade 0 options (PWP package), $T_J = -40^\circ\text{C}$ to $+165^\circ\text{C}$, over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(\text{Line-Reg})}$	Line regulation	$V_{IN} = 6\text{ V to }40\text{ V}$, $I_{OUT} = 10\text{ mA}$			10	mV
$V_{(\text{Load-Reg})}$	Load regulation	$V_{IN} = 14\text{ V}$, $I_{OUT} = 1\text{ mA to }300\text{ mA}$			20	mV
$V_{(\text{Dropout})}$	Dropout voltage ⁽¹⁾	$V_{OUT(\text{NOM})} = 5\text{ V}$	$I_{OUT} = 300\text{ mA}$		630	mV
			$I_{OUT} = 200\text{ mA}$		420	
			$I_{OUT} = 100\text{ mA}$		210	
		$V_{OUT} = 3.3\text{ V}$	$I_{OUT} = 300\text{ mA}$		730	
			$I_{OUT} = 200\text{ mA}$		475	
			$I_{OUT} = 100\text{ mA}$		450	
I_{OUT}	Output current	V_{OUT} in regulation	0		300	mA
$I_{(\text{CL})}$	Output current limit	V_{OUT} short to $90\% \times V_{OUT}$	310	510	690	mA
PSRR	Power-supply ripple rejection	$V_{(\text{Ripple})} = 0.5\text{ V}_{PP}$, $I_{OUT} = 10\text{ mA}$, frequency = 100 Hz, $C_{OUT} = 2.2\text{ }\mu\text{F}$		60		dB
OPERATING TEMPERATURE RANGE						
$T_{(\text{SD})}$	Junction shutdown temperature			185		$^\circ\text{C}$
$T_{(\text{HYST})}$	Hysteresis of thermal shutdown			20		$^\circ\text{C}$

6.7 Typical Characteristics

$V_{IN} = 14\text{ V}$, $V_{EN} \geq 2\text{ V}$, $T_J = -40^\circ\text{C}$ to 150°C (unless otherwise noted)

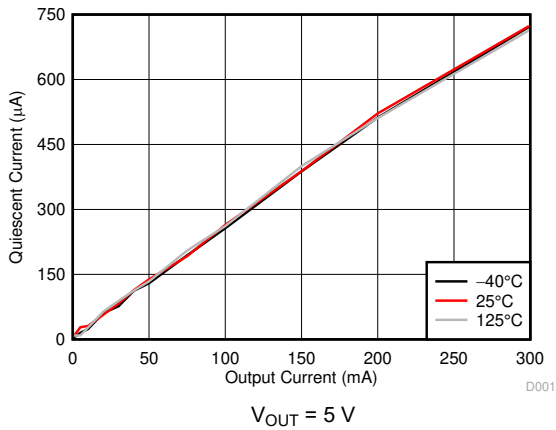


图 6-1. Quiescent Current vs Output Current

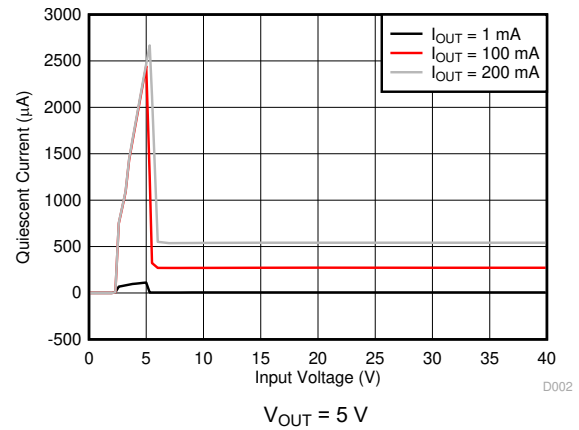


图 6-2. Quiescent Current vs Input Voltage

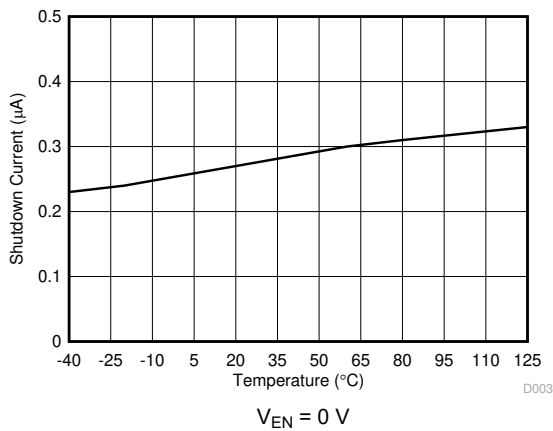


图 6-3. Shutdown Current vs Ambient Temperature

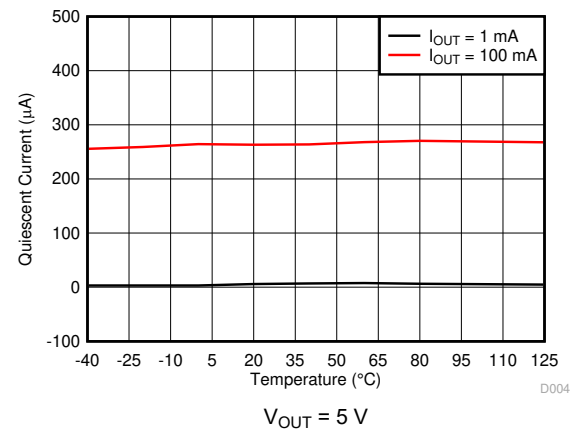


图 6-4. Quiescent Current vs Ambient Temperature

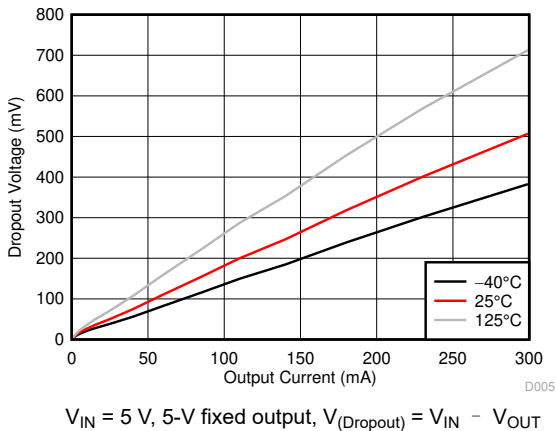


图 6-5. Dropout Voltage vs Output Current

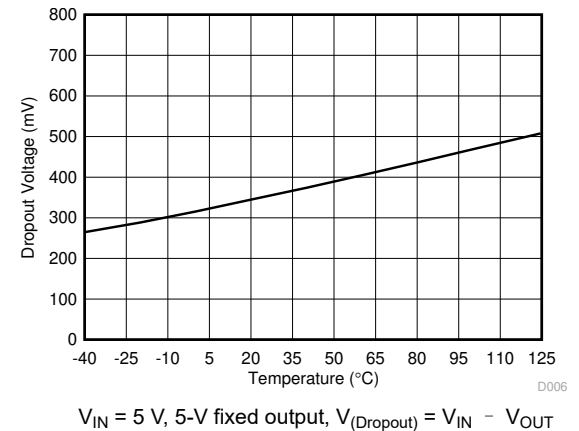


图 6-6. Dropout Voltage vs Ambient Temperature

6.7 Typical Characteristics (continued)

$V_{IN} = 14\text{ V}$, $V_{EN} \geq 2\text{ V}$, $T_J = -40^\circ\text{C}$ to 150°C (unless otherwise noted)

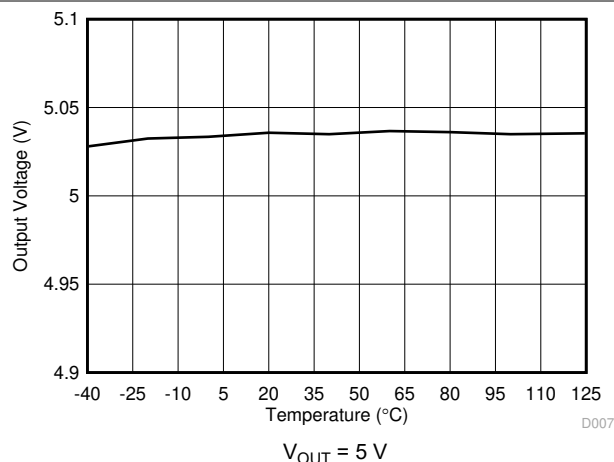


图 6-7. Output Voltage vs Ambient Temperature

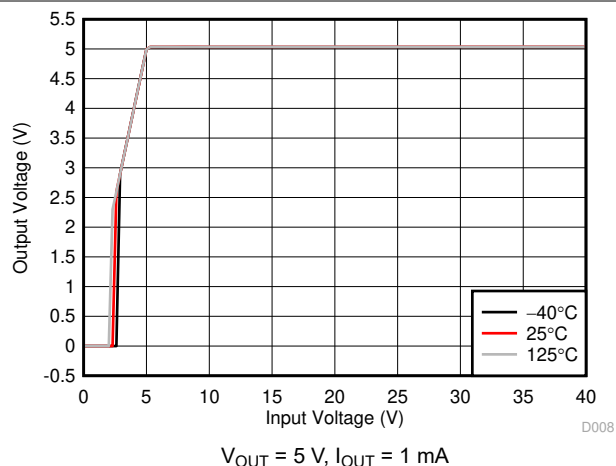


图 6-8. Output Voltage vs Input Voltage

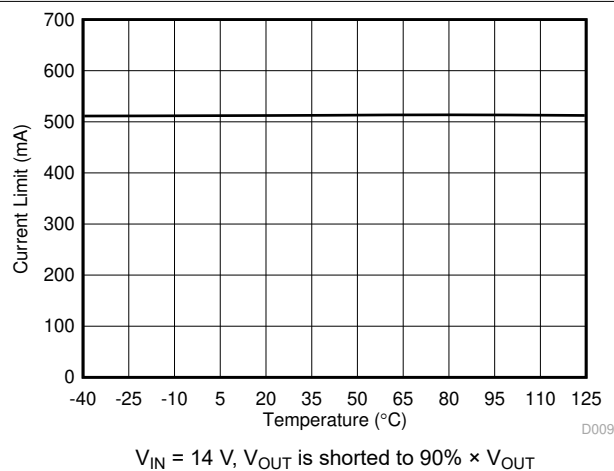


图 6-9. Output Current Limit vs Ambient Temperature

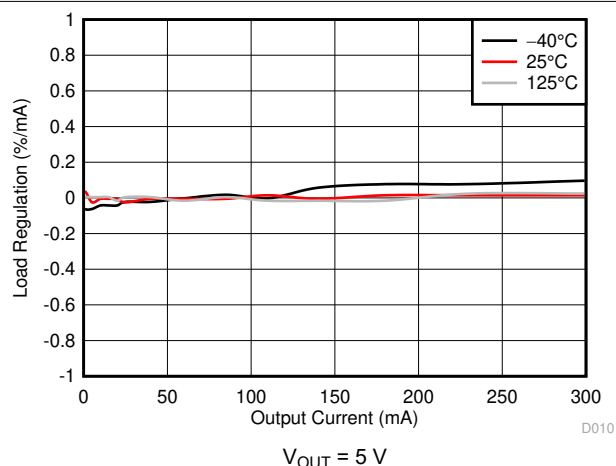


图 6-10. Load Regulation

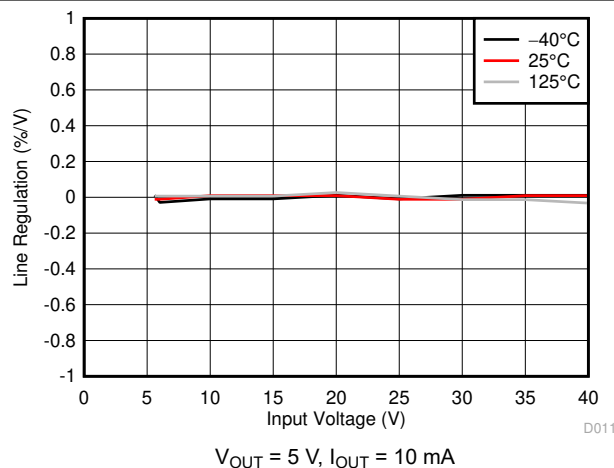


图 6-11. Line Regulation

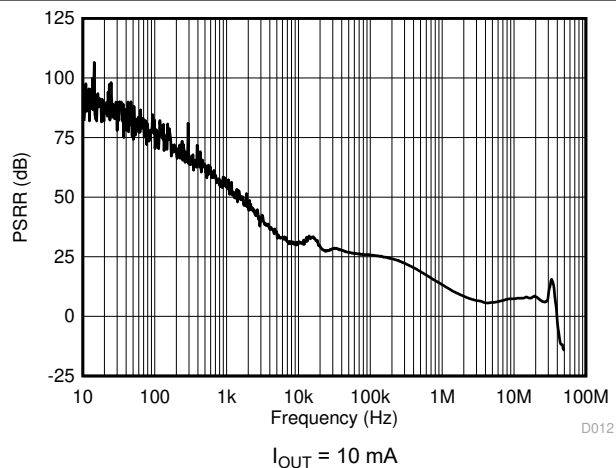


图 6-12. PSRR vs Frequency

6.7 Typical Characteristics (continued)

$V_{IN} = 14\text{ V}$, $V_{EN} \geq 2\text{ V}$, $T_J = -40^{\circ}\text{C}$ to 150°C (unless otherwise noted)

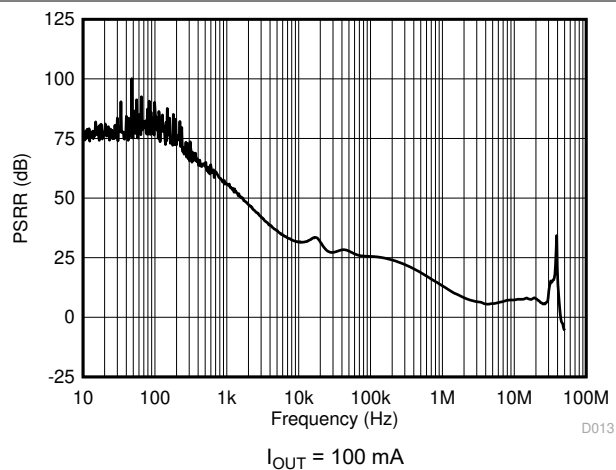


图 6-13. PSRR vs Frequency

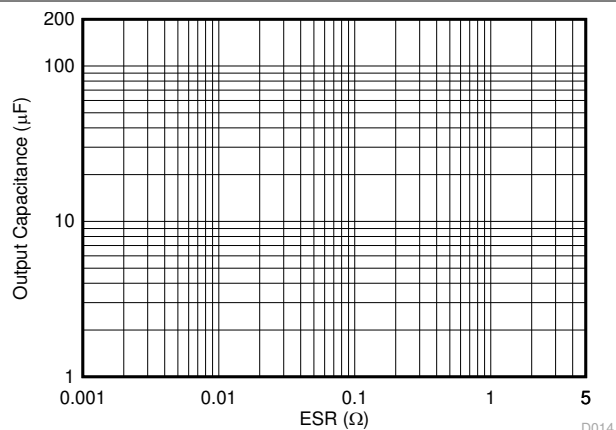


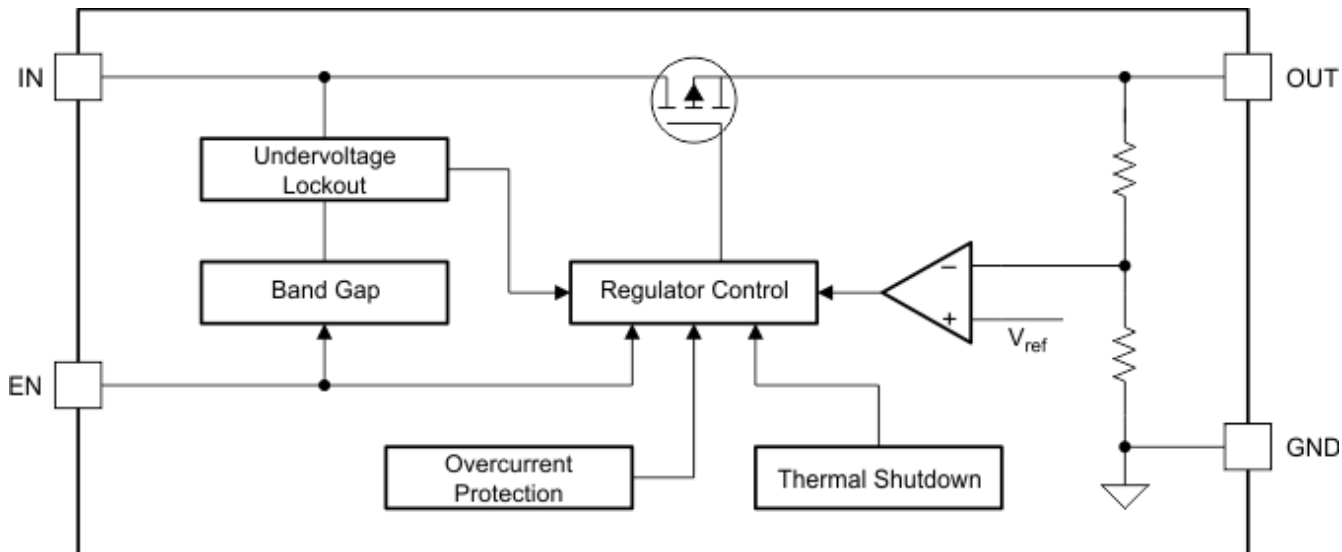
图 6-14. Output Capacitance vs ESR Stability

7 Detailed Description

7.1 Overview

The TPS7B82-Q1 is a 40-V, 300-mA low-dropout (LDO) linear regulator with ultra-low quiescent current. This voltage regulator consumes only 3 μ A of quiescent current at light load, and is designed for the automotive always-on application.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Device Enable (EN)

The EN pin is a high-voltage-tolerant pin. A high input activates the device and turns the regulation ON. Connect this pin to an external microcontroller or a digital circuit to enable and disable the device, or connect to the IN pin for self-bias applications.

7.3.2 Undervoltage Shutdown

This device has an integrated undervoltage lockout (UVLO) circuit to shut down the output if the input voltage (V_{IN}) falls below an internal UVLO threshold ($V_{(UVLO)}$). This threshold limit ensures that the regulator does not latch into an unknown state during low-input-voltage conditions. If the input voltage has a negative transient that drops below the UVLO threshold and recovers, the regulator shuts down and powers up with a normal power-up sequence when the input voltage is above the required level.

7.3.3 Current Limit

This device features current-limit protection to keep the device in a safe operating area when an overload or output short-to-ground condition occurs. This limit protects the device from excessive power dissipation. For example, during a short-circuit condition on the output, fault protection limits the current through the pass element to $I_{(LIM)}$ to protect the device from excessive power dissipation.

7.3.4 Thermal Shutdown

This device incorporates a thermal shutdown (TSD) circuit as a protection from overheating. For continuous normal operation, the junction temperature must not exceed the TSD trip point. The junction temperature exceeding the TSD trip point causes the output to turn off. When the junction temperature falls below the TSD trip point minus thermal shutdown hysteresis, the output turns on again.

7.4 Device Functional Modes

7.4.1 Operation With V_{IN} Lower Than 3 V

The device normally operates with input voltages above 3 V. The device can also operate at lower input voltages; the maximum UVLO voltage is 2.7 V. At input voltages below the actual UVLO voltage, the device does not operate.

7.4.2 Operation With V_{IN} Larger Than 3 V

When V_{IN} is greater than 3 V, if V_{IN} is also higher than the output set value plus the device dropout voltage, V_{OUT} is equal to the set value. Otherwise, V_{OUT} is equal to V_{IN} minus the dropout voltage.

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The TPS7B82-Q1 is a 300-mA, 40-V low-dropout linear regulator with ultra-low quiescent current. The PSpice transient model is available for download on the product folder and can be used to evaluate the basic function of the device.

8.2 Typical Application

图 8-1 shows a typical application circuit for the TPS7B82-Q1. Different values of external components can be used, depending on the end application. An application may require a larger output capacitor during fast load steps to prevent a large drop on the output voltage. Use a low-ESR ceramic capacitor with a dielectric of type X5R or X7R.

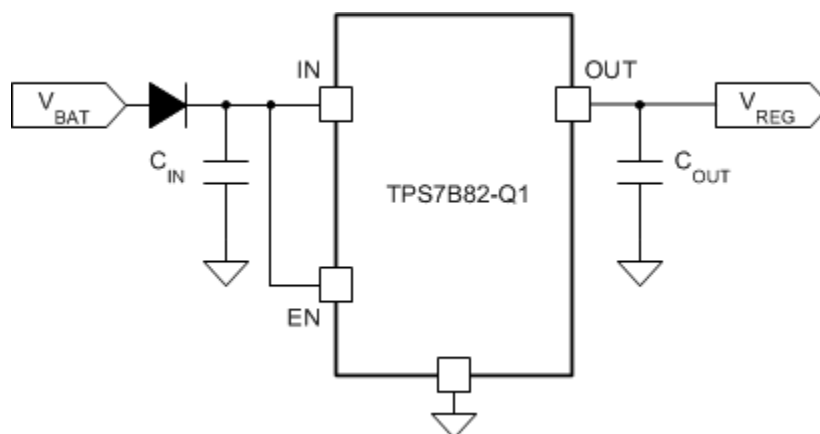


图 8-1. TPS7B82-Q1 Typical Application Schematic

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-1.

表 8-1. Design Requirements Parameters

PARAMETER	VALUE
Input voltage range	3 V to 40 V
Output voltage	5 V or 3.3 V
Output current	300 mA maximum

8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output voltage
- Output current

8.2.2.1 Input Capacitor

Although an input capacitor is not required for stability, good analog design practice is to connect a 10- μ F to 22- μ F capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple rejection, and PSRR. The voltage rating must be greater than the maximum input voltage.

8.2.2.2 Output Capacitor

To ensure the stability of the TPS7B82-Q1, the device requires an output capacitor with a value in the range from 1 μ F to 200 μ F and with an ESR range between 0.001 Ω and 5 Ω . Select a ceramic capacitor with low ESR to improve the load transient response.

8.2.3 Application Curve

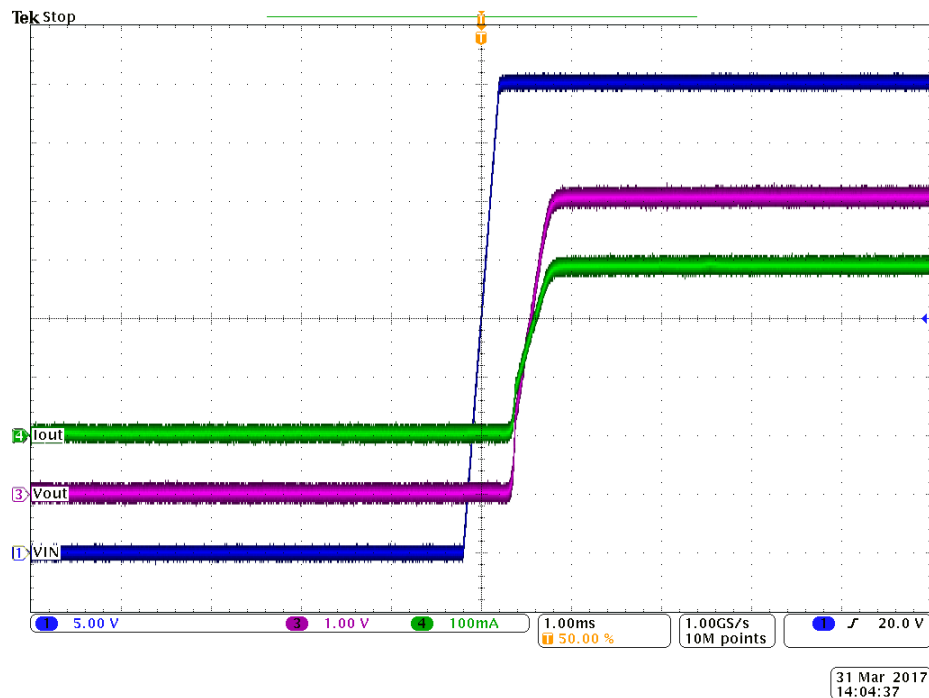


图 8-2. TPS7B82-Q1 Power-Up Waveform (5 V)

8.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 3 V to 40 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7B82-Q1, add a capacitor with a value greater than or equal to 10 μ F with a 0.1- μ F bypass capacitor in parallel at the input.

8.4 Layout

8.4.1 Layout Guidelines

For LDO power supplies, especially high-voltage and large output current supplies, layout is an important step. If layout is not carefully designed, the regulator can fail to deliver enough output current because of thermal limitation. To improve the thermal performance of the device, and to maximize the current output at high ambient temperature, spread the copper under the thermal pad as far as possible and place enough thermal vias on the copper under the thermal pad. [Figure 8-3](#) shows an example layout.

8.4.2 Layout Example

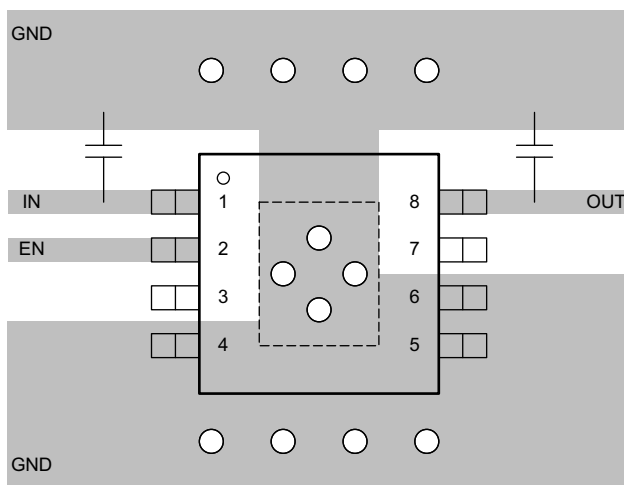


图 8-3. TPSB82-Q1 Example Layout Diagram

9 Device and Documentation Support

9.1 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.2 支持资源

TI E2E™ 支持论坛 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

9.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.5 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7B8225QDGNRQ1	Active	Production	HVSSOP (DGN) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	1QFX
TPS7B8233EPWPRQ1	Active	Production	HTSSOP (PWP) 14	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 165	7B8233E
TPS7B8233QDGNRQ1	Active	Production	HVSSOP (DGN) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	1GGX
TPS7B8233QDRVRQ1	Active	Production	WSOP (DRV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	1ORH
TPS7B8233QKVURQ1	Active	Production	TO-252 (KVU) 5	2500 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 150	7B8233Q1
TPS7B8250EPWPRQ1	Active	Production	HTSSOP (PWP) 14	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 165	7B8250E
TPS7B8250QDGNRQ1	Active	Production	HVSSOP (DGN) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	19TX
TPS7B8250QDRVRQ1	Active	Production	WSOP (DRV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	1UFH
TPS7B8250QKVURQ1	Active	Production	TO-252 (KVU) 5	2500 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 150	7B8250Q1

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

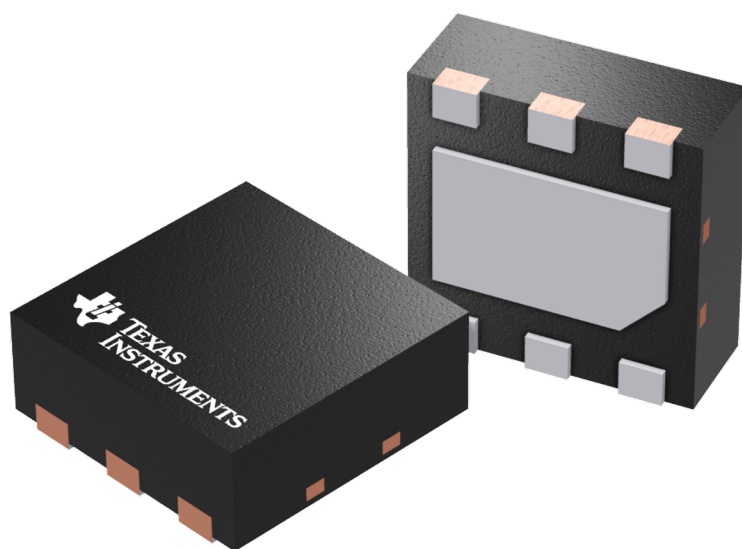
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7B8225QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7B8233EPWPRQ1	HTSSOP	PWP	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS7B8233QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7B8233QDRVRQ1	WSOP	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7B8233QKVURQ1	TO-252	KVU	5	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TPS7B8250EPWPRQ1	HTSSOP	PWP	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS7B8250QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7B8250QDRVRQ1	WSOP	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7B8250QKVURQ1	TO-252	KVU	5	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS

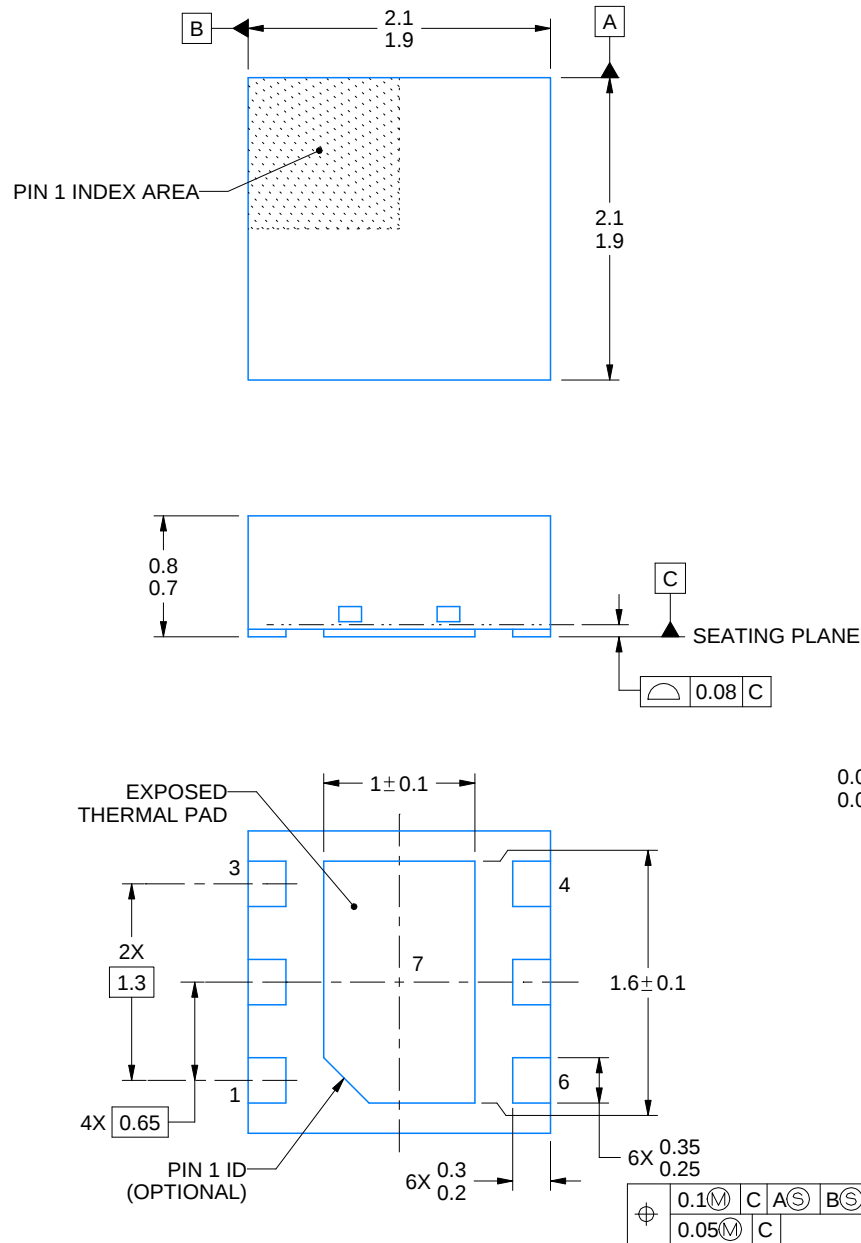
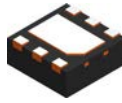


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7B8225QDGNRQ1	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS7B8233EPWPRQ1	HTSSOP	PWP	14	2500	356.0	356.0	35.0
TPS7B8233QDGNRQ1	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS7B8233QDRVRQ1	WSOP	DRV	6	3000	210.0	185.0	35.0
TPS7B8233QKVURQ1	TO-252	KVU	5	2500	340.0	340.0	38.0
TPS7B8250EPWPRQ1	HTSSOP	PWP	14	2500	356.0	356.0	35.0
TPS7B8250QDGNRQ1	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS7B8250QDRVRQ1	WSOP	DRV	6	3000	210.0	185.0	35.0
TPS7B8250QKVURQ1	TO-252	KVU	5	2500	340.0	340.0	38.0



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4222173/B 04/2018

NOTES:

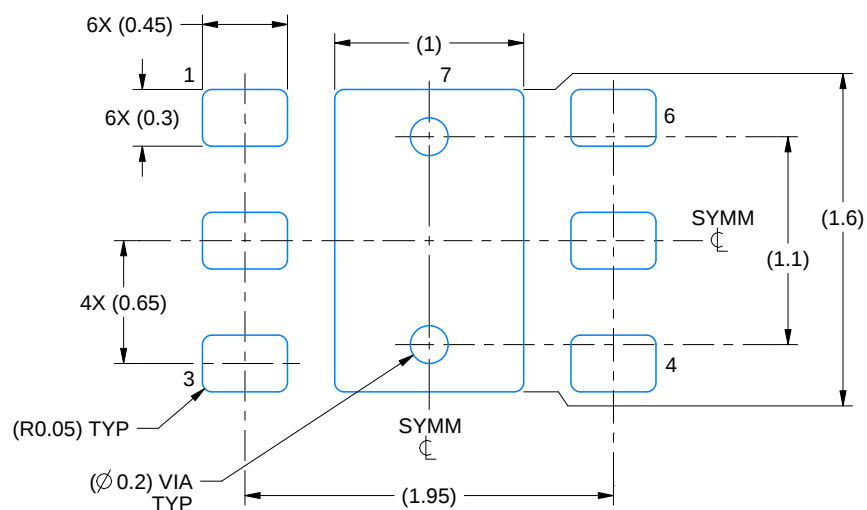
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

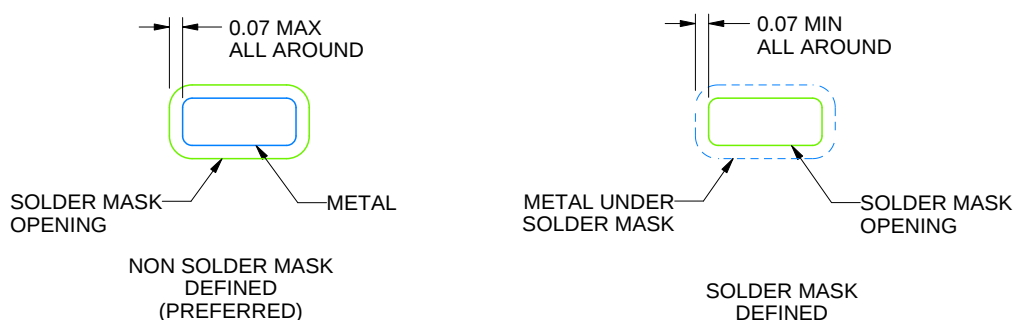
DRV0006A

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS

4222173/B 04/2018

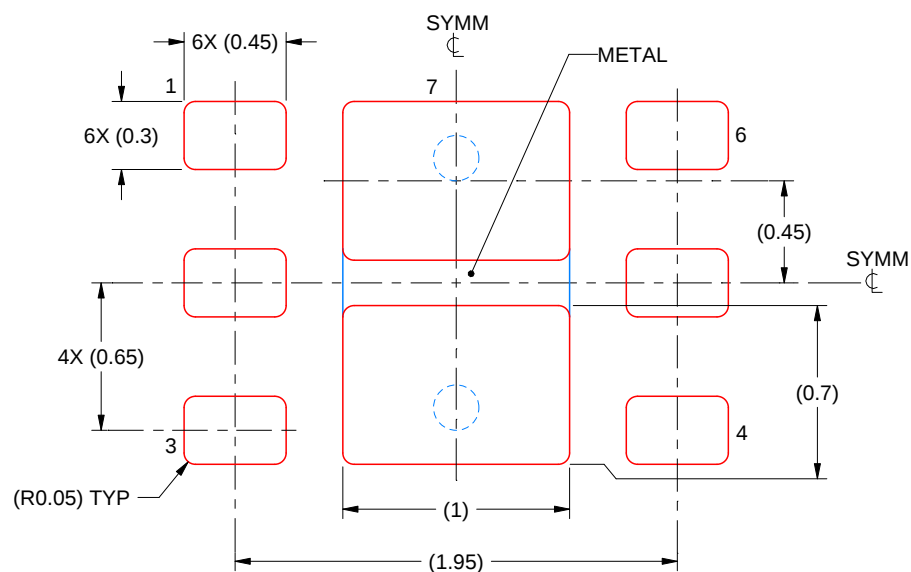
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slue271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/B 04/2018

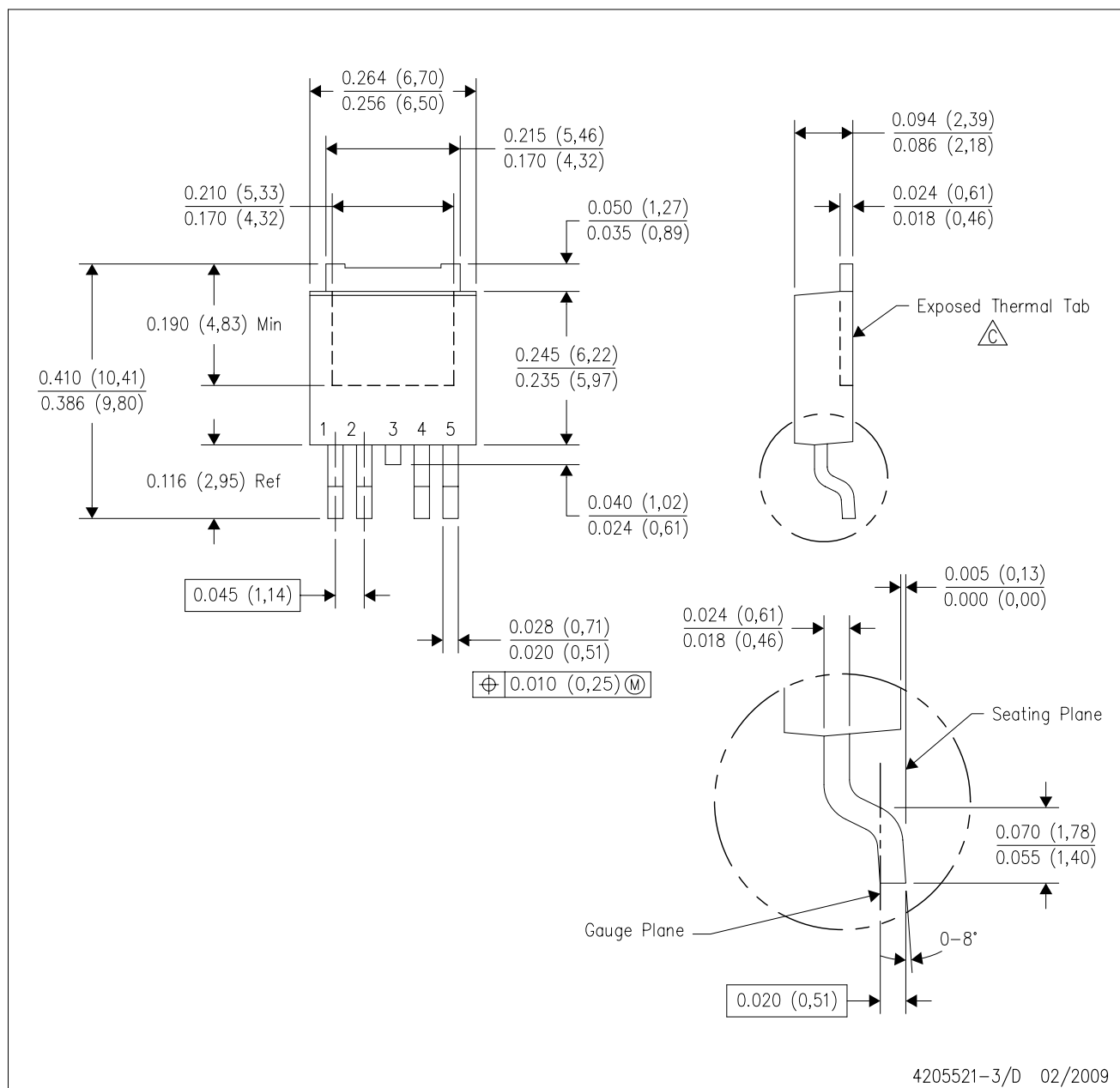
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

KVU (R-PSFM-G5)

PLASTIC FLANGE-MOUNT PACKAGE

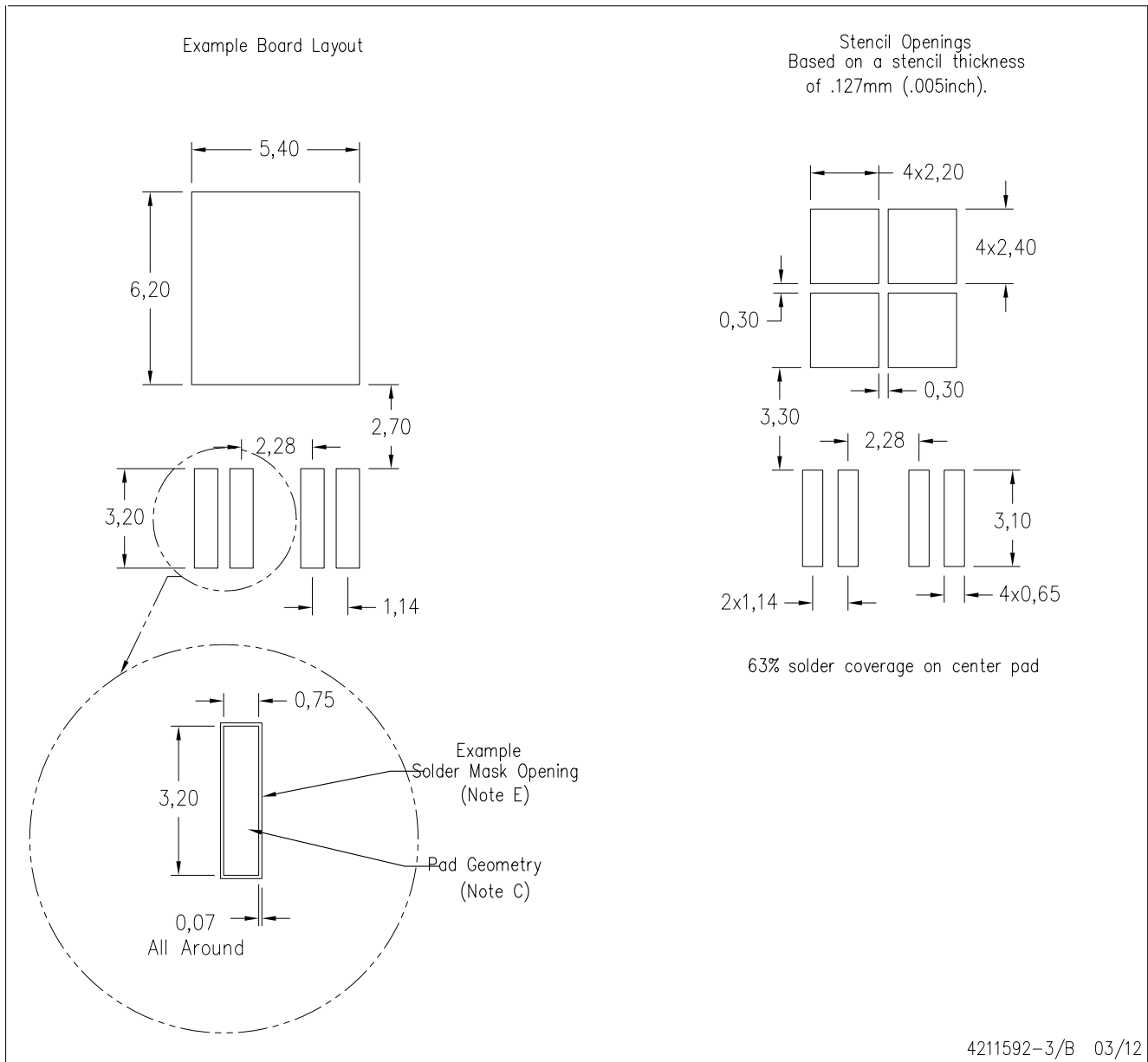


NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the exposed thermal tab.
D. Body Dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.006 (0,15) per side.
E. Falls within JEDEC TO-252 variation AD.

KVU (R-PSFM-G5)

PLASTIC FLANGE MOUNT PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-SM-782 is an alternate information source for PCB land pattern designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

GENERIC PACKAGE VIEW

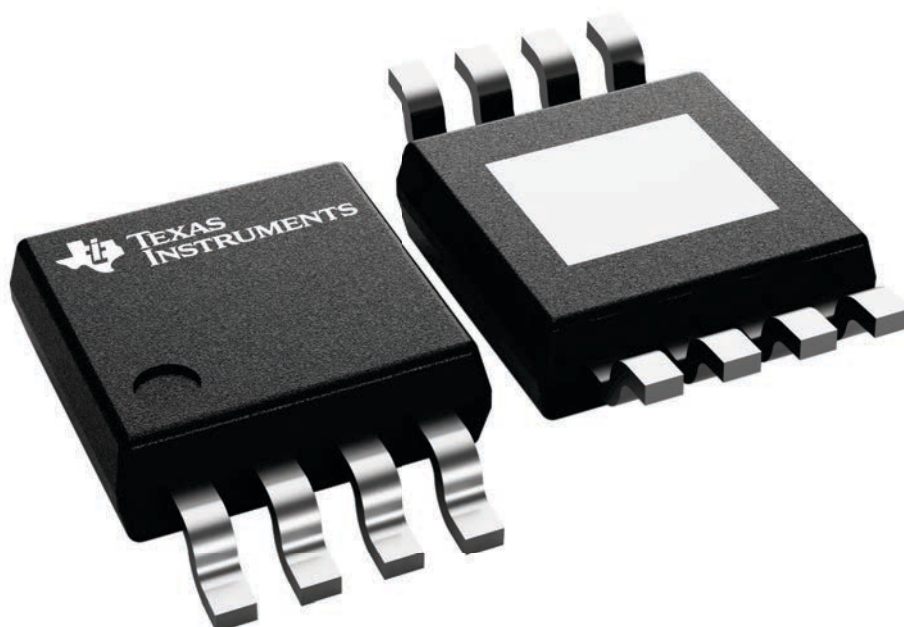
DGN 8

PowerPAD™ HVSSOP - 1.1 mm max height

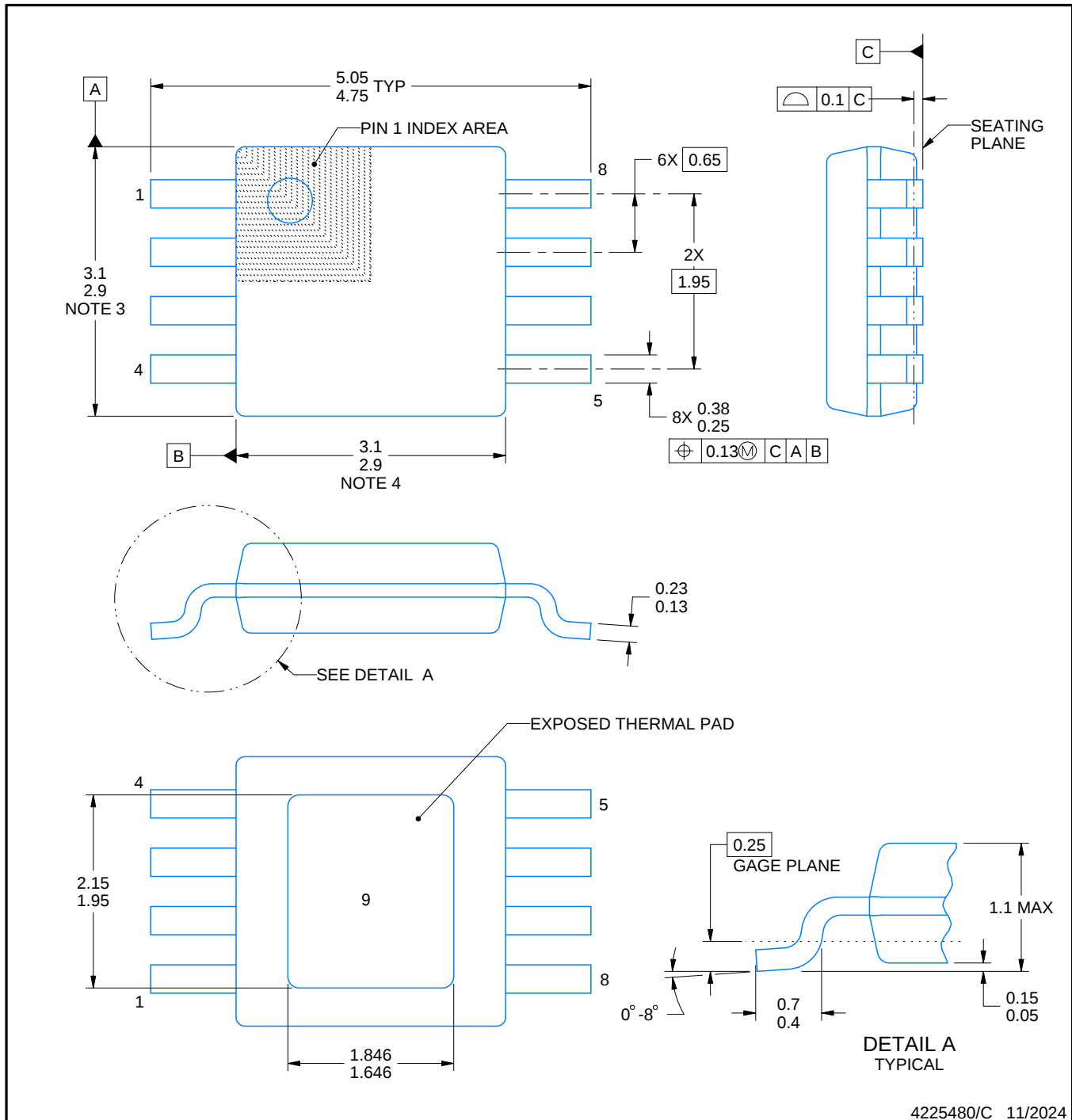
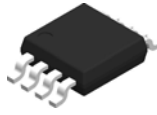
3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/B



4225480/C 11/2024

NOTES:

PowerPAD is a trademark of Texas Instruments.

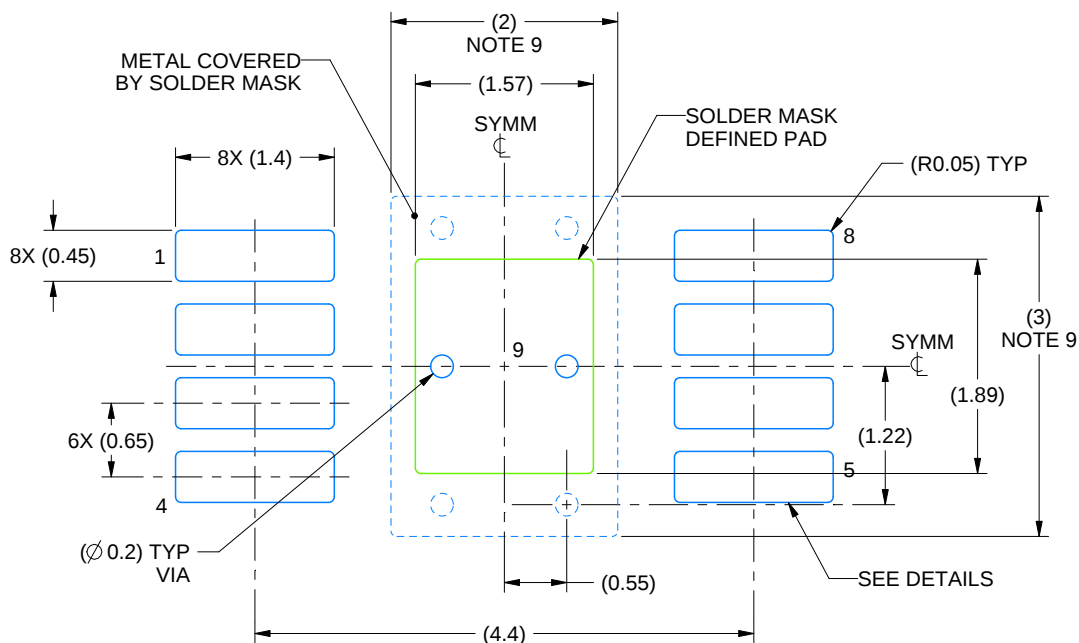
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

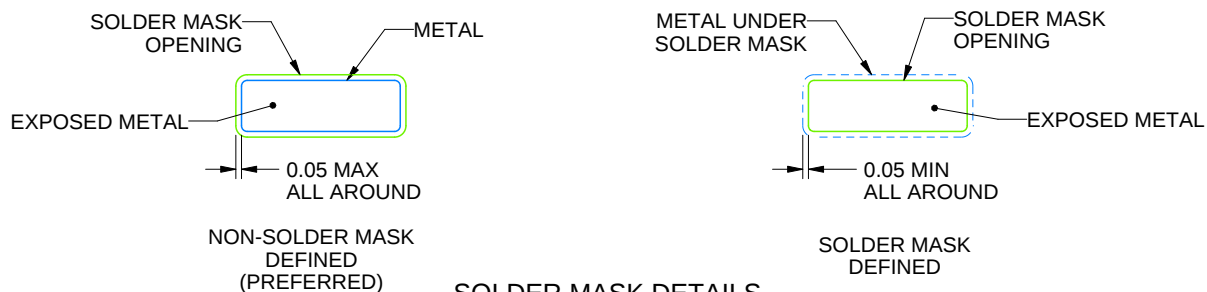
DGN0008G

PowerPAD™ HVSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4225480/C 11/2024

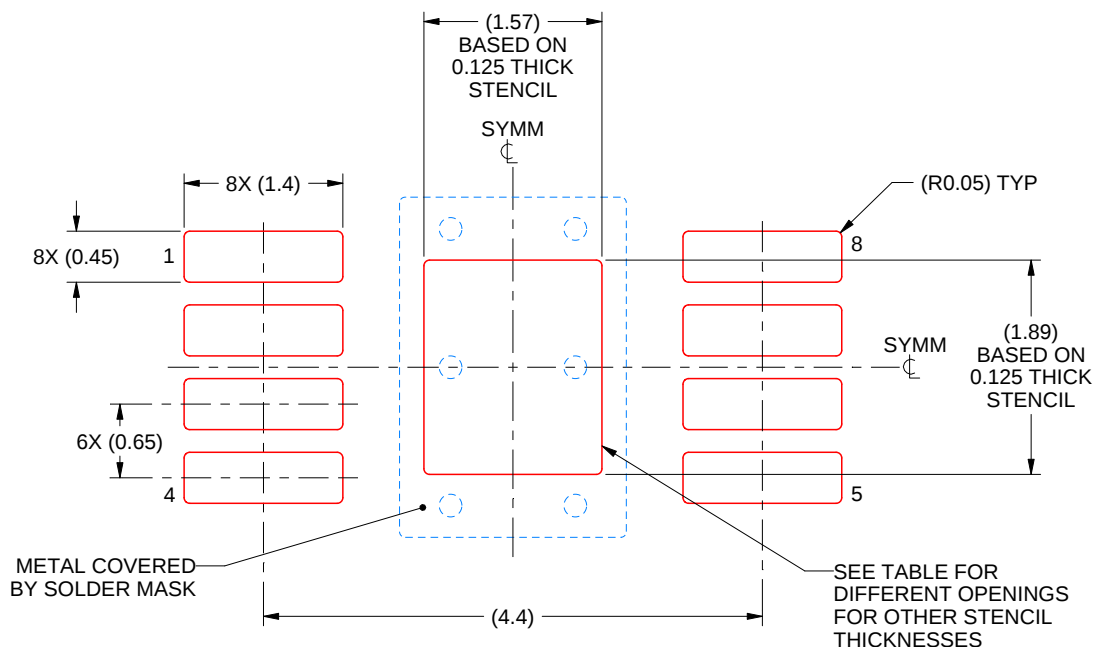
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

DGN0008G

PowerPAD™ HVSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE

EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225480/C 11/2024

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

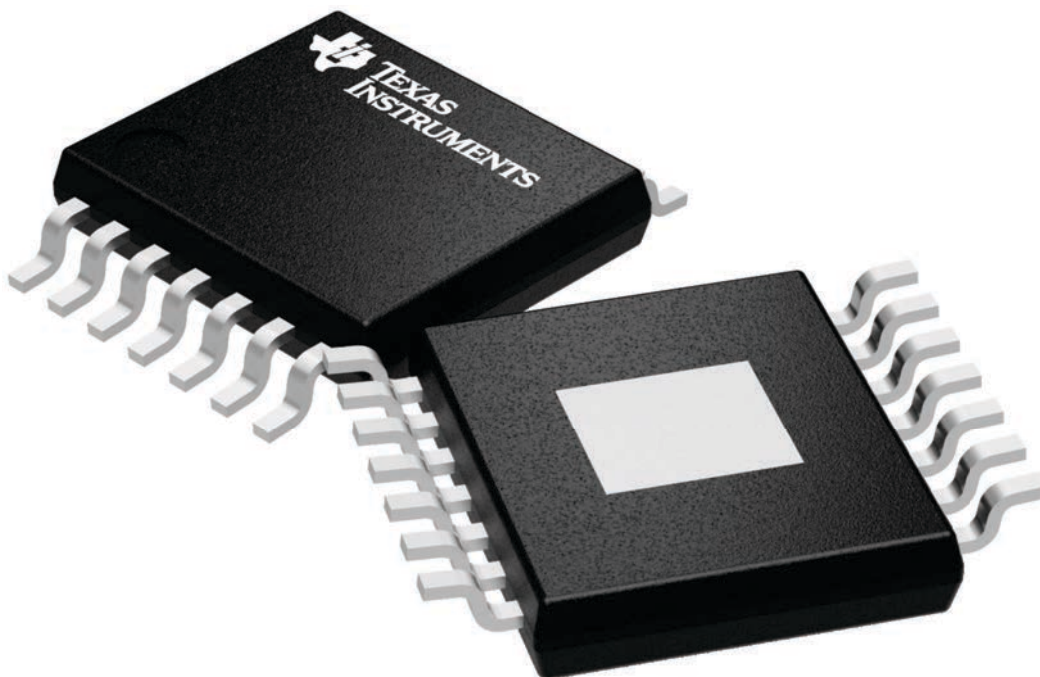
PWP 14

PowerPAD TSSOP - 1.2 mm max height

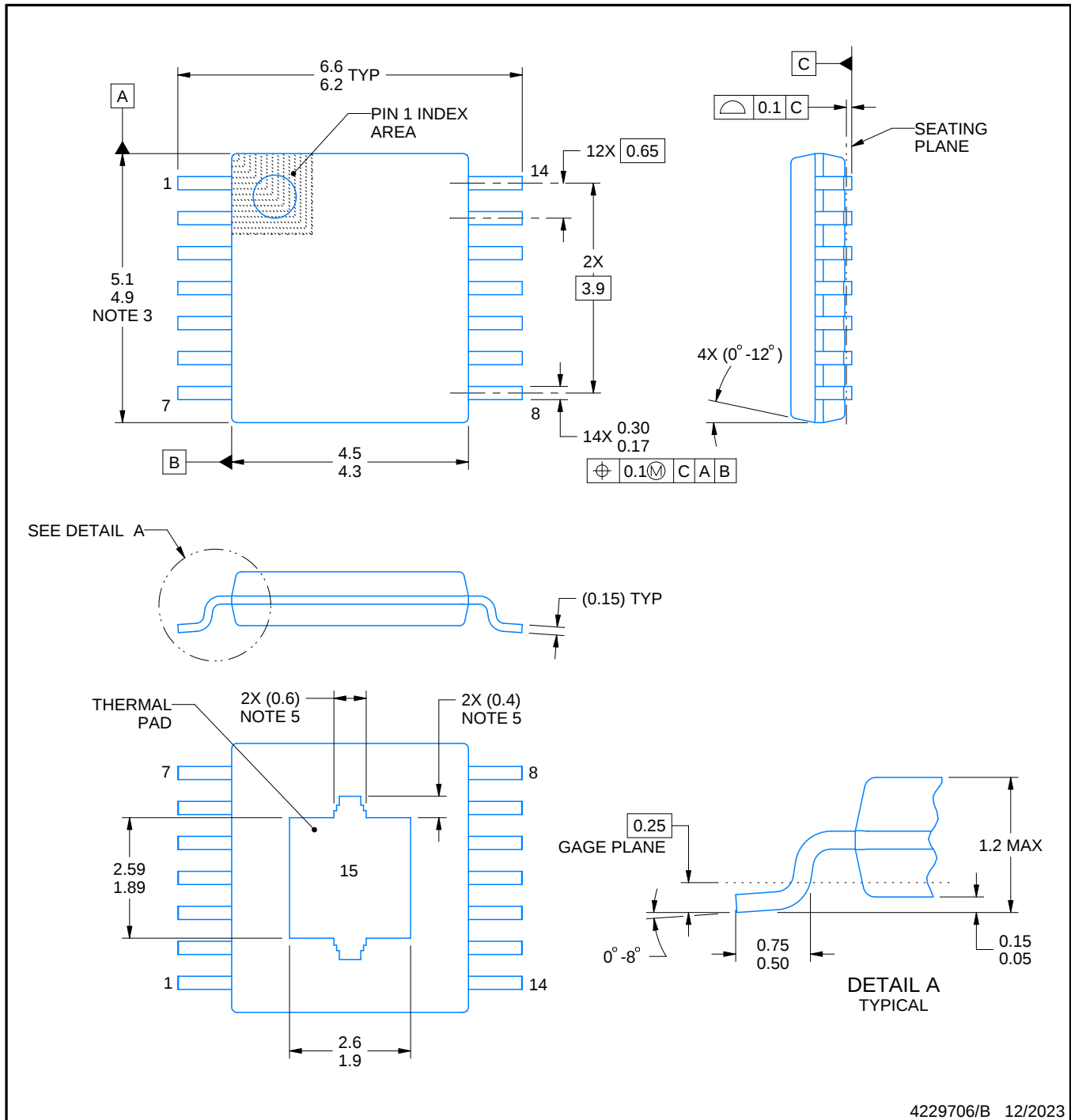
4.4 x 5.0, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224995/A



4229706/B 12/2023

NOTES:

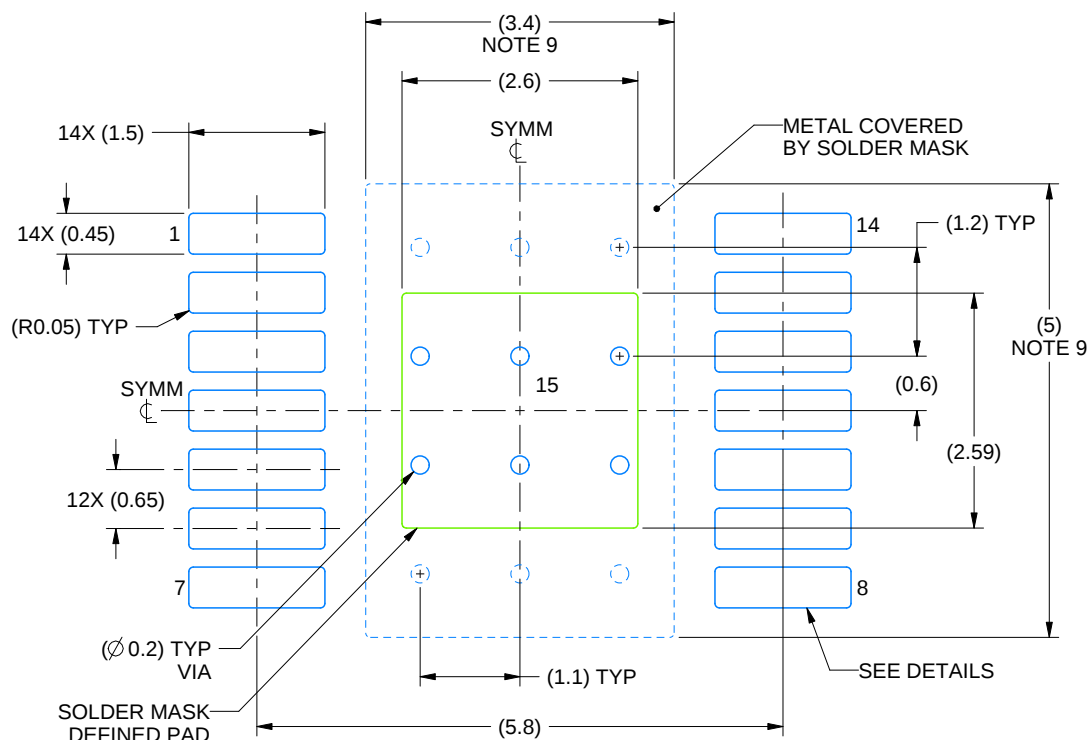
PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

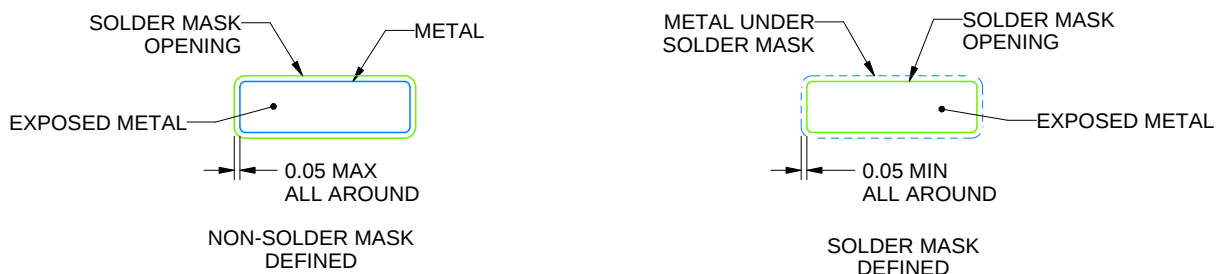
PWP0014K

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X



SOLDER MASK DETAILS

4229706/B 12/2023

NOTES: (continued)

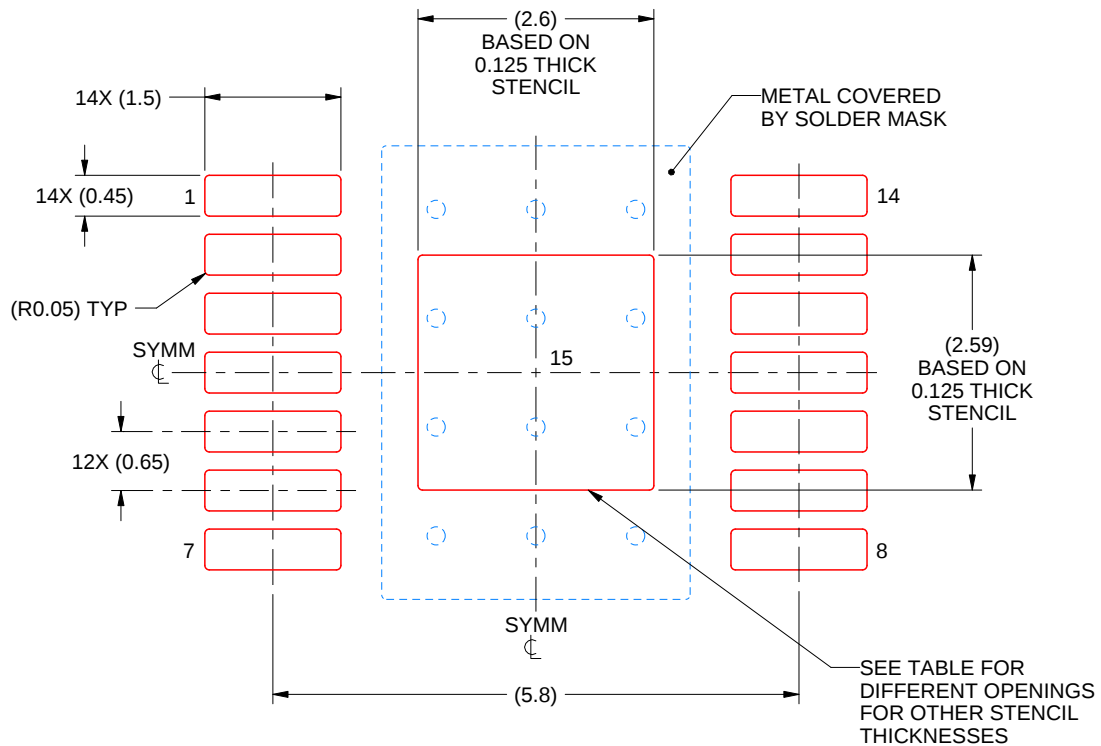
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

PWP0014K

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 2.90
0.125	2.60 X 2.59 (SHOWN)
0.15	2.37 X 2.36
0.175	2.20 X 2.19

4229706/B 12/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
版权所有 © 2025，德州仪器 (TI) 公司