

SNx4AC14 六路施密特触发反相器

1 特性

- V_{CC} 工作范围为 2V 至 6V
- 输入电压高达 6V
- t_{pd} 最大值为 9.5ns (5V 时)

2 应用

- 同步反相时钟输入
- 对开关进行去抖
- 对数字信号进行反相

3 说明

这些施密特触发器件包含六个独立的逆变器。

器件信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾	本体尺寸 ⁽³⁾
SNx4AC14	BQA (WQFN , 14)	3.00mm × 2.50mm	3.00mm × 2.50mm
	D (SOIC , 14)	8.65mm × 6mm	8.65mm × 3.9mm
	DB (SSOP , 14)	6.2mm × 7.8mm	6.2mm × 5.3mm
	N (PDIP , 14)	19.3mm × 9.4mm	19.3mm × 6.35mm
	NS (SOP , 14)	10.2mm × 7.8mm	10.3mm × 5.3mm
	PW (TSSOP , 14)	5mm × 6.4mm	5mm × 4.4mm

- 有关更多信息，请参阅节 11。
- 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。
- 本体尺寸 (长 × 宽) 为标称值，不包括引脚。



逻辑图 (正逻辑)



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4 引脚配置和功能

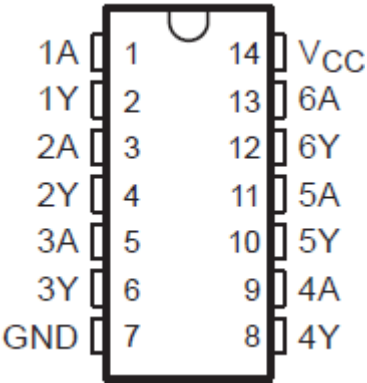


图 4-1. SN54AC14 J 或 W 封装；SN74AC14 D、DB、N、NS 或 PW 封装；14 引脚 CDIP、CFP、SSOP、SOIC、PDIP、SOP 或 TSSOP (顶视图)

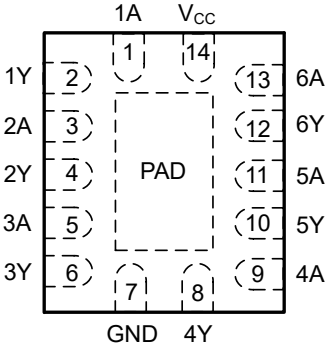
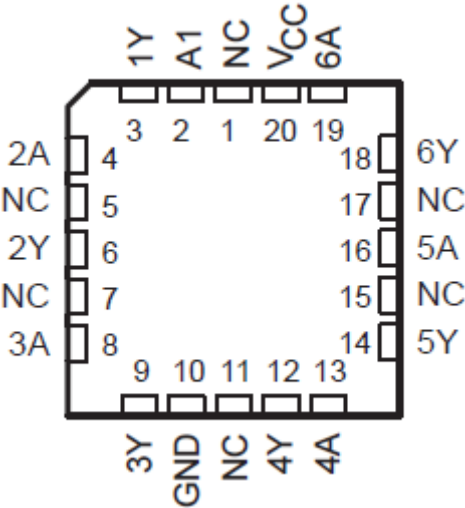


图 4-2. SN54AC14 BQA 封装，14 引脚 WQFN (顶视图)



NC - 无内部连接

图 4-3. SN54AC14 FK 封装，20 引脚 LCCC (顶视图)

表 4-1. 引脚功能

名称	引脚		I/O	说明
	D、DB、N、NS、PW、BQA、J 或 W	FK		
1A	1	2	输入	通道 1，输入 A
1Y	2	3	输出	通道 1，输出 Y
2A	3	4	输入	通道 2，输入 A
2Y	4	6	输出	通道 2，输出 Y
3A	5	8	输入	通道 3，输入 A
3Y	6	9	输出	通道 3，输出 Y
GND	7	10	—	接地

表 4-1. 引脚功能 (续)

引脚			I/O	说明
名称	D、DB、N、NS、PW、BQA、J 或 W	FK		
4Y	8	12	输出	通道 4，输出 Y
4A	9	13	输入	通道 4，输入 A
5Y	10	14	输出	通道 5，输出 Y
5A	11	16	输入	通道 5，输入 A
6Y	12	18	输出	通道 6，输出 Y
6A	13	19	输入	通道 6，输入 A
V _{CC}	14	20	—	正电源
NC		1、5、7、11、15、17	—	无内部连接
散热焊盘 ⁽¹⁾			—	散热焊盘可连接到 GND 或悬空。请勿连接到任何其他信号或电源。

(1) 仅限 BQA 封装。

5 规格

5.1 绝对最大额定值

在自然通风条件下的工作温度范围内测得 (除非另有说明) ⁽¹⁾

		最小值	最大值	单位
V _{CC}	电源电压范围	-0.5V	7	V
V _I ⁽²⁾	输入电压范围	-0.5V	V _{CC} + 0.5	V
V _O ⁽²⁾	输出电压范围	-0.5V	V _{CC} + 0.5	V
I _{IK}	输入钳位电流	(V _I < 0 或 V _I > V _{CC})	±20	mA
I _{OK}	输出钳位电流	(V _O < 0 或 V _O > V _{CC})	±20	mA
I _O	持续输出电流	(V _O = 0 至 V _{CC})	±50	mA
	通过 V _{CC} 或 GND 的持续电流		±200	mA
T _{stg}	贮存温度范围	-65	150	°C

- (1) 应力超出绝对最大额定值下列出的值可能会对器件造成永久损坏。这些仅为应力额定值，并不表示器件在这些条件下以及在建议运行条件以外的任何其他条件下能够正常运行。长时间处于绝对最大额定条件下可能会影响器件的可靠性。
- (2) 如果遵守输入和输出电流额定值，输入和输出电压可超过额定值。

5.2 ESD 等级

			值	单位
V _(ESD)	静电放电	人体放电模型 (HBM)，符合 ANSI/ESDA/JEDEC JS-001 标准，所有引脚 ⁽¹⁾	±4000	V
		充电器件模型 (CDM)，符合 JEDEC 规范 JESD22-C101，所有引脚 ⁽²⁾	±2000	

- (1) JEDEC 文档 JEP155 指出：500V HBM 时能够在标准 ESD 控制流程下安全生产。
- (2) JEDEC 文档 JEP157 指出：250V CDM 时能够在标准 ESD 控制流程下安全生产。

5.3 建议运行条件

		SN54AC14		SN74AC14		单位
		最小值	最大值	最小值	最大值	
V _{CC}	电源电压	2	6	2	6	V
V _I	输入电压	0	V _{CC}	0	V _{CC}	V
V _O	输出电压	0	V _{CC}	0	V _{CC}	V
I _{OH}	高电平输出电流	V _{CC} = 3V		-12		mA
		V _{CC} = 4.5V		-24		
		V _{CC} = 5.5V		-24		
I _{OL}	低电平输出电流	V _{CC} = 3V		12		mA
		V _{CC} = 4.5V		24		
		V _{CC} = 5.5V		24		
T _A	自然通风条件下的工作温度范围	-55	125	-40	85	°C

5.4 热性能信息

热性能指标 ⁽¹⁾		SN74AC14						单位
		BQA (WQFN)	D (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	
		14 引脚						
R _{θJA}	结至环境热阻	93.4	89.9	96	72.1	92.4	148	°C/W

- (1) 有关新旧热指标的更多信息，请参阅 [半导体和 IC 封装热指标](#) 应用报告。

5.5 电气特性

在自然通风条件下的建议运行温度范围内测得（除非另有说明）

参数	测试条件	V _{CC}	T _A = 25°C			SN54AC14		SN74AC14		单位
			最小值	典型值	最大值	最小值	最大值	最小值	最大值	
V _{T+} 正向 阈值		3V	0.8	1.8	2.2	0.8	2.2	0.8	2.2	V
		4.5V	1.5	2.6	3.2	1.5	3.2	1.5	3.2	
		5.5V	1.6	3.2	3.9	1.6	3.9	1.6	3.9	
V _{T-} 负向 阈值		3V	0.5	0.8	1	0.5	1.2	0.5	1	V
		4.5V	0.9	1.4	1.8	0.9	1.8	0.9	1.8	
		5.5V	1.1	1.8	2.3	1.1	2.3	1.1	2.3	
Δ V _T 迟滞 (V _{T+} - V _{T-})		3V	0.3	1	1.2	0.3	1.2	0.3	1.2	V
		4.5V	0.4	1.2	1.4	0.4	1.4	0.4	1.4	
		5.5V	0.5	1.4	1.6	0.5	1.6	0.5	1.6	
V _{OH}	I _{OH} = -50 μ A	3V	2.9			2.9		2.9		V
		4.5V	4.4			4.4		4.4		
		5.5V	5.4			5.4		5.4		
	I _{OH} = -12mA	3V	2.56			2.4		2.48		
	I _{OH} = -24mA	4.5V	3.86			3.7		3.8		
		5.5V	4.86			4.7		4.8		
	I _{OH} = -50mA ⁽¹⁾	5.5V				3.85				
	I _{OH} = -75mA ⁽¹⁾							3.85		
V _{OL}	I _{OL} = 50 μ A	3V	0.1			0.1		0.1		V
		4.5V	0.1			0.1		0.1		
		5.5V	0.1			0.1		0.1		
	I _{OL} = 12mA	3V	0.36			0.44		0.44		
	I _{OL} = 24mA	4.5V	0.36			0.44		0.44		
		5.5V	0.36			0.44		0.44		
	I _{OL} = 50mA ⁽¹⁾	5.5V				1.65				
	I _{OL} = 75mA ⁽¹⁾							1.65		
I _I	V _I = V _{CC} 或 GND	5.5V	±0.1			±1		±1		μ A
I _{CC}	V _I = V _{CC} 或 GND , I _O = 0	5.5V	2			40		20		μ A
C _i	V _I = V _{CC} 或 GND	5V	4.5							pF

(1) 一次不应测试超过一个输出，且测试持续时间不应超过 10 ms。

5.6 开关特性

在自然通风条件下的建议工作温度范围内测得，V_{CC} = 3.3V ± 0.3V（除非另有说明）（请参阅[负载电路和电压波形](#)）

参数	从 (输入)	至 (输出)	T _A = 25°C			SN54AC14		SN74AC14		单位
			最小值	典型值	最大值	最小值	最大值	最小值	最大值	
t _{PLH}	A	Y	1.5	6	13.5	1	16	1.5	15	ns
t _{PHL}			1.5	6	11.5	1	14	1.5	13	

5.7 开关特性

在自然通风条件下的建议工作温度范围内测得， $V_{CC} = 5V \pm 0.5V$ (除非另有说明) (请参阅[负载电路和电压波形](#))

参数	从 (输入)	至 (输出)	$T_A = 25^\circ\text{C}$			SN54AC14		SN74AC14		单位
			最小值	典型值	最大值	最小值	最大值	最小值	最大值	
t_{PLH}	A	Y	1.5	5	10	1.5	12	1.5	11	ns
t_{PHL}			1.5	5	8.5	1.5	10	1.5	9.5	

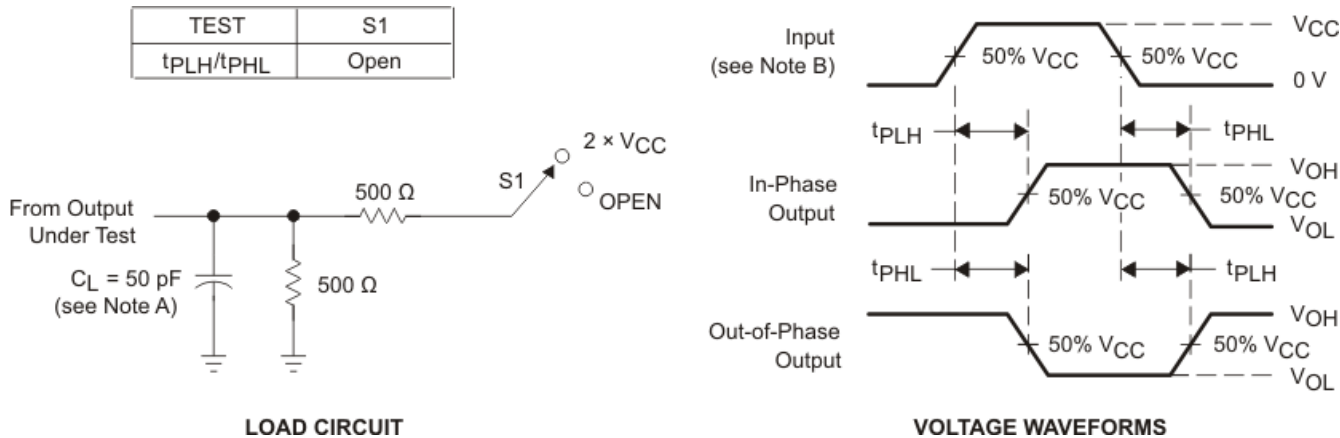
5.8 工作特性

$V_{CC} = 5V$, $T_A = 25^\circ\text{C}$

参数		测试条件	典型值	单位
C_{pd}	功率耗散电容	$C_L = 50\text{pF}$, $f = 1\text{ MHz}$	25	pF

6 参数测量信息

6.1



- A. C_L 包括探针和夹具电容。
- B. 所有输入脉冲均由具有以下特性的发生器提供： $PRR \leq 1\text{MHz}$ ， $Z_O = 50 \Omega$ ， $t_r \leq 2.5 \text{ ns}$ ， $t_f \leq 2.5 \text{ ns}$ 。
- C. 一次测量一个输出，每次测量一个输入转换。

图 6-1. 负载电路和电压波形

7 详细说明

7.1 概述

这些 'AC14 器件执行布尔函数 $Y = \overline{A}$ 。但出于施密特操作方面的原因，对于正向 (V_{T+}) 和负向 (V_{T-}) 信号，这些器件可能具有不同的输入阈值。

这些电路经过温度补偿，可由非常慢的输入斜坡触发，并且仍然能够提供干净无抖动的输出信号。与传统反相器相比，它们还具有更大的噪声容限。

7.2 功能方框图



7.3 特性说明

- V_{CC} 优化为 5V
- 允许从 3.3V 至 5V 的升压转换
 - 输入接受 2V 的 V_{IH} 电平
- 慢速边沿速率可更大限度减少输出振铃
- 输入兼容 TTL 电压

7.3.1 平衡 CMOS 推挽式输出

该器件包括平衡 CMOS 推挽输出。术语 *平衡* 表示器件可以灌入和拉出相似的电流。此器件的驱动能力可能在轻负载时产生快速边缘，因此应考虑布线和负载条件以防止振铃。此外，该器件的输出能够驱动比此器件能够承受的电流更大，而不会损坏器件。务必限制器件的输出功率，以避免因过流而损坏器件。必须始终遵守 *绝对最大额定值* 中规定的电气和热限值。

未使用的推挽 CMOS 输出必须保持断开状态。

7.3.2 钳位二极管结构

该器件的输入和输出同时具有正和负钳位二极管，如图 7-1 所示。

小心

电压超出绝对最大额定值表中规定的值可能会损坏器件。如果遵守输入和输出钳制电流额定值，输入和输出电压可超过额定值。

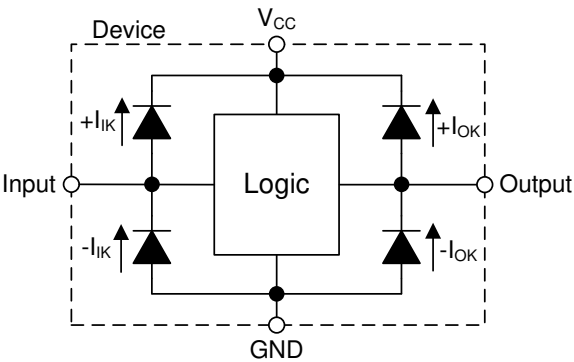


图 7-1. 每个输入和输出的钳位二极管的电气布置

7.4 器件功能模式

表 7-1. 功能表

输入	输出
A	Y
H	L
L	H

8 应用信息免责声明

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 应用信息

SNx4AC14 器件是一款低驱动 CMOS 器件，可用于需要考虑输出振铃的多种总线接口类型应用。低驱动和慢速边沿速率将更大幅度地减少输出上的过冲和下冲。在任何有效的 V_{CC} 下，输入可耐受 5.5V 电压。这个特性使其非常适合向下转换至 V_{CC} 电平。[开关特性比较](#) 展示了该器件与更高驱动器件（如交流驱动）相比的振铃降低。

8.2 典型应用

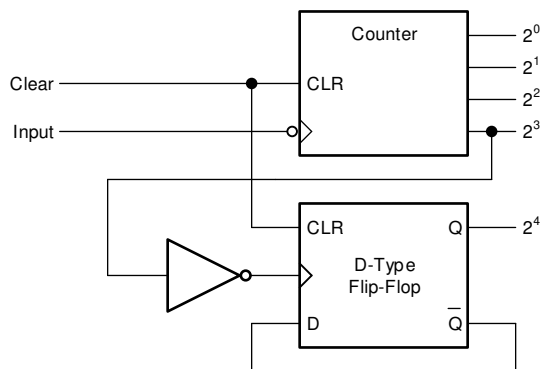


图 8-1. 典型应用原理图

8.2.1 设计要求

此器件采用 CMOS 技术并具有平衡输出驱动。注意避免总线争用，因为它可以驱动超过最大限制的电流。高驱动也会在轻负载时产生快速边缘，因此应考虑布线和负载条件以防止振铃。

8.2.2 详细设计过程

1. 建议的输入条件

- 有关上升时间和下降时间规格，请参阅 [节 5.3](#) 表中的 $\Delta t / \Delta V$ 。
- 有关指定的高电平和低电平，请参阅 [节 5.3](#) 表中的 V_{IH} 和 V_{IL} 。
- 输入具有过压容限，允许它们在任何有效 V_{CC} 下高达 5.5V。

2. 建议的输出条件

- 每个输出的负载电流不应超过 35mA，该器件的总电流不应超过 70mA。
- 输出不应被拉至高于 V_{CC} 。

8.2.3 应用曲线

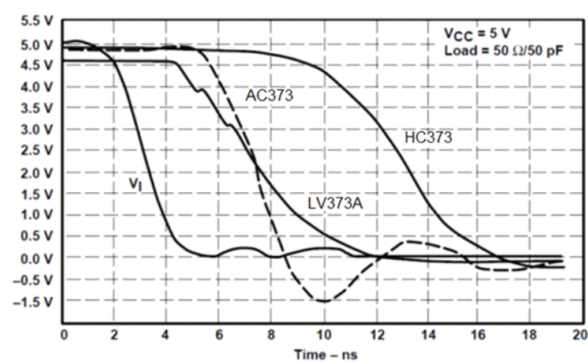


图 8-2. 开关特性比较

8.3 电源相关建议

电源可以是 [节 5.3](#) 中最小和最大电源电压额定值之间的任意电压。

每个 V_{CC} 引脚应具有一个良好的旁路电容器，以防止功率干扰。对于单电源器件，建议使用 $0.1\ \mu\text{f}$ ；如果有多个 V_{CC} 引脚，则建议每个电源引脚使用 $0.01\ \mu\text{f}$ 或 $0.022\ \mu\text{f}$ 。可以并联多个旁路电容器以抑制不同的噪声频率。 $0.1\ \mu\text{f}$ 和 $1\ \mu\text{f}$ 通常并联使用。为了获得更佳效果，旁路电容器应尽可能靠近电源引脚安装。

8.4 布局

8.4.1 布局指南

当使用多位逻辑器件时，输入不应悬空。在许多情况下，数字逻辑器件的功能或部分功能未被使用。例如，在仅使用三输入与门的两个输入，或仅使用 4 个缓冲门中的 3 个时。此类输入引脚不应悬空，因为外部连接处的未定义电压会导致未定义的运行状态。

布局图指定了在所有情况下都必须遵守的规则。数字逻辑器件的所有未使用输入必须连接至一个高或低偏置以防止悬空。应为任何特定未使用输入施加的逻辑电平取决于器件的功能。通常，将这些输入连接到 **GND** 或 V_{CC} ，具体取决于哪种更合理或更方便。使输出悬空是可以接受的，除非该器件是收发器。如果该收发器有一个输出使能引脚，它会在置为有效时禁用该器件的输出部分。这不会禁用 I/O 的输入部分，因此输入在禁用后也无法悬空。

8.4.2 布局示例

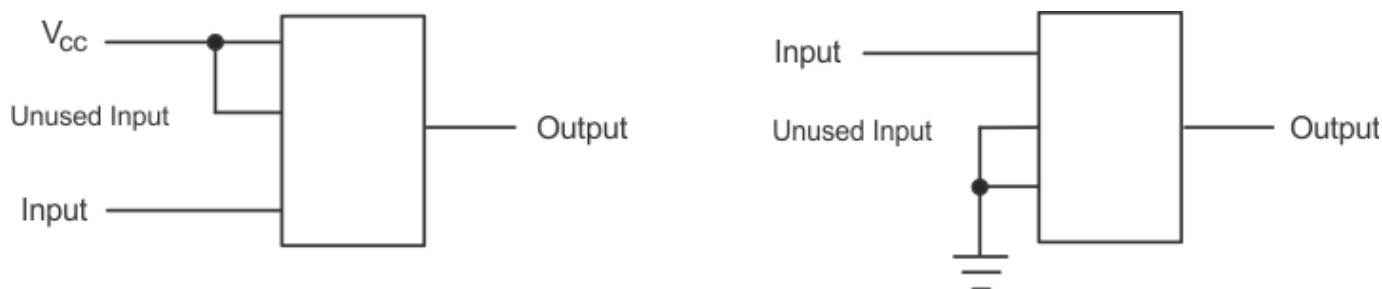


图 8-3. 布局图

9 器件和文档支持

9.1 文档支持

9.1.1 相关文档

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 9-1. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具和软件	支持和社区
SN54AC14	点击此处	点击此处	点击此处	点击此处	点击此处
SN74AC14	点击此处	点击此处	点击此处	点击此处	点击此处

9.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](#) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

9.4 商标

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

9.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

10 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision H (January 2023) to Revision I (July 2024)	Page
• 向 封装信息 表、“引脚配置和功能”部分以及 热性能信息 表中添加了 BQA 封装尺寸.....	1
• 向 器件信息 表中添加了封装尺寸.....	1
• 更新了 R _{θJA} 值：D 封装从 86 更新为 89.9，DB 封装从 96 更新为 101.2，N 封装从 80 更新为 72.1，NS 封装从 76 更新为 92.4，PW 封装从 113 更新为 148，所有值均以 °C/W 为单位.....	5

Changes from Revision G (August 2008) to Revision H (January 2023)

Page

- 添加了应用、器件信息表、引脚功能表、ESD 等级表、热性能信息表、典型特性、特性说明部分、器件功能模式、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分 [1](#)

11 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-87624012A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 87624012A SNJ54AC 14FK
5962-8762401CA	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8762401CA SNJ54AC14J
5962-8762401DA	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8762401DA SNJ54AC14W
5962-8762401VCA	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8762401VC A SNV54AC14J
5962-8762401VDA	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8762401VD A SNV54AC14W
5962-8762402VCA	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8762402VC A SNV54AC14J
5962-8762402VDA	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8762402VD A SNV54AC14W
SN74AC14BQAR	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC14
SN74AC14D	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	-40 to 85	AC14
SN74AC14DBR	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC14
SN74AC14DR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC14
SN74AC14N	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74AC14N
SN74AC14NSR	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC14
SN74AC14PW	Obsolete	Production	TSSOP (PW) 14	-	-	Call TI	Call TI	-40 to 85	AC14
SN74AC14PWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC14
SN74AC14PWRG4	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC14
SNJ54AC14FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 87624012A SNJ54AC 14FK

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54AC14J	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8762401CA SNJ54AC14J
SNJ54AC14W	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8762401DA SNJ54AC14W

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54AC14, SN54AC14-SP, SN74AC14 :

- Catalog : [SN74AC14](#), [SN54AC14](#)

- Automotive : [SN74AC14-Q1](#), [SN74AC14-Q1](#)
- Military : [SN54AC14](#)
- Space : [SN54AC14-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

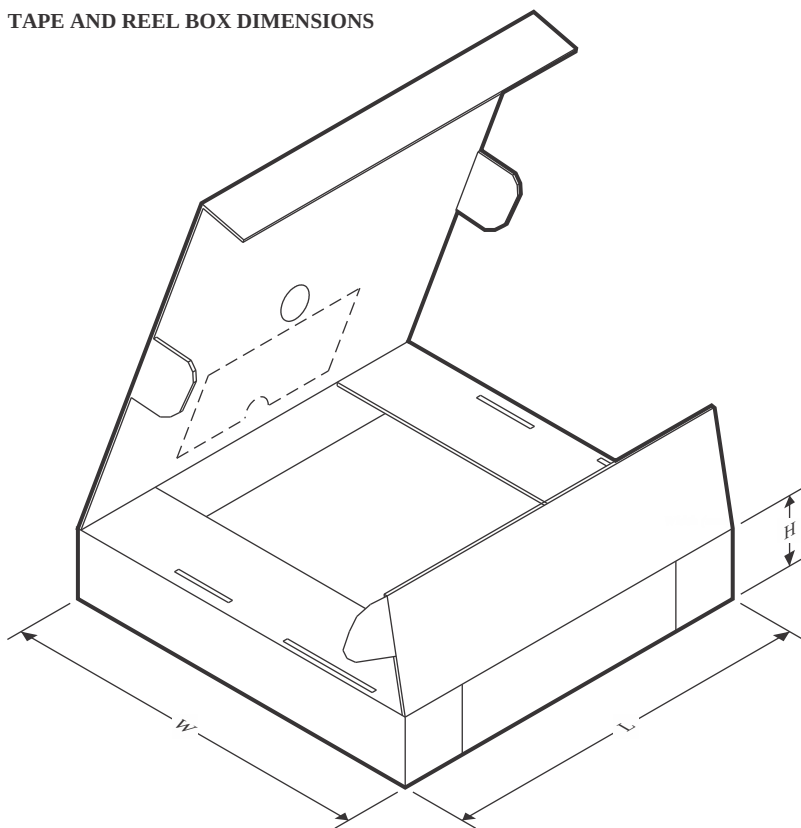
TAPE AND REEL INFORMATION



*All dimensions are nominal

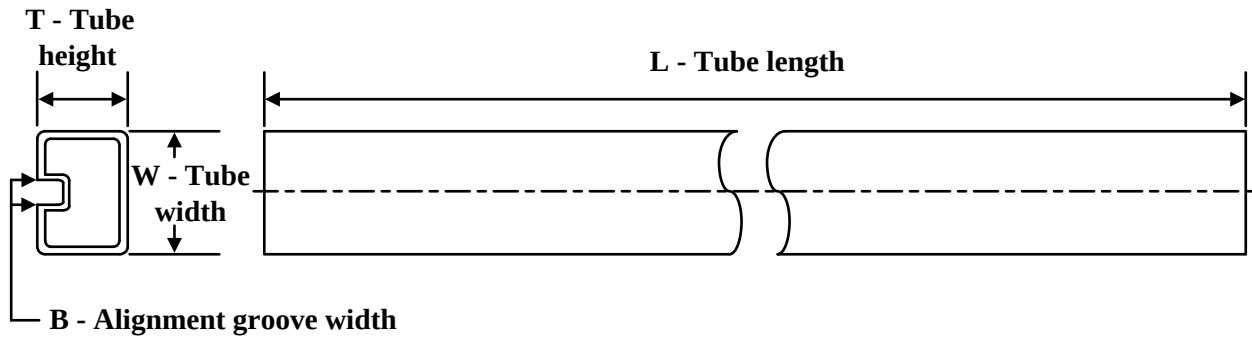
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC14BQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74AC14DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AC14DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AC14DR	SOIC	D	14	2500	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
SN74AC14DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AC14DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AC14NSR	SOP	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AC14NSR	SOP	NS	14	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
SN74AC14PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AC14PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AC14PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AC14PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



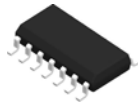
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AC14BQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74AC14DBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74AC14DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74AC14DR	SOIC	D	14	2500	340.5	336.1	32.0
SN74AC14DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74AC14DR	SOIC	D	14	2500	356.0	356.0	35.0
SN74AC14NSR	SOP	NS	14	2000	356.0	356.0	35.0
SN74AC14NSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74AC14PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74AC14PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AC14PWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AC14PWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0

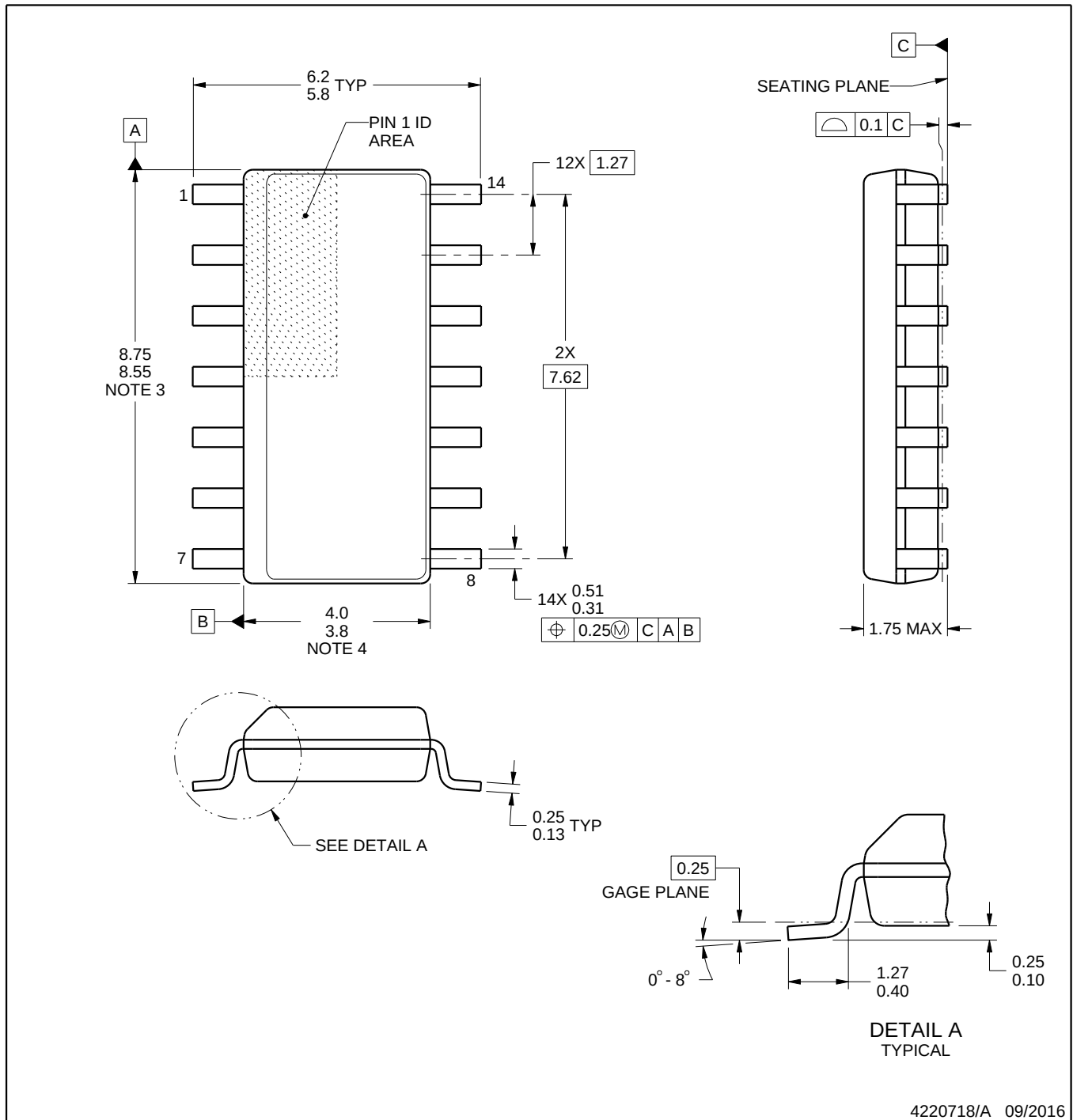
TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-87624012A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-8762401DA	W	CFP	14	25	506.98	26.16	6220	NA
5962-8762401VDA	W	CFP	14	25	506.98	26.16	6220	NA
5962-8762402VDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74AC14N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AC14N	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54AC14FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AC14W	W	CFP	14	25	506.98	26.16	6220	NA

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

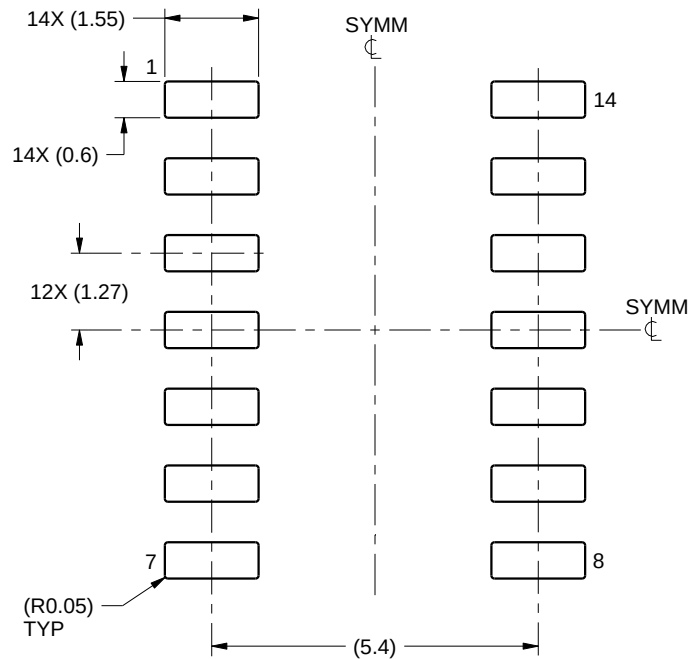
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

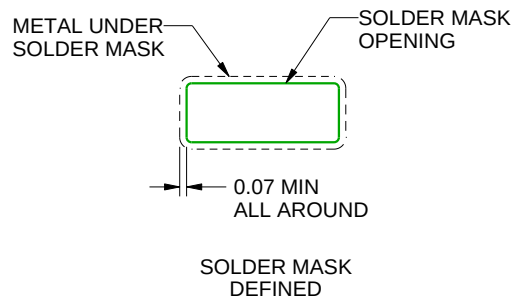
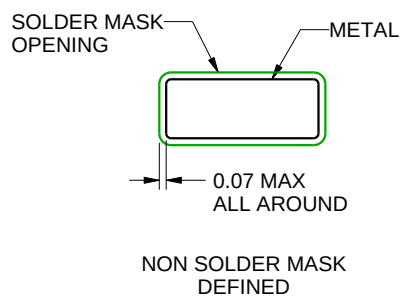
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

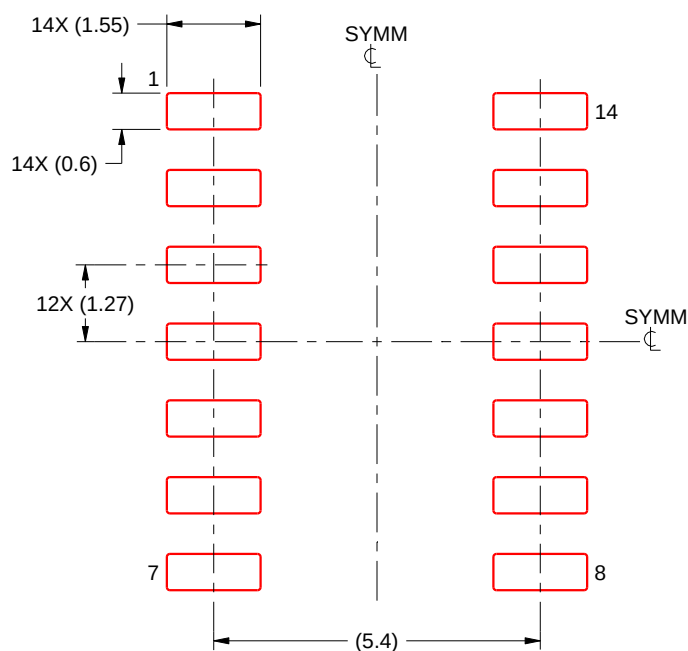
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

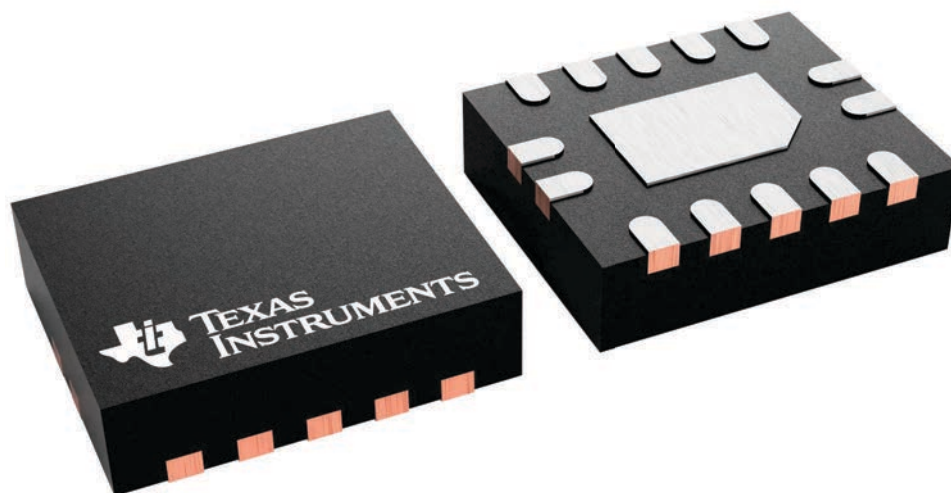
BQA 14

WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4227145/A

WQFN - 0.8 mm max height

Top View:

- Width: 2.6 (2.4)
- Height: 3.1 (2.9)
- PIN 1 INDEX AREA (shaded region)

Side View:

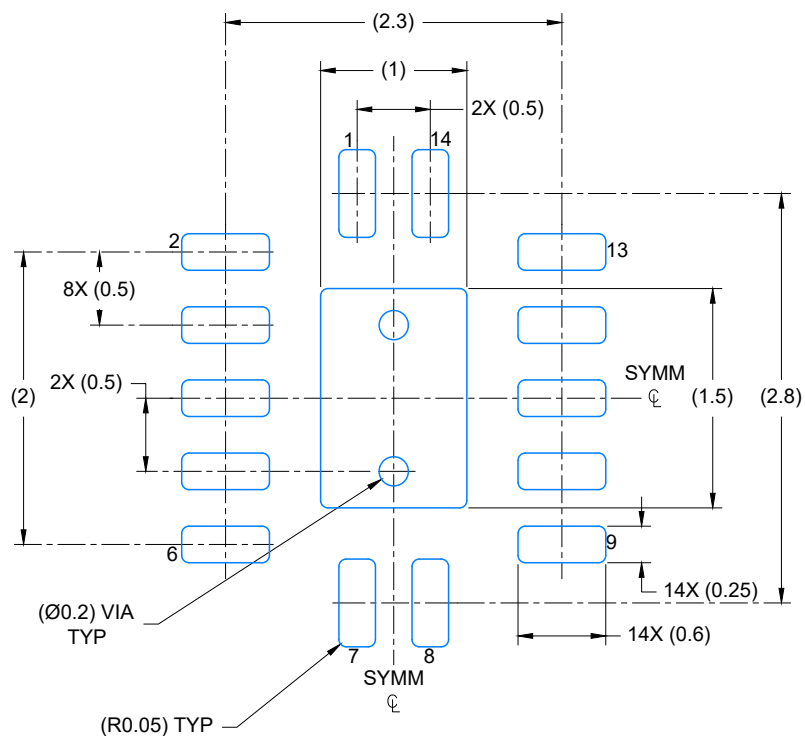
- Top wall thickness: 0.8
- Internal wall thickness: 0.7
- Base thickness: 0.05 (0.00)
- SEATING PLANE
- Radius: 0.08

Front View:

- Pin 1 ID (OPTIONAL)
- Pin 15 (SYM)
- Pin 14 (SYM)
- Pin 13 (14X 0.3, 0.2)
- Pin 9 (14X 0.5, 0.3)
- Pin 8 (2X 0.5)
- Pin 7 (1.1, 0.9)
- Pin 6 (8X 0.5)
- Pin 2 (2X 2)
- Pin 1 (1.6, 1.4)
- Pin 15 (1.6, 1.4)
- Pin 13 (14X 0.5, 0.3)
- Pin 14 (14X 0.5, 0.3)
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- Pin 144 (14X 0.5, 0.3)
- Pin 145 (14X 0.5, 0.3)
- Pin 146 (14X 0.5, 0.3)
- Pin 147 (14X 0.5, 0.3)
- Pin 148 (14X 0.5, 0.3)
- Pin 149 (14X 0.5, 0.3)
- Pin 150 (14X 0.5, 0.3)
- Pin 151 (14X 0.5, 0.3)
- Pin 152 (14X 0.5, 0.3)
- Pin 153 (14X 0.5, 0.3)
- Pin 154 (14X 0.5, 0.3)
- Pin 155 (14X 0.5, 0.3)
- Pin 156 (14X 0.5, 0.3)
- Pin 157 (14X 0.5, 0.3)
- Pin 158 (14X 0.5, 0.3)
- Pin 159 (14X 0.5, 0.3)
- Pin 160 (14X 0.5, 0.3)
- Pin 161 (14X 0.5, 0.3)
- Pin 162 (14X 0.5, 0.3)
- Pin 163 (14X 0.5, 0.3)
- Pin 164 (14X 0.5, 0.3)
- Pin 165 (14X 0.5, 0.3)
- Pin

NOTES:

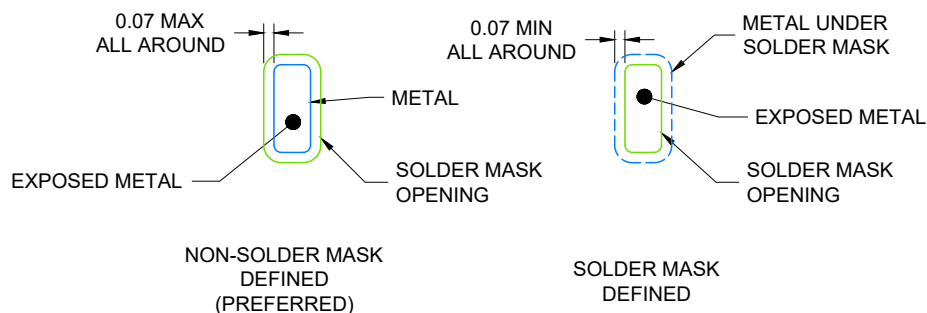
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

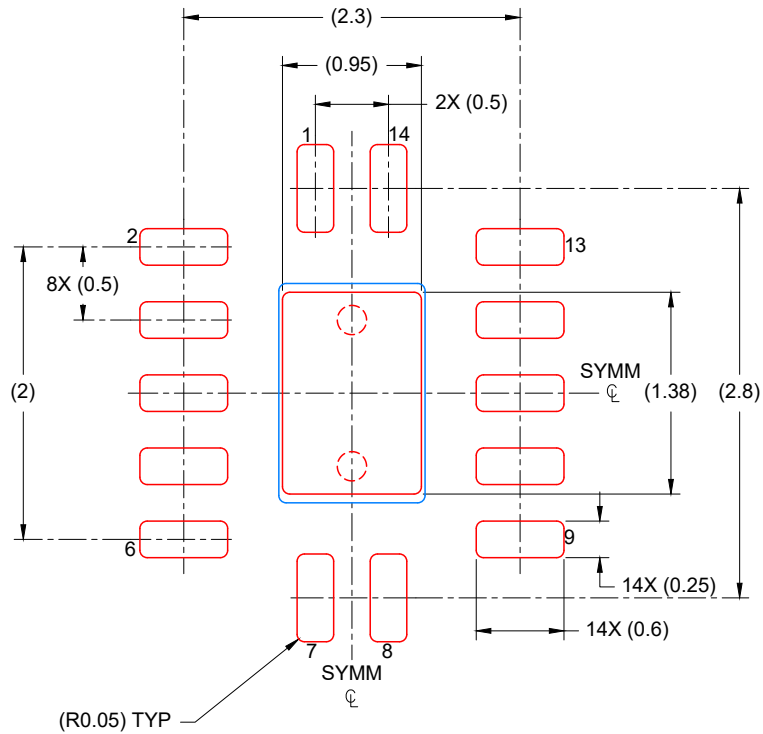
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

BQA0014A

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 20X

4224636/A 11/2018

NOTES: (continued)

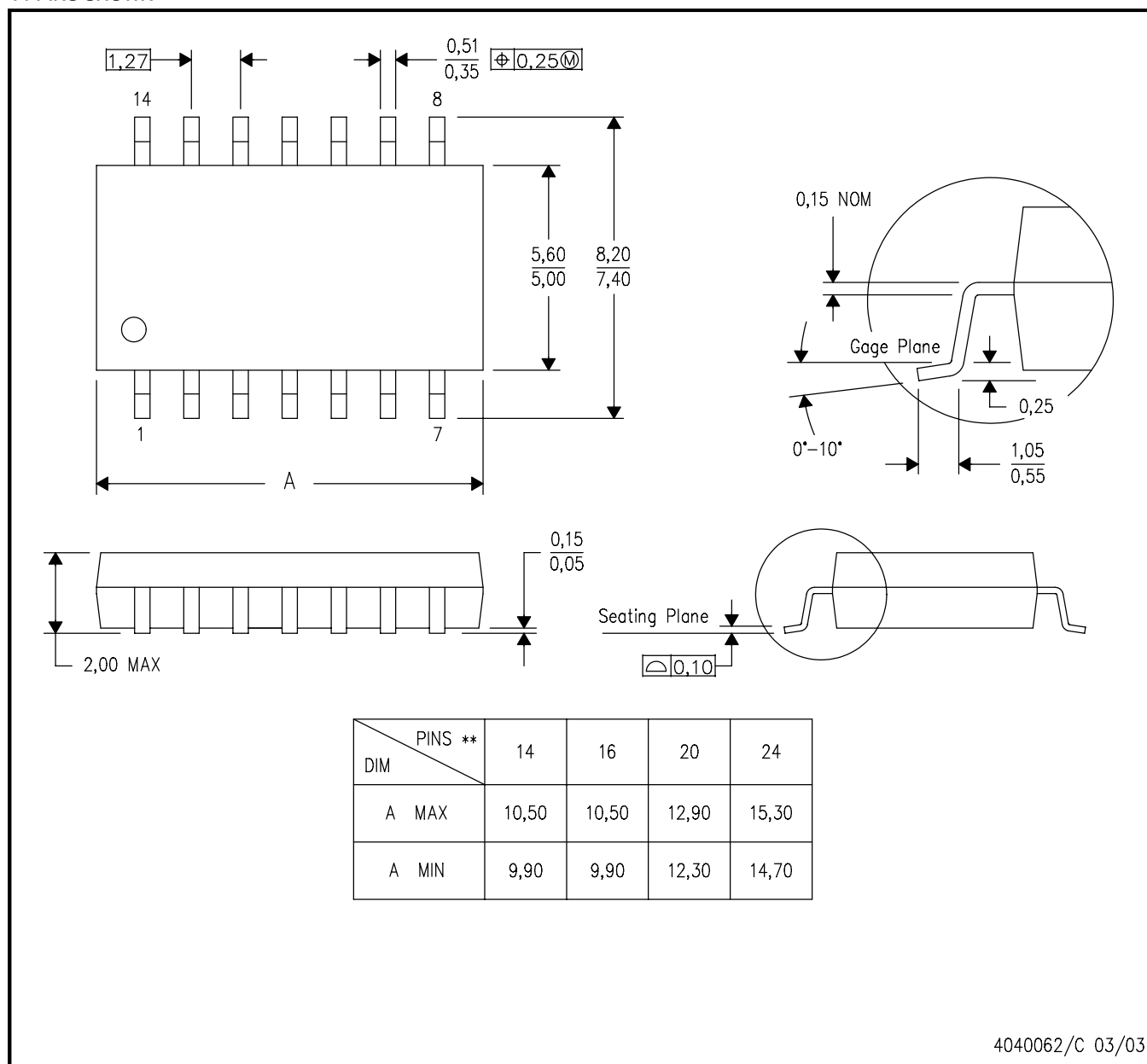
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

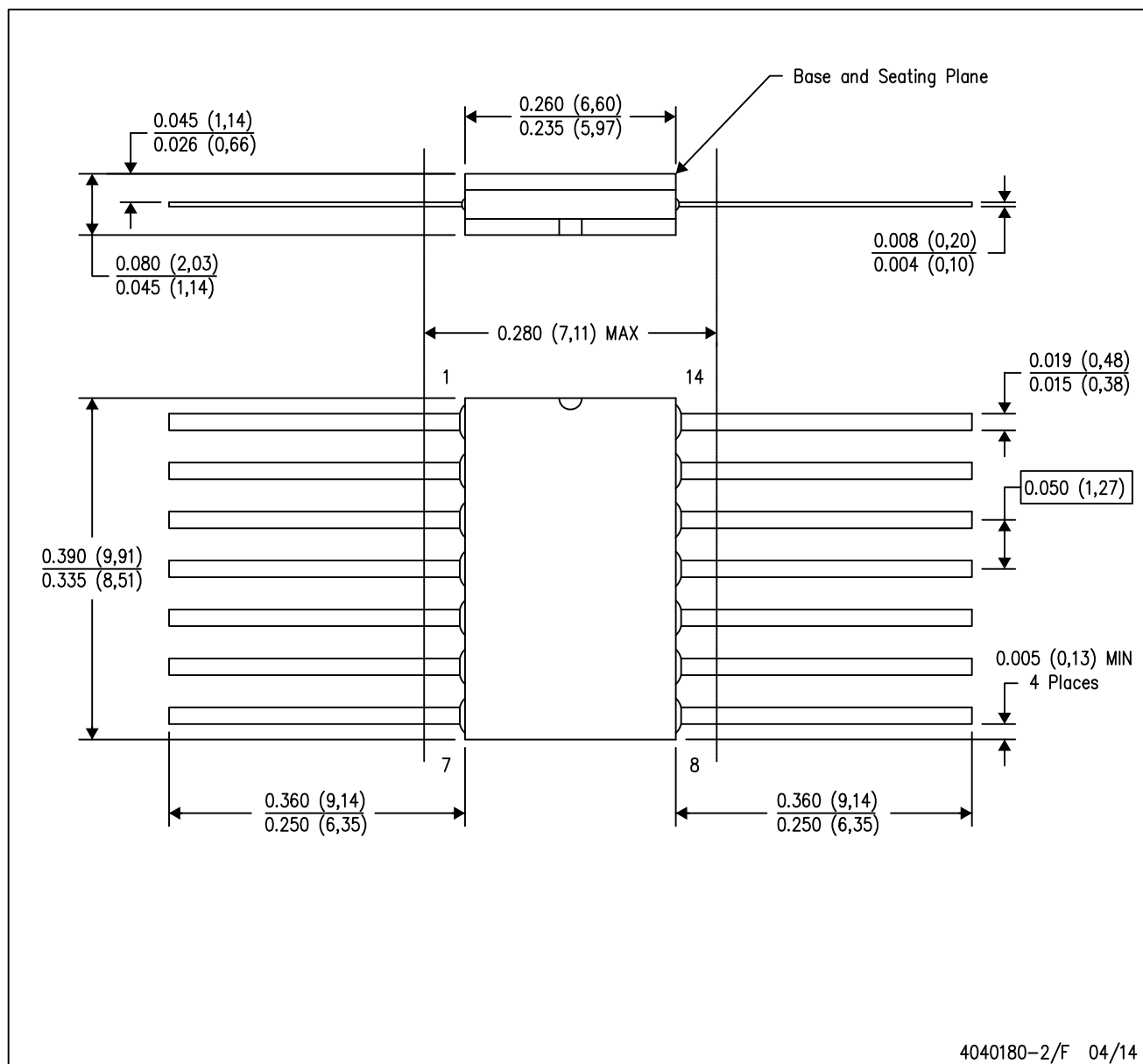
14-PINS SHOWN

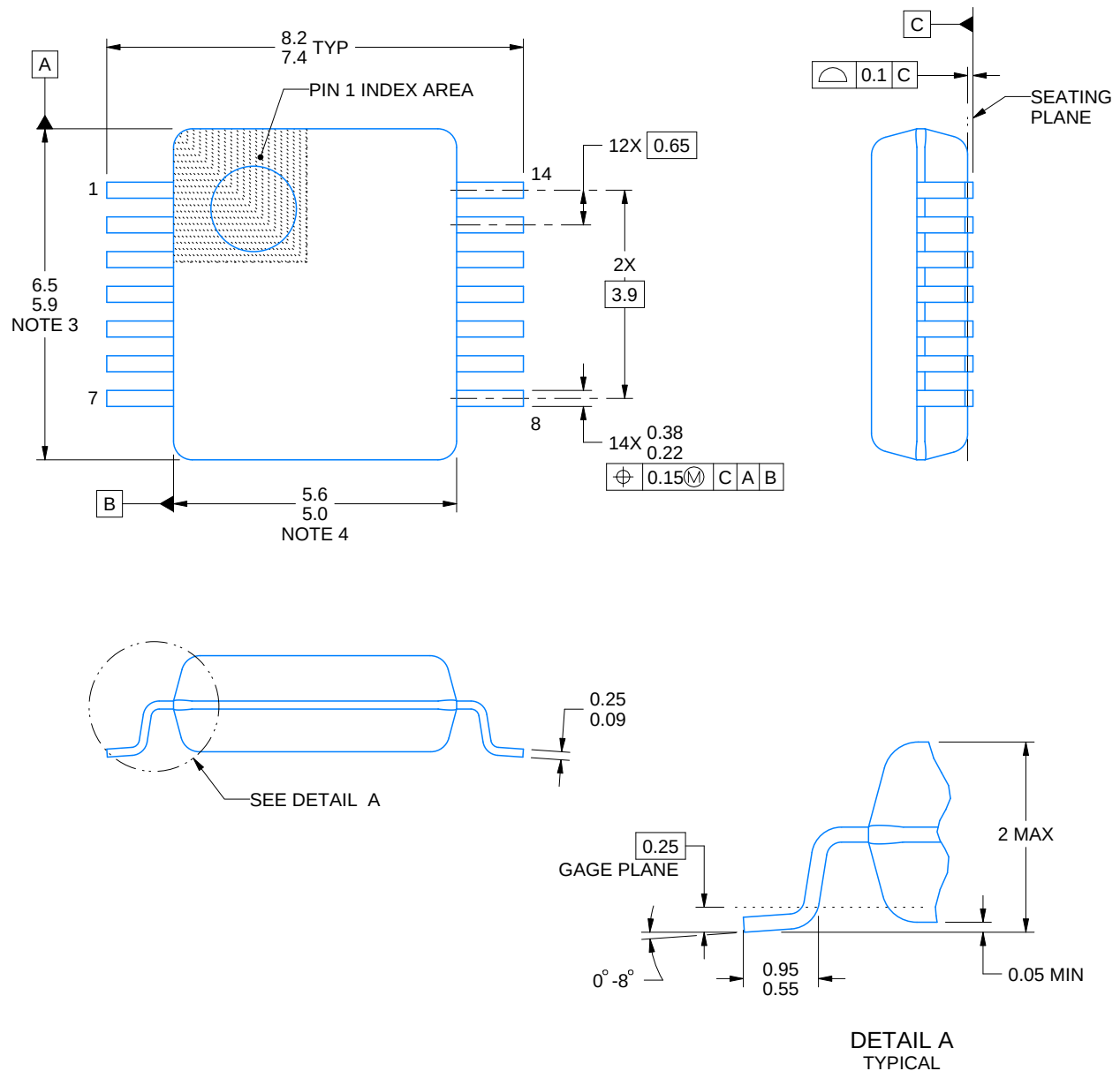
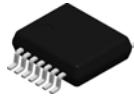


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK





4220762/A 05/2024

NOTES:

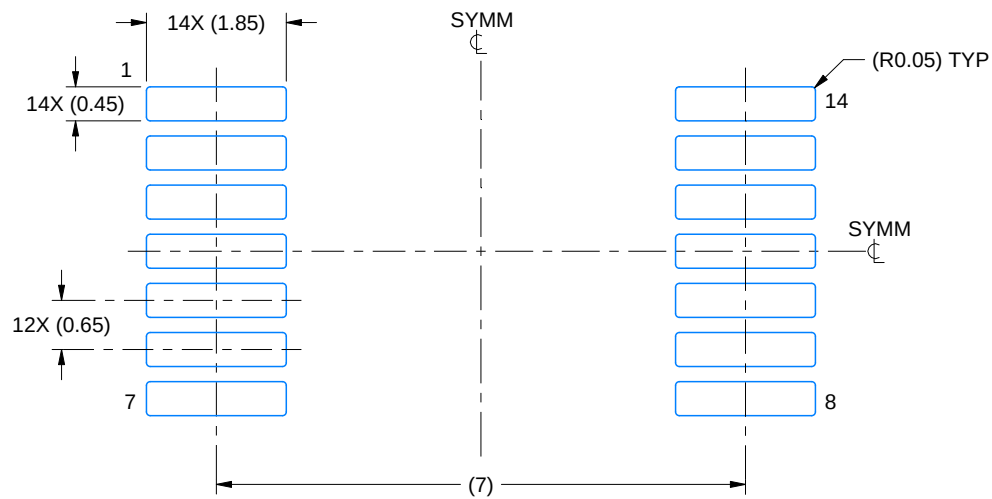
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

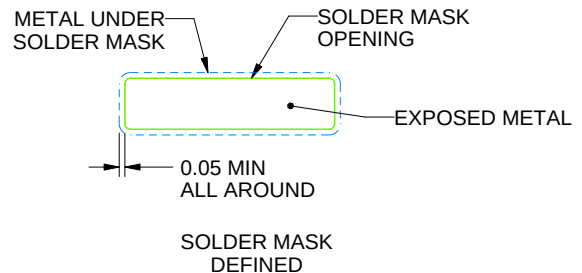
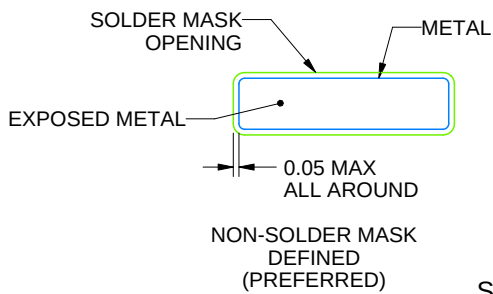
DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

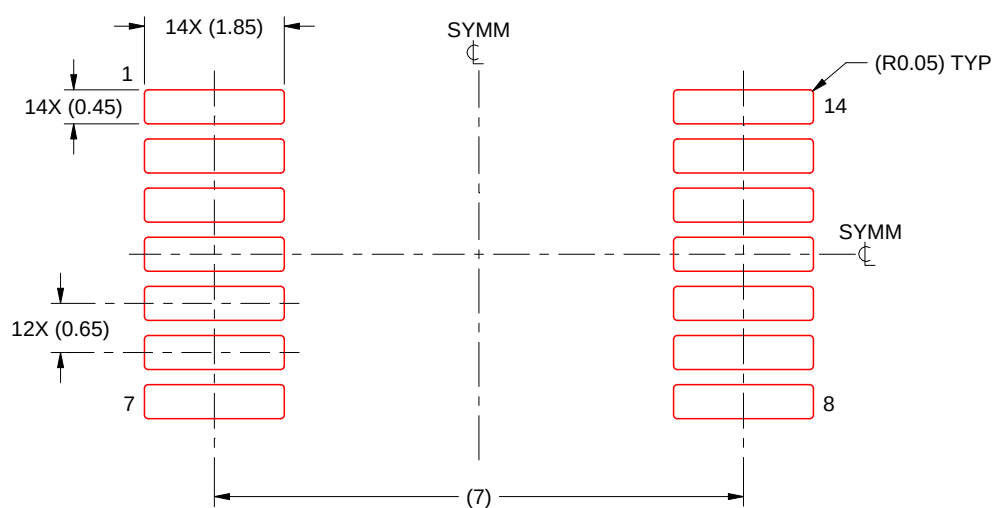
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

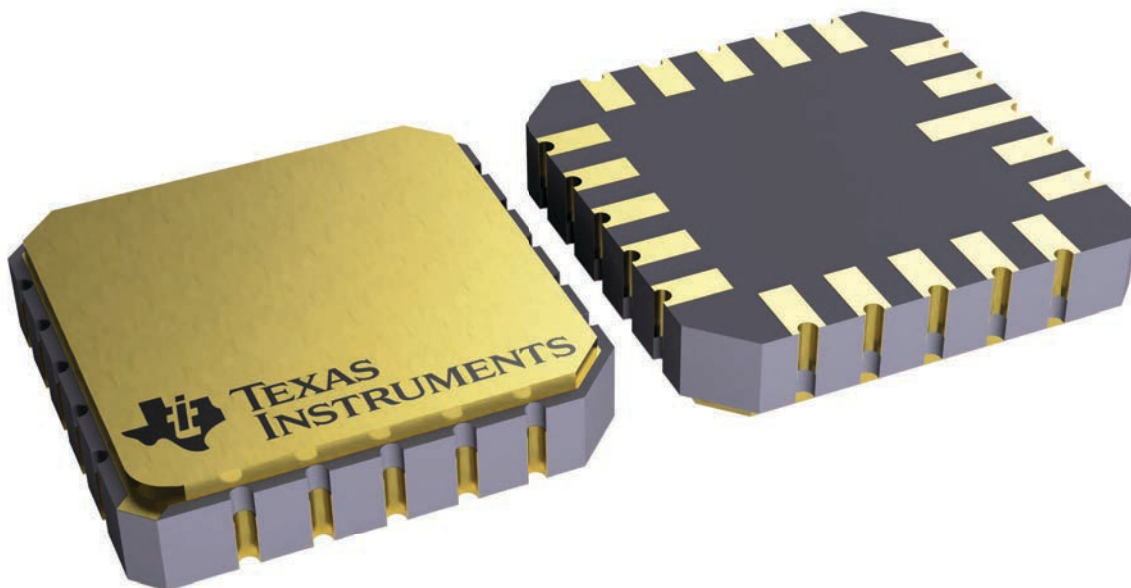
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



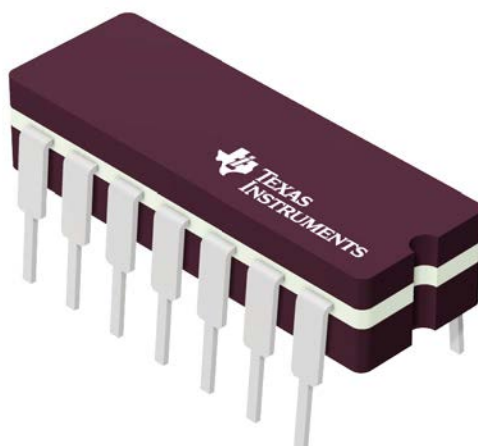
4229370VA\

J 14

GENERIC PACKAGE VIEW

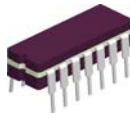
CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE

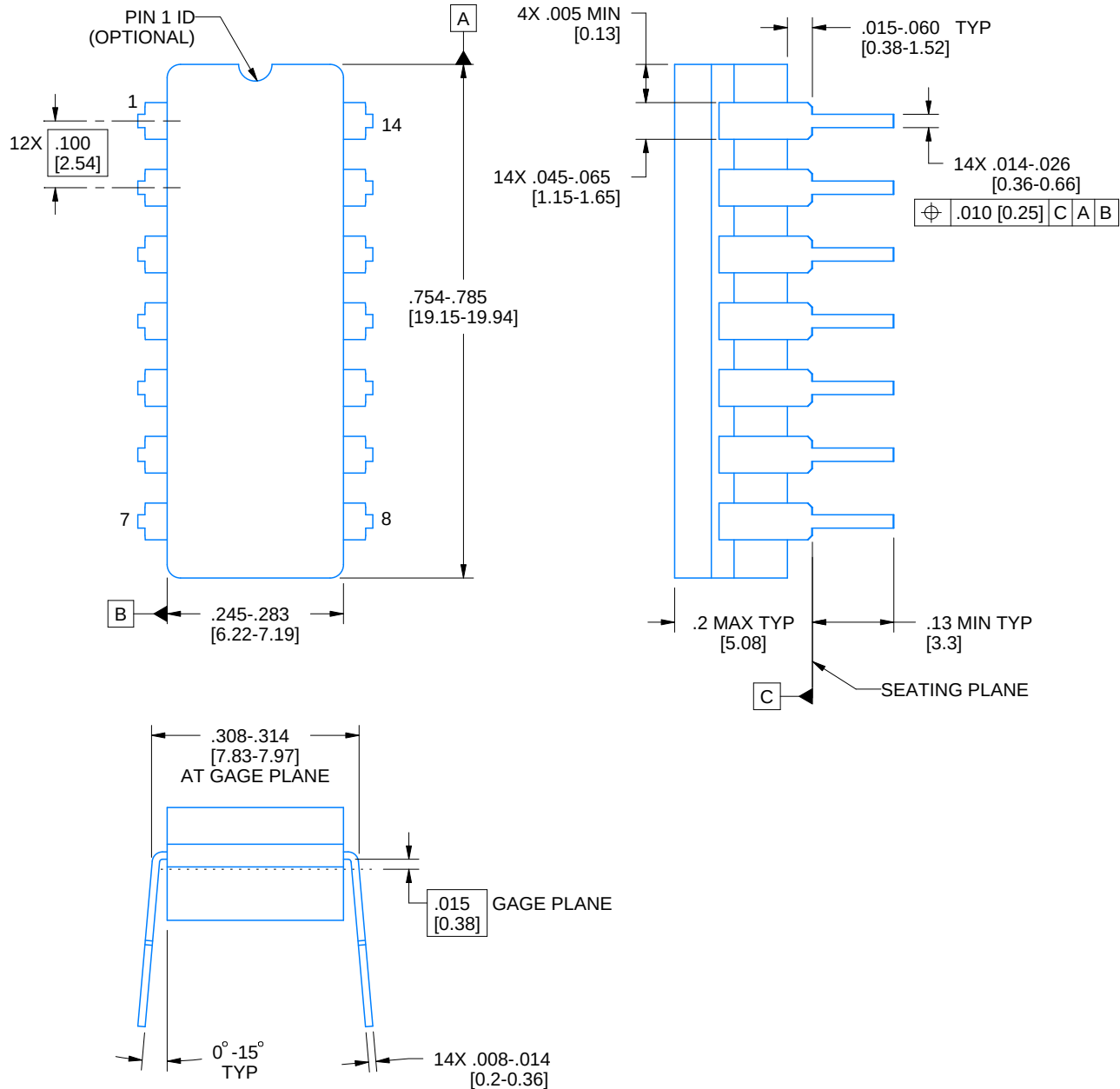


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A**PACKAGE OUTLINE****CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.



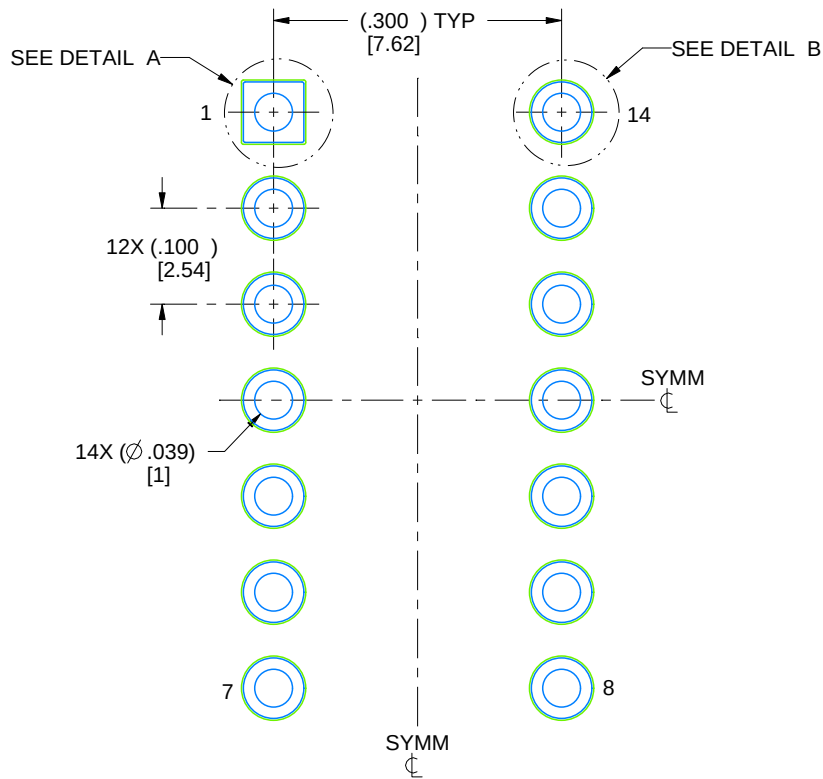
**TEXAS
INSTRUMENTS**
www.ti.com

EXAMPLE BOARD LAYOUT

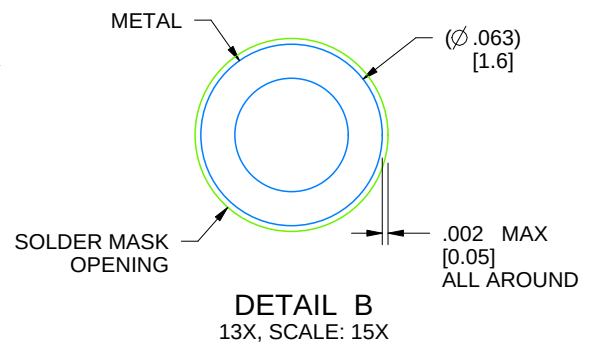
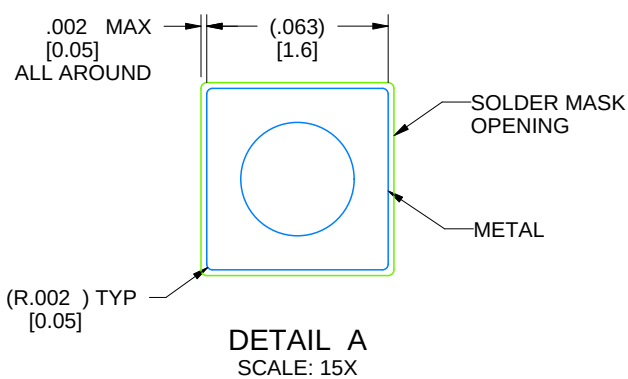
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X

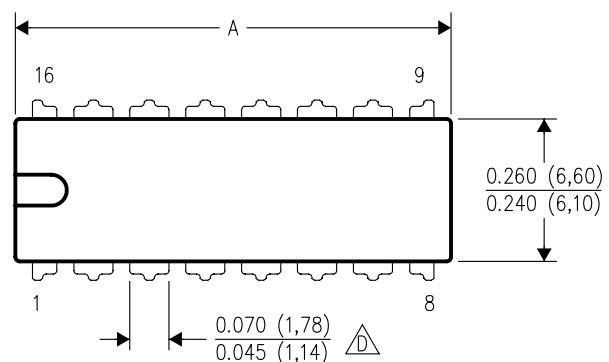


4214771/A 05/2017

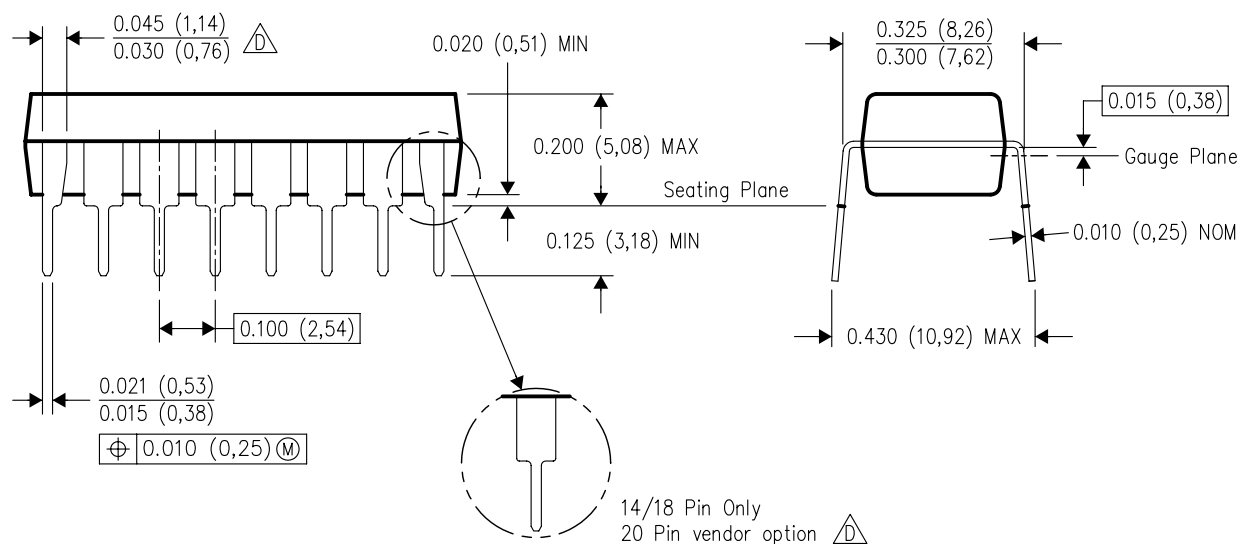
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

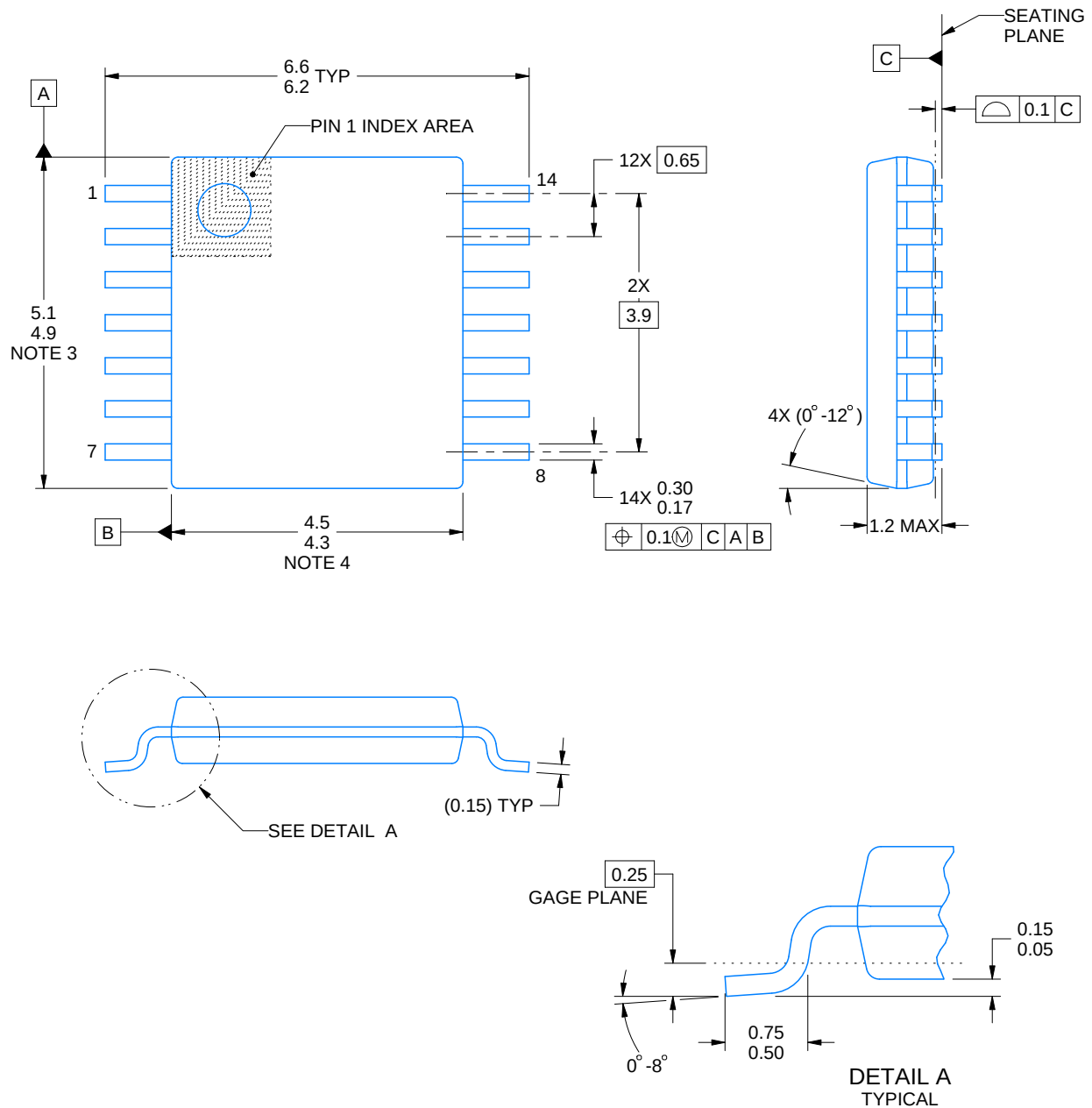
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

PW0014A

PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

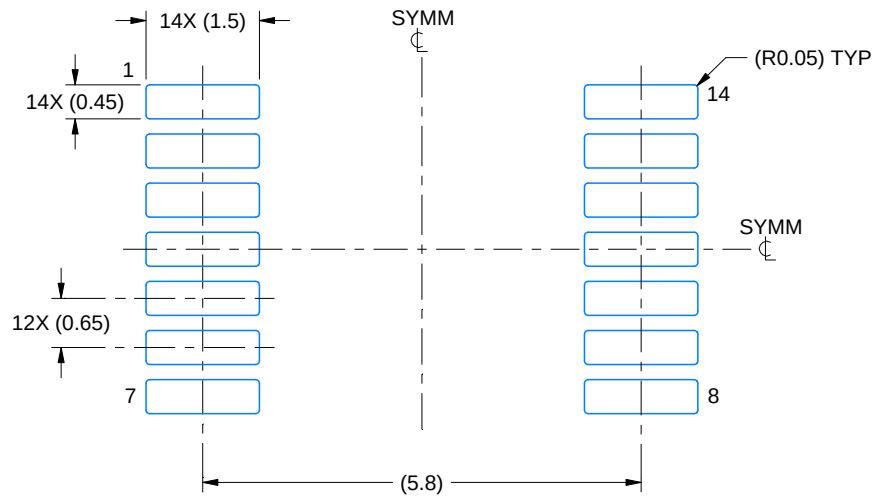
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

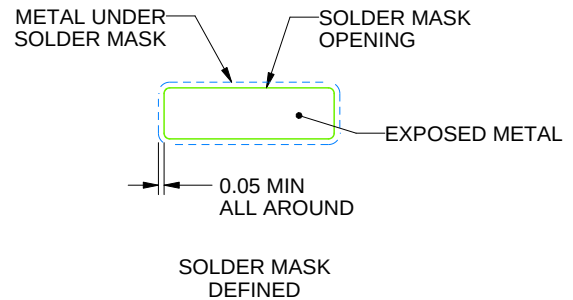
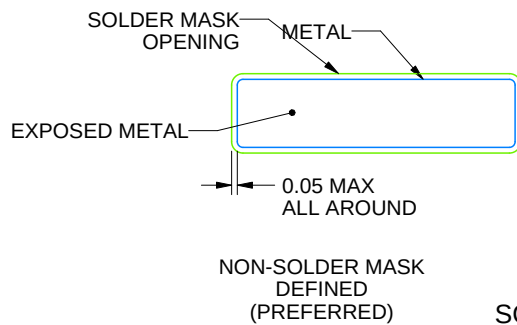
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

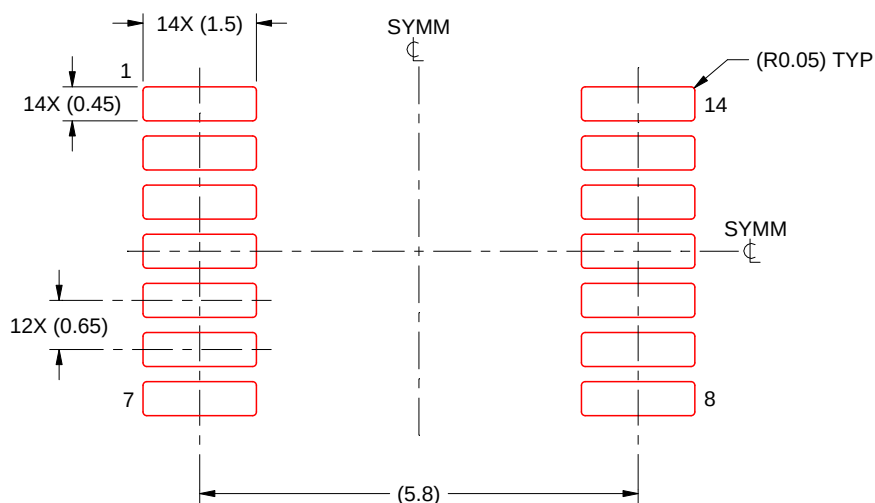
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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