INA117 高共模电压差分放大器

1 特性

- 共模输入范围：±200V (V_S = ±15V)
- 受保护的输入：
  - ±500V 共模电压
  - ±500V 差分电压
- 单位增益：0.05% 增益误差（最大值）
- 非线性度：0.001%（最大值）
- CMRR：70dB（最小值）

2 应用

- 单轴及多轴伺服驱动器
- 工业机械和机床
- 半导体测试和 ATE
- 超声波扫描仪

3 说明

INA117 是一款精密单位增益差分放大器，具有非常高的共模输入电压范围。INA117 是一款单片 IC，包括一个精密运算放大器和一个集成式薄膜电阻器网络。该器件可在出现高达 ±200V 共模信号时精确测量小差分电压。INA117 输入可防止瞬时共模或高达 ±500V 差分过载的影响。

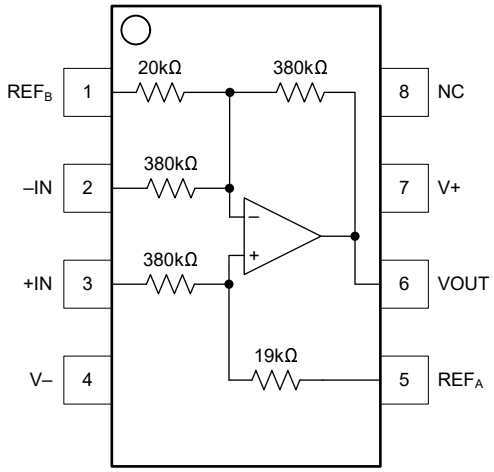
在很多无需电隔离的应用中，INA117 可以取代隔离放大器。这一设计可以免除对于成本高昂的隔离式输入侧电源的需要并去除相关的纹波、噪声、和静态电流。INA117 出色的 0.001% 非线性和 200kHz 带宽优于传统隔离放大器的相应特性。

INA117 采用 8 引脚塑料迷你 DIP 和 SO-8 表面贴装式封装，其额定温度范围为 –40°C 至 85°C。

封装信息

器件型号	封装(1)	封装尺寸(2)
INA117P	P（DIP，8）	6.35mm x 9.81mm
INA117KU	D（SOIC，8）	3.91mm x 4.9mm
INA117KU/2K5		

(1) 有关更多信息，请参阅节 10。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



INA117 D 封装（顶视图）

Table of Contents

4 Pin Configuration and Functions

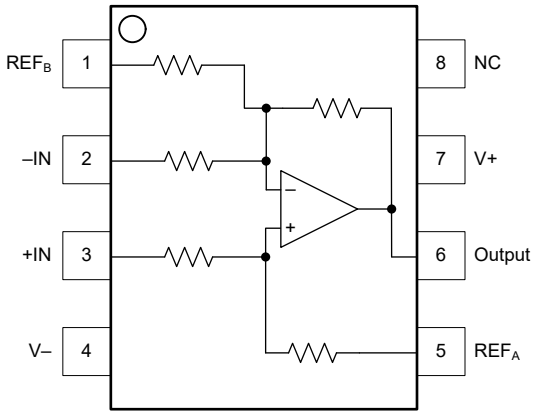


图 4-1. DIP/SO
INA117P, KU
Top View

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
-In	2	I	Inverting input.
+In	3	I	Non-inverting input.
NC	8	_	No internal connection. Can be grounded or disconnected.
Output	6	O	Output of the amplifier.
Ref_A	5	I	Reference A.
Ref_B	1	I	Reference B.
V-	4	P	Negative power supply.
V+	7	P	Positive power supply.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S		Dual supply, V_S = (V+) – (V–)		±22	V
	Signal input pins	Continuous		±200	V
		Peak (0.1s)		±500	V
	Output short-circuit(2)		Continuous		
T_A	Operating temperature		–40	85	°C
T_{stg}	Storage temperature		–55	125	°C
	Junction temperature			150	°C
	Lead temperature (soldering, 10s)			300	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to V_S / 2.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V_S	Supply voltage	Single-supply	10	30	36	V
		Dual-supply	±5	±15	±18	
T_A	Specified temperature		–40		85	°C

5.4 Thermal Information

THERMAL METRIC(1)		INA117 D (SOIC) 8 PINS	INA117 P (PDIP) 8 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	150	80	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

at T_A = 25°C, V_S = ±15V, R_L = 10kΩ, V_{REF} = 0V, V_{CM} = V_S/2, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT							
V_{OS}	Offset voltage	RTO (P package)			120	1000	µV
		RTO (KU package)			600	2000	µV
	Offset voltage drift	RTO, T_A = –40℃ to 85℃			8.5		µV/°C
	Long term drift				200		µV/mo
PSRR	Power-supply rejection ratio	RTO, V_S = ±5V to ±18V		74	90		dB
	Common-mode voltage (1)			–200		200	V
	Differential voltage			–10		10	V
CMRR	Common-mode voltage rejection	DC, V_{CM} = –200V to 200V		70	80		dB
			T_A = –40℃ to 85℃		75		
		AC, 60Hz, V_{CM} = –200V to 200V		66	80		
	Differential input impedance				800		kΩ
	Common-mode input impedance				200		
NOISE							
e_N	Voltage noise	RTO, f_B = 0.1Hz to 10Hz			25		μV_{PP}
		RTO, f = 1kHz			550		nV/ $\sqrt{Hz}$
GAIN							
GE	Gain error				±0.01	±0.05	%
	Gain error drift	T_A = –40°C to 85°C			±2		ppm/°C
	Gain nonlinearity(2)				±0.0005	±0.001	% of FSR
OUTPUT							
	Output voltage	I_O = 20mA, –5mA		10	12		V
	Output impedance				0.01		Ω
C_L	Load capacitance	Stable operation			1		nF
	Short-circuit current	Continuous to V_S/2			49, –13		mA
FREQUENCY RESPONSE							
BW	Bandwidth, –3dB				200		kHz
	Full power bandwidth	V_O = 20V_{pp}		30			kHz
SR	Slew rate			1.7	2.6		V/µs
t_S	Settling time	To 0.1%,	V_O = 10V step		6.5		µs
		To 0.01%	V_O = 10V step		10		
			V_{CM} = 10V step, V_{DIFF} = 0V		4.5		
POWER SUPPLY							
I_Q	Quiescent current	V_{IN} = 0V			1.5	±2	mA

(1) Input common-mode voltage varies with output voltage; see *Typical Characteristics*.
(2) Specified by wafer test.

6 Typical Characteristics

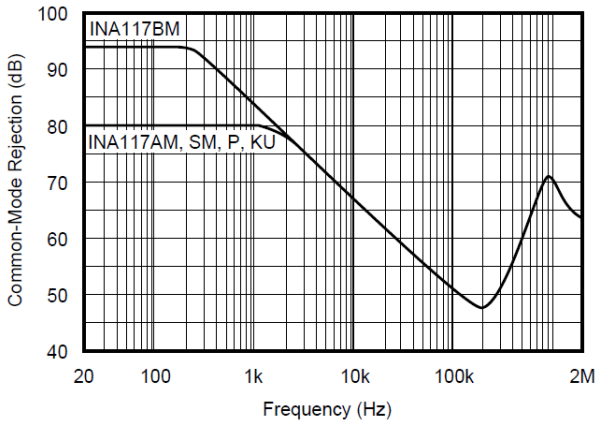


图 6-1. Common-mode Rejection vs Frequency

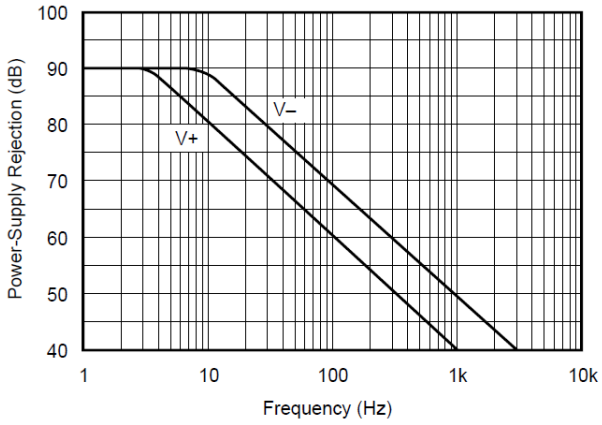


图 6-2. Power-supply Rejection vs Frequency

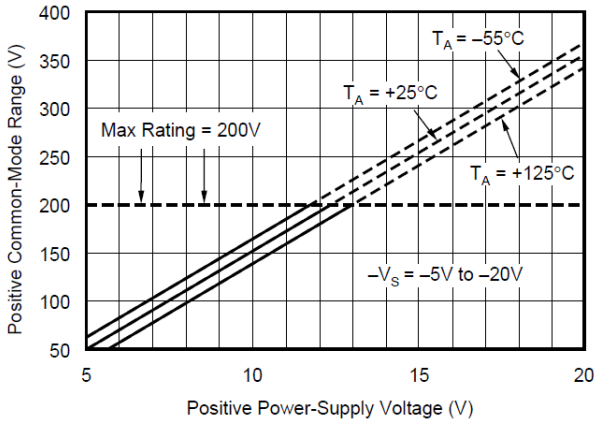


图 6-3. Positive Common-mode Voltage Range vs Positive Power-supply Voltage

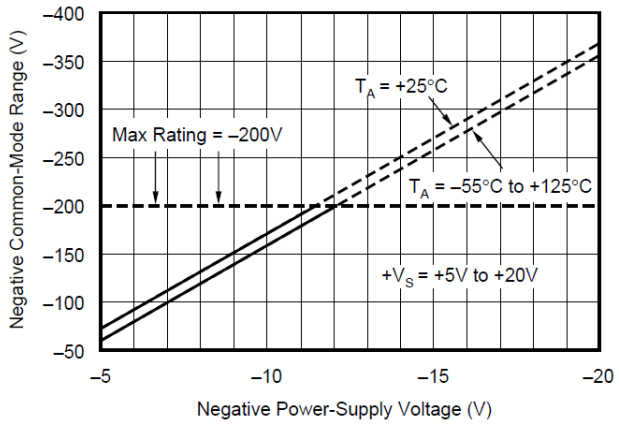


图 6-4. Negative Common-mode Voltage Range vs Negative Power-supply Voltage

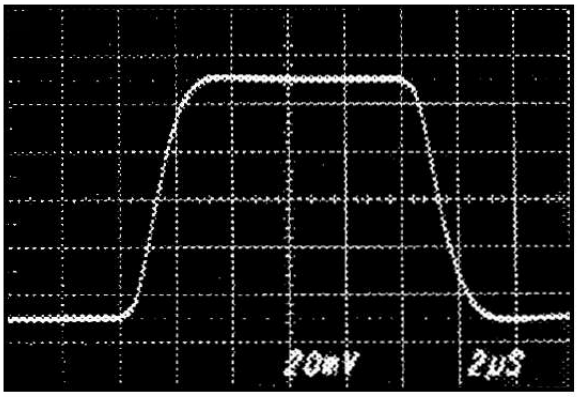


图 6-5. Small Signal Step Response C_L = 0pF

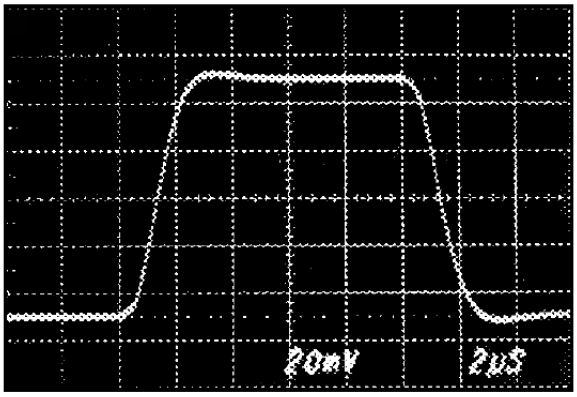


图 6-6. Small Signal Step Response C_L = 1000pF

6 Typical Characteristics (continued)

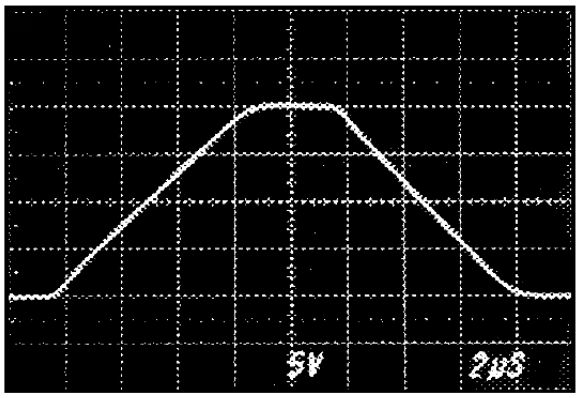


图 6-7. Large Signal Step Response

7 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

图 7-1 shows the basic connections required for operation.

Applications with noisy or high-impedance power-supply lines can require decoupling capacitors close to the device pins.

The output voltage is equal to the differential input voltage between pins 2 and 3. The common mode input voltage is rejected.

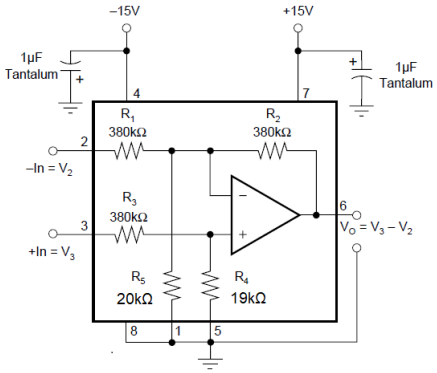


图 7-1. Basic Power and Signal Connections

7.1.1 Common-mode Rejection

Common-mode rejection (CMR) of the INA117 is dependent on the input resistor network, which is laser-trimmed for accurate ratio matching. To maintain high CMR, having low source impedances is important for driving the two inputs. A 75Ω resistance in series with pin 2 or 3 decreases CMR from 86dB to 72dB.

Resistance in series with the reference pins also degrades CMR. A 4Ω resistance in series with pin 1 or 5 decreases CMRR from 86dB to 72dB.

Most applications do not require trimming. 图 7-2 and 图 7-3 show optional circuits that can be used for trimming offset voltage and common-mode rejection.

7.1.2 Transfer Function

Most applications use the INA117 as a simple unity-gain difference amplifier. The transfer function is:

$V_0 = V_3 - V_2$

V_3 and V_2 are the voltages at pins 3 and 2.

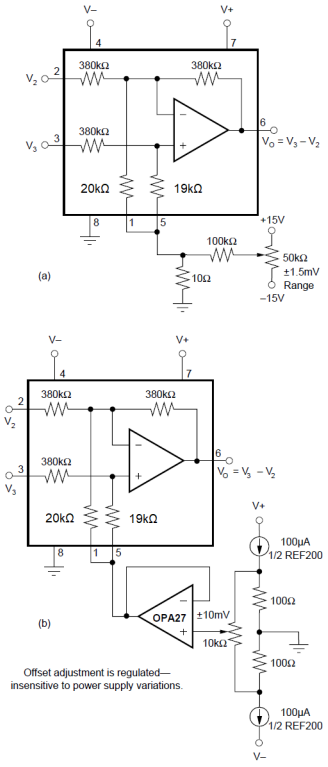


图 7-2. Offset Voltage Trim Circuits

Some applications, however, apply voltages to the reference terminals (pins 1 and 5). A more complete transfer function is:

$V_0 = V_3 - V_2 + 19 \times V_5 - 18 \times V_1$

V_5 and V_1 are the voltages at pins 5 and 1.

7.1.3 Measuring Current

The INA117 can be used to measure a current by sensing the voltage drop across a series resistor, R_S. 图 7-4 shows the INA117 used to measure the supply currents of a device under test. The circuit in 图 7-5 measures the output current of a power supply. If the power supply has a sense connection, the power supply can be connected to the output side of R_S to eliminate the voltage-drop error. Another common application is current-to-voltage conversion, as shown in 图 7-6.

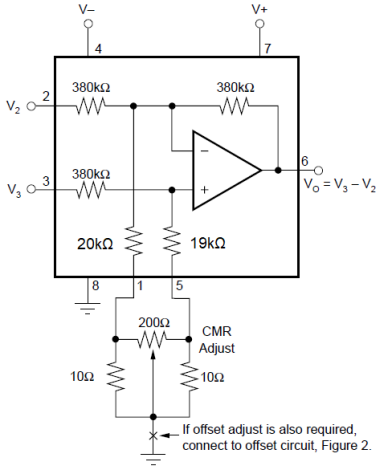


图 7-3. CMR Trim Circuit

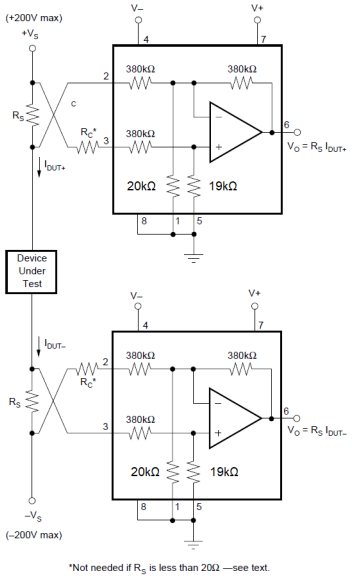


图 7-4. Measuring Supply Currents of Device Under Test

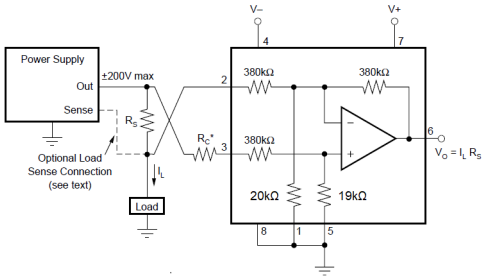


图 7-5. Measuring Power Supply Output Current

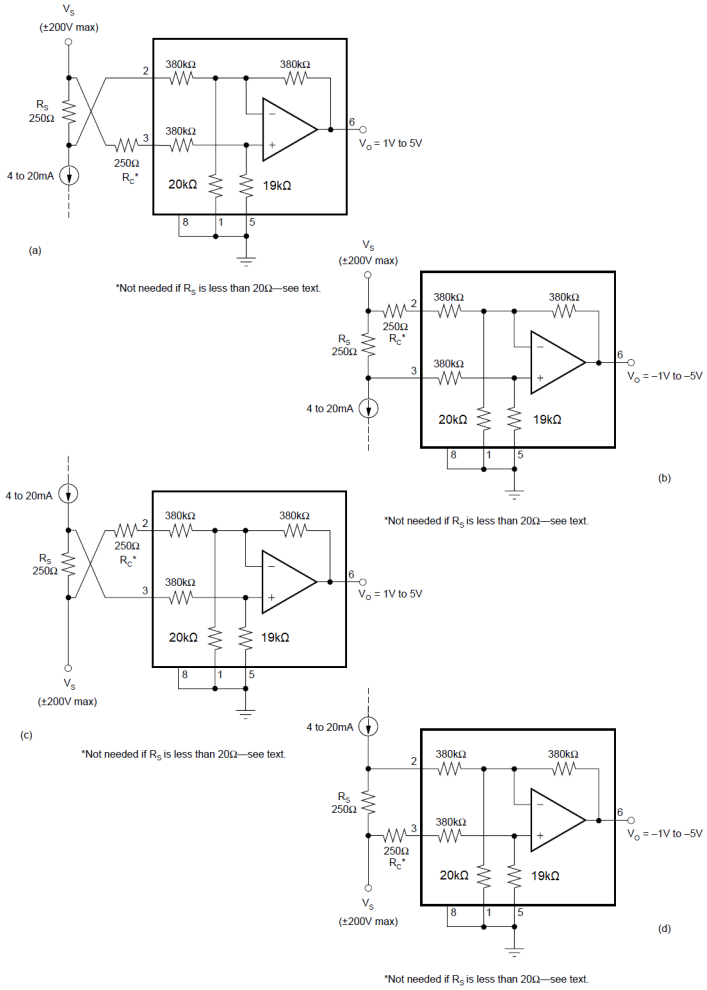


图 7-6. Current to Voltage Converter

In all cases, the sense resistor imbalances the input resistor matching of the INA117, degrading the CMR. Also, the input impedance of the INA117 loads R_S, causing gain error in the voltage-to-current conversion. Both of these errors can be easily corrected.

The CMR error can be corrected with the addition of a compensation resistor, R_C, equal in value to R_S as shown in 图 7-4, 图 7-5, and 图 7-6. If R_S is less than 20 Ω, the degradation in CMR is negligible and R_C can be omitted. If R_S is larger than approximately 2k Ω, trimming R_C can be required to achieve greater than 86dB CMR. This trim is because the actual INA117 input impedances have 1% typical mismatch. If R_S is more than approximately 100 Ω, the gain error is greater than the 0.05% specification of the INA117. This gain error can be corrected by slightly increasing the value of R_S. The corrected value, R_S', can be calculated by:

$$R_S' = \frac{R_S \times 380k\Omega}{380k\Omega - R_S} \quad (1)$$

Example: For a 1V/mA transfer function, the nominal, uncorrected value for R_S is 1k Ω. A slightly larger value, R_S' = 1002.6 Ω, compensates for the gain error due to loading.

The 380k Ω term in the equation for R_S' has a tolerance of ±25%, so sense resistors above approximately 400 Ω can require trimming to achieve gain accuracy better than 0.05%.

Of course, if a buffer amplifier is added as shown in 图 7-7, both inputs see a low source impedance, and the sense resistor is not loaded. As a result, there is no gain error or CMR degradation. The buffer amplifier can operate as a unity gain buffer or as an amplifier with non-inverting gain. Gain added ahead of the INA117 improves both CMR and signal-to-noise. Added gain also allows a lower voltage drop across the sense resistor. The OPA1013 is a good choice for the buffer amplifier since both the input and output can swing close to the negative power supply.

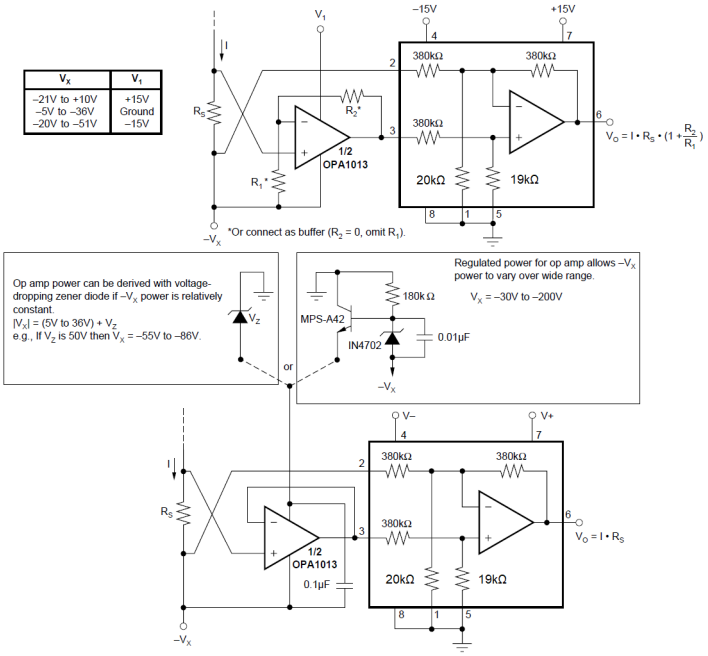


图 7-7. Current Sensing With Input Buffer

图 7-8 shows very high input impedance buffer used to measure low leakage currents. Here, the buffer operational amplifier is powered with an isolated, split-voltage power supply. Using an isolated power supply allows full ±200V common-mode input range.

7.1.4 Noise Performance

The noise performance of the INA117 is dominated by the internal resistor network. The thermal or Johnson noise of these resistors produces approximately 550nV/ √ Hz noise. The internal op amp contributes virtually no excess noise at frequencies above 100Hz.

Many applications can be satisfied with less than the full 200kHz bandwidth of the INA117. In these cases, the noise can be reduced with a low-pass filter on the output. The two- pole filter shown in 图 7-9 limits bandwidth to 1kHz and reduces noise by more than 15:1. Since the INA117 has a 1/f noise corner frequency of approximately 100Hz, a cutoff frequency below 100Hz does not further reduce noise.

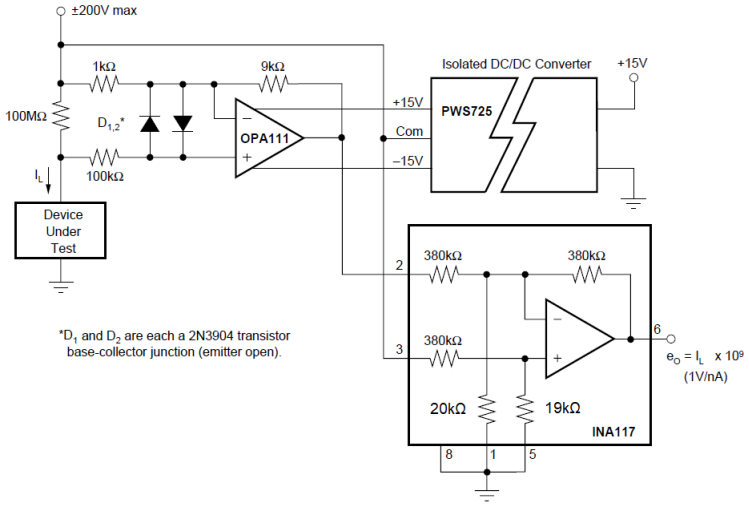
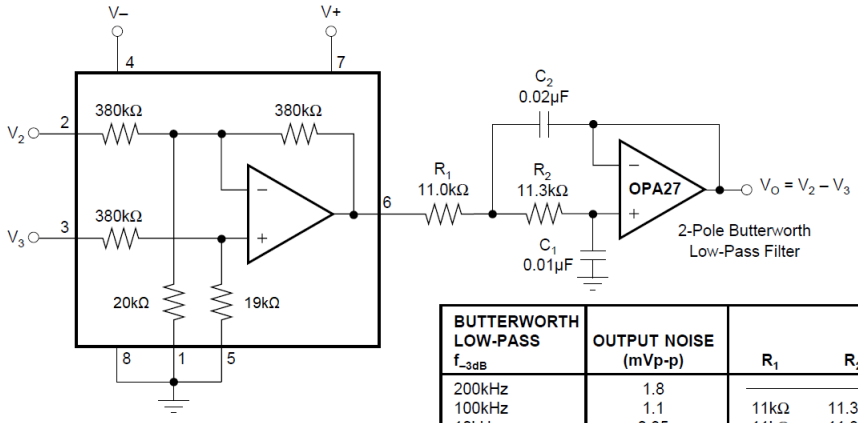


图 7-8. Leakage Current Measurement Circuit



See Application Bulletin AB-017 for other filters.

BUTTERWORTH LOW-PASS f_{-3dB}	OUTPUT NOISE (mVp-p)	R_1	R_2	C_1	C_2
200kHz	1.8	No Filter			
100kHz	1.1	11kΩ	11.3kΩ	100pF	200pF
10kHz	0.35	11kΩ	11.3kΩ	1nF	2nF
1kHz	0.11	11kΩ	11.3kΩ	10nF	20nF
≤100Hz(1)	0.05	11kΩ	11.3kΩ	0.1µF	0.2µF

NOTE: (1) Since the INA117 has a 1/f noise corner frequency of approximately 100Hz, bandwidth reduction below this frequency will not significantly reduce noise.

图 7-9. Output Filter for Noise Reduction

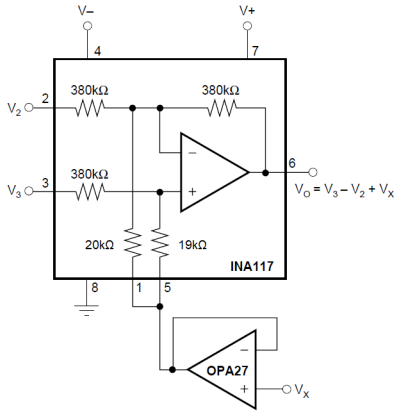


图 7-10. Summing V_X in Output

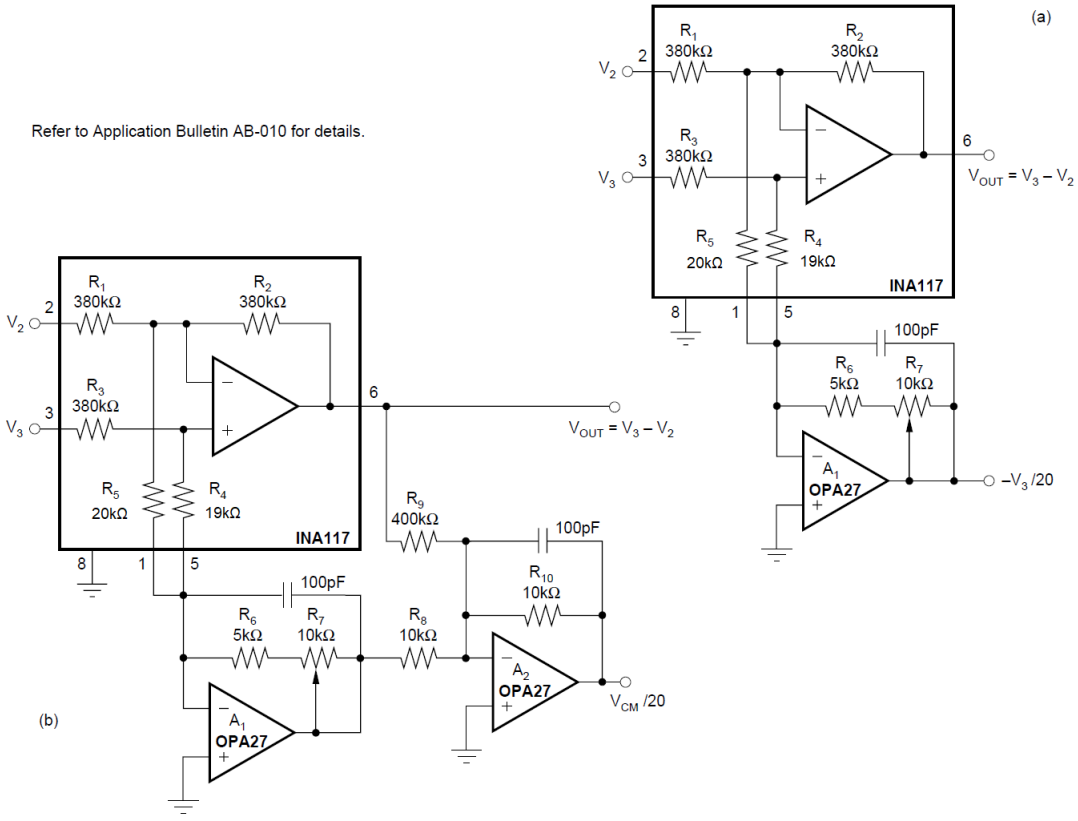


图 7-11. Common-mode Voltage Monitoring

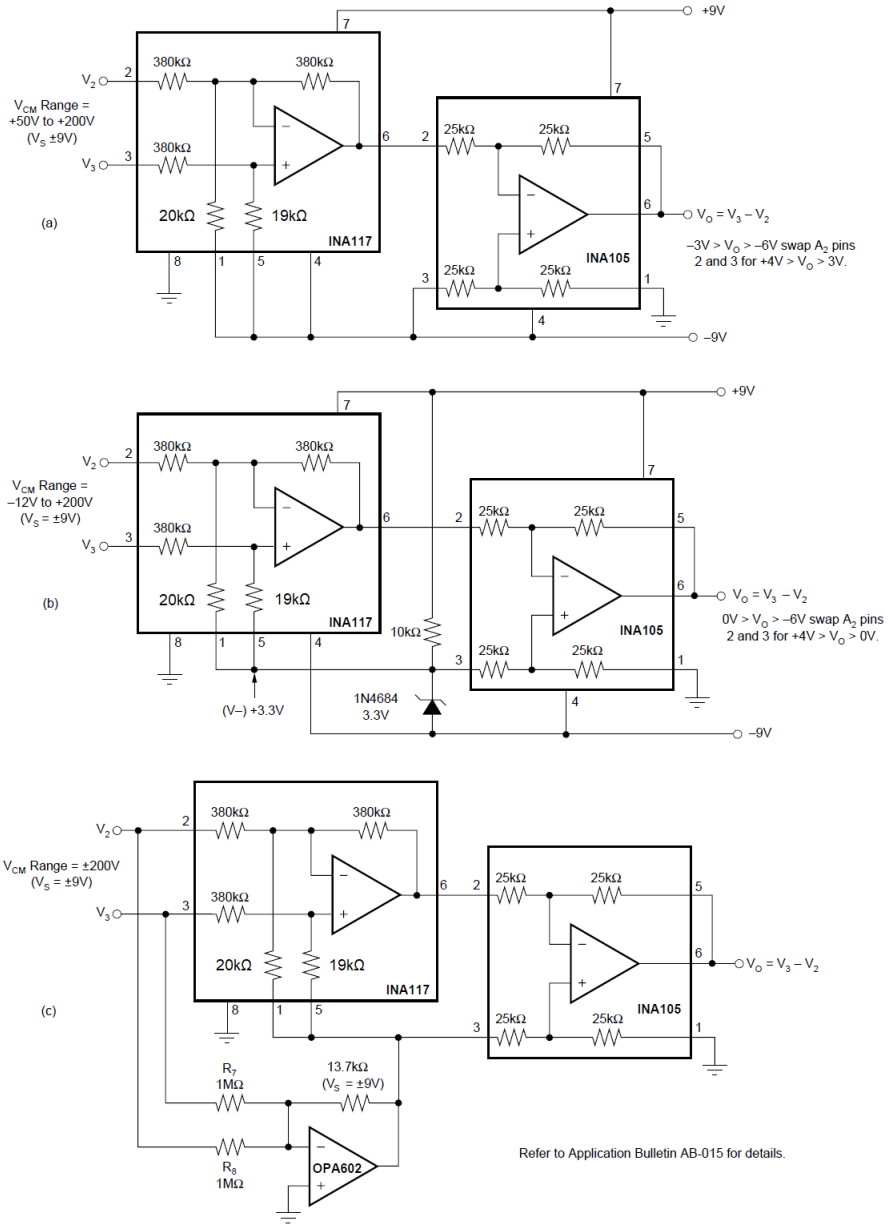


图 7-12. Offsetting or Boosting Common-mode Voltage Range for Reduced Power-supply Voltage Operation

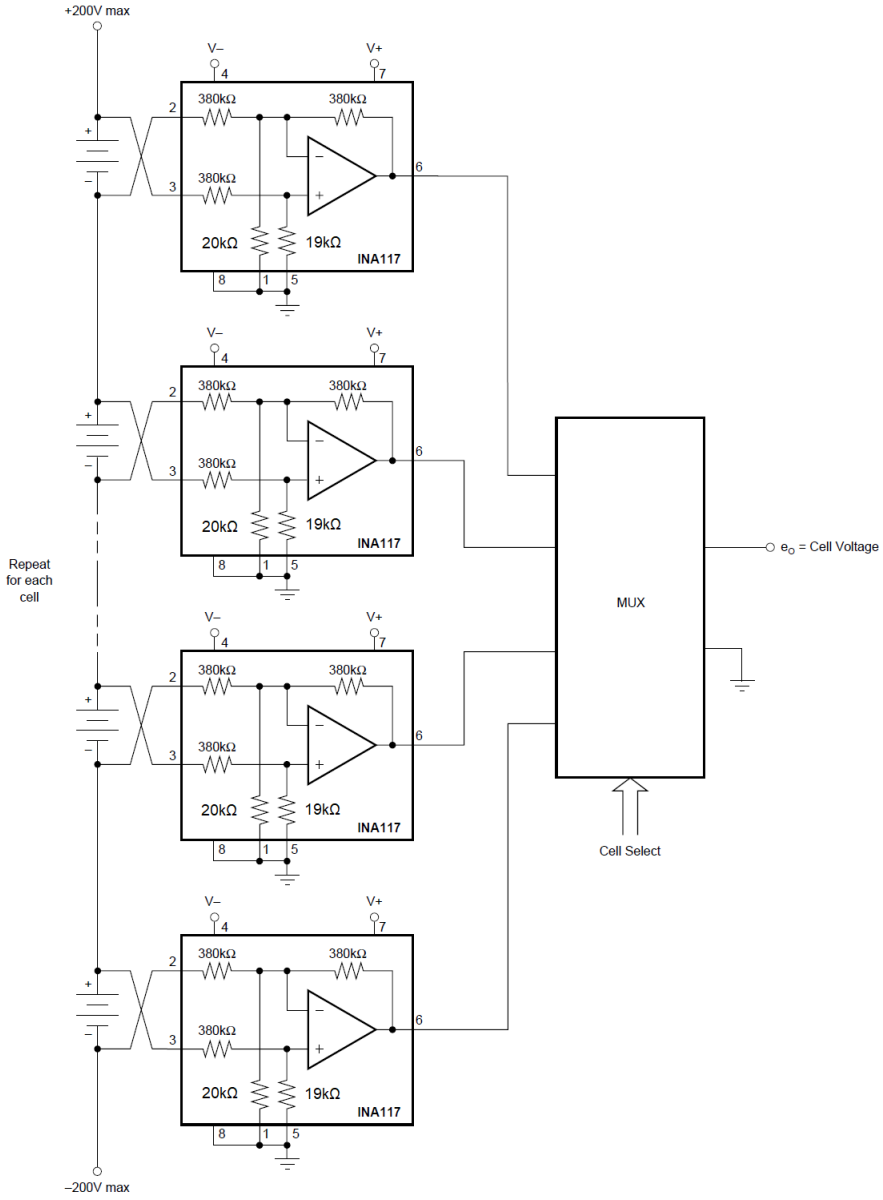


图 7-13. Battery Cell Voltage Monitor

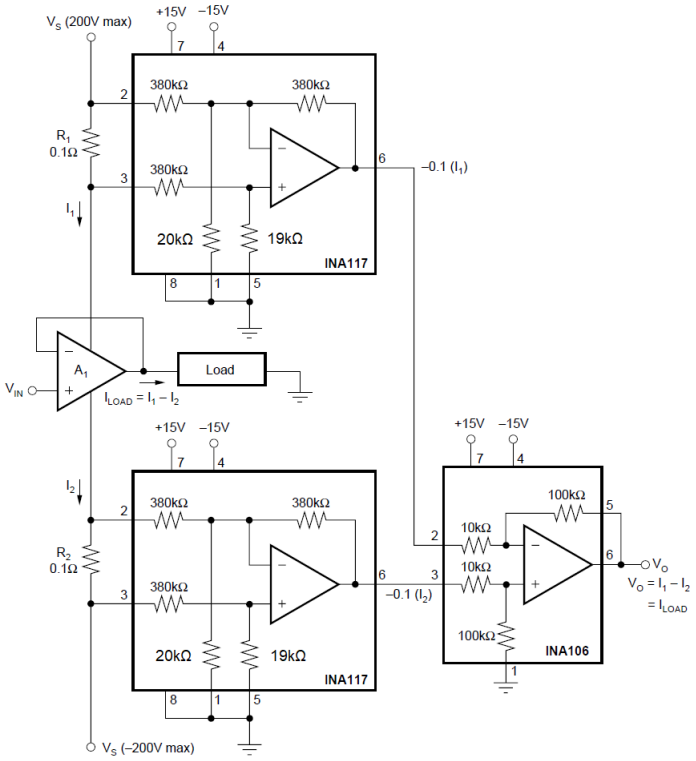


图 7-14. Measuring Amplifier Load Current

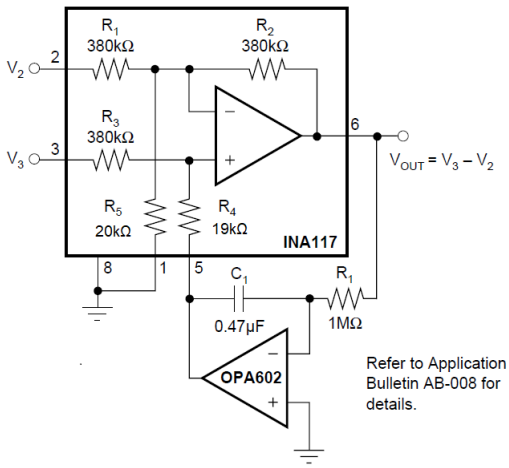


图 7-15. AC-coupled INA117

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support

8.1.1 Related Documentation

- Texas Instruments, *Precision labs series: Instrumentation amplifier*, videos
- Texas Instruments, *INA149 High common mode voltage difference amplifier*, data sheet
- Texas Instruments, *Supporting High Voltage Common Mode Using Difference Amplifier*, application brief

8.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

8.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (November 2000) to Revision B (April 2024)	Page
• 更新了整个文档中的表格、图和交叉参考的格式	1
• 通篇删除了有关 INA117AM 和 INA117SM 型号的信息	1
• 在 *说明* 及 *引脚配置和功能* 部分中将引脚 8 从“Comp”更改为“NC”	1
• 向 *说明* 部分添加了 *封装信息* 表	1
• Added *Pin Functions* table	2
• Added ESD Ratings table	3
• Added single supply specification to *Recommended Operating Conditions*	3
• Added specified temperature range to *Recommended Operating Conditions*	3
• Added VREF = 0V, VCM = VS/2, and G = 1 to "unless otherwise noted" conditions in *Electrical Characteristics* and *Typical Characteristics* for clarity	4
• Changed parameter from "Offset voltage vs Temperature" to "Offset voltage drift" in *Electrical Characteristics*	4
• Added test condition of "TA = –40°C to +85°C" for "Offset voltage drift" in *Electrical Characteristics*	4
• Changed parameter from "Offset Voltage vs Power Supply" to "Power-supply rejection ratio" in *Electrical Characteristics*	4
• Added test condition of "TA = –40°C to +85°C" for "CMRR" in *Electrical Characteristics*	4
• Changed "Common-mode input impedance" typical value from 400kΩ to 200kΩ in *Electrical Characteristics*	4
• Added test condition "TA = –40°C to +85°C" for "Gain error vs temperature" in *Electrical Characteristics* and renamed to "Gain error drift" for clarity	4
• Changed "Gain nonlinearity" typical value from 0.0002% to 0.0005% in *Electrical Characteristics*	4
• Added test condition "Continuous to V_S/2" to Short-circuit current specification in *Electrical Characteristics* for clarity	4
• Change minimum Slew rate from 2V/µs to 1.7V/µs in *Electrical Characteristics*	4
• Deleted redundant voltage range, operating temperature range, and specification temperature range specifications from *Electrical Characteristics*	4
• Deleted *Reducing Differential Gain* application circuit figure	11
• Added *Documentation Support* and *Related Documentation* sections	17

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA117AM	NRND	Production	TO-99 (LMC) | 8	20 | TUBE	Yes	Call TI	N/A for Pkg Type	-	INA117AM
INA117BM	Active	Production	TO-99 (LMC) | 8	20 | TUBE	Yes	Call TI	N/A for Pkg Type	-	INA117BM
INA117KU	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU | NIPDAU	Level-3-260C-168 HR	-40 to 85	INA 117KU
INA117KU/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-3-260C-168 HR	-	INA 117KU
INA117P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	Call TI | Nipdau	N/A for Pkg Type	-	INA117P
INA117SM	NRND	Production	TO-99 (LMC) | 8	20 | TUBE	Yes	AU	N/A for Pkg Type	-	INA117SM
INA117SMQ	NRND	Production	TO-99 (LMC) | 8	20 | TUBE	Yes	AU	N/A for Pkg Type	-	INA117SMQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

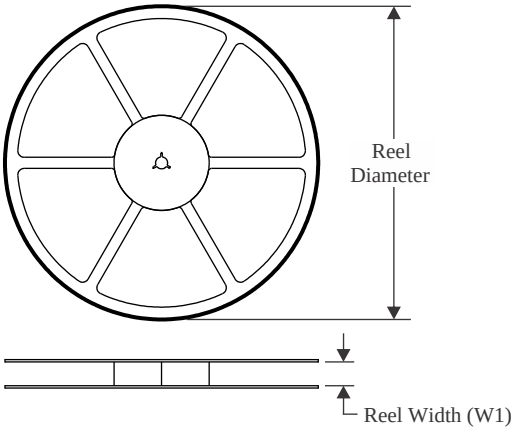
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

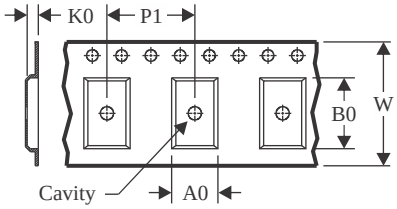
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

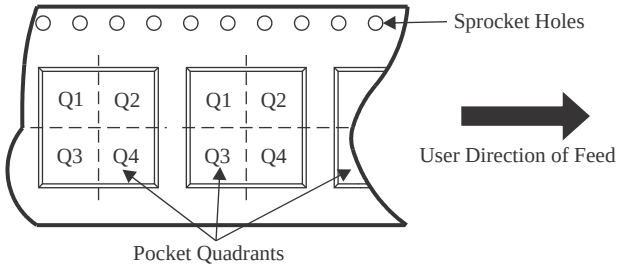


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

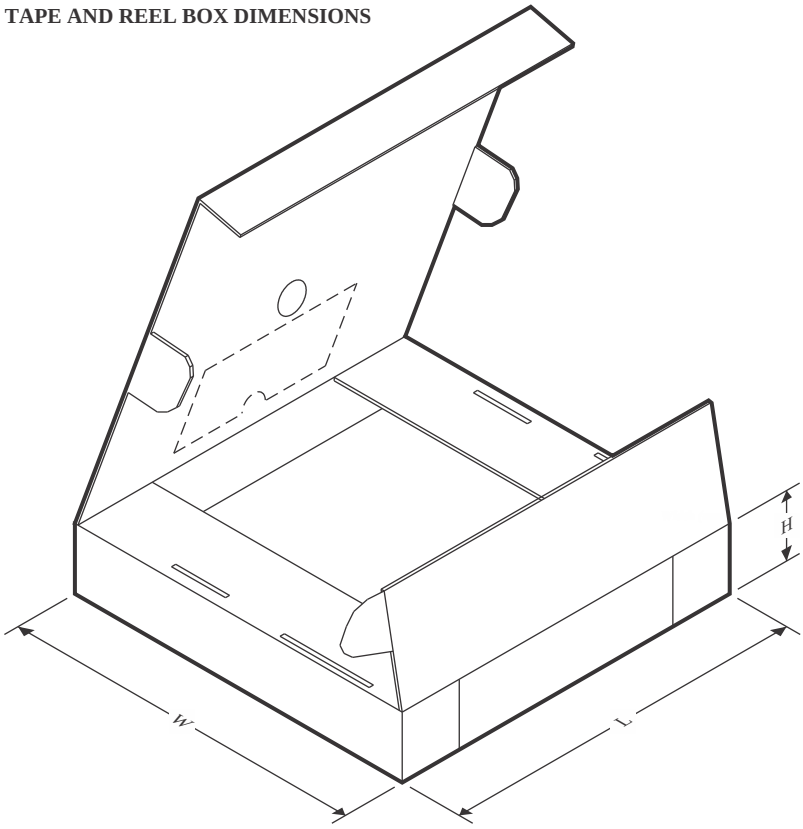
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA117KU/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA117KU/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

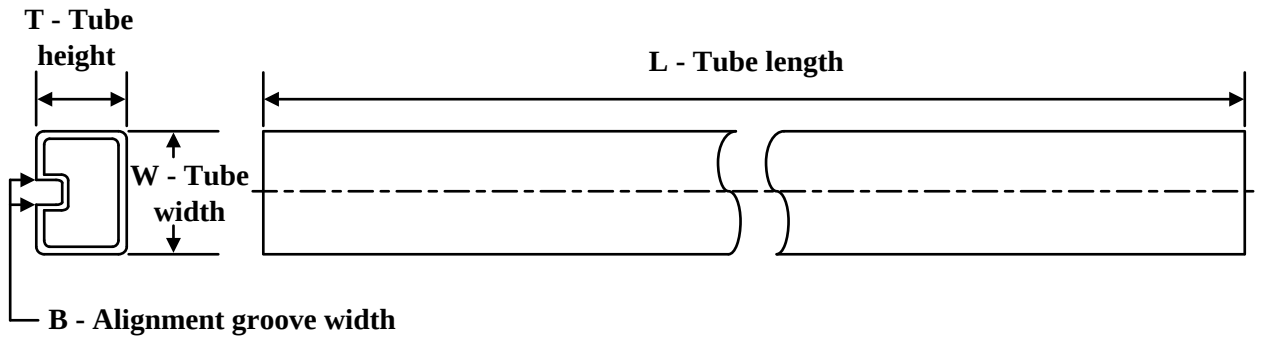
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA117KU/2K5	SOIC	D	8	2500	353.0	353.0	32.0
INA117KU/2K5	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA117AM	LMC	TO-CAN	8	20	532.13	21.59	889	NA
INA117BM	LMC	TO-CAN	8	20	532.13	21.59	889	NA
INA117KU	D	SOIC	8	75	506.6	8	3940	4.32
INA117P	P	PDIP	8	50	506	13.97	11230	4.32
INA117SM	LMC	TO-CAN	8	20	532.13	21.59	889	NA
INA117SMQ	LMC	TO-CAN	8	20	532.13	21.59	889	NA

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