

LP5907-Q1 汽车 250mA 超低噪声、低 I_Q LDO

1 特性

- 符合汽车应用 要求
- 具有符合 AEC-Q100 标准的下列结果：
 - 器件温度 1 级：-40°C 至 125°C 的环境工作温度范围
 - 器件 HBM ESD 分类等级 2
 - 器件 CDM ESD 分类等级 C6
- 输入电压范围：2.2V 至 5.5V
- 输出电压范围：1.2V 至 4.5V
- 与 1 μ F 陶瓷输入和输出电容搭配使用，性能稳定
- 无需噪声旁路电容
- 支持输出电容远端布置
- 热过载保护和短路保护
- 输出电流：250mA
- 输出电压噪声低：小于 6.5 μ V_{RMS}
- 电源抑制比 (PSRR)：1kHz 频率时为 82dB
- 输出电压容差： $\pm 2\%$
- 几乎没有 I_Q (已禁用)：< 1 μ A
- 极低 I_Q (使能时)：12 μ A
- 启动时间：80 μ s
- 低压降：120mV (典型值)
- 运行结温范围：-40°C 到 125°C

2 应用

- ADAS 摄像机和雷达
- 汽车信息娱乐系统
- 车载通讯系统
- 导航系统

3 说明

LP5907-Q1 是一款能提供 250mA 输出电流的低噪声 LDO。LP5907-Q1 符合射频和模拟电路要求，可提供低噪声、高 PSRR、低静态电流以及低线路或负载瞬态响应系数。LP5907-Q1 采用创新的设计技术，无需噪声旁路电容便可提供出色的噪声性能，并且支持远距离安置输出电容。

此器件可与 1 μ F 输入和 1 μ F 输出陶瓷电容搭配使用（无需独立的噪声旁路电容）。

其固定输出电压介于 1.2V 至 4.5V 之间（阶跃为 25mV）。如需特定的电压选项，请联系德州仪器 (TI) 销售代表。

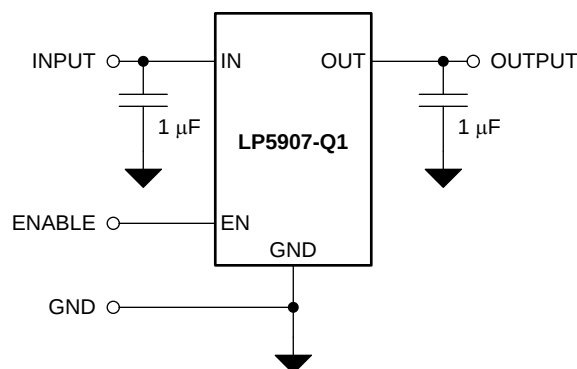
器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
LP5907-Q1	SOT-23 (5)	2.90mm × 1.60mm
	X2SON (4) ⁽²⁾	1.00mm × 1.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

(2) 预览器件。

简化原理图



目录

1	特性	1	7.3	Feature Description	12
2	应用	1	7.4	Device Functional Modes	13
3	说明	1	8	Application and Implementation	14
4	修订历史记录	2	8.1	Application Information	14
5	Pin Configuration and Functions	3	8.2	Typical Application	14
6	Specifications	4	9	Power Supply Recommendations	17
6.1	Absolute Maximum Ratings	4	10	Layout	18
6.2	ESD Ratings	4	10.1	Layout Guidelines	18
6.3	Recommended Operating Conditions	4	10.2	Layout Examples	18
6.4	Thermal Information	4	11	器件和文档支持	19
6.5	Electrical Characteristics	5	11.1	接收文档更新通知	19
6.6	Output and Input Capacitors	6	11.2	社区资源	19
6.7	Typical Characteristics	7	11.3	商标	19
7	Detailed Description	11	11.4	静电放电警告	19
7.1	Overview	11	11.5	术语表	19
7.2	Functional Block Diagram	11	12	机械、封装和可订购信息	19

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

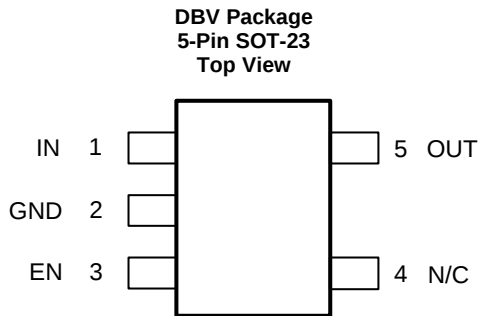
Changes from Revision C (May 2018) to Revision D	Page
• 已添加 向文档添加了 DQN (X2SON) 封装（预览版）	1
• Added <i>Layout Example for the DQN Package</i> figure	18

Changes from Revision B (September 2016) to Revision C	Page
• 已添加 向特性 部分中添加了 ESD 分类级别子项目	1
• Changed DBV values in <i>Thermal Information</i> table	4
• Deleted footnote 1 from <i>Thermal Information</i> table	4
• Added <i>Overshoot on start-up with EN</i> row to <i>Electrical Characteristics</i> table	6
• Changed <i>Device Comparison</i> table: changed table title, added new rows and new data, moved to new sub-section	12

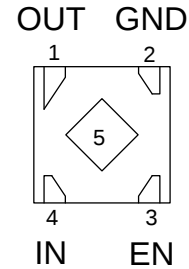
Changes from Revision A (June 2016) to Revision B	Page
• 已更改 标题措辞	1
• 已更改 将“低输出电压噪声：小于 10 μ V _{RMS} ”更改成了“低输出电压噪声：小于 6.5 μ V _{RMS} ”	1
• 已更改 更改了“应用”中所列的项目	1
• 已更改 更改了说明中第一个句子的措辞	1

Changes from Original (September 2014) to Revision A	Page
• 已添加 特性项目修改：汽车	1
• 已添加 TI 设计的顶部导航图标	1
• 已更改 “线性稳压器”更改为“LDO”	1
• Changed storage temperature from <i>Handling Ratings</i> to <i>Abs Max</i> table; replaced <i>Handling Ratings</i> with <i>ESD Ratings</i> per new format	4

5 Pin Configuration and Functions



DQN Package (Preview)
4-Pin X2SON
Bottom View



Pin Functions

NAME	PIN		I/O	DESCRIPTION
	SOT23-5	X2SON-4		
EN	3	3	I	Enable input. A low voltage ($< V_{IL}$) on this pin turns the regulator off and discharges the output pin to GND through an internal 230- Ω pulldown resistor. A high voltage ($> V_{IH}$) on this pin enables the regulator output. This pin has an internal 1-M Ω pulldown resistor to hold the regulator off by default.
GND	2	2	–	Common ground
IN	1	4	I	Input voltage supply. Connect a 1- μ F capacitor at this input.
N/C	4	–	–	No internal electrical connection.
OUT	5	1	O	Regulated output voltage. Connect a minimum 1- μ F low-ESR capacitor to this pin. Connect this output to the load circuit. An internal 230- Ω (typical) pulldown resistor prevents a charge remaining on V_{OUT} when the regulator is in the shutdown mode (V_{EN} low).

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

		MIN	MAX	UNIT
V _{IN}	Input voltage	−0.3	6	V
V _{OUT}	Output voltage	−0.3	See ⁽³⁾	V
V _{EN}	Enable input voltage	−0.3	6	V
	Continuous power dissipation ⁽⁴⁾	Internally limited		W
T _{JMAX}	Junction temperature		150	°C
T _{stg}	Storage temperature	−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to the GND pin.
- (3) Abs Max V_{OUT} is the V_{IN} + 0.3 V or 6 V, whichever is less.
- (4) Internal thermal shutdown circuitry protects the device from permanent damage.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	
		Other pin (2)	±1000	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

		MIN	MAX	UNIT
V _{IN}	Input supply voltage	2.2	5.5	V
V _{EN}	Enable input voltage	0	5.5	V
I _{OUT}	Output current	0	250	mA
T _{J-MAX-OP}	Operating junction temperature ⁽³⁾	−40	125	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to the GND pin.
- (3) $T_{J-MAX-OP} = [T_{A(MAX)} + (P_{D(MAX)} \times R_{\theta JA})]$.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LP5907-Q1		UNIT
		DBV (SOT-23)	DQN (X2SON-4)	
		5 PINS	4-PINS	
R _{θJA}	Junction-to-ambient thermal resistance	186.9	198.4	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	112.3	109.3	°C/W
R _{θJB}	Junction-to-board thermal resistance	52.3	128.3	°C/W
ψ _{JT}	Junction-to-top characterization parameter	27.5	2.6	°C/W
ψ _{JB}	Junction-to-board characterization parameter	51.8	128.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

 $V_{IN} = V_{OUT(NOM)} + 1\text{ V}$, $V_{EN} = 1.2\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_{OUT} = 1\text{ }\mu\text{F}$ (unless otherwise noted)⁽¹⁾⁽²⁾⁽³⁾

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
GENERAL							
V _{IN}	Input voltage	T _A = 25°C		2.2		5.5	V
ΔV _{OUT}	Output voltage tolerance	V _{IN} = (V _{OUT(NOM)} + 1 V) to 5.5 V, I _{OUT} = 1 mA to 250 mA, V _{OUT} ≥ 1.8 V		–2		2	%V _{OUT}
		V _{IN} = (V _{OUT(NOM)} + 1 V) to 5.5 V, I _{OUT} = 1 mA to 250 mA, V _{OUT} < 1.8 V		–3		3	
	Line regulation	V _{IN} = (V _{OUT(NOM)} + 1 V) to 5.5 V, I _{OUT} = 1 mA			0.02		%/V
	Load regulation	I _{OUT} = 1 mA to 250 mA			0.001		%/mA
I _{LOAD}	Output load current			0		250	mA
I _Q	Quiescent current ⁽⁴⁾	V _{EN} = 1.2 V, I _{OUT} = 0 mA			12	25	μA
		V _{EN} = 1.2 V, I _{OUT} = 250 mA			250	425	
		V _{EN} = 0.3 V (Disabled)			0.2	1	
I _G	Ground current ⁽⁵⁾	V _{EN} = 1.2 V, I _{OUT} = 0 mA			14		μA
V _{DO}	Dropout voltage ⁽⁶⁾	I _{OUT} = 100 mA			50		mV
		I _{OUT} = 250 mA				250	
I _{SC}	Short-circuit current limit	T _A = 25°C ⁽⁷⁾		250	500		mA
PSRR	Power-supply rejection ratio ⁽⁸⁾	f = 100 Hz, I _{OUT} = 20 mA			90		dB
		f = 1 kHz, I _{OUT} = 20 mA			82		
		f = 10 kHz, I _{OUT} = 20 mA			65		
		f = 100 kHz, I _{OUT} = 20 mA			60		
e _N	Output noise voltage ⁽⁸⁾	BW = 10 Hz to 100 kHz	I _{OUT} = 1 mA		10		μV _{RMS}
			I _{OUT} = 250 mA		6.5		
R _{AD}	Output automatic discharge pulldown resistance	V _{EN} < V _{IL} (output disabled)			230		Ω
T _{SD}	Thermal shutdown	T _J rising			160		°C
	Thermal hysteresis	T _J falling from shutdown			15		
LOGIC INPUT THRESHOLDS							
V _{IL}	Low input threshold	V _{IN} = 2.2 V to 5.5 V, V _{EN} falling until the output is disabled				0.4	V
V _{IH}	High input threshold	V _{IN} = 2.2 V to 5.5 V, V _{EN} rising until the output is enabled		1.2			V
I _{EN}	Input current at EN pin ⁽⁹⁾	V _{EN} = 5.5 V and V _{IN} = 5.5 V			5.5		μA
		V _{EN} = 0 V and V _{IN} = 5.5 V			0.001		

- (1) All voltages are with respect to the device GND terminal, unless otherwise stated.
- (2) Minimum and maximum limits are ensured through test, design, or statistical correlation over the junction temperature (T_J) range of -40°C to 125°C , unless otherwise stated. Typical values represent the most likely parametric norm at $T_A = 25^\circ\text{C}$, and are provided for reference purposes only.
- (3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP} = 125^\circ\text{C}$), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} - (R_{\theta JA} \times P_{D-MAX})$. See [Application and Implementation](#).
- (4) Quiescent current is defined here as the difference in current between the input voltage source and the load at V_{OUT} .
- (5) Ground current is defined here as the total current flowing to ground as a result of all input voltages applied to the device.
- (6) Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100 mV below its nominal value.
- (7) Short-circuit current (I_{SC}) for the LP5907-Q1 is equivalent to current limit. To minimize thermal effects during testing, I_{SC} is measured with V_{OUT} pulled to 100 mV below its nominal voltage.
- (8) This specification is verified by design.
- (9) There is a 1-M Ω resistor between EN and ground on the device.

Electrical Characteristics (continued)

 $V_{IN} = V_{OUT(NOM)} + 1\text{ V}$, $V_{EN} = 1.2\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_{OUT} = 1\text{ }\mu\text{F}$ (unless otherwise noted)⁽¹⁾⁽²⁾⁽³⁾

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TRANSIENT CHARACTERISTICS						
ΔV_{OUT}	Line transient ⁽⁸⁾	$V_{IN} = (V_{OUT(NOM)} + 1\text{ V})$ to $(V_{OUT(NOM)} + 1.6\text{ V})$ in $30\text{ }\mu\text{s}$	–1			mV
		$V_{IN} = (V_{OUT(NOM)} + 1.6\text{ V})$ to $(V_{OUT(NOM)} + 1.6\text{ V})$ in $30\text{ }\mu\text{s}$			1	
	Load transient ⁽⁸⁾	$I_{OUT} = 1\text{ mA}$ to 250 mA in $10\text{ }\mu\text{s}$	–40			
		$I_{OUT} = 250\text{ mA}$ to 1 mA in $10\text{ }\mu\text{s}$			40	
	Overshoot on start-up ⁽⁸⁾	Stated as a percentage of $V_{OUT(NOM)}$			5%	
	Overshoot on start-up with EN ⁽⁸⁾	Stated as a percentage of $V_{OUT(NOM)}$, $V_{IN} = V_{OUT} + 1\text{ V}$ to 5.5 V , $0.7\text{ }\mu\text{F} < C_{OUT} < 10\text{ }\mu\text{F}$, $0\text{ mA} < I_{OUT} < 250\text{ mA}$, EN rising until the output is enabled			1%	
t_{ON}	Turnon time	From $V_{EN} > V_{IH}$ to $V_{OUT} = 95\%$ of $V_{OUT(NOM)}$, $T_A = 25^\circ\text{C}$		80	150	μs

6.6 Output and Input Capacitors

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN ⁽¹⁾	TYP	MAX	UNIT
C_{IN}	Input capacitance ⁽²⁾	Capacitance for stability	0.7	1		μF
C_{OUT}	Output capacitance ⁽²⁾		0.7	1	10	
ESR	Output/input capacitance ⁽²⁾		5		500	$\text{m}\Omega$

- (1) The minimum capacitance should be greater than $0.5\text{ }\mu\text{F}$ over the full range of operating conditions. The capacitor tolerance should be 30% or better over the full temperature range. The full range of operating conditions for the capacitor in the application should be considered during device selection to ensure this minimum capacitance specification is met. X7R capacitors are recommended however capacitor types X5R, Y5V and Z5U may be used with consideration of the application and conditions.
- (2) This specification is verified by design.

6.7 Typical Characteristics

$V_{IN} = 3.7\text{ V}$, $V_{OUT} = 2.8\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_{OUT} = 1\text{ }\mu\text{F}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

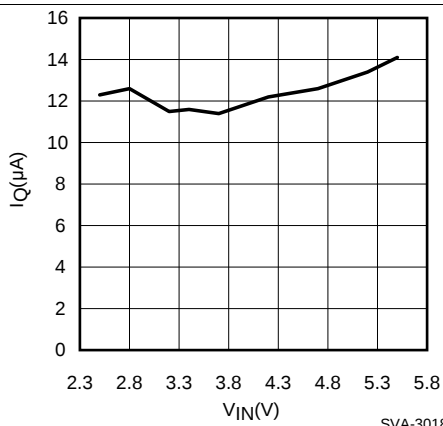


Figure 1. Quiescent Current vs Input Voltage

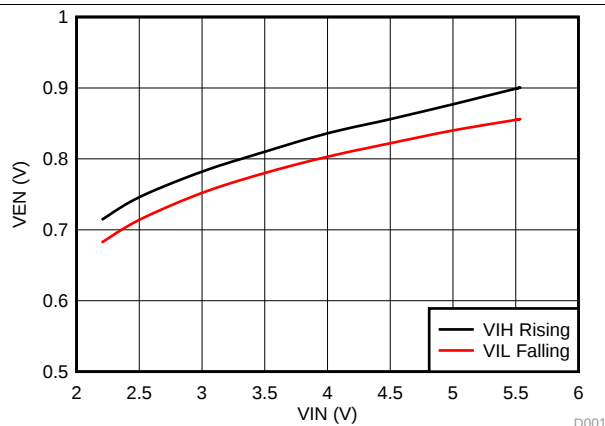


Figure 2. V_{EN} Thresholds vs V_{IN}

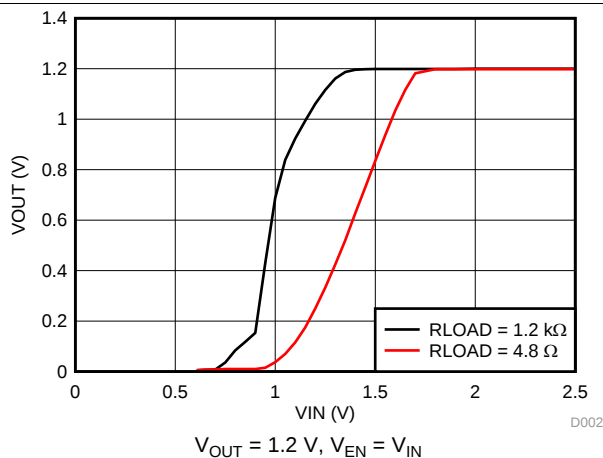


Figure 3. V_{OUT} vs V_{IN}

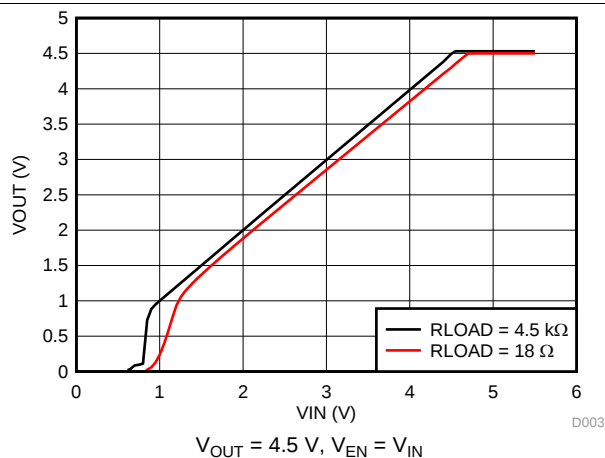


Figure 4. V_{OUT} vs V_{IN}

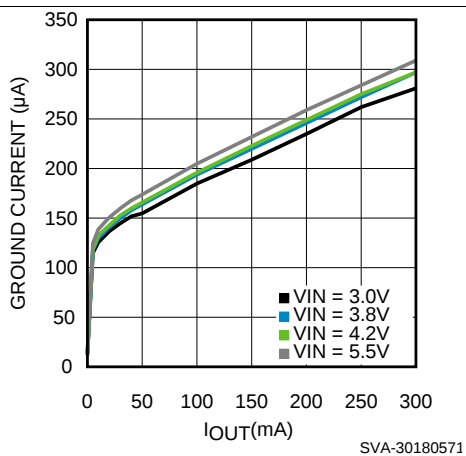


Figure 5. Ground Current vs Output Current

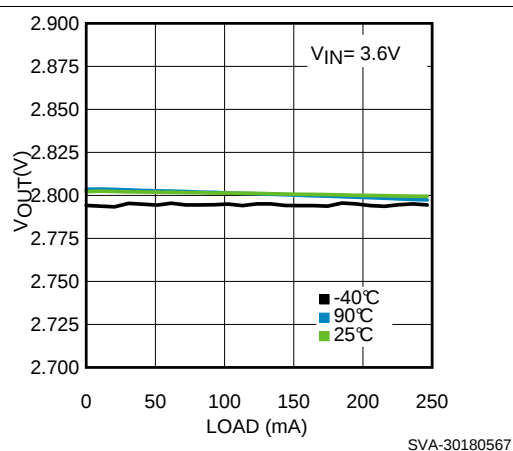


Figure 6. Load Regulation

Typical Characteristics (continued)

$V_{IN} = 3.7\text{ V}$, $V_{OUT} = 2.8\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_{OUT} = 1\text{ }\mu\text{F}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

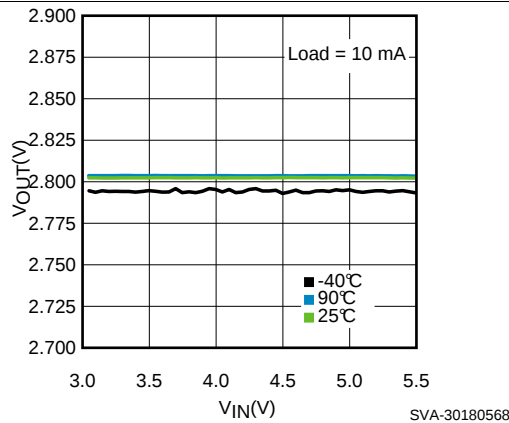


Figure 7. Line Regulation

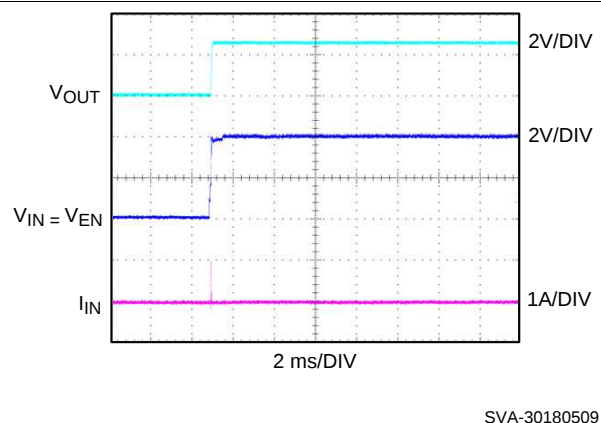


Figure 8. Inrush Current

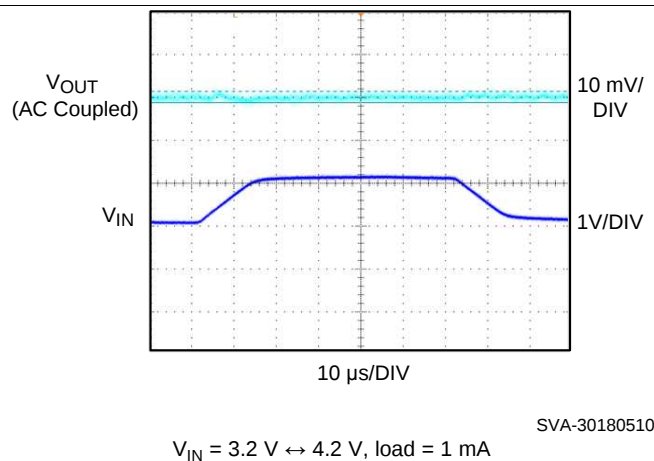


Figure 9. Line Transient

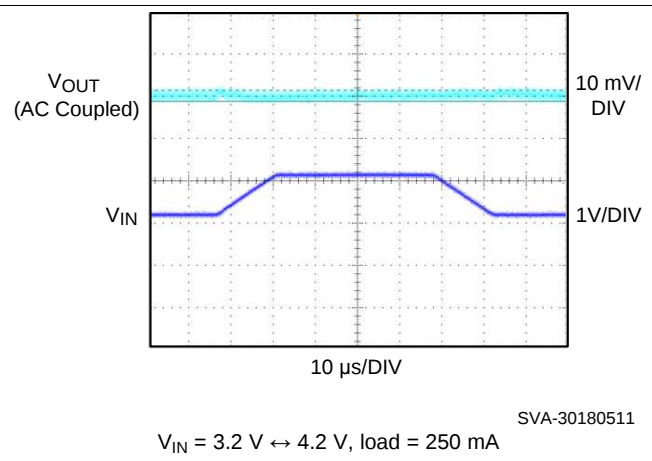


Figure 10. Line Transient

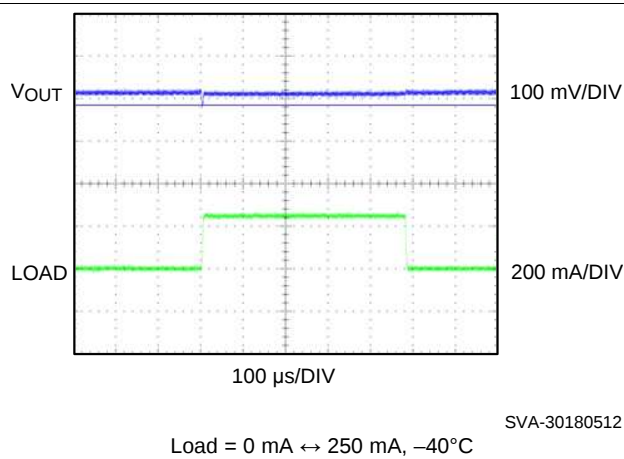


Figure 11. Load Transient

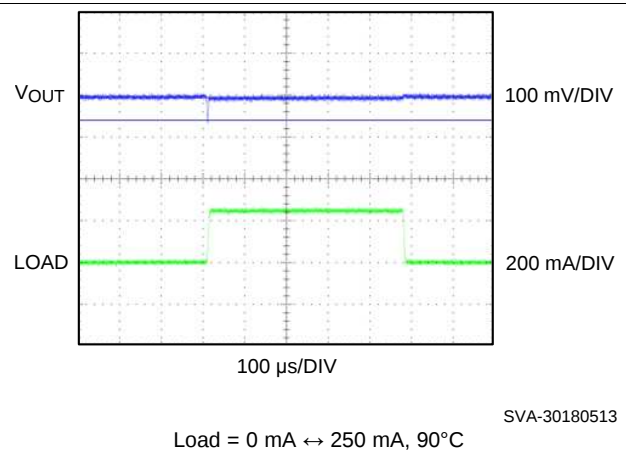
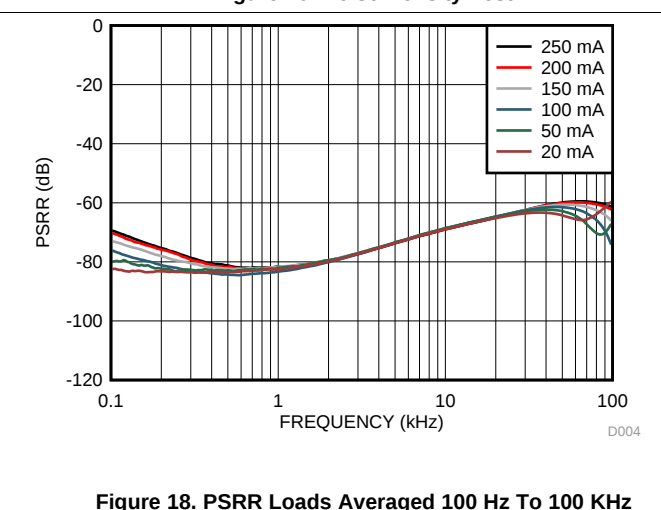
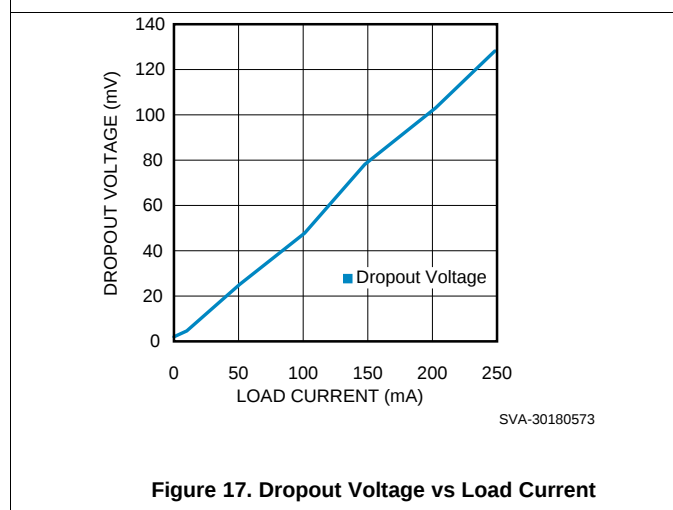
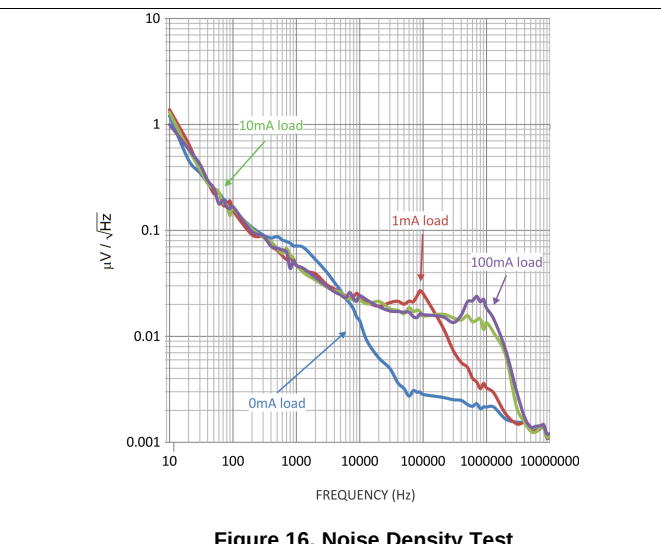
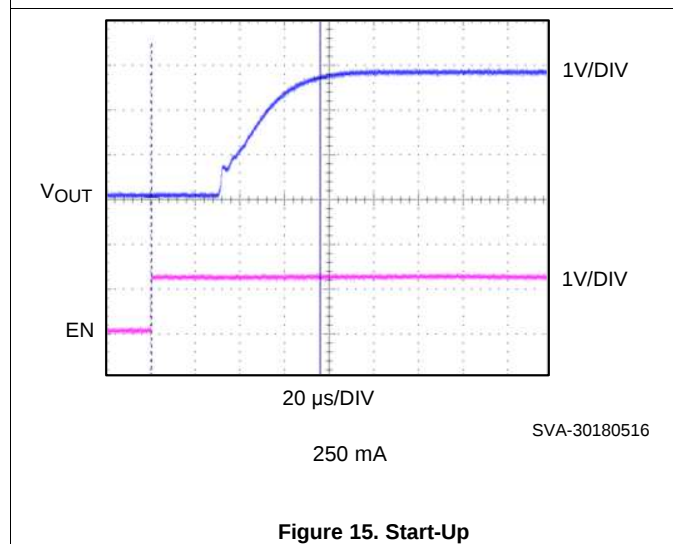
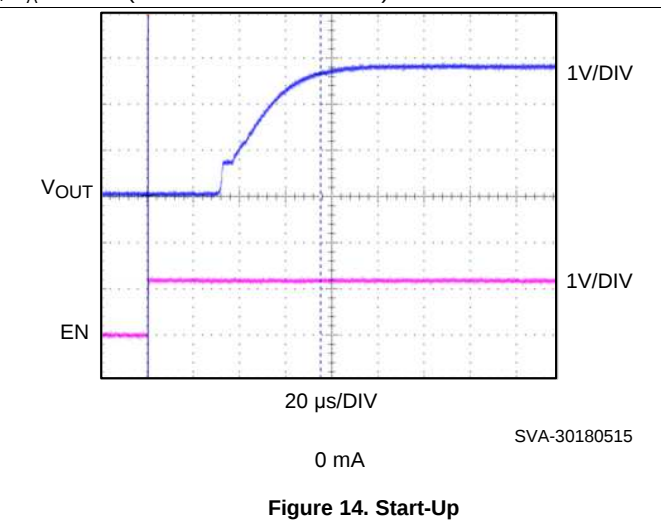
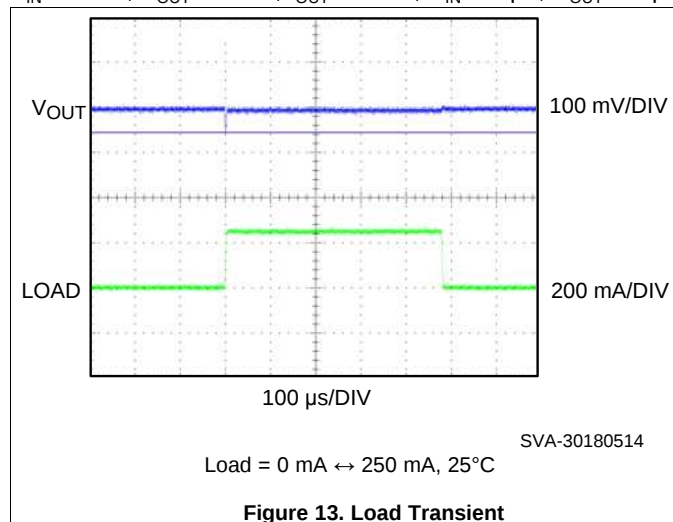


Figure 12. Load Transient

Typical Characteristics (continued)

$V_{IN} = 3.7\text{ V}$, $V_{OUT} = 2.8\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_{OUT} = 1\text{ }\mu\text{F}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)



LP5907-Q1

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Typical Characteristics (continued)

$V_{IN} = 3.7\text{ V}$, $V_{OUT} = 2.8\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_{OUT} = 1\text{ }\mu\text{F}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

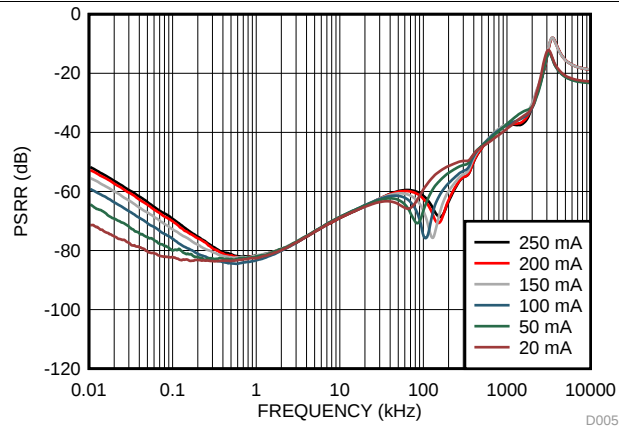


Figure 19. PSRR Loads Averaged 10 Hz To 10 MHz

7.3 Feature Description

7.3.1 LP5907-Q1 Voltage Options

Table 1 lists the available voltage options for the LP5907-Q1 SOT-23 package.

Table 1. Voltage Options

SOT-23 PACKAGE ORDER NUMBER	VOLTAGE OPTION (V)
LP5907QMF1.2Q1	1.2
—	1.3
—	1.5
LP5907QMF1.8Q1	1.8
LP5907QMF2.5Q1	2.5
LP5907QMF2.8Q1	2.8
	2.85
	2.9
LP5907QMF3.0Q1	3.0
LP5907QMF3.3Q1	3.3
LP5907QMF3.8Q1	3.8
LP5907QMF4.5Q1	4.5

7.3.2 Enable (EN)

The LP5907-Q1 EN pin is internally held low by a 1-M Ω resistor to GND. The EN pin voltage must be higher than the V_{IH} threshold to ensure that the device is fully enabled under all operating conditions. The EN pin voltage must be lower than the V_{IL} threshold to ensure that the device is fully disabled and the automatic output discharge is activated.

7.3.3 Low Output Noise

Any internal noise at the LP5907-Q1 reference voltage is reduced by a first order low-pass RC filter before it is passed to the output buffer stage. The low-pass RC filter has a –3 dB cut-off frequency of approximately 0.1 Hz.

7.3.4 Output Automatic Discharge

The LP5907-Q1 output employs an internal 230- Ω (typical) pulldown resistance to discharge the output when the EN pin is low, and the device is disabled.

7.3.5 Remote Output Capacitor Placement

The LP5907-Q1 requires at least a 1- μ F capacitor at the OUT pin, but there are no strict requirements about the location of the capacitor in regards to the OUT pin. In practical designs, the output capacitor may be located up to 10 cm away from the LDO.

7.3.6 Thermal Overload Protection (T_{SD})

Thermal shutdown disables the output when the junction temperature rises to approximately 160°C which allows the device to cool. When the junction temperature cools to approximately 145°C, the output circuitry enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This thermal cycling limits the dissipation of the regulator and protects it from damage as a result of overheating.

The thermal shutdown circuitry of the LP5907-Q1 has been designed to protect against temporary thermal overload conditions. The thermal shutdown circuitry was not intended to replace proper heat-sinking. Continuously running the LP5907-Q1 device into thermal shutdown may degrade device reliability.

7.4 Device Functional Modes

7.4.1 Enable (EN)

The LP5907-Q1 Enable (EN) pin is internally held low by a 1-M Ω resistor to GND. The EN pin voltage must be higher than the V_{IH} threshold to ensure that the device is fully enabled under all operating conditions.

When the EN pin is pulled low, and the output is disabled, the output automatic discharge circuitry is activated. Any charge on the OUT pin is discharged to GND through the internal 230- Ω (typical) pull-down resistance.

7.4.2 Minimum Operating Input Voltage (V_{IN})

The LP5907-Q1 does not include any dedicated undervoltage lockout circuitry. The LP5907-Q1 internal circuitry is not fully functional until V_{IN} is at least 2.2 V. The output voltage is not regulated until V_{IN} has reached at least the greater of 2.2 V or ($V_{OUT} + V_{DO}$).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Figure 20 shows the typical application circuit for the LP5907-Q1. Input and output capacitances may need to be increased above the 1 μF minimum for some applications.

8.2 Typical Application

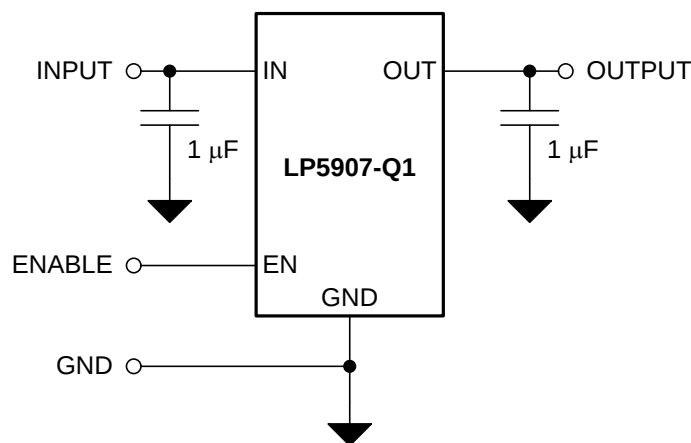


Figure 20. LP5907-Q1 Typical Application

8.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.2 to 5.5 V
Output voltage	1.8 V
Output current	200 mA
Output capacitor range	0.7 to 10 μF
Input/output capacitor ESR range	5 to 500 m Ω

8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Available input voltage range
- Output voltage needed
- Output current needed
- Input and Output capacitors

8.2.2.1 Power Dissipation and Device Operation

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the device, to the ultimate heat sink, the ambient environment. Thus, the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

The maximum allowable power dissipation for the device in a given package can be calculated using [Equation 1](#):

$$P_{D-MAX} = ((T_{J-MAX} - T_A) / R_{\theta JA}) \quad (1)$$

The actual power being dissipated in the device can be represented by [Equation 2](#):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

[Equation 1](#) and [Equation 2](#) establish the relationship between the maximum power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These two equations should be used to determine the optimum operating conditions for the device in the application.

In applications where lower power dissipation (P_D) and/or excellent package thermal resistance ($R_{\theta JA}$) is present, the maximum ambient temperature (T_{A-MAX}) may be increased.

In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature (T_{A-MAX}) may have to be derated. T_{A-MAX} is dependent on the maximum operating junction temperature ($T_{J-MAX-OP} = 125^\circ\text{C}$), the maximum allowable power dissipation in the device package in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by [Equation 3](#):

$$T_{A-MAX} = (T_{J-MAX-OP} - (R_{\theta JA} \times P_{D-MAX})) \quad (3)$$

Alternately, if T_{A-MAX} can not be derated, the P_D value must be reduced. This can be accomplished by reducing V_{IN} in the $V_{IN} - V_{OUT}$ term as long as the minimum V_{IN} is met, or by reducing the I_{OUT} term, or by some combination of the two.

8.2.2.2 External Capacitors

Like most LDOs, the LP5907-Q1 requires external capacitors for regulator stability. The device is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

8.2.2.3 Input Capacitor

An input capacitor is required for stability. The input capacitor should be at least equal to, or greater than, the output capacitor for good load transient performance. At least a 1- μF capacitor has to be connected between the LP5907-Q1 input pin and ground for stable operation over full load current range. Basically, it is acceptable to have more output capacitance than input, as long as the input is at least 1 μF .

The input capacitor must be located a distance of not more than 1 cm from the IN pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: To ensure stable operation it is essential that good PCB practices are employed to minimize ground impedance and keep input inductance low. If these conditions cannot be met, or if long leads are to be used to connect the battery or other power source to the LP5907-Q1, TI recommends increasing the input capacitor to at least 10 μF . Also, tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be verified by the manufacturer to have a surge current rating sufficient for the application. The initial tolerance, applied voltage de-rating, and temperature coefficient must all be considered when selecting the input capacitor to ensure the actual capacitance is never less than 0.7 μF over the entire operating range.

8.2.2.4 Output Capacitor

The LP5907-Q1 is designed specifically to work with a very small ceramic output capacitor, typically 1 μF . A ceramic capacitor (dielectric types X5R or X7R) in the 1- μF to 10- μF range, and with equivalent series resistance (ESR) between 5 m Ω to 500 m Ω , is suitable in the LP5907-Q1 application circuit. For this device connect the output capacitor between the OUT pin and a good connection back to the GND pin.

It may also be possible to use tantalum or film capacitors at the device output, V_{OUT} , but these are not as attractive for reasons of size and cost (see [Capacitor Characteristics](#)).

The output capacitor must meet the requirement for the minimum value of capacitance and have an ESR value that is within the range 5 m Ω to 500 m Ω for stability. Like the input capacitor, the initial tolerance, applied voltage de-rating, and temperature coefficient must all be considered when selecting the input capacitor to ensure the actual capacitance is never less than 0.7 μF over the entire operating range.

8.2.2.5 Capacitor Characteristics

The LP5907-Q1 is designed to work with ceramic capacitors on the input and output to take advantage of the benefits they offer. For capacitance values in the range of 1 μF to 10 μF , ceramic capacitors are the smallest, least expensive, and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1- μF ceramic capacitor is in the range of 20 m Ω to 40 m Ω , which easily meets the ESR requirement for stability for the LP5907-Q1.

A better choice for temperature coefficient in a ceramic capacitor is X7R. This type of capacitor is the most stable and holds the capacitance within $\pm 15\%$ over the temperature range. Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1 μF to 10 μF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. The ESR of a typical tantalum increases about 2:1 as the temperature goes from 25°C down to -40°C, so some guard band must be allowed.

8.2.2.6 Remote Capacitor Operation

The LP5907-Q1 requires at least a 1- μF capacitor at the OUT pin, but there are no strict requirements about the location of the capacitor in regards to the pin. In practical designs the output capacitor may be located up to 10 cm away from the LDO. This means that there is no need to have a special capacitor close to the output pin if there is already respective capacitors in the system (like a capacitor at the input of supplied part). The remote capacitor feature helps user to minimize the number of capacitors in the system.

As a good design practice, keep the wiring parasitic inductance at a minimum, which means to use as wide as possible traces from the LDO output to the capacitors, keeping the LDO output trace layer as close as possible to ground layer and avoiding vias on the path. If there is a need to use vias, implement as many as possible vias between the connection layers. The recommendation is to keep parasitic wiring inductance less than 35 nH. For the applications with fast load transients, it is recommended to use an input capacitor equal to or larger to the sum of the capacitance at the output node for the best load transient performance.

8.2.2.7 No-Load Stability

The LP5907-Q1 remains stable, and in regulation, with no external load.

8.2.2.8 Enable Control

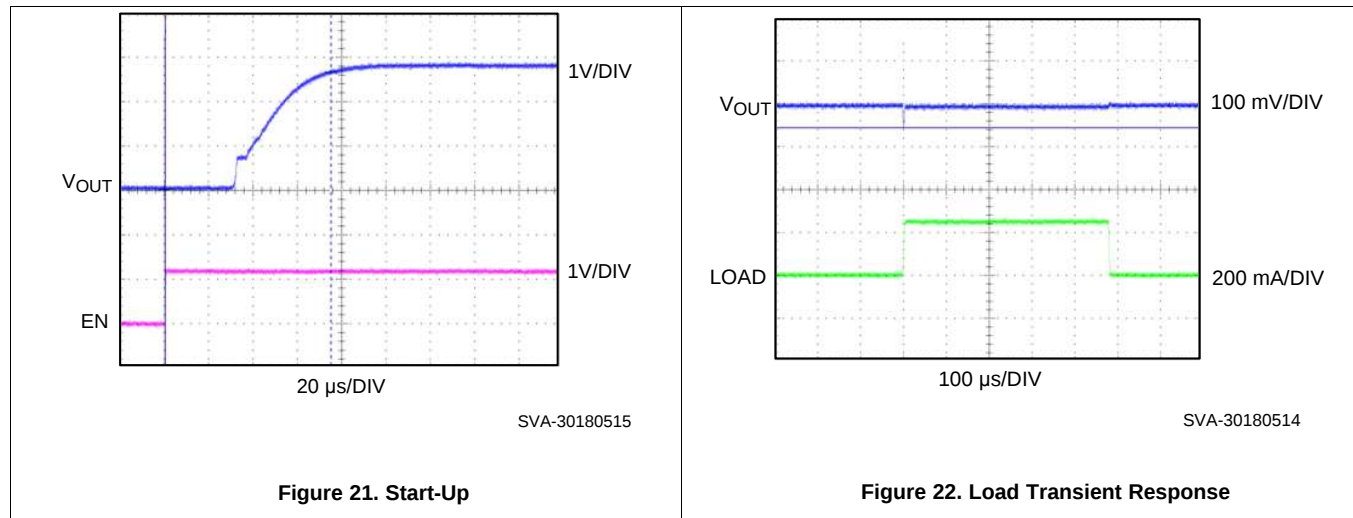
The LP5907-Q1 may be switched ON or OFF by a logic input at the EN pin. A voltage on this pin greater than V_{IH} turns the device on, while a voltage less than V_{IL} turns the device off.

When the EN pin is low, the regulator output is off and the device typically consumes less than 1 μA . Additionally, an output pulldown circuit is activated which ensures that any charge stored on C_{OUT} is discharged to ground.

If the application does not require the use of the shutdown feature, the EN pin can be tied directly to the IN pin to keep the regulator output permanently on.

An internal 1-M Ω pulldown resistor ties the EN input to ground, ensuring that the device remains off if the EN pin is left open circuit. To ensure proper operation, the signal source used to drive the EN pin must be able to swing above and below the specified turnon or turnoff voltage thresholds listed in the [Electrical Characteristics](#) under V_{IL} and V_{IH} .

8.2.3 Application Curves



9 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 2.2 V to 5.5 V. The input supply must be well regulated and free of spurious noise. To ensure that the LP5907-Q1 output voltage is well regulated and dynamic performance is optimum, the input supply must be at least $V_{OUT} + 1$ V. A minimum capacitor value of 1 μ F is required to be within 1 cm of the IN pin.

10 Layout

10.1 Layout Guidelines

The dynamic performance of the LP5907-Q1 is dependant on the layout of the PCB. PCB layout practices that are adequate for typical LDOs may degrade the PSRR, noise, or transient performance of the LP5907-Q1.

Best performance is achieved by placing C_{IN} and C_{OUT} on the same side of the PCB as the LP5907-Q1, and as close as is practical to the package. The ground connections for C_{IN} and C_{OUT} must be back to the LP5907-Q1 ground pin using as wide and short copper traces as are practical.

Avoid connections using long trace lengths, narrow trace widths, and/or connections through vias. These add parasitic inductances and resistance that results in inferior performance especially during transient conditions

10.2 Layout Examples

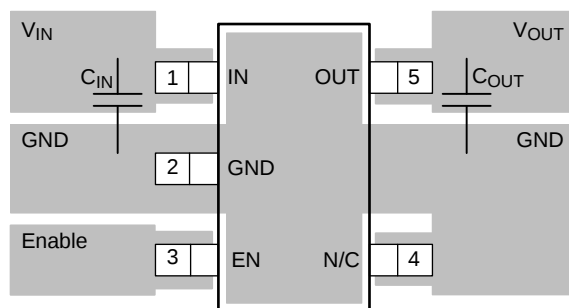


Figure 23. LP5907MF-x.x (SOT-23) Typical Layout

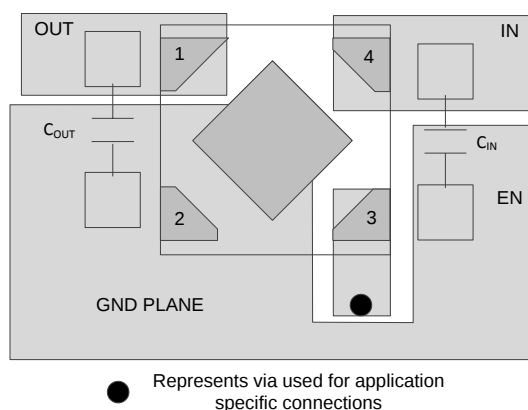


Figure 24. Layout Example for the DQN Package

11 器件和文档支持

11.1 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的通知我进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

TI E2E™ 在线社区 [TI 的工程师对工程师 \(E2E\) 社区](http://e2e.ti.com)。此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 [TI 参考设计支持](#) 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

11.3 商标

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

11.4 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.5 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP590712QDQNRQ1	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	D1
LP590713QDQNRQ1	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	D2
LP590715QDQNRQ1	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	D3
LP590718QDQNRQ1	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	D4
LP590722QDQNRQ1	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	FV
LP590725QDQNRQ1	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	D5
LP5907285QDQNRQ1	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	D7
LP590728QDQNRQ1	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	D6
LP590729QDQNRQ1	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	D8
LP590730QDQNRQ1	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	D9
LP590733QDQNRQ1	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	DA
LP590738QDQNRQ1	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	DB
LP590745QDQNRQ1	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	DC
LP5907QMFx-1.2Q1	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	RAFQ
LP5907QMFx-1.8Q1	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	RAGQ
LP5907QMFx-2.5Q1	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	RAJQ
LP5907QMFx-2.8Q1	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	RAKQ
LP5907QMFx-3.0Q1	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	RALQ
LP5907QMFx-3.3Q1	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	RAHQ
LP5907QMFx-3.8Q1	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	RAMQ
LP5907QMFx-4.5Q1	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	Call TI Sn	Level-1-260C-UNLIM	-40 to 125	RAIQ

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LP5907-Q1 :

- Catalog : [LP5907](#)

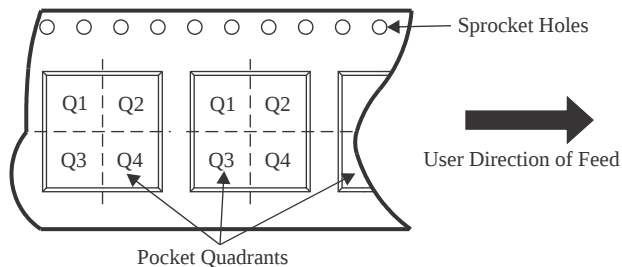
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP590712QDQNRQ1	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
LP590713QDQNRQ1	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
LP590715QDQNRQ1	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
LP590718QDQNRQ1	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
LP590722QDQNRQ1	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
LP590725QDQNRQ1	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
LP5907285QDQNRQ1	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
LP590728QDQNRQ1	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
LP590729QDQNRQ1	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
LP590730QDQNRQ1	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
LP590733QDQNRQ1	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
LP590738QDQNRQ1	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
LP590745QDQNRQ1	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
LP5907QMFx-1.2Q1	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907QMFx-1.8Q1	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907QMFx-2.5Q1	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5907QMFx-2.8Q1	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907QMFx-3.0Q1	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907QMFx-3.3Q1	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907QMFx-3.8Q1	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907QMFx-4.5Q1	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

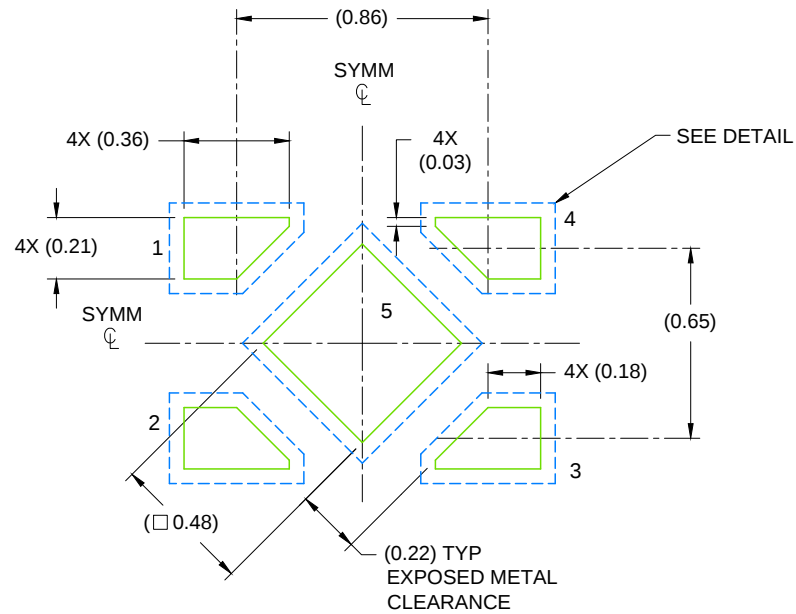
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP590712QDQNRQ1	X2SON	DQN	4	3000	213.0	191.0	35.0
LP590713QDQNRQ1	X2SON	DQN	4	3000	213.0	191.0	35.0
LP590715QDQNRQ1	X2SON	DQN	4	3000	213.0	191.0	35.0
LP590718QDQNRQ1	X2SON	DQN	4	3000	213.0	191.0	35.0
LP590722QDQNRQ1	X2SON	DQN	4	3000	213.0	191.0	35.0
LP590725QDQNRQ1	X2SON	DQN	4	3000	213.0	191.0	35.0
LP5907285QDQNRQ1	X2SON	DQN	4	3000	213.0	191.0	35.0
LP590728QDQNRQ1	X2SON	DQN	4	3000	213.0	191.0	35.0
LP590729QDQNRQ1	X2SON	DQN	4	3000	213.0	191.0	35.0
LP590730QDQNRQ1	X2SON	DQN	4	3000	213.0	191.0	35.0
LP590733QDQNRQ1	X2SON	DQN	4	3000	213.0	191.0	35.0
LP590738QDQNRQ1	X2SON	DQN	4	3000	213.0	191.0	35.0
LP590745QDQNRQ1	X2SON	DQN	4	3000	213.0	191.0	35.0
LP5907QMFx-1.2Q1	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907QMFx-1.8Q1	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907QMFx-2.5Q1	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907QMFx-2.8Q1	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907QMFx-3.0Q1	SOT-23	DBV	5	3000	208.0	191.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5907QMFx-3.3Q1	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907QMFx-3.8Q1	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907QMFx-4.5Q1	SOT-23	DBV	5	3000	208.0	191.0	35.0

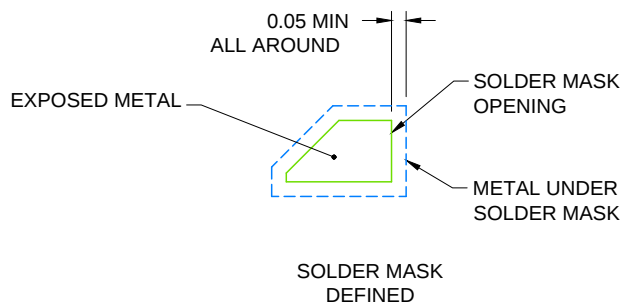
PLASTIC SMALL OUTLINE - NO LEAD



1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.
5. Shape of exposed side leads may differ.
6. Number and location of exposed tie bars may vary.



LAND PATTERN EXAMPLE
SCALE: 40X

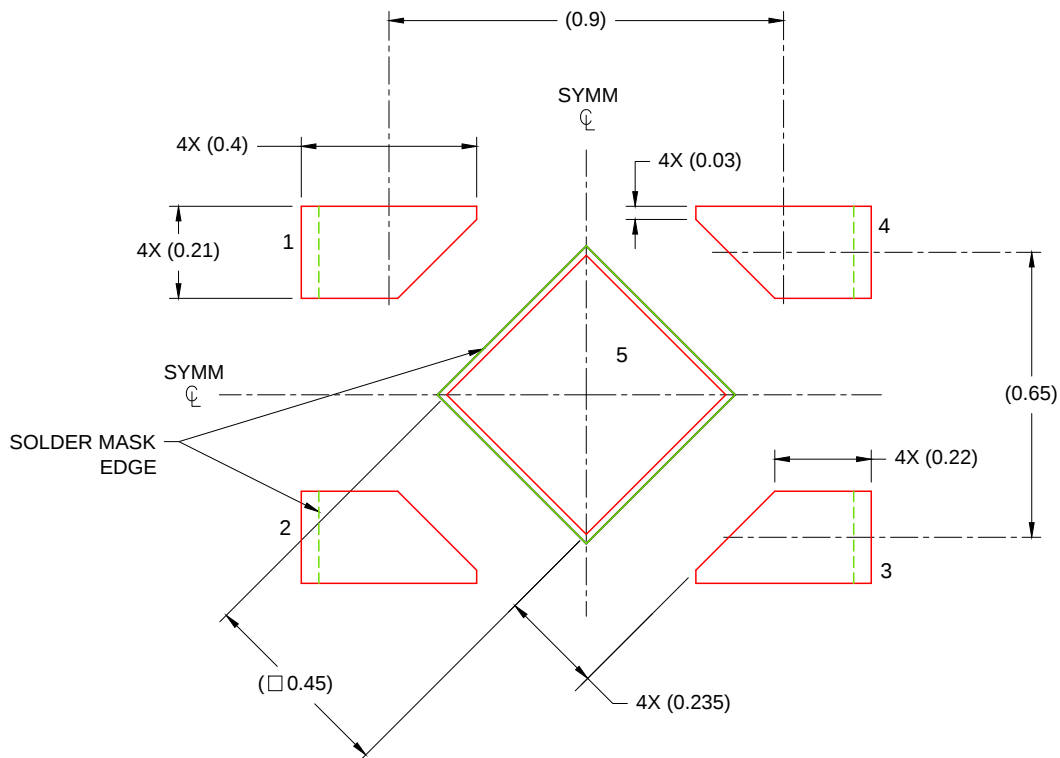


SOLDER MASK DETAIL

4215302/E 12/2016

NOTES: (continued)

7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
8. If any vias are implemented, it is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
 BASED ON 0.075 - 0.1mm THICK STENCIL

EXPOSED PAD
 88% PRINTED SOLDER COVERAGE BY AREA
 SCALE: 60X

4215302/E 12/2016

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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