TPS2294x Low-input-voltage Current-limited Load Switches With Shut Off And Auto-Restart Feature

1 Features

- Input Voltage Range: 1.62 V to 5.5 V
- Low ON resistance
  - r_{ON} = 0.4 Ω at V_{IN} = 5.5 V
  - r_{ON} = 0.5 Ω at V_{IN} = 3.3 V
  - r_{ON} = 0.6 Ω at V_{IN} = 2.5 V
  - r_{ON} = 0.8 Ω at V_{IN} = 1.8 V
- Minimum Current Limit: 40 mA or 100 mA
- Undervoltage Lockout (UVLO)
- Thermal Shutdown
- Shutdown Current < 1 µA
- Fast Current Limit Response Time
- Fault Blanking
- Auto Restart
- 1.8-V Compatible Control Input Thresholds
- ESD Performance Tested Per JESD 22
  - 4000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Tiny SC-70 (DCK) Package
- UL Recognized Component (UL File 169910)
- Evaluated to IEC 60950-1, Ed 2, Am1, Annex CC, Test Program 2 with CB Report

2 Applications

- Low-Current Sensor Protection
- HDMI Connector Protection
- Notebooks
- PDAs
- GPS Devices
- MP3 Players
- Peripheral Ports

3 Description

The TPS22941/2/3/4/5 load switches provide protection to systems and loads in high-current conditions. The devices contain a 0.4-Ω current-limited P-channel MOSFET that can operate over an input voltage range of 1.62 V to 5.5 V. Current is prevented from flowing when the MOSFET is off. The switch is controlled by an on/off input (ON), which is capable of interfacing directly with low-voltage control signals. The TPS22941/2/3/4/5 includes thermal shutdown protection that prevents damage to the device when a continuous over-current condition causes excessive heating by turning off the switch.

These devices provide an integrated, robust solution to provide current limiting the output current to a safe level by switching into a constant-current mode when the ouptut load exceeds the current-limit threshold. The OC logic output asserts low during overcurrent, undervoltage, or overtemperature conditions. These additional features make the TPS22941/2/3/4/5 an ideal solution for applications where current limiting is necessary.

This family of devices are available in a SC70-5 (DCK) package. It is characterized for operation over the free-air temperature range of –40°C to 85°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22941	SC70 (5)	2.00mm × 2.10 mm
TPS22942		
TPS22943		
TPS22944		
TPS22945		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

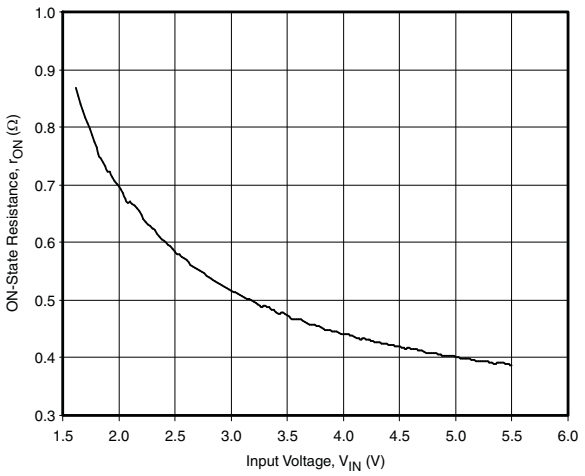


Table of Contents

4 Revision History

Changes from Revision C (November 2009) to Revision D **Page**

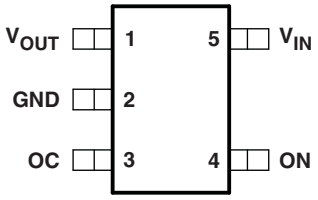
- Added *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

5 Device Comparison Table

DEVICE	MINIMUM CURRENT LIMIT (mA)	CURRENT LIMIT BLANKING TIME (ms)	AUTO-RESTART TIME (ms)	ON PIN ACTIVITY
TPS22941	40	10	80	Active LOW
TPS22942	100	10	80	Active LOW
TPS22943	40	0	N/A	Active HIGH
TPS22944	100	0	N/A	Active HIGH
TPS22945	100	10	80	Active HIGH

6 Pin Configuration and Functions

DCK PACKAGE
(TOP VIEW)



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	SOT (DCK) PIN NO.		
V_{OUT}	1	O	Switch Output. Place ceramic bypass capacitor(s) between this terminal and GND. See the *Application Information* section for more information.
GND	2	–	Ground
OC	3	O	Over current output flag: active LOW, open drain output that indicates an over current, supply under voltage, or over temperature state.
ON	4	I	Switch control input. Do not leave floating.
V_{IN}	5	I	Switch Input. Place ceramic bypass capacitor(s) between this terminal and GND. See the *Application Information* section for more information.

7 Specifications

7.1 Absolute Maximum Ratings(1)

			MIN	MAX	UNIT
V_I	Input voltage range	V_{IN}, V_{OUT}, ON	–0.3	6	V
T_J	Operating junction temperature range		Internally Limited		°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–4	4	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–1	1	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage	1.62	5.5	V
V_{OUT}	Output voltage		V_{IN}	
T_A	Ambient free-air temperature	–40	85	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS22941/2/3/4/5 DCK 5 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	294	°C/W
$\theta_{JC(top)}$	Junction-to-case (top) thermal resistance	59.2	
θ_{JB}	Junction-to-board thermal resistance	95.4	
ψ_{JT}	Junction-to-top characterization parameter	0.7	
ψ_{JB}	Junction-to-board characterization parameter	93.9	
$\theta_{JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

V_{IN} = 1.62 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP(1)	MAX	UNIT
I_{IN}	Quiescent current	I_{OUT} = 0 mA,	V_{IN} = 1.62 V to 5.5 V	Full		40	80	µA
$I_{IN(OFF)}$	OFF-State supply current	V_{ON} = 0 V (TPS22943/4/5) or V_{ON} = V_{IN} (TPS22941/2)	V_{IN} = 3.6 V, V_{OUT} open	Full			1	µA
$I_{OUT(LEAKAGE)}$	OFF-State switch current	V_{ON} = 0 V (TPS22943/4/5) or V_{ON} = V_{IN} (TPS22941/2)	V_{IN} = 3.6 V, V_{OUT} short to GND	Full			1	µA
r_{ON}	ON-state resistance	I_{OUT} = 20 mA	V_{IN} = 5.5 V	25°C		0.4	0.5	Ω
				Full			0.6	
			V_{IN} = 3.3 V	25°C		0.5	0.6	
				Full			0.7	
			V_{IN} = 2.5 V	25°C		0.6	0.7	
				Full			0.8	
			V_{IN} = 1.8 V	25°C		0.8	0.9	
				Full			1.1	
			V_{IN} = 1.62 V	25°C		0.9	1.1	
				Full			1.2	
I_{ON}	ON input leakage current	V_{ON} = V_{IN} or GND		Full			1	µA
I_{LIM}	Current limit	V_{IN} = 3.3 V, V_{OUT} = 3 V	TPS22941/3	Full	40	65	80	mA
			TPS22942/4/5		100	150	200	
T_{SD}	Thermal shutdown	Shutdown threshold		Full		140		°C
		Return from shutdown				130		
		Hysteresis				10		

(1) Typical values are at V_{IN} = 3.3 V and T_A = 25°C.

Electrical Characteristics (continued)

V_{IN} = 1.62 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP(1)	MAX	UNIT
UVLO	Undervoltage shutdown	V_{IN} increasing	Full	1.32	1.42	1.52	V
	Undervoltage shutdown hysteresis		Full		45		mV
Control Output (OC)							
Vol	OC output logic low voltage	V_{IN} = 5 V, I_{SINK} = 10 mA	Full		0.1	0.2	V
		V_{IN} = 1.8 V, I_{SINK} = 10 mA			0.1	0.3	
Ioz	OC output high leakage current voltage	V_{IN} = 5 V, Switch ON	Full			0.5	µA
Control Input (ON)							
Vih	ON high-level input voltage	V_{IN} = 1.8 V	Full	1.1			V
		V_{IN} = 2.5 V	Full	1.3			V
		V_{IN} = 3.3 V	Full	1.4			V
		V_{IN} = 5.5 V	Full	1.7			V
Vil	ON low-level input voltage	V_{IN} = 1.8 V	Full			0.5	V
		V_{IN} = 2.5 V	Full			0.7	V
		V_{IN} = 3.3 V	Full			0.8	V
		V_{IN} = 5.5 V	Full			0.9	V
Ii	ON high-level input leakage current	V_{IN} = 1.8 V to 5 V, Switch ON	Full			1	µA

7.6 Switching Characteristics

V_{IN} = 3.3 V, R_L = 500 Ω, C_L = 0.1 µF, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{ON}	Turn-ON time	R_L = 500 Ω,	C_L = 0.1 µF		60		µs
t_{OFF}	Turn-OFF time	R_L = 500 Ω,	C_L = 0.1 µF		30		µs
t_r	V_{OUT} rise time	R_L = 500 Ω,	C_L = 0.1 µF		10		µs
t_f	V_{OUT} fall time	R_L = 500 Ω,	C_L = 0.1 µF		90		µs
t_{BLANK}	Over current blanking time	TPS22941/2/5		5	10	20	ms
t_{RSTART}	Auto-restart time	TPS22941/2/5		40	80	160	ms
	Short-circuit response time	V_{IN} = V_{ON} = 3.3 V, moderate overcurrent condition			9		µs
		V_{IN} = V_{ON} = 3.3 V, hard short			4		µs

7.7 Typical Characteristics

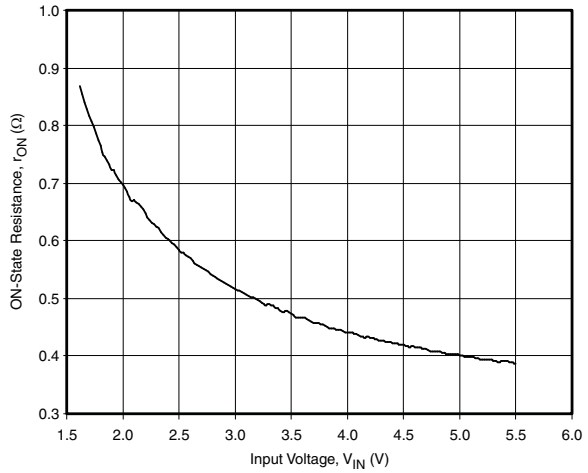


Figure 1. r_{ON} vs V_{IN}

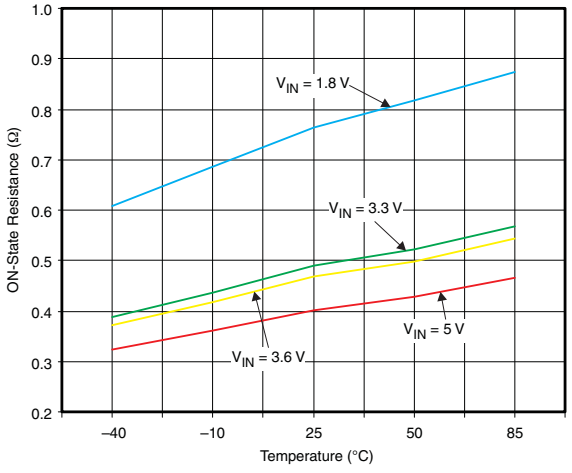


Figure 2. r_{ON} vs Temperature

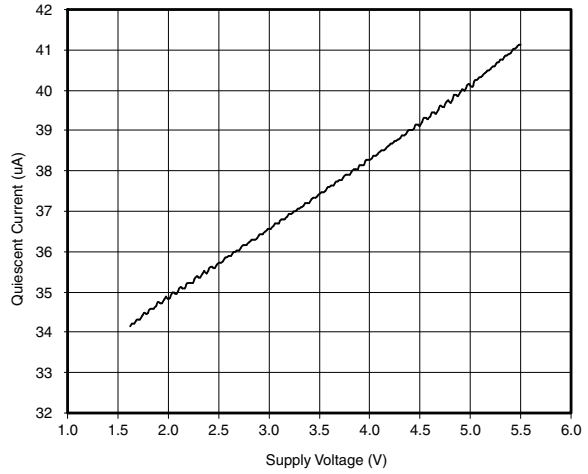


Figure 3. Quiescent Current vs V_{IN}

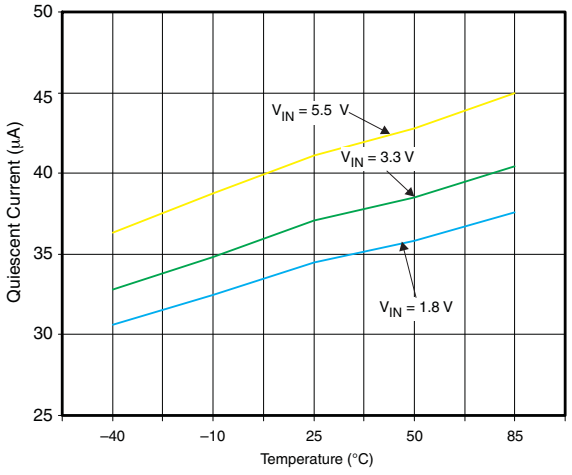


Figure 4. Quiescent Current vs Temperature

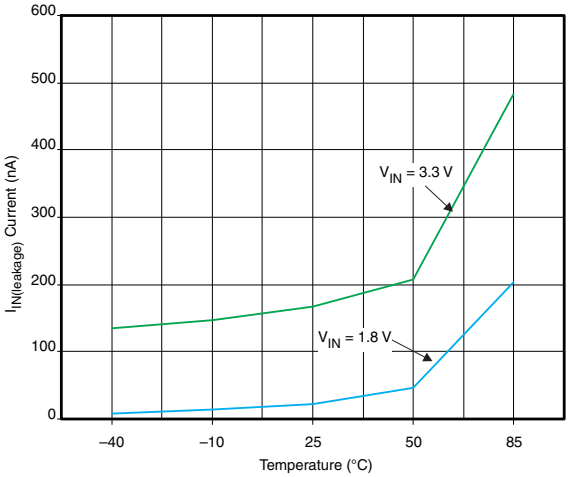


Figure 5. $I_{IN(Leakage)}$ vs Temperature

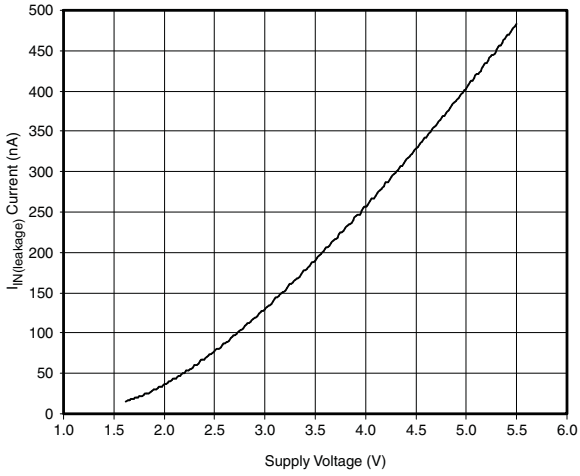


Figure 6. $I_{IN(Leakage)}$ vs V_{IN}

Typical Characteristics (continued)

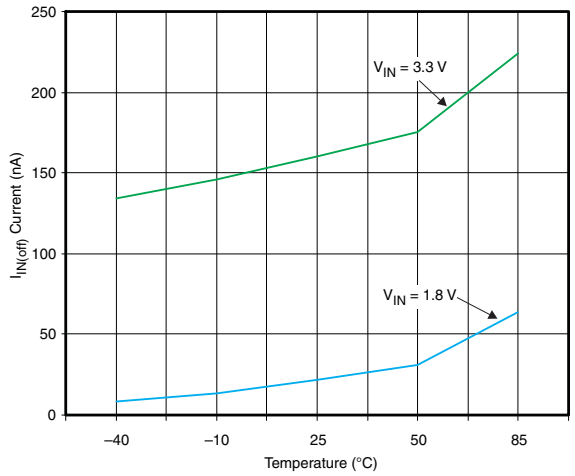


Figure 7. $I_{IN(off)}$ vs Temperature

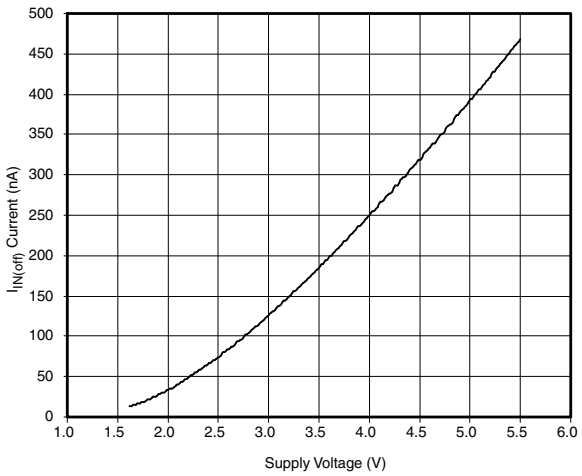


Figure 8. $I_{IN(off)}$ vs V_{IN}

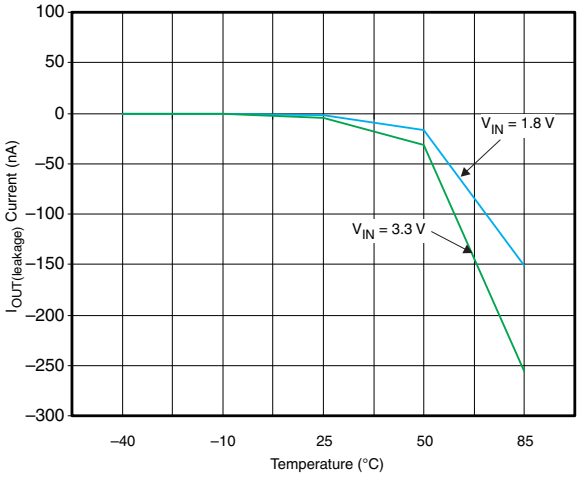


Figure 9. $I_{OUT(leakage)}$ vs Temperature

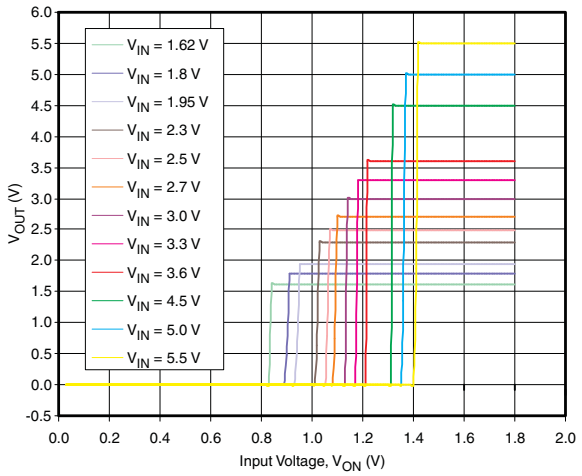


Figure 10. V_{OUT} vs ON Threshold

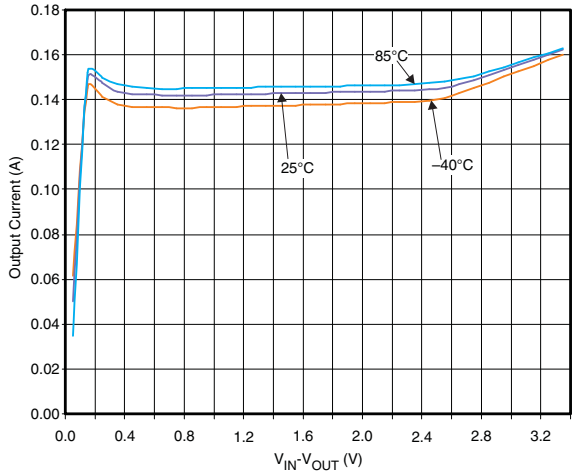


Figure 11. I_{LIM} vs Output Voltage (TPS22942, TPS22944, TPS22945)

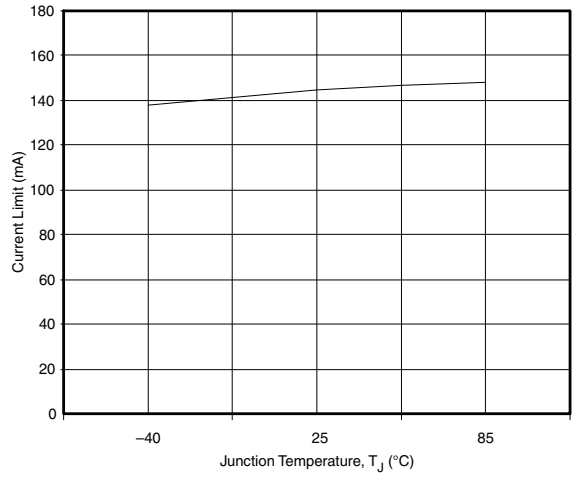


Figure 12. I_{LIM} vs Temperature (TPS22942, TPS22944, TPS22945)

Typical Characteristics (continued)

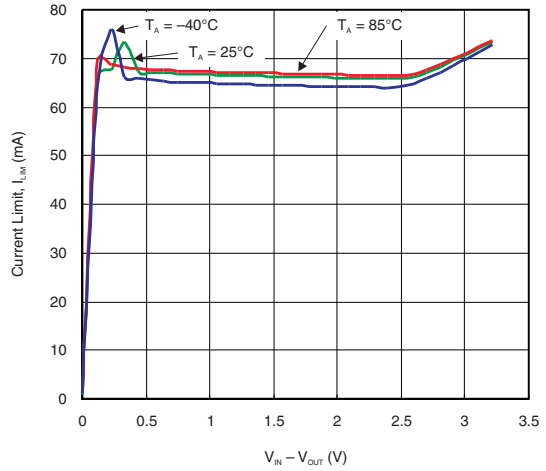


Figure 13. I_{LIM} vs (V_{IN}-V_{OUT}) (TPS22941, TPS22943)

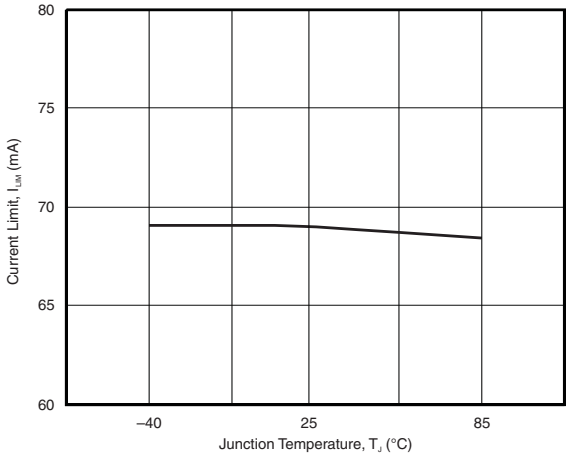
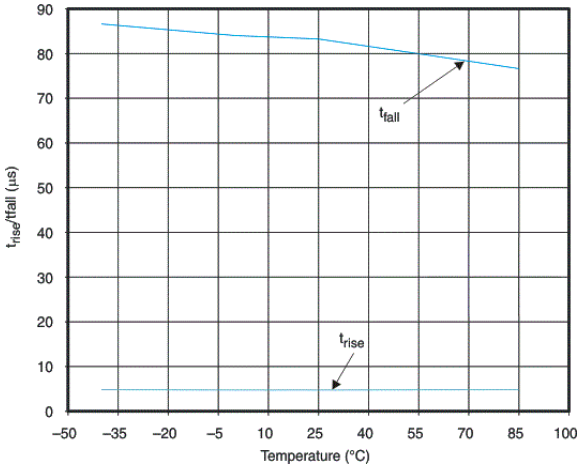
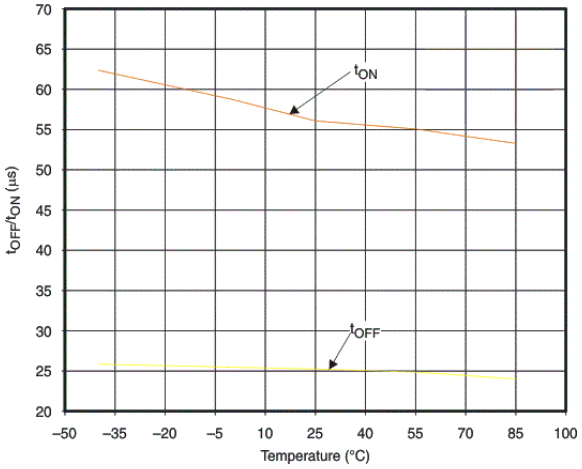


Figure 14. I_{LIM} vs Temperature (TPS22941, TPS22943)



C_L = 0.1 µF R_L = 350 Ω V_{IN} = 3.3 V

Figure 15. t_{rise}/t_{fall} vs Temperature



C_L = 0.1 µF R_L = 350 Ω V_{IN} = 3.3 V

Figure 16. t_{ON}/t_{OFF} vs Temperature

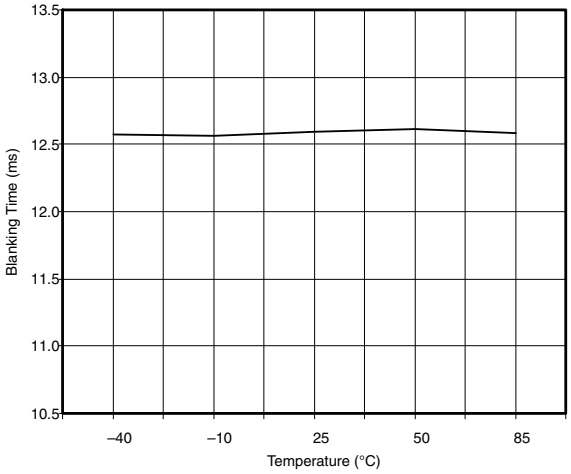


Figure 17. t_{BLANK} vs Temperature (V_{IN} = 3.3 V)

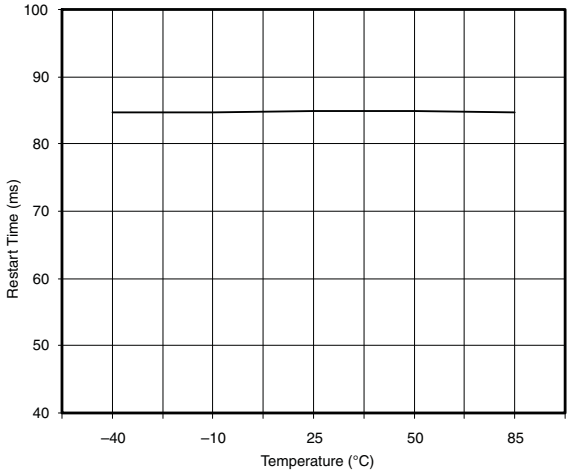


Figure 18. $t_{RESTART}$ vs Temperature (V_{IN} = 3.3 V)

8 Detailed Description

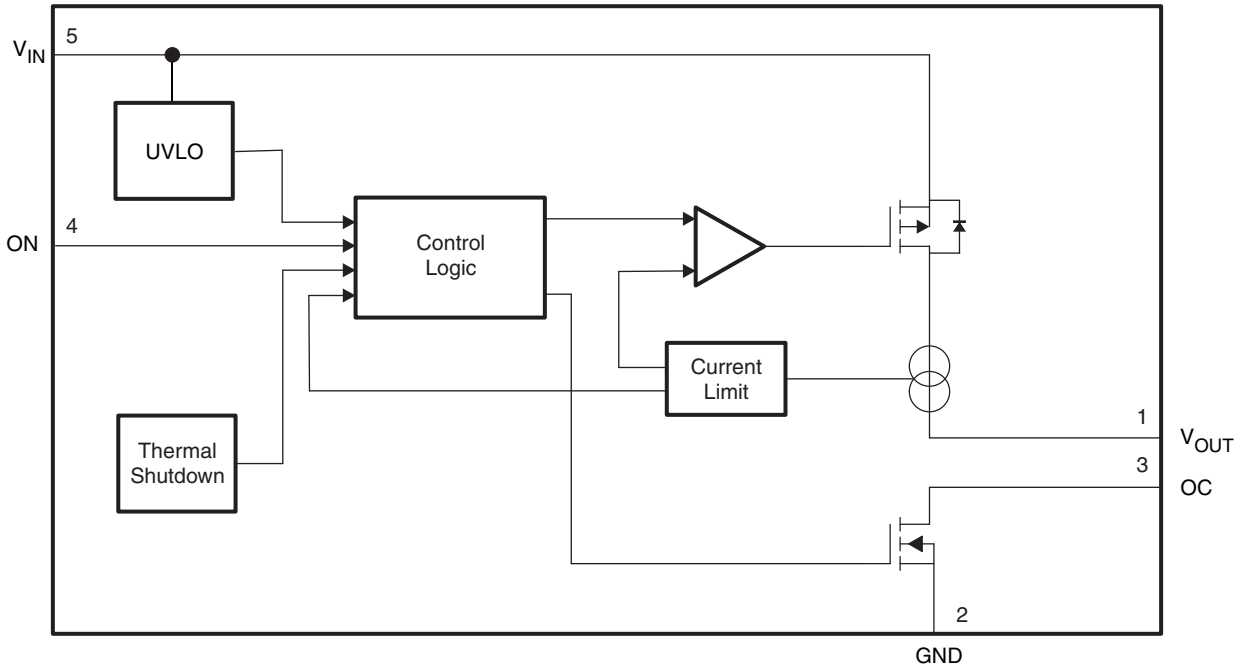
8.1 Overview

The TPS22941/2/3/4/5 load switches are 5.5V, current limited load switches in a SC-70 package. The devices contain a 0.4-Ω current-limited P-channel MOSFET that can operate over an input voltage range of 1.62 V to 5.5 V.

When the switch current reaches the maximum limit, the TPS22941/2/3/4/5 operates in a constant-current mode to prohibit excessive currents from causing damage. TPS22941/3 has a current limit of 40 mA and TPS22942/4/5 has a current limit of 100 mA.

For the TPS22941/2/5, if the constant current condition still persists after 10ms, these parts shut off the switch and pull the fault signal pin (OC) low. The TPS22941/2/5 have an auto-restart feature that turns the switch on again after 80 ms if the ON pin is still active. A current limit condition on the TPS22943 and on the TPS22944 immediately pull the fault signal pin low (OC pin) and the part remains in the constant-current mode until the switch current falls below the current limit.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Fault Reporting

When an overcurrent, input undervoltage, or overtemperature condition is detected, OC is set active low to signal the fault mode. OC is an open-drain MOSFET and requires a pullup resistor between V_{IN} and OC. During shutdown, the pulldown on OC is disabled, reducing current draw from the supply.

8.3.2 Current Limiting

When the switch current reaches the maximum limit, the TPS22921/2/3/4/5 operates in a constant-current mode to prohibit excessive currents from causing damage. TPS22921/3 has a current limit of 40 mA and TPS22922/4/5 has a current limit of 100 mA. A current limit condition immediately pulls the fault signal pin low (OC pin), and the part remains in the constant-current mode until the switch current falls below the current limit.

Feature Description (continued)

8.3.3 Thermal Shutdown

Thermal shutdown protects the part from internally or externally generated excessive temperatures. During an overtemperature condition the switch is turned off. The switch automatically turns on again if the temperature of the die drops below the threshold temperature.

8.4 Device Functional Modes

When the ON pin is actively pulled high and no fault conditions are present, the switch will be turned on, connecting VIN to VOUT. When the ON pin is actively pulled low regardless of the fault condition, the switch will be turned off.

In the event that the current limit is exceeded, the device will operate in a constant-current mode and pull the OC pin low until the fault condition is removed. If the condition persists after the current limit blanking time, the device will automatically turn off.

During thermal shutdown conditions, the switch will automatically turn off and will turn back on again if the temperature of the die drops below the threshold temperature.

9 Application and Implementation

This section will highlight some of the design considerations when implementing this device in various applications.

9.1 Application Information

9.1.1 On/Off Control

The ON pin controls the state of the switch. Activating ON continuously holds the switch in the on state as long as there is no fault. An undervoltage lockout or thermal shutdown event will override the ON pin control and turn off the switch. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals.

9.1.2 Undervoltage Lockout

The undervoltage lockout turns off the switch if the input voltage drops below the undervoltage lockout threshold. With the ON pin active, the input voltage rising above the undervoltage lockout threshold causes a controlled turn-on of the switch, which limits current overshoots.

9.1.3 Reverse Voltage

If the voltage at the V_{OUT} pin is larger than the V_{IN} pin, large currents may flow and can cause permanent damage to the device. TPS22941/2/3/4/5 is designed to control current flow only from V_{IN} to V_{OUT}.

9.1.4 Input Capacitor

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharged load capacitor or a short-circuit, a capacitor needs to be placed between V_{IN} and GND. A 1-µF ceramic capacitor, C_{IN}, placed close to the pins is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop.

9.1.5 Output Capacitor

A 0.1-µF capacitor, C_{OUT}, should be placed between V_{OUT} and GND. This capacitor will prevent parasitic board inductances from forcing V_{OUT} below GND when the switch turns off. For the TPS22941/2/3/4/5, the total output capacitance needs to be kept below a maximum value, $C_{OUT(MAX)}$, to prevent the part from registering an over-current condition and turning-off the switch.

Due to the integrated body diode in the PMOS switch, a C_{IN} greater than C_{OUT} is highly recommended. A C_{OUT} greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN}.

9.2 Typical Application

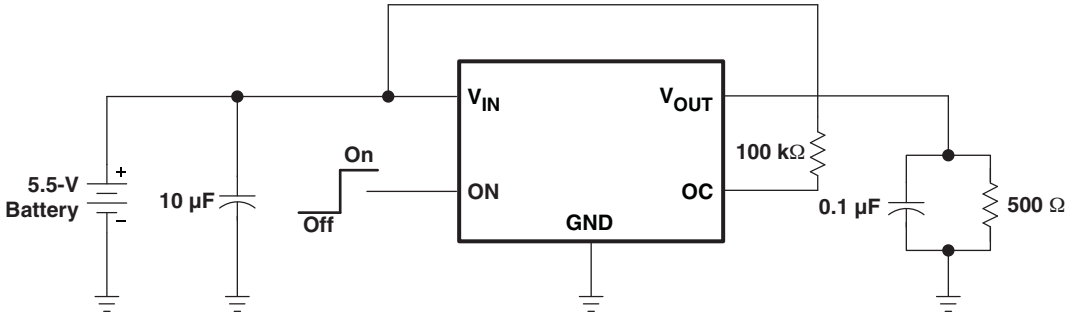


Figure 19. Typical Application Circuit, Active-High Enabled Device (TPS22943, TPS22944 and TPS22945 Only)

Typical Application (continued)

9.2.1 Design Requirements

For this design example, use the following as the input parameters:

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	5.0 V
Load Current	50mA

9.2.2 Detailed Design Procedure

To begin the design process, the designer needs to know the following:

- VIN voltage
- Load current

9.2.2.1 VIN to VOUT Voltage Drop

The VIN to VOUT voltage drop in the device is determined by the R_{ON} of the device and the load current. The R_{ON} of the device depends upon the V_{IN} condition of the device. Refer to the R_{ON} specification of the device in the Electrical Characteristics table of this datasheet.

Once the R_{ON} of the device is determined based upon the VIN conditions, use Equation 1 to calculate the VIN to VOUT voltage drop:

$$\Delta V = I_{LOAD} \times R_{ON} \quad (1)$$

where:

- ΔV = voltage drop from VIN to VOUT
- I_{LOAD} = load current
- R_{ON} = ON-resistance of the device for a specific V_{IN}

9.2.2.2 Maximum Output Capacitance

When designing this device, it is important to ensure the inrush current of the output capacitance does not cause the device to exceed the current limiting time beyond the blanking time. The maximum output capacitance can be determined from Equation 2 :

$$C_{OUT} = \frac{I_{LM(MAX)} \times t_{BLANK(MIN)}}{V_{IN}} \quad (2)$$

where:

- C_{OUT} = output capacitance
- $I_{LIM(MAX)}$ = maximum current limit
- $t_{BLANK(MIN)}$ = minimum blanking time
- V_{IN} = input voltage

9.2.2.3 Power Dissipation

During normal operation as a switch, the power dissipation is small and has little effect on the operating temperature of the part. The parts with the higher current limits will dissipate the most power and that will only be,

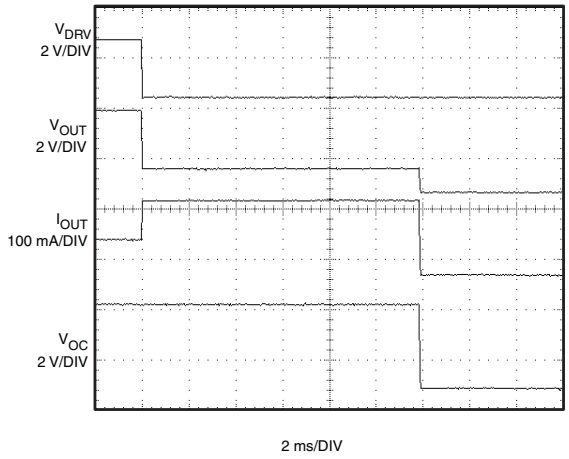
$$P_D = (I_{LIM})^2 \times r_{ON} \quad (3)$$

If the part goes into current limit the maximum power dissipation will occur when the output is shorted to ground. For TPS22941/2/5, the power dissipation scales by the auto-restart time ($t_{RESTART}$) and the overcurrent blanking time (t_{BLANK}) so that the maximum power dissipated is:

$$P_{D(MAX)} = \left(\frac{t_{BLANK}}{t_{RESTART} + t_{BLANK}}\right) \times V_{IN(MAX)} \times I_{LIM(MAX)} \quad (4)$$

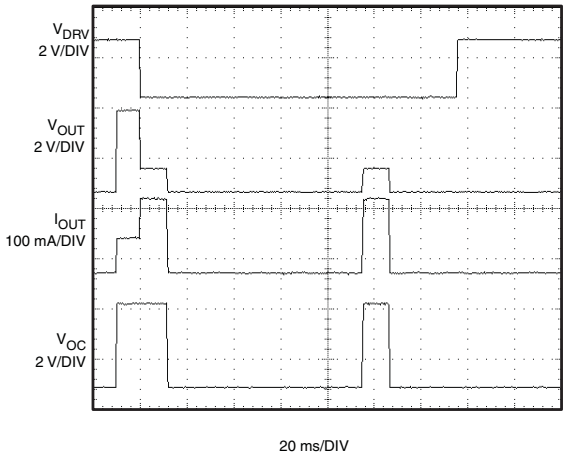
When using the TPS22943 and TPS22944, a short on the output causes the part to operate in a constant current state, dissipating a worst-case power as calculated above until the thermal shutdown activates. It then cycles in and out of thermal shutdown so long as the ON pin is active and the short is present.

9.2.2.4 Application Curves



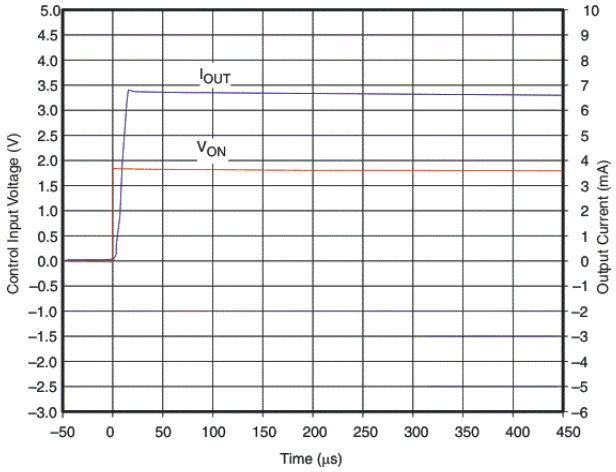
V_{DRV} signal forces the device to go into over-current mode.

Figure 20. t_{BLANK} Response



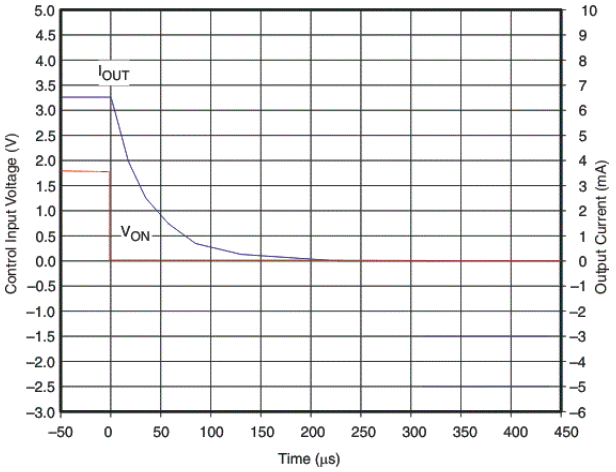
V_{DRV} signal forces the device to go into over-current mode.

Figure 21. $t_{RESTART}$ Response



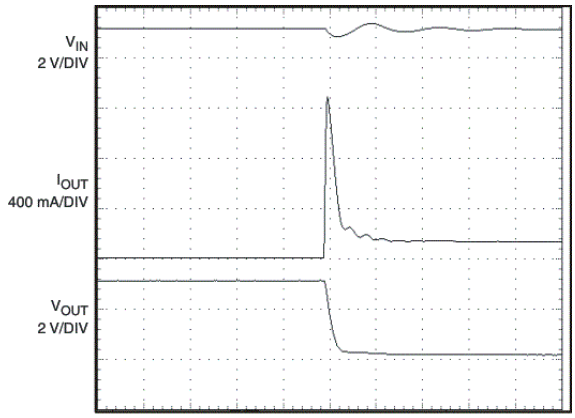
C_L = 0.1 µF R_L = 500 Ω V_{IN} = 3.3 V

Figure 22. t_{ON} Response



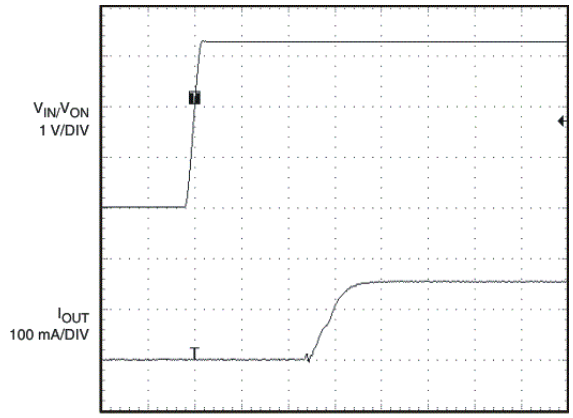
C_L = 0.1 µF R_L = 500 Ω V_{IN} = 3.3 V

Figure 23. t_{ON} Response



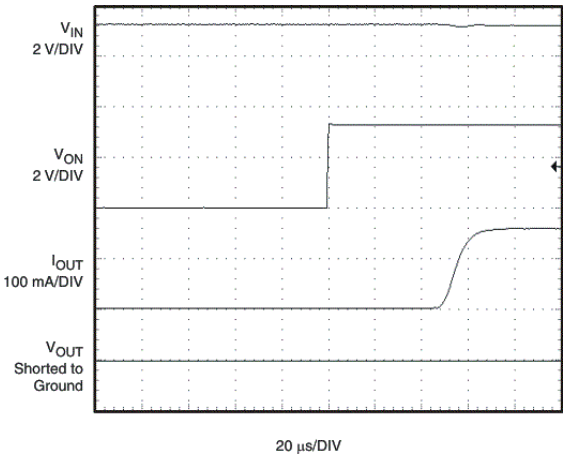
C_{IN} = 10 µF C_{OUT} = 1 µF

Figure 24. Short-Circuit Response Time (Output Shorted to Ground)



C_{IN} = 10 µF C_{OUT} = 1 µF

Figure 25. Short-Circuit Response Time (Switch Powerup to Hard Short)



C_{IN} = 10 µF C_{OUT} = 1 µF

Figure 26. Current Limit Response Time

10 Power Supply Recommendations

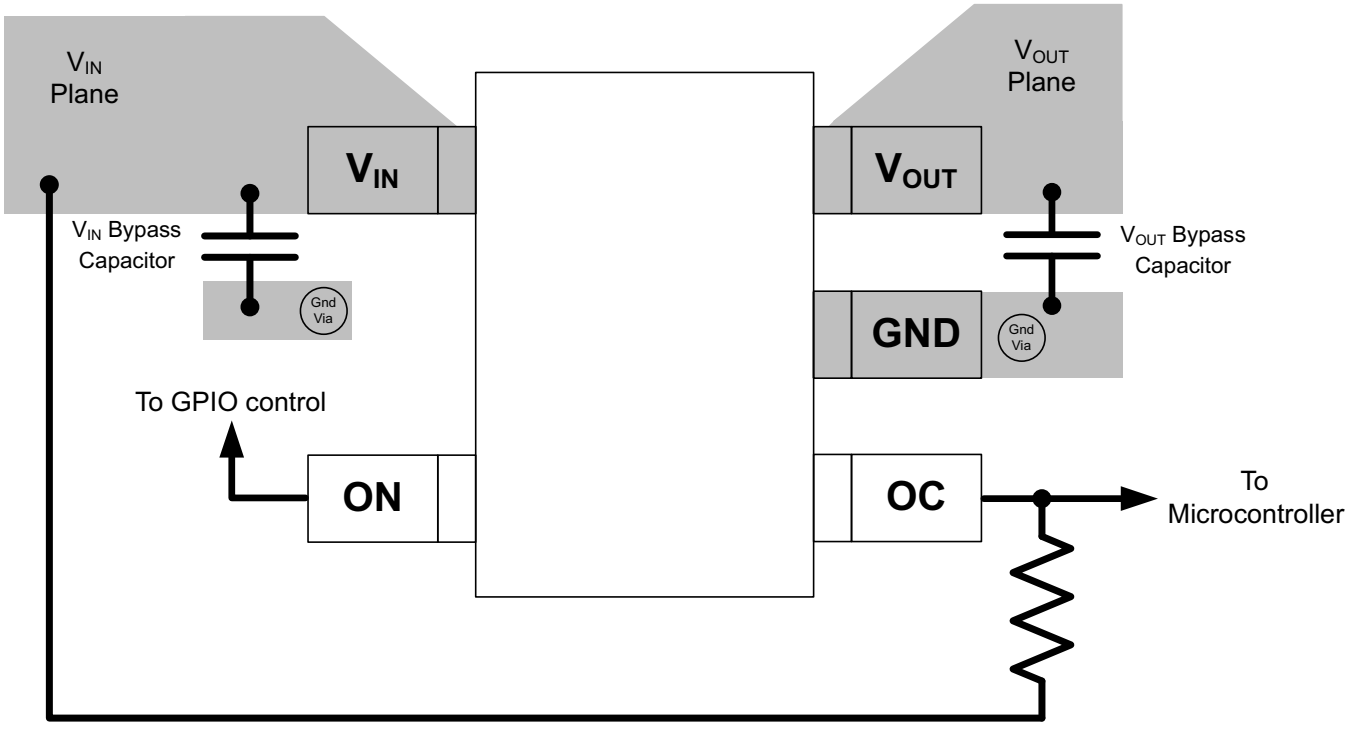
The device is designed to operate from a V_{IN} range of 1.62-V to 5.5-V. This supply must be well regulated and placed as close to the device terminal as possible with the recommended 1µF bypass capacitor. If the supply is located more than a few inches from the device terminals, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 10-µF may be sufficient.

11 Layout

11.1 Layout Guidelines

- For best performance, all traces should be as short as possible.
- To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal and short-circuit operation.
- The V_{IN} terminal should be bypassed to grond with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 1-µF ceramic with X5R or X7R dielectric. This capacitor should be placed as close to the device terminals as possible.
- The V_{OUT} terminal should be bypassed to grond with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is one-tenth of the VIN bypass capacitor of X5R or X7R dielectric. This capacitor should be placed as close to the device terminals as possible.
- Using wide traces for V_{IN}, V_{OUT}, and GND will help minimize parasitic electrical effects along with minimizing the case to ambient thermal impedance.

11.2 Layout Example



11.3 Thermal Considerations

The maximum junction temperature will be internally limited by the thermal shutdown (T_{SD}). To calculate the maximum allowable dissipation, $P_{D(MAX)}$ for a given ambient temperature, use Equation 5.

$$P_{D(MAX)} = \frac{T_{SD} - T_A}{\theta_{JA}} \quad (5)$$

where:

- $P_{D(MAX)}$ = maximum allowable power dissipation
- T_{SD} = thermal shutdown threshold (140 °C typical)
- T_A = ambient temperature of the device
- θ_{JA} = junction to air thermal impedance. See the section. This parameter is highly dependent upon board layout.

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS22941	Click here	Click here	Click here	Click here	Click here
TPS22942	Click here	Click here	Click here	Click here	Click here
TPS22943	Click here	Click here	Click here	Click here	Click here
TPS22944	Click here	Click here	Click here	Click here	Click here
TPS22945	Click here	Click here	Click here	Click here	Click here

12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS22941DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4AN
TPS22942DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(4BJ, 4BN)
TPS22943DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4CN
TPS22944DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4DN
TPS22945DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(4EJ, 4EN)

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

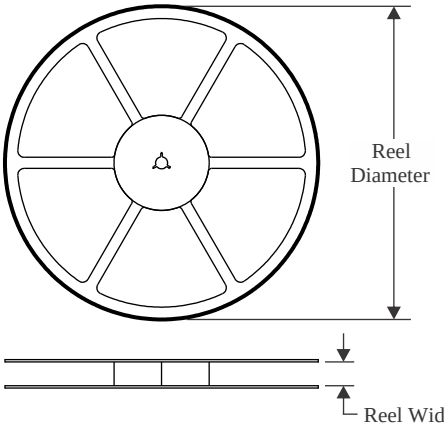
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

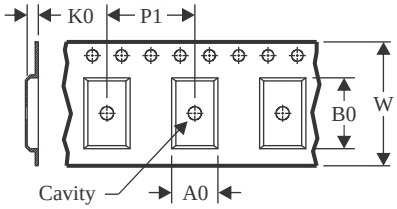
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

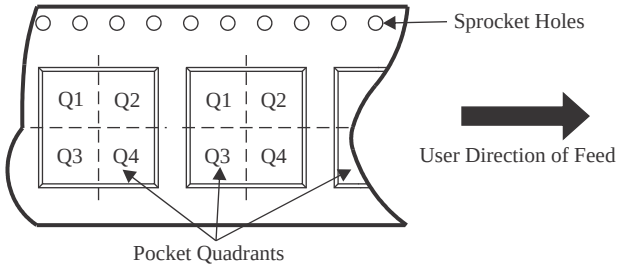


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

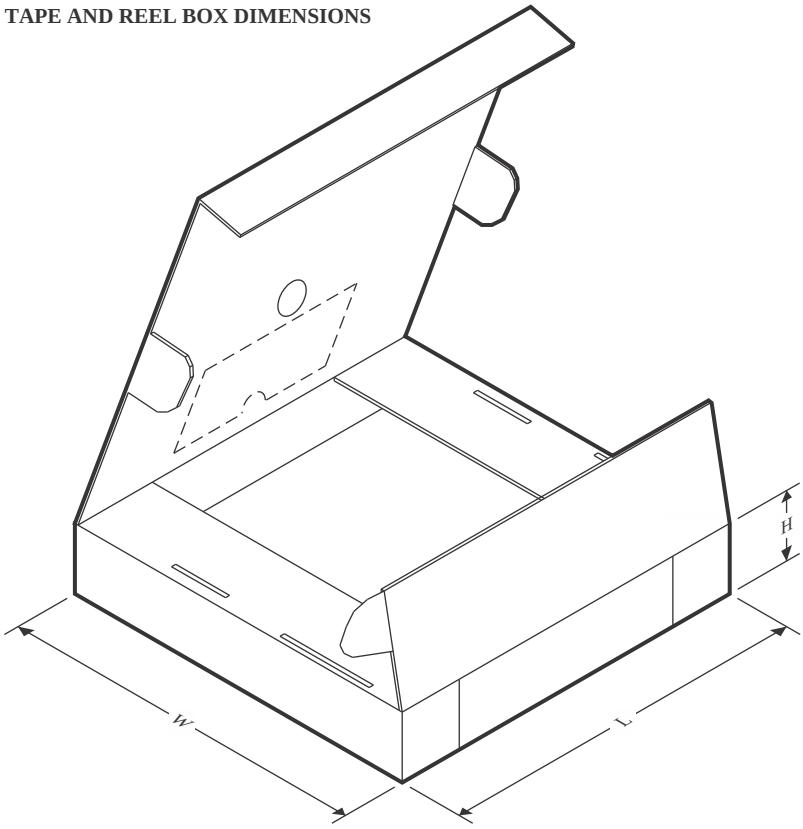
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22941DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
TPS22942DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
TPS22942DCKR	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TPS22943DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
TPS22944DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
TPS22945DCKR	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TPS22945DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

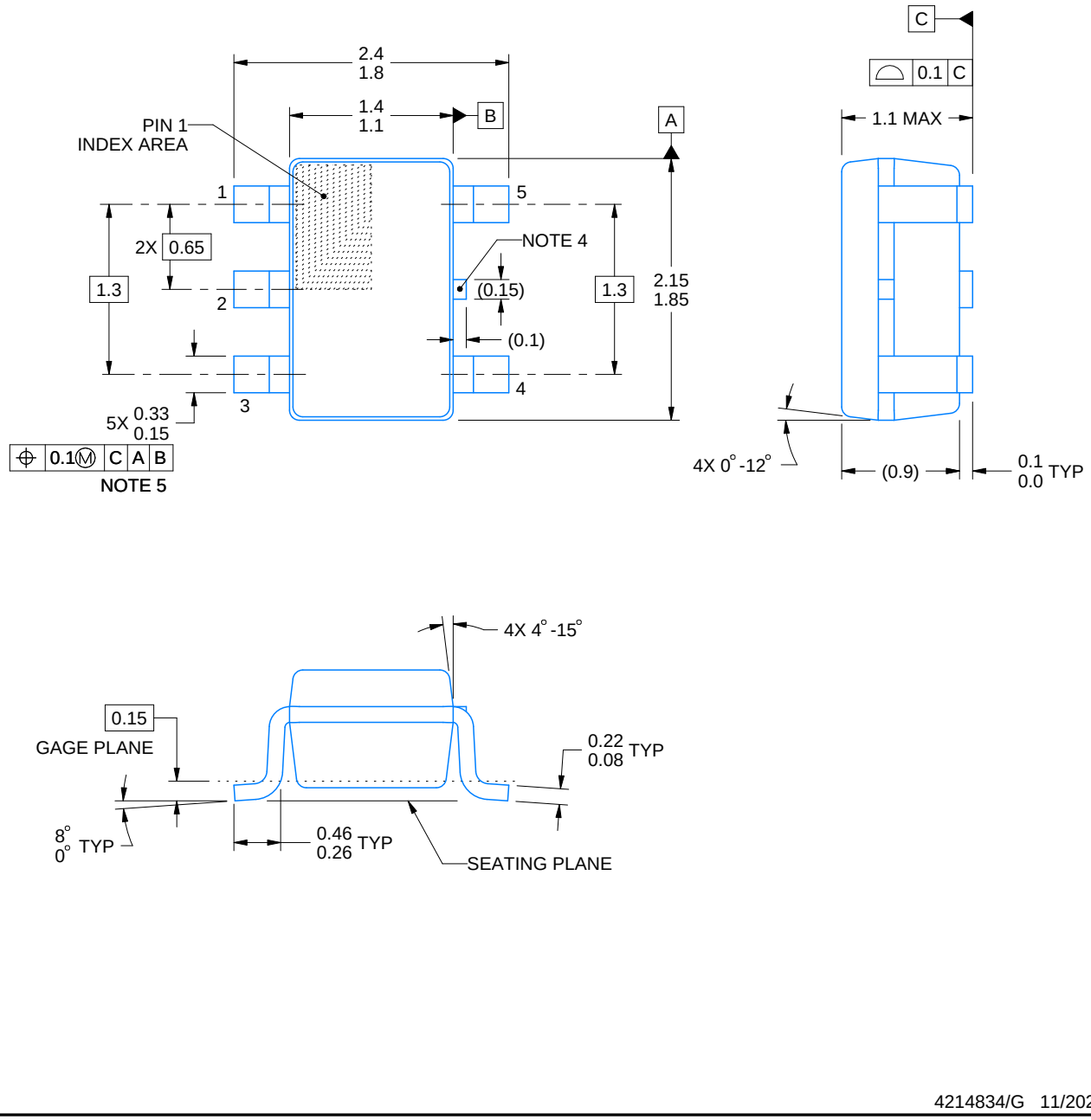
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22941DCKR	SC70	DCK	5	3000	205.0	200.0	33.0
TPS22942DCKR	SC70	DCK	5	3000	205.0	200.0	33.0
TPS22942DCKR	SC70	DCK	5	3000	203.0	203.0	35.0
TPS22943DCKR	SC70	DCK	5	3000	205.0	200.0	33.0
TPS22944DCKR	SC70	DCK	5	3000	205.0	200.0	33.0
TPS22945DCKR	SC70	DCK	5	3000	200.0	183.0	25.0
TPS22945DCKR	SC70	DCK	5	3000	205.0	200.0	33.0

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

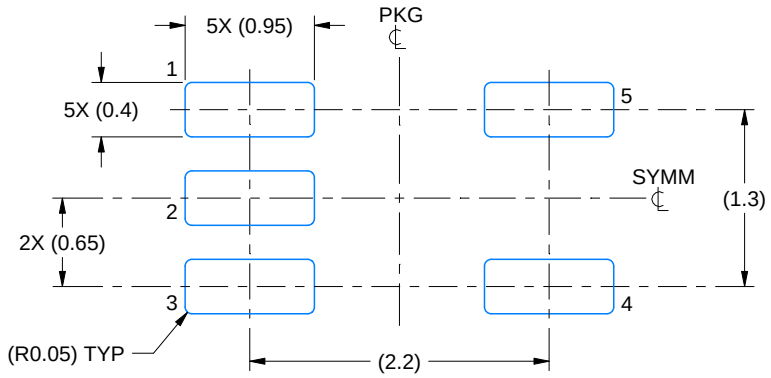
SMALL OUTLINE TRANSISTOR



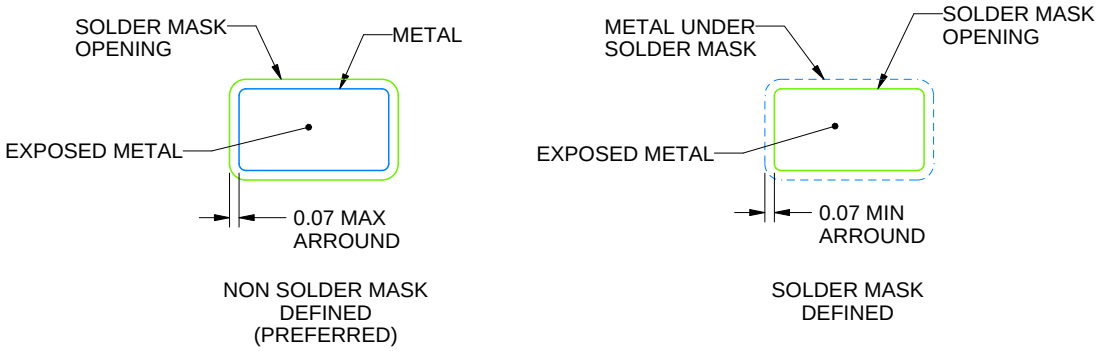
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

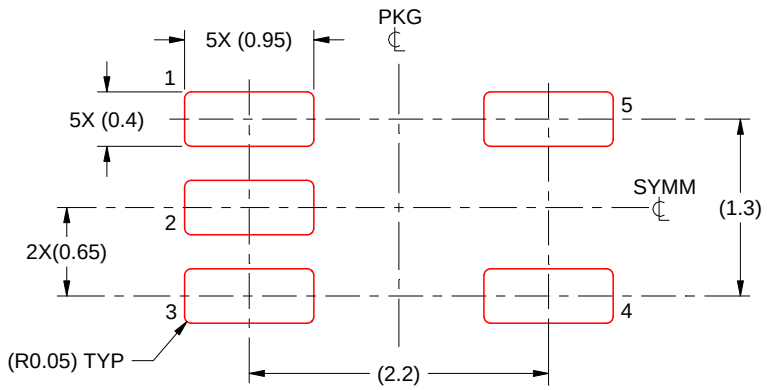


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265