60-V 3.5-A Step-Down DC/DC Converter

Features

- High Efficiency at Light Loads with Pulse Skipping
- 80-mΩ High-Side MOSFET
- 160-μA Operating Quiescent Current and 2.25-μA Shutdown Current
- 100-kHz to 2.5-MHz Adjustable Switching Frequency
- Integrated PLL to Synchronize with External Clock
- Adjustable UVLO Voltage and Hysteresis
- Soft-Start and Sequencing
- 0.8-V 1.5% Internal Voltage Reference
- 8-Pin ESOP8 with Exposed Pad Package
- –40°C to 125°C Operation Ambient Temperature Range

Applications

- 12-V, 24-V, 48-V Industrial Power Application
- Telecom & Communication Equipment Power Applications

Description

The TPP60308 is a 60-V, 3.5-A output, non-synchronous, step-down, and switch-mode converter with integrated high-side power MOSFET.

The TPP60308 employs current-mode control supporting simple external compensation and flexible component selection. It also supports low quiescent current mode with pulse-skipping and ultra-low sleep current.

With the integrated phase-locked loop, the TPP60308 can synchronize with an external clock source with wide frequency selection, optimized for efficiency, physical dimensions, and electromagnetic interference (EMI).

Protection and diagnostic features protect the device as well as the system power supply. The soft-start feature controls the output ramping. Current limit, frequency foldback, and over-temperature protection improve system-level robustness.

Typical Application Circuit

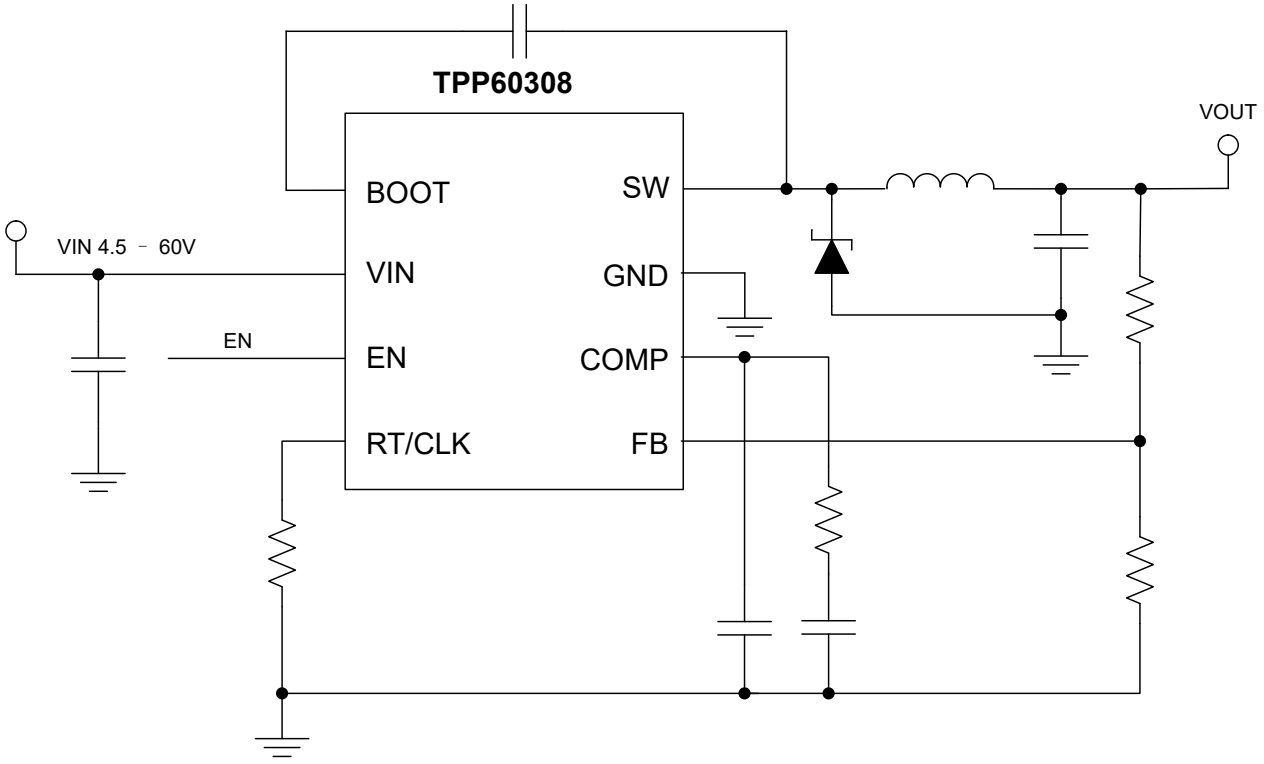


Table of Contents

Product Family Table

Order Number	Package
TPP60308-ES1R-S	ESOP8
TPP60308-ES1R	ESOP8

Revision History

Date	Revision	Notes
2023-09-26	Rev.A.0	Initial Revision
2024-10-21	Rev.A.1	Updated POD of the ESOP8 package

Pin Configuration and Functions

TPP60308
ESOP8
Top View

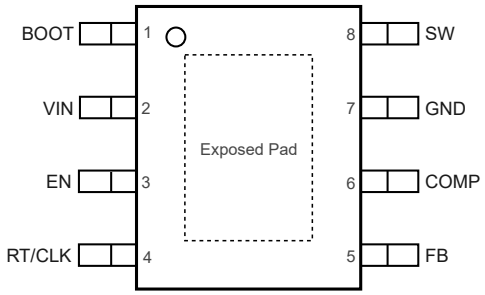


Table 1. Pin Functions: TPP60308

Pin No	Pin Name	I/O	Description
1	BOOT	I	Bootstrap capacitor between BOOT and SW, recommend using a 0.1-μF ceramic capacitor with a 10-V or higher voltage rating.
2	VIN	O	Supply voltage with 4.5-V to 60-V operating range.
3	EN	O	Device enable pin with internal pull-up current source. The threshold can be increased via external resistors.
4	RT/CLK	–	Frequency selection and external clock input. When using it as frequency setting mode, an external connected resistor sets the switching frequency; When using it as clock synchronization input, the input is a high impedance clock input for internal PLL.
5	FB	I	Feedback input, connected to internal inverting input of gm error amplifier.
6	COMP	I/O	Error amplifier output and input to the PWM comparator, Connect frequency compensation network to this pin.
7	GND	G	Device ground pin.
8	SW	O	Switching output.
	Exposed Pad	G	Device exposed pad, must be connected to GND with heat sink area for thermal dissipation.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
VIN	Supply Voltage	−0.3	65	V
SW	Switching Node Voltage	−0.6	VIN + 0.3	V
	Switching Node Voltage, SW 5-ns Transient	−7	VIN + 0.3	V
	Switching Node Voltage, SW 10-ns Transient	−2	VIN + 0.3	V
BOOT – SW	Bootstrap Voltage	−0.3	6.5	V
FB	Feedback Voltage	−0.3	3	V
COMP	Compensation Voltage	−0.3	3	V
EN	Enable Input Voltage	−0.3	8.4	V
RT/CLK	Switching frequency setting / PLL Input	−0.3	3	V
T_J	Operating Junction Temperature Range	−40	150	°C
T_A	Ambient Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering, 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Max	Unit
V_{IN}	Power Supply Voltage	4.5	60	V
V_O	Output Voltage Range	0.8	58	V
I_O	Output Current Range	0	3.5	A
T_J	Operating Junction Temperature Range	–40	150	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
ESOP8	53.1	75.2	°C/W

Electrical Characteristics

All test conditions: V_{IN} = 4.5 V to 60 V, T_J = −40°C to 150°C, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
Power Supply						
V_{IN}	Operating Voltage Range		4.5		60	V
$V_{(UVLO)}$	Internal Under-voltage Lockout Threshold	Rising threshold	4.1	4.3	4.48	V
$V_{(UVLO,hys)}$				325		mV
I_Q	Quiescent Supply Current	EN = 5 V, T_A = 25 °C, $V_{(FB)}$ = 0.9 V		152	200	μA
I_{QSD}	Shut-down Supply Current	EN = 0 V, T_A = 25 °C		2.25	50	μA
VFB Voltage						
V_{FB}	V_{FB} Threshold Voltage		0.788	0.8	0.812	V
MOSFFET						
HS_{RDSON}	HS Switching On-Resistance	V_{IN} = 12 V, BOOT − SW = 5 V		80	185	mΩ
Current Limit						
I_{Limit}	Current Limit	Full voltage and temperature range, Open-Loop	4.5	5.5	6.8	A
		Full temperature range, V_{IN} = 12 V, Open-Loop	4.5	5.5	6.25	A
		TA = 25 °C, V_{IN} = 12 V, Open-Loop	5.2	5.5	5.85	A
Error Amplifier						
$I_{(FB)}$	Input Current			50		nA
g_m	Error Amplifier Transconductance	−2 μA < I_{COMP} < 2 μA, V_{COMP} = 1 V		350		μMhos
g_m	Error Amplifier Transconductance during Soft-Start	−2 μA < I_{COMP} < 2 μA, V_{COMP} = 1 V ， V_{FB} = 0.4 V		77		μMhos
A_{DC}	Error Amplifier Gain	$V_{(FB)}$ = 0.8 V		10000		V/V
$f_{(GBW),min}$	Minimal Unity Gain Bandwidth			2500		kHz
$I_{(COMP)}$	Error Amplifier Output Current Capability	$V_{(COMP)}$ = 1 V, 100-mV overdrive		±31		μA
$g_{COMP-SW}$	COMP to SW Current Transconductance			12		A/V
Thermal Shutdown						
T_{SD}	Thermal Shutdown Temperature			161		°C
T_{HYS}	Thermal Hysteresis			20		°C
LOGIC						
V_{EN}	EN Threshold Voltage		1.1	1.2	1.3	V

Parameter		Conditions	Min	Typ	Max	Unit
I_{EN}	EN Threshold + 50 mV			−4.6		μA
	EN Threshold −50 mV		−0.58	−1.2	−1.8	μA
$I_{EN,hys}$	EN Threshold Hysteresis		−2.2	−3.4	−4.5	μA
$V_{th(RT/CLK),rising}$	RT/CLK Rising Threshold			1.55	2	V
$V_{th(RT/CLK),falling}$	RT/CLK Falling Threshold		0.5	1.2		V
Timing Characteristics						
t_{OCP}	Over-Current Protection Delay			60		ns
$t_{d,EN}$	Enable to COMP Delay			540		μs
t_{ss}	Soft-start Timer	f_{SW} = 500 kHz		2		ms
$t_{CLK,min}$	Minimal CLK Input Pulse Width			15		ns
$t_{d,CLK}$	RT/CLK Falling Edge to SW Rising Edge Delay	f_{SW}= 500 kHz		55		ns
f_{SW}	Switching Frequency	R_T = 200 kΩ	450	500	550	kHz
	Switching Frequency using RT Mode		100		2500	kHz
	Switching Frequency using CLK Mode		160		2300	kHz
D_{MAX}	Maximum Duty Cycle			99.9%		
t_{PLL}	PLL Lock in Time	f_{SW} = 500 kHz		78		μs

Typical Performance Characteristics

All test conditions: V_{IN} = 12 V, T_A = 25°C, unless otherwise noted.

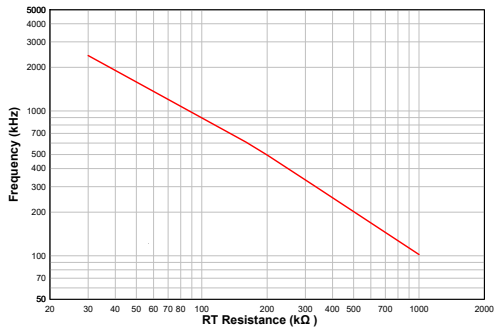


Figure 1. Frequency vs RT Resistance

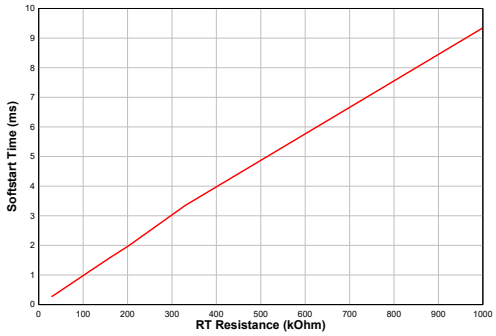


Figure 2. Soft-Start Time vs. RT Resistance

f = 500 kHz, C_L = 500 pF, V_{IN} = 12 V

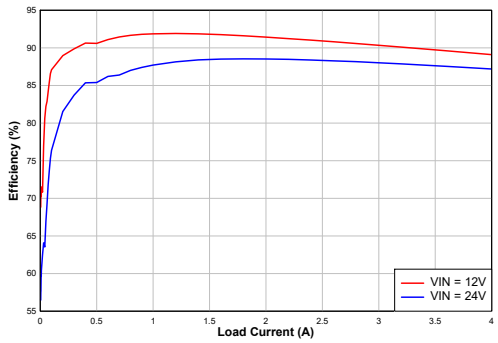


Figure 3. Efficiency vs. Load Current

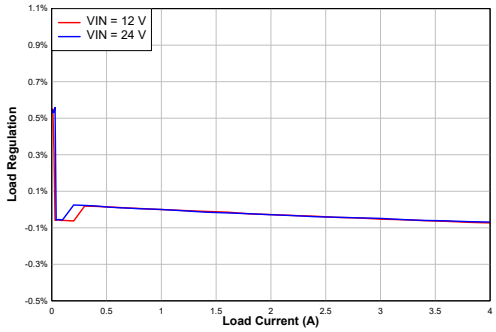


Figure 4. Load Regulation

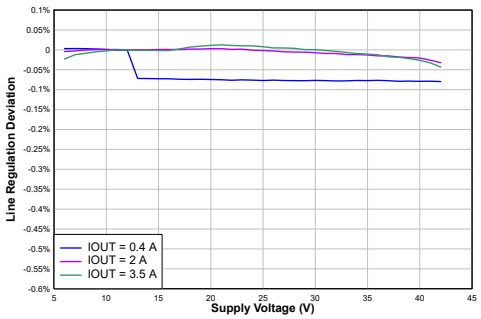


Figure 5. Line Regulation

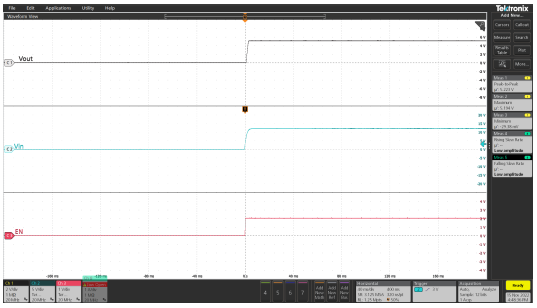


Figure 6. Power Up, No Load

I_{OUT} = 0 A

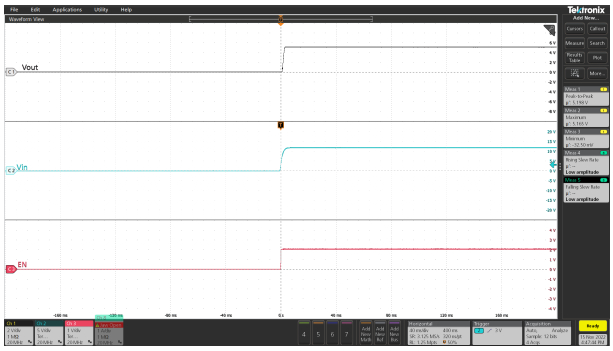


Figure 7. Power Up, Full Load

I_{OUT} = 3.5 A

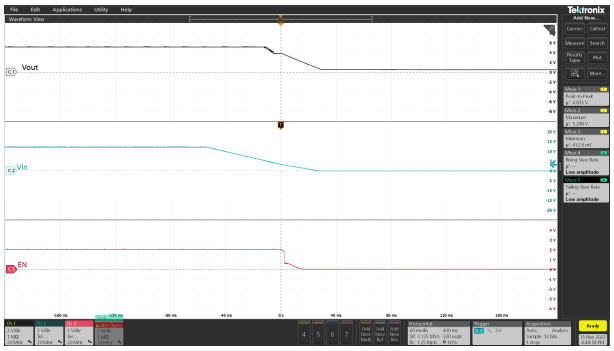


Figure 8. Power Down, No Load

I_{OUT} = 0 A

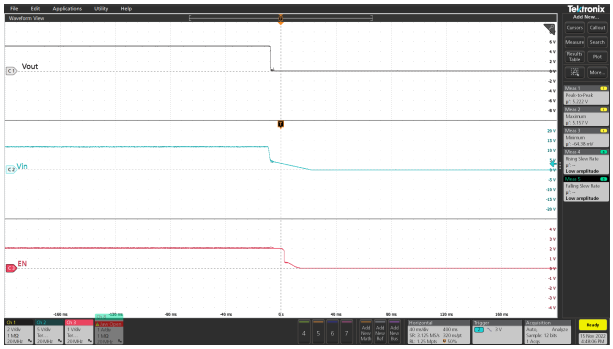


Figure 9. Power Down, Full Load

I_{OUT} = 3.5 A

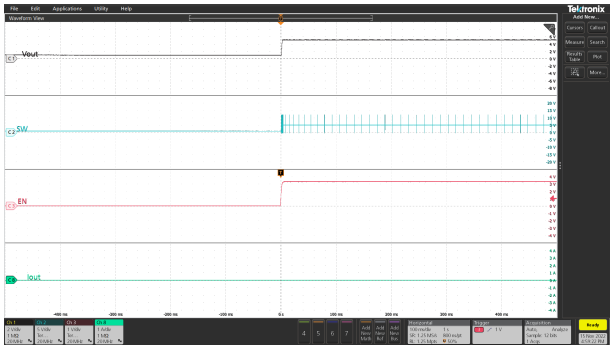


Figure 10. Power Up by EN, No Load

I_{OUT} = 0 A

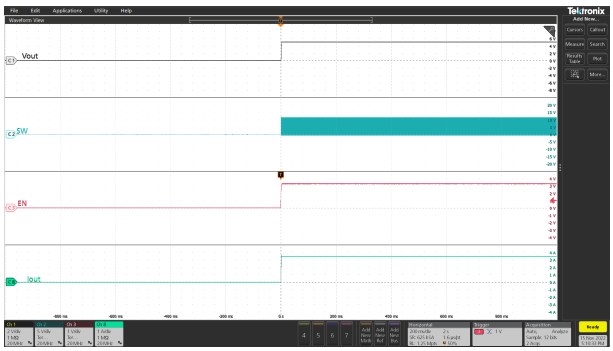


Figure 11. Power Up by EN, Full Load

I_{OUT} = 3.5 A

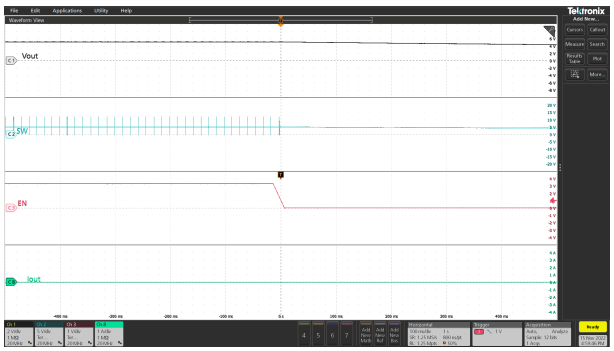


Figure 12. Power Down by EN, No Load

I_{OUT} = 0 A

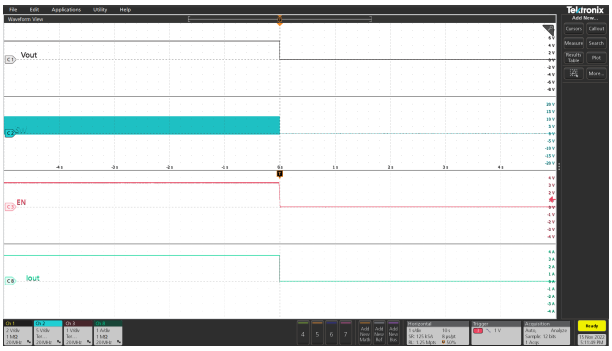


Figure 13. Power Down by EN, Full Load

I_{OUT} = 3.5 A

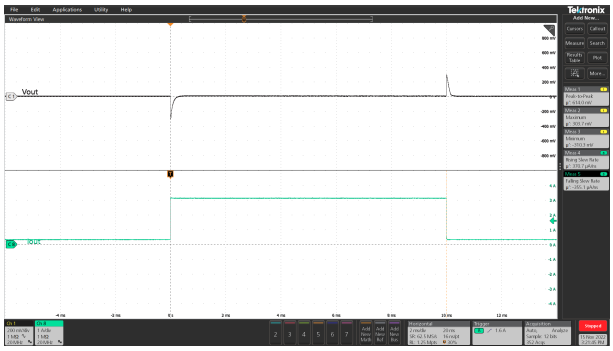


Figure 14. Load Transient

I_{OUT} = 0.35 A to 3.5 A to 0.35 A

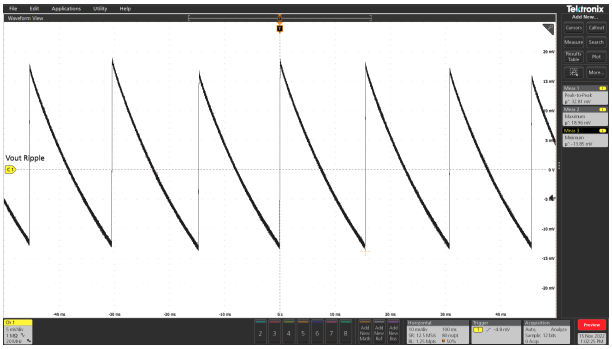


Figure 15. Ripple Voltage, 0 A

I_{OUT} = 0 A

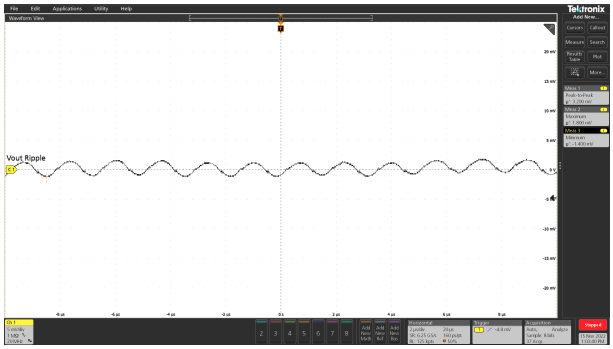


Figure 16. Ripple Voltage, 0.35 A

I_{OUT} = 0.35 A

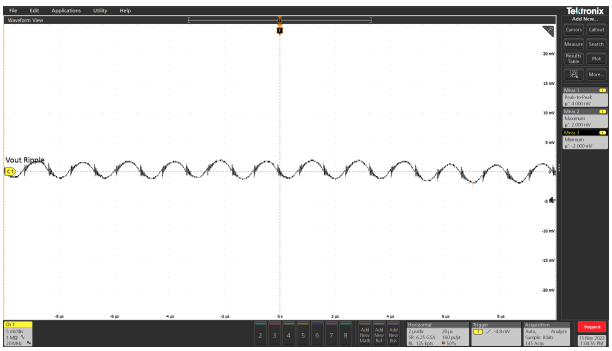


Figure 17. Ripple Voltage, 3.5 A

I_{OUT} = 3.5 A

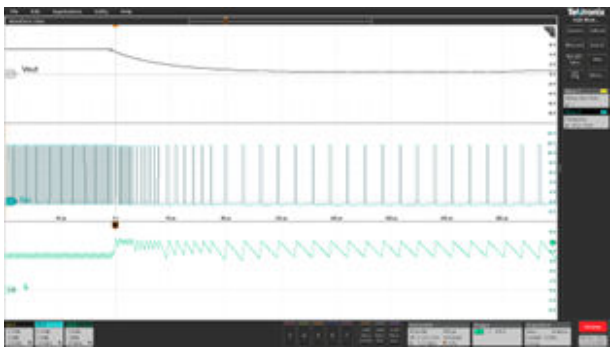


Figure 18. Short Protection

Detailed Description

Overview

The TPP60308 is a 60-V, 3.5-A output, non-synchronous, step-down, and switch-mode converter with the integrated high-side power MOSFET.

The TPP60308 employs current mode control supporting simple external compensation and flexible component selection. It also supports low quiescent current mode with pulse-skipping and ultra-low sleep current.

With the integrated phase-locked loop, it can synchronize with external clock source with wide frequency selection, optimized for efficiency, physical dimensions, and electro-magnetic interference (EMI).

Protection and diagnostics features protect the device as well as the system power supply. Soft-start features control the output ramping. Current limit, frequency foldback, and over-temperature protection improve system-level robustness.

Functional Block Diagram

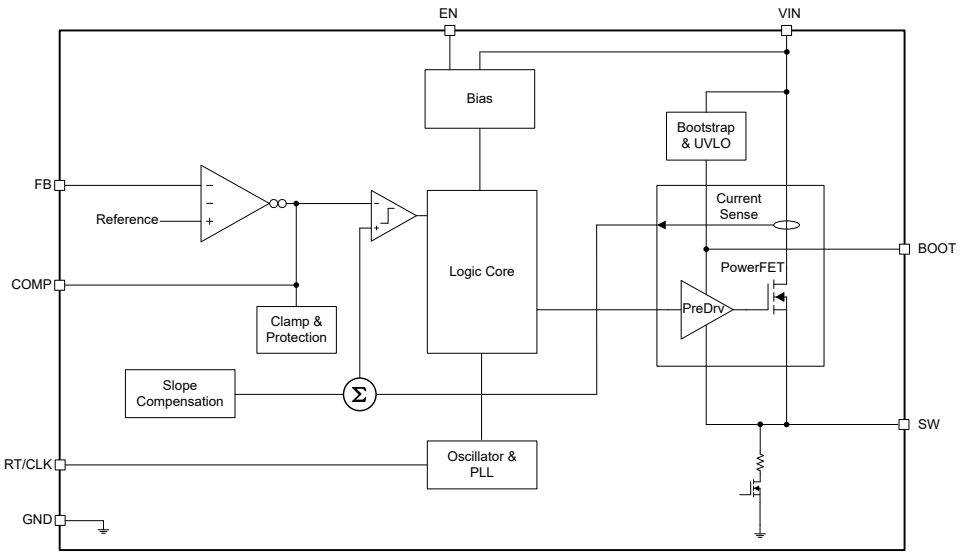


Figure 19. Functional Block Diagram

Feature Description

Fixed Frequency Peak Current Mode Control

The TPP60308 uses peak current mode control with adjustable switching frequency. The feedback voltage is sensed through the FB pin to compare with the internal voltage reference by an error amplifier. The PWM comparator compares the output of the error amplifier with an internal voltage ramp and controls the high-side power switch. The internal oscillator controls the frequency of switching high-side MOSFET.

The high-side switching current is sensed internally as part of the voltage ramp. The internal voltage ramp compensates the control loop from sub-harmonic oscillations when duty cycles are greater than 50%. Once the PWM comparator detects peak switching current reaches the threshold level set by the COMP voltage, the high-side MOSFET is switched off. The COMP pin is also clamped for current limiting and pulse-skipping mode.

The transconductance error amplifier converts the error voltage between the FB pin voltage and the internal voltage, whichever is lower than the soft-start voltage or internal voltage reference V_{FB}, to current with transconductance gm of 350 μMhos during normal operation conditions. During soft-start operation, transconductance is reduced to ensure smooth soft-start. It is recommended to connect the compensation network between the COMP pin and the GND pin to ensure stability across all working ranges. The details are discussed in the application chapter.

Setting Output Voltage

The precision internal voltage reference produces a 0.8-V voltage reference with ±1.5% tolerance across operating temperature and voltage ranges. The resistor divider from the output voltage to the FB pin sets the output voltage.

$$R_H = R_L \times \left(\frac{V_{OUT} - V_{FB}}{V_{FB}} \right) \quad (1)$$

Pulse-Skipping Light-Load Operation

The TPP60308 enters pulse-skipping operation when the peak switching current is below the internal threshold. In the pulse-skipping mode, the device clamps COMP at 0.6 V and stops switching high-side MOSFET. The error amplifier output increases as the output voltage falls and the differential input voltage increases. When the COMP voltage rises above the pulse-skipping threshold, the device resumes switching the high-side MOSFET.

The current threshold is equivalent to the current of a nominal COMP voltage at 1 V. As the device uses peak switching current for the pulse-skipping threshold, the threshold is also dependent on the output inductance.

Soft-Start with Pre-Biased Capability

The device has a soft-start feature by controlling ramping up reference voltage. The timing of soft-start is set internally and can be programmed via RT resistance.

$$t_{ss} = k_{ss} \cdot R_{RT} \quad (2)$$

$k_{ss}=10^{-8}$

RT/CLK

The device supports a wide switching frequency range from 100 kHz to 2500 kHz. The frequency is programmable via a resistor connected between RT/CLK and GND. The switching frequency will affect solution size, efficiency, and minimal duty cycle. It is suggested that all factors be taken care of when selecting switching frequency. The resistor can be calculated via the following equation:

$$f = \frac{k}{R_{RT}} \quad (3)$$

$k=10^{11}$

The device switching clock supports external clock sources for synchronization. Once a square wave is applied at the RT/CLK pin, the rising edge of SW synchronizes with the falling edge of RT/CLK. It is also suggested to connect a frequency set resistor to the RT/CLK pin in case the external clock source is not available.

The first rising edge of RT/CLK sets the device from free-running frequency mode to synchronization mode. The internal 0.5-V voltage source is removed and the RT/CLK is set to the high impedance mode. It takes 78 μs to lock on external clock frequency. When the external clock source stops, the device will switch back to the free-running frequency mode with a frequency set by the external resistor. During the transition, the device frequency will stay at 70 kHz and then switch to the free-running frequency.

The device will foldback frequency by 1, 2, 4, and 8 depending on the FB voltage. This is to ensure that during normal start-up and fault conditions, the device is able to increase its period and off time. This is helpful when output is short-circuit to GND, the longer off time allows the inductor current to decay.

Protection

Undervoltage Lockout (UVLO)

The device has a undervoltage lockout feature with a default rising threshold of 4.3 V. It can be adjusted by using the EN pin with external resistors. A weak current source of 1.2 μA pulls up the EN pin to the internal voltage rail. Another 3.4-μA hysteresis current source provides the hysteresis voltage between the rising and falling threshold. The resistor values can be calculated via the below equations.

$V_{SYS\_UVLO\_H}$ is the desired system-level undervoltage protection rising threshold voltage, $V_{SYS\_UVLO\_L}$ is the desired system-level undervoltage protection falling threshold voltage. RUVLOH and RUVLOL are depicted in the Figure 8.

$$R_{UVLOH} = \frac{V_{SYS\_UVLO\_H} - V_{SYS\_UVLO\_L}}{I_{EN\_hys}} \quad (4)$$

$$R_{UVLOL} = \frac{V_{EN}}{\frac{V_{SYS\_UVLO\_H} - V_{EN}}{R_{UVLOH}} + I_{EN}} \quad (5)$$

Over-Current Protection

The device employs peak current mode control by controlling the peak current of the internal high-side power transistor. The high-side transistor current is converted to a voltage signal and compared to the COMP pin. When the peak switching current is above the threshold set by the COMP voltage, the device turns off the high-side power transistor.

When the device is in the over-current scenario, the output voltage is pulled low, and the device increases the switching current threshold until it reaches the internal current limit threshold. Once the switching current is above the threshold, the device will turn off the transistor as the current limit. Delay needs to be taken into account that may cause the peak inductor current slightly higher than the open-loop current limit.

Once the over-current load is removed, the device will resume normal operation in the following cycle.

Over-Voltage Protection

The device stops high-side FET switching when it detects the FB voltage is above the over-voltage protection (OVP) rising threshold (108% of internal reference voltage). When the voltage falls below the falling threshold (106% of internal reference voltage), it resumes switching high-side FET. With the OVP feature, the device is able to minimize the voltage overshoot during the load transient with low-output capacitance.

Over-Temperature Shutdown

When the device senses the junction temperature is above the internal rising threshold of 161°C, the device stops the high-side FET switching. Once the device junction temperature falls below the falling threshold of 141°C, the device restarts the device with a power-up sequence.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPP60308 is a non-synchronous 60-V 3.5-A step-down regulator with the integrated high-side FET. The device is capable of supporting a wide range of voltage rails including 12 V, 24 V, and 48 V. It is widely used in communication, industrial, and automotive applications.

Typical Application

Figure 20 shows the typical application schematic.

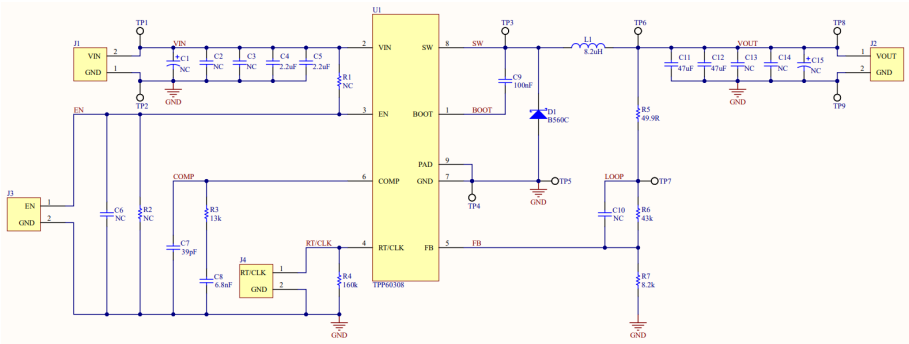


Figure 20. Typical Application Circuit

Table 2. TPP60308 Bill of Material

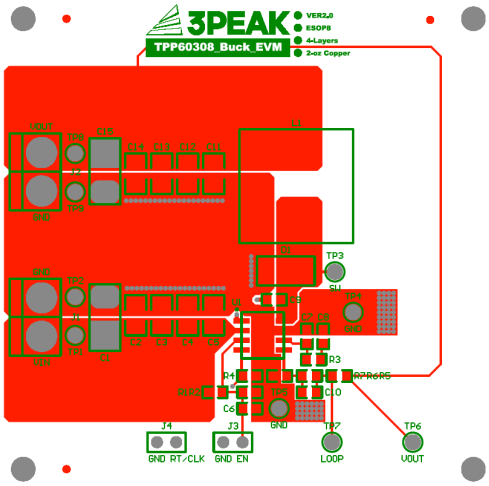
RefDes	Value	Description	Package	MFR	Part No.	Qty
U1		Buck Converter, 60V, 3.5A, low Iq	ESOP8	3PEAK	TPP60308-ES1R-S	1
C1	NC					0
C2	NC					0
C3	NC					0
C4	2.2uF	Capacitor, 2.2uF, 100VDC, X7R, ±10%	1210	muRata	C3225X7R2A225KT5LOU	1
C5	2.2uF	Capacitor, 2.2uF, 100VDC, X7R, ±10%	1210	muRata	C3225X7R2A225KT5LOU	1

RefDes	Value	Description	Package	MFR	Part No.	Qty
R1	NC					0
R2	NC					0
C3	NC					0
C7	39pF	Capacitor, 39F, 50VDC, X7R, ±5%	0603	muRata	GRM1881X1H390JA01	1
R3	13K	Resistor ,13K, ±1%,0.1W	0603	Viking	ARG03FTC1302	1
C8	6.8F	Capacitor, 6.8nF, 50VDC, X7R, ±5%	0603	muRata	GRM1881X1H390JA01	1
R4	160K	Resistor ,160K, ±1%,0.1W	0603	Viking	ARG03FTC1603	1
C9	100nF	Capacitor, 100nF, 50VDC, X7R, ±15%	0805	muRata	GGD21BR71H104KA02	1
D1	diode	60V,7A ,0.62V@5A	POWERDI-5	DIODES	PDS760-13	1
L1	8.2uH	8.2uH,19.11mΩ,7.2A Rated，12.8A Satueeted	15×3×15mm	Wurth	7448880820	1
R5	49.9R	Resistor, 49.9Ω, ±1%, 0.1W	0603	Viking	ARG03FTC49R9	1
C10	NC					0
R6	43K	Resistor, 43K, ±1%, 0.1W	0603	Viking	ARG03FTC4302	1
R7	8.2K	Resistor, 8.2K, ±1%, 0.1W	0603	Viking	ARG03FTC8201	1
C11	47uF	Capacitor, 47uF, 10VDC, X7S, ±10%	1210	muRata	GCM32EC71A476KE02	1
C12	47uF	Capacitor, 47uF, 10VDC, X7S, ±10%	1210	muRata	GCM32EC71A476KE02	1
C13	NC					0
C14	NC					0
C15	NC					0

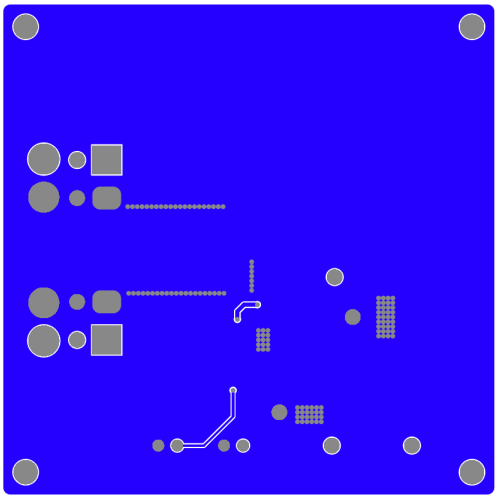
Layout

Layout Example

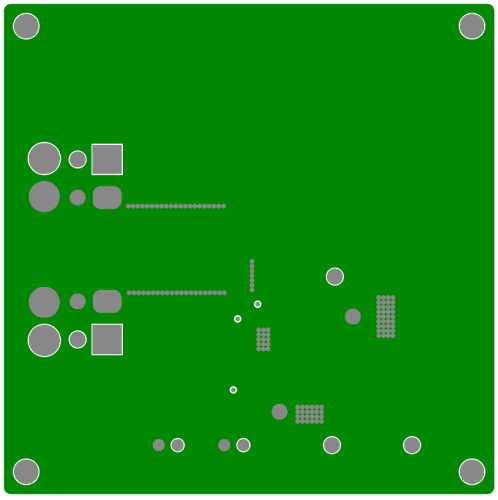
The following figures show the location of external components as they appear on the PCB.diagram.



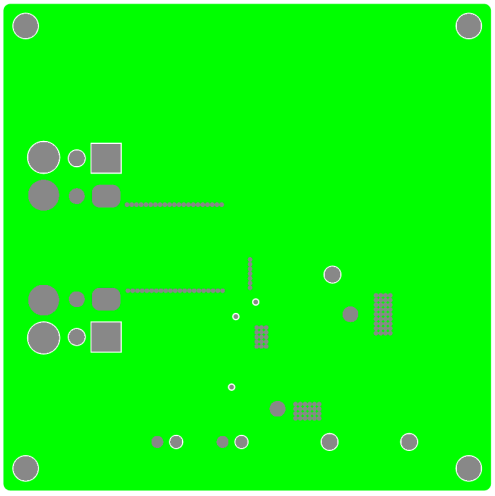
Layer top



Layer Bottom

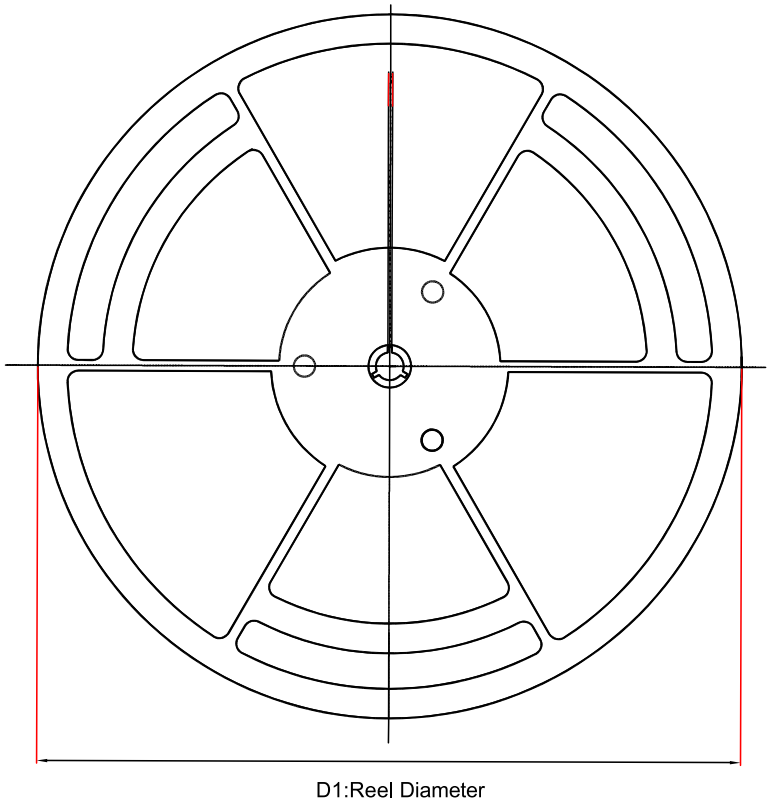


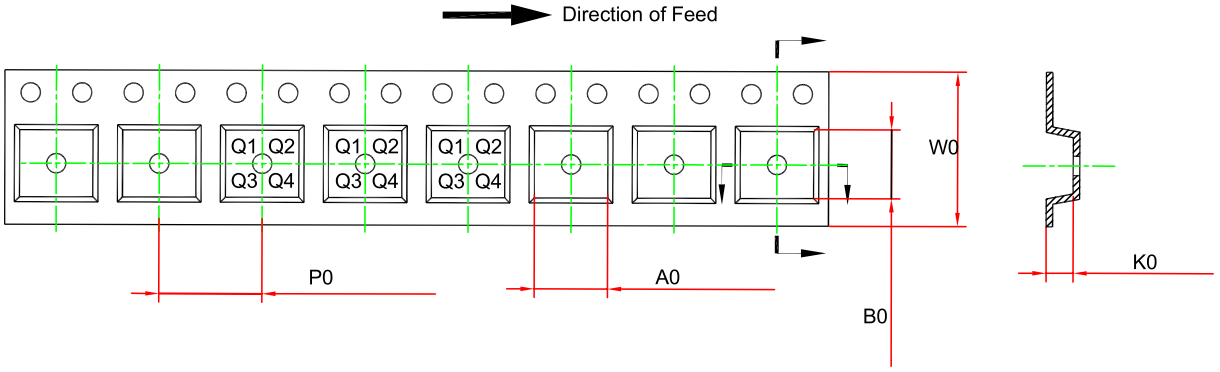
Layer M1



Layer M2

Tape and Reel Information



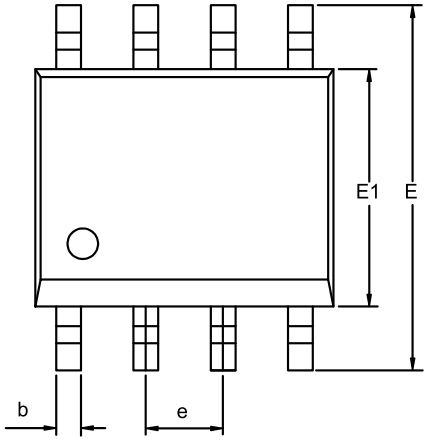


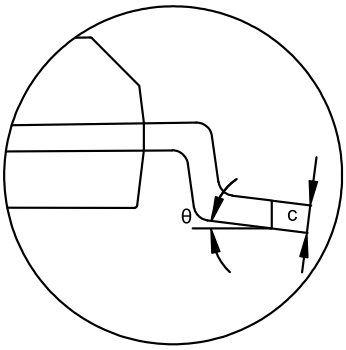
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPP60308-ES1R-S	ESOP8	330	17.6	6.4	5.4	2.1	8.0	12	Q1
TPP60308-ES1R	ESOP8	330	17.6	6.4	5.4	2.1	8.0	12	Q1

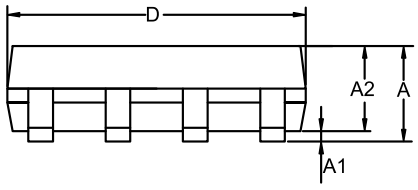
Package Outline Dimensions

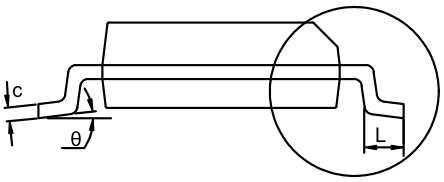
ESOP8

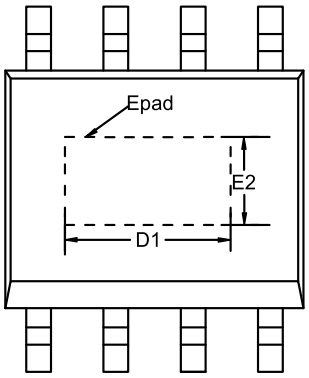
Package Outline Dimensions ES1(ESOP-8-F)











Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.300	1.700	0.051	0.067
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
D1	2.850	3.250	0.112	0.128
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
E2	1.950	2.360	0.077	0.093
e	1.270 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Ambient Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPP60308-ES1R-S	−40°C to 125°C	ESOP8	638	Level 2	Tape & Reel, 4000	Green
TPP60308-ES1R	−40°C to 125°C	ESOP8	638	Level 2	Tape & Reel, 4000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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