

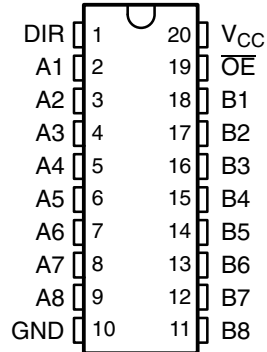
# SN74LVT245B

## 3.3-V ABT OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

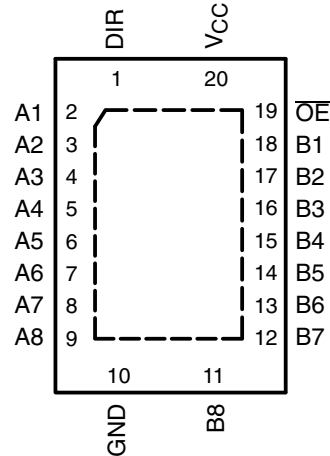
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- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- $I_{off}$  and Power-Up 3-State Support Hot Insertion
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

DB, DW, NS, OR PW PACKAGE  
(TOP VIEW)



RGY PACKAGE  
(TOP VIEW)



### description/ordering information

This octal bus transceiver is designed specifically for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

The SN74LVT245B is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so the buses are effectively isolated.

### ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Tape and reel	SN74LVT245BRGYR	LX245B
	SOIC – DW	Tube	SN74LVT245BDW	LVT245B
		Tape and reel	SN74LVT245BDWR	
	SOP – NS	Tape and reel	SN74LVT245BNSR	LVT245B
	SSOP – DB	Tape and reel	SN74LVT245BDBR	LX245B
	TSSOP – PW	Tube	SN74LVT245BPW	LX245B
		Tape and reel	SN74LVT245BPWR	
	VFBGA – GQN	Tape and reel	SN74LVT245BGQNR	LX245B
	VFBGA – ZQN (Pb-free)		SN74LVT245BZQNR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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# SN74LVT245B 3.3-V ABT OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

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## description/ordering information (continued)

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

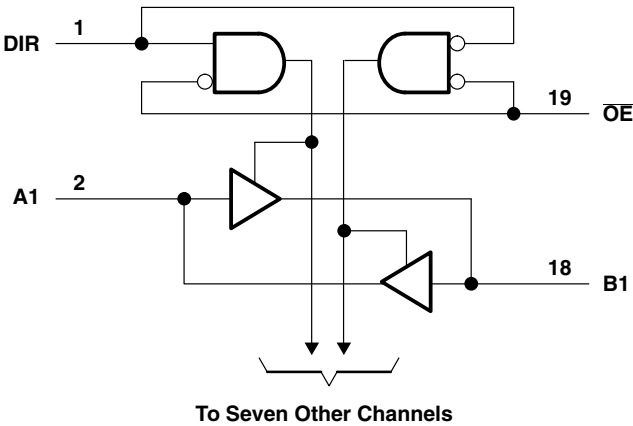
**GQN OR ZQN PACKAGE  
(TOP VIEW)**

**terminal assignments**

	1	2	3	4
A	A1	DIR	$V_{CC}$	$\overline{OE}$
B	A3	B2	A2	B1
C	A5	A4	B4	B3
D	A7	B6	A6	B5
E	GND	A8	B8	B7

FUNCTION TABLE		
INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

## logic diagram (positive logic)



Pin numbers shown are for the DB, DW, NS, PW, and RGY packages.

# SN74LVT245B

## 3.3-V ABT OCTAL BUS TRANSCEIVER

### WITH 3-STATE OUTPUTS

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, $I_O$	128 mA
Current into any output in the high state, $I_O$ (see Note 2)	64 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DB package	70°C/W
(see Note 3): DW package	58°C/W
(see Note 3): GQN/ZQN package	78°C/W
(see Note 3): NS package	60°C/W
(see Note 3): PW package	83°C/W
(see Note 4): RGY package	37°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .
  3. The package thermal impedance is calculated in accordance with JESD 51-7.
  4. The package thermal impedance is calculated in accordance with JESD 51-5.

#### recommended operating conditions (see Note 5)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		2.7	3.6	V
V <sub>IH</sub>	High-level input voltage		2		V
V <sub>IL</sub>	Low-level input voltage			0.8	V
V <sub>I</sub>	Input voltage			5.5	V
I <sub>OH</sub>	High-level output current			−32	mA
I <sub>OL</sub>	Low-level output current			64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10	ns/V
Δt/ΔV <sub>CC</sub>	Power-up ramp rate		200		μs/V
T <sub>A</sub>	Operating free-air temperature		−40	85	°C

NOTE 5: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



# SN74LVT245B

## 3.3-V ABT OCTAL BUS TRANSCEIVER

### WITH 3-STATE OUTPUTS

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{IK}$		$V_{CC} = 2.7\text{ V}$ , $I_I = -18\text{ mA}$			-1.2	V
$V_{OH}$		$V_{CC} = 2.7\text{ V to } 3.6\text{ V}$ , $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC}-0.2$			V
		$V_{CC} = 2.7\text{ V}$ , $I_{OH} = -8\text{ mA}$	2.4			
		$V_{CC} = 3\text{ V}$ , $I_{OH} = -32\text{ mA}$	2			
$V_{OL}$	$V_{CC} = 2.7\text{ V}$	$I_{OL} = 100\text{ }\mu\text{A}$			0.2	V
		$I_{OL} = 24\text{ mA}$			0.5	
	$V_{CC} = 3\text{ V}$	$I_{OL} = 16\text{ mA}$			0.4	
		$I_{OL} = 32\text{ mA}$			0.5	
		$I_{OL} = 64\text{ mA}$			0.55	
$I_I$	Control inputs	$V_{CC} = 3.6\text{ V}$ , $V_I = V_{CC}\text{ or GND}$			$\pm 1$	$\mu\text{A}$
		$V_{CC} = 0\text{ or } 3.6\text{ V}$ , $V_I = 5.5\text{ V}$			10	
	A or B ports‡	$V_{CC} = 3.6\text{ V}$ , $V_I = 5.5\text{ V}$			20	
		$V_{CC} = 3.6\text{ V}$ , $V_I = V_{CC}$			1	
		$V_{CC} = 3.6\text{ V}$ , $V_I = 0$			-5	
$I_{off}$		$V_{CC} = 0$ , $V_I\text{ or } V_O = 0\text{ to } 4.5\text{ V}$			$\pm 100$	$\mu\text{A}$
$I_{OZH}$		$V_{CC} = 3.6\text{ V}$ , $V_O = 3\text{ V}$			5	$\mu\text{A}$
$I_{OZL}$		$V_{CC} = 3.6\text{ V}$ , $V_O = 0.5\text{ V}$			-5	$\mu\text{A}$
$I_{OZPU}$		$V_{CC} = 0\text{ to } 1.5\text{ V}$ , $V_O = 0.5\text{ V to } 3\text{ V}$ , $\overline{OE} = \text{don't care}$			$\pm 100$	$\mu\text{A}$
$I_{OZPD}$		$V_{CC} = 1.5\text{ V to } 0$ , $V_O = 0.5\text{ V to } 3\text{ V}$ , $\overline{OE} = \text{don't care}$			$\pm 100$	$\mu\text{A}$
$I_{CC}$	$V_{CC} = 3.6\text{ V}$ , $I_O = 0$ , $V_I = V_{CC}\text{ or GND}$	Outputs high			0.19	mA
		Outputs low			5	
		Outputs disabled			0.19	
$\Delta I_{CC}^{\S}$		$V_{CC} = 3\text{ V to } 3.6\text{ V}$ , One input at $V_{CC} - 0.6\text{ V}$ , Other inputs at $V_{CC}\text{ or GND}$			0.2	mA
$C_i$		$V_I = 3\text{ V or } 0$		4		pF
$C_{io}$		$V_O = 3\text{ V or } 0$		9		pF

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Unused terminals are at  $V_{CC}\text{ or GND}$ .

§ This is the increase in supply current for each input that is at the specified TTL-voltage level, rather than  $V_{CC}\text{ or GND}$ .

**switching characteristics over recommended operating free-air temperature range,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$		UNIT
			MIN	TYP†	MAX	MIN	MAX	
$t_{PLH}$	A or B	B or A	1.2	2.3	3.5	4		ns
$t_{PHL}$			1.2	2.1	3.5	4		
$t_{PZH}$	$\overline{OE}$	A or B	1.3	3.2	5.5	7.1		ns
$t_{PZL}$			1.7	3.4	5.5	6.5		
$t_{PHZ}$	$\overline{OE}$	A or B	2.2	3.5	5.9	6.5		ns
$t_{PLZ}$			2.2	3.4	5	5.1		

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .



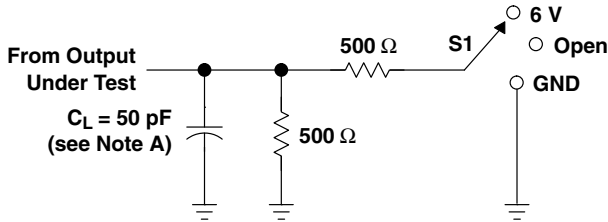
# SN74LVT245B

## 3.3-V ABT OCTAL BUS TRANSCEIVER

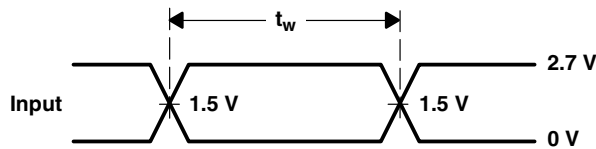
### WITH 3-STATE OUTPUTS

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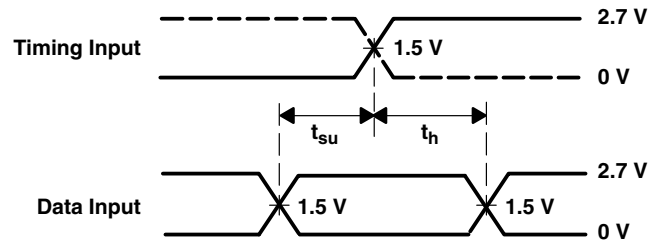
#### PARAMETER MEASUREMENT INFORMATION



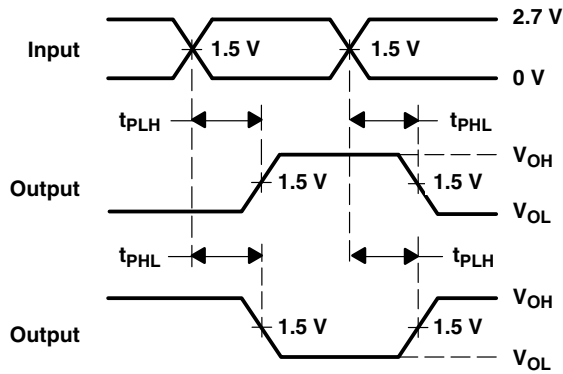
LOAD CIRCUIT



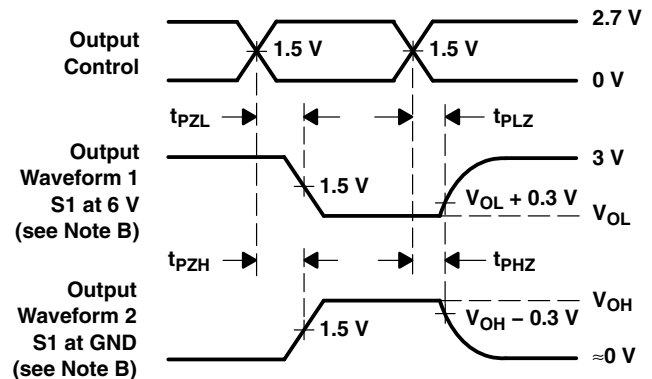
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74LVT245BDBR</a>	Active	Production	SSOP (DB)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LX245B
<a href="#">SN74LVT245BDWV</a>	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT245B
SN74LVT245BDWG4	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT245B
<a href="#">SN74LVT245BDWR</a>	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT245B
<a href="#">SN74LVT245BNSR</a>	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT245B
<a href="#">SN74LVT245BPWV</a>	Active	Production	TSSOP (PW)   20	70   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LX245B
<a href="#">SN74LVT245BPWR</a>	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LX245B
SN74LVT245BPWRG4	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LX245B
<a href="#">SN74LVT245BRGYR</a>	Active	Production	VQFN (RGY)   20	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LX245B

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVT245BDBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LVT245BDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LVT245BNSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LVT245BPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LVT245BRGYR	VQFN	RGY	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1



## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVT245BDBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74LVT245BDWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LVT245BNSR	SOP	NS	20	2000	367.0	367.0	45.0
SN74LVT245BPWR	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74LVT245BRGYR	VQFN	RGY	20	3000	356.0	356.0	35.0

## TUBE



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LVT245BDW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LVT245BDWE4	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LVT245BDWG4	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LVT245BPW	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74LVT245BPWG4	PW	TSSOP	20	70	530	10.2	3600	3.5



## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



# EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## GENERIC PACKAGE VIEW

**RGY 20**

**VQFN - 1 mm max height**

3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

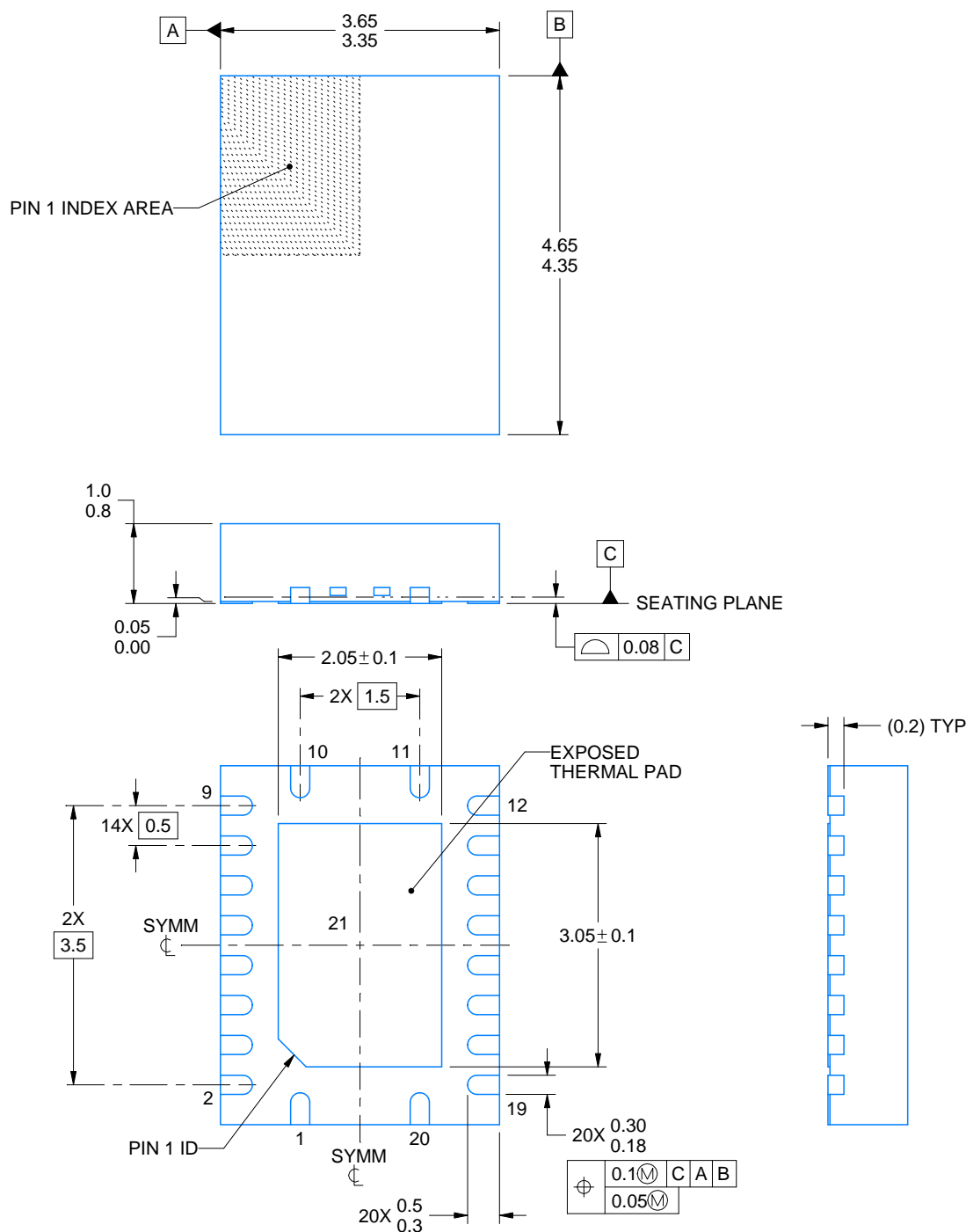


4225264/A



**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



4225320/A 09/2019

NOTES:

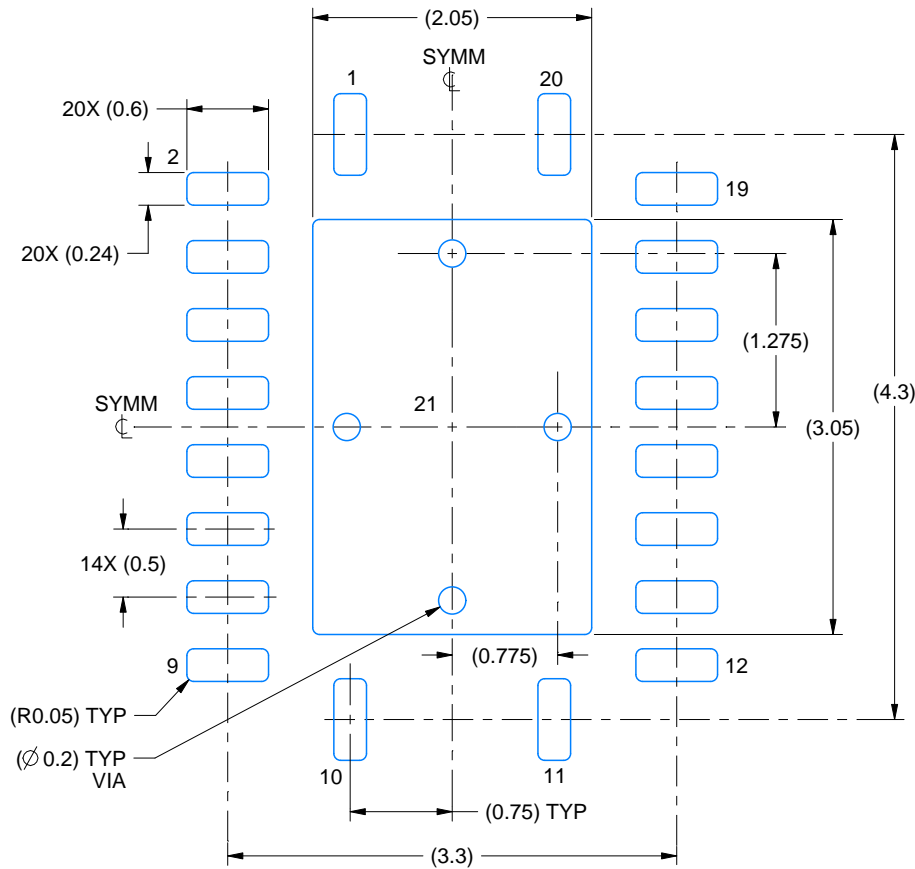
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

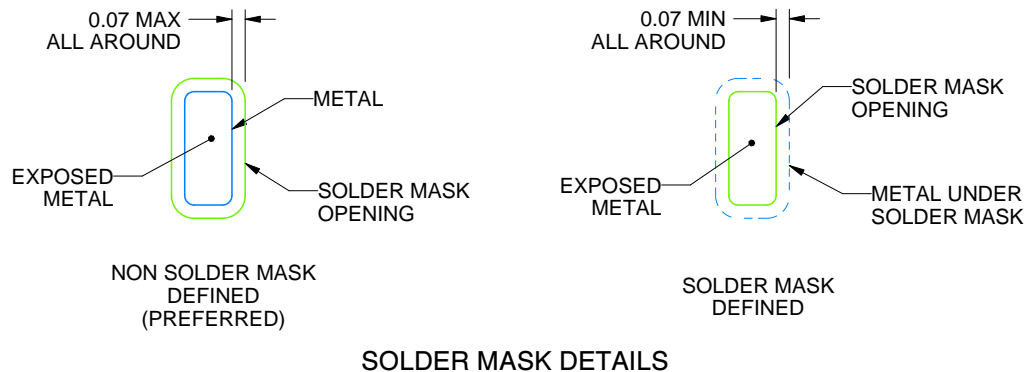
RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



4225320/A 09/2019

NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 21  
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

4225320/A 09/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

**DW0020A**

## PACKAGE OUTLINE

**SOIC - 2.65 mm max height**

SOIC



4220724/A 05/2016

NOTES:

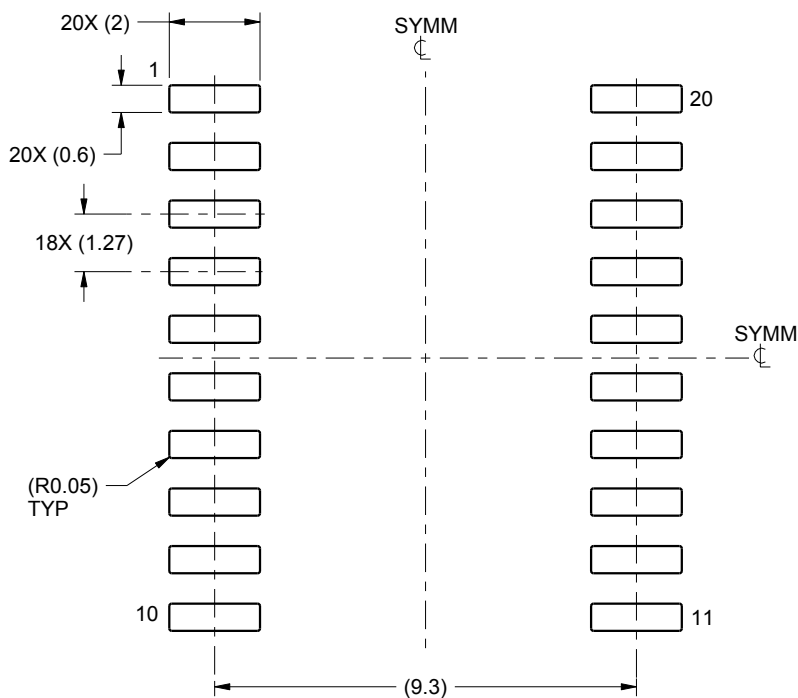
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

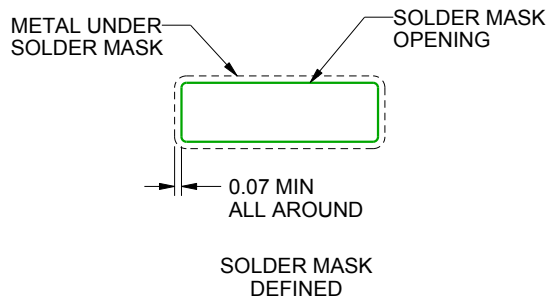
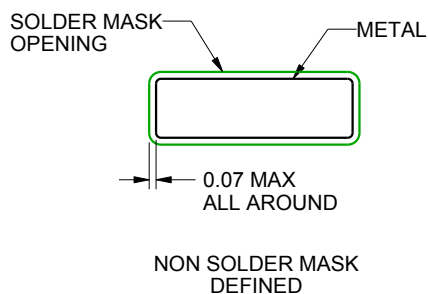
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



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