

SN65HVD23x 3.3V CAN 总线收发器

1 特性

- 3.3V 单电源电压
- 总线引脚故障保护大于 $\pm 36V$
- 总线引脚 ESD 保护大于 $\pm 16kV$ HBM
- 符合 ISO 11898-2 标准
- 符合 GIFT/ICT 标准
- 数据速率高达 1Mbps
- 扩展级共模范围: $-7V$ 至 $12V$
- 高输入阻抗支持 120 个节点
- LVTTTL I/O 可承受 5V 的电压
- 可调节的驱动器转换时间, 能够改善辐射性能
- 未供电节点不会干扰总线
- 低电流待机模式, 200 μA (典型值)
- SN65HVD233: 环回模式
- SN65HVD234: 超低电流休眠模式
 - 50nA 典型电流消耗
- SN65HVD235: 自动波特环回模式
- 热关断保护
- 加电和断电时总线输入和输出上无干扰
 - 具有低 V_{CC} 的高输入阻抗
 - 功率循环过程中单片输出

2 应用

- 工业自动化、控制、传感器和驱动系统
- 电机和机器人控制
- 楼宇和温度控制 (HVAC)
- 背板通信和控制
- CANopen、DeviceNet、CAN Kingdom、NMEA 2000、SAE J1939 等 CAN 总线标准

3 说明

SN65HVD233、SN65HVD234 和 SN65HVD235 用于采用符合 ISO 11898 标准的控制器局域网 (CAN) 串行通信物理层的应用。作为 CAN 收发器, 每种器件在差分 CAN 总线和 CAN 控制器间提供传输和接收功能, 信令速度高达 1Mbps。

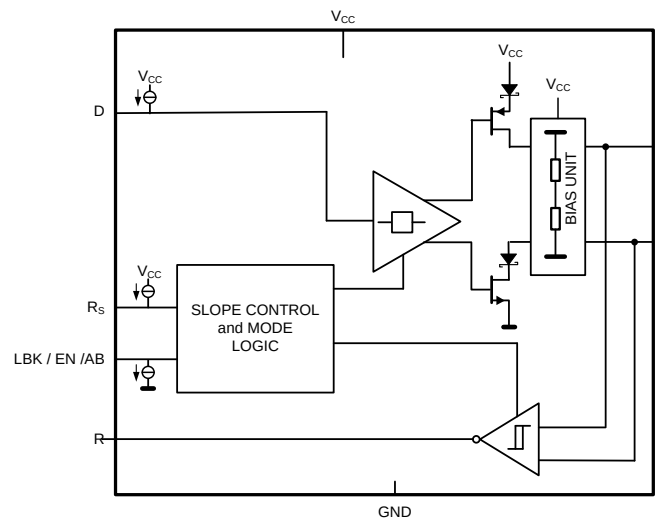
这些器件专为在特别恶劣的环境中工作而设计, 具有交叉线保护、高达 $\pm 36V$ 的过压保护、接地失效保护、过热 (热关断) 保护以及 $\pm 100V$ 的共模瞬态保护功能。这些器件可在 $-7V$ 至 $12V$ 的宽共模范围内运行。这些收发器是微处理器上的主机 CAN 控制器与工业、楼宇自动化, 运输和汽车应用中使用的差分 CAN 总线之间的接口。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
SN65HVD233	SOIC (8)	4.90mm $\times$ 3.91mm
SN65HVD234		
SN65HVD235		

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

方框图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision G (January 2015) to Revision H	Page
• 从最后一个应用项目中删除了“ISO 11783”	1

Changes from Revision F (August 2008) to Revision G	Page
• 已添加 引脚配置和功能 部分、ESD 额定值 表、特性 说明 部分、器件功能模式、应用和实施 部分、电源建议 部分、布局 部分、器件和文档支持 部分以及机械、封装和可订购信息 部分	1
• Changed the Functional Block Diagrams	4
• Added the THERMAL SHUTDOWN paragraph to the Application Information section	21
• Changed the BUS CABLE paragraph to BUS LOADING, LENGTH AND NUMBER OF NODES paragraph in the Application Information section	24
• Added the CAN TERMINATION paragraph to the Application Information section	24

Changes from Revision E (October 2007) to Revision F	Page
• Changed Figure 17 , Receiver Test Circuit and Voltage Waveform. From: $C_L = 50 \text{ pF} \pm 20\%$ to: $C_L = 15 \text{ pF} \pm 20\%$	13

Changes from Revision D (June 2005) to Revision E	Page
• Added 60-Ω load test condition to Figure 3	10
• Deleted INTEROPERABILITY WITH 5-V CAN SYSTEMS section	26
• Added ISO 11898 COMPLIANCE OF SN65HVD230 FAMILY OF 3.3-V CAN TRANSCEIVERS section	26

Changes from Revision C (March 2005) to Revision D **Page**

- 已添加 添加了特性 项目: 符合 GIFT/ICT 标准 (SN65HVD234) [1](#)
-

Changes from Revision B (June 2003) to Revision C **Page**

- Added $I_{O, Receiver}$ output current to the Abs Max Table [5](#)
-

Changes from Revision A (March 2003) to Revision B **Page**

- 已更改 针对器件型号 SN65HVD234 和 SN65HVD235 将数据表从“产品预览”更改成了“生产数据”。 [1](#)
 - Changed the APPLICATION INFORMATION section..... [23](#)
-

Changes from Original (November 2002) to Revision A **Page**

- 已更改 针对器件型号 SN65HVD233 将数据表从“产品预览”更改成了“生产数据”。 [1](#)
-

5 （说明（续））

模式: SN65HVD233、SN65HVD234 和 SN65HVD235 的 R_S 引脚（引脚 8）提供三种运行模式：高速、斜率控制和低功耗待机模式。将引脚 8 直接接地可选择高速工作模式，该工作模式允许驱动器输出晶体管以尽可能快的速度导通和关断，而且对上升和下降斜率没有限制。通过在 R_S 引脚与地之间连接一个电阻器可以调节上升和下降斜率。斜率将与引脚的输出电流成正比。当电阻器值为 10k Ω 时，器件驱动器的压摆率约为 15V/ μ s；当电阻器值为 100k Ω 时，器件的压摆率约为 2.0V/ μ s。有关斜率控制的更多信息，请参阅[特性说明](#)。

如果对 R_S 引脚施加逻辑高电平，那么 SN65HVD233、SN65HVD234 和 SN65HVD235 会进入低电流待机（仅监听）模式，在此模式下，驱动器将关断并且接收器保持活动状态。如果本地协议控制器需要向总线发送消息，则必须通过 R_S 引脚将器件返回至高速模式或斜率控制模式。

环回 (SN65HVD233): 当 SN65HVD233 的环回 (LBK) 引脚（引脚 5）为逻辑高电平时，会将总线输出和总线输入置于高阻抗状态。器件内部的 D 至 R 路径保持活动状态，可用于驱动器至接收器环回，从而实现在不干扰总线的情况下执行自诊断节点功能。有关环回模式的更多信息，请参阅[特性说明](#)。

超低电流睡眠 (SN65HVD234): 如果对 EN 引脚（引脚 5）施加逻辑低电平，则 SN65HVD234 会进入超低电流睡眠模式，在该模式下将停用驱动器和接收器电路。在通过向引脚 5 施加逻辑高电平来激活电路之前，器件将一直处于该睡眠模式。

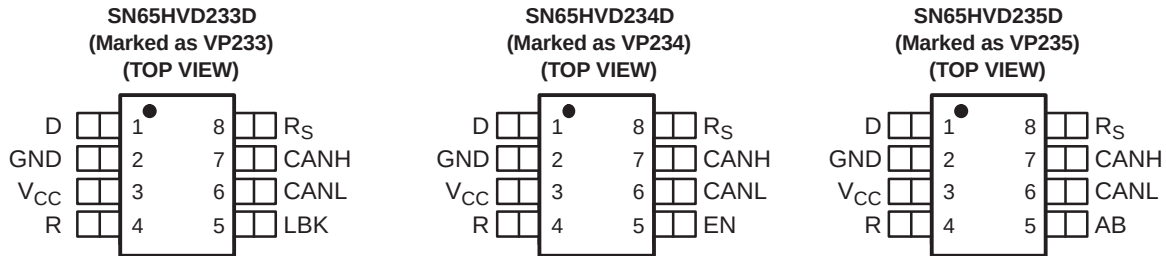
自动波特环回 (SN65HVD235): SN65HVD235 的 AB 引脚（引脚 5）实现了总线仅监听环回功能，允许本地节点控制器将其波特率与 CAN 总线的波特率同步。在自动波特模式下，驱动器的总线输出处于高阻抗状态，而接收器的总线输入保持活动状态。器件内部有一条 D 引脚到 R 引脚的环回路径，可帮助控制器执行波特率检测或自动波特功能。有关自动波特模式的更多信息，请参阅[特性说明](#)。

6 Device Comparison Table⁽¹⁾

PART NUMBER	LOW POWER MODE	SLOPE CONTROL	DIAGNOSTIC LOOPBACK	AUTOBAUD LOOPBACK
SN65HVD233D	200- μ A standby mode	Adjustable	Yes	No
SN65HVD234D	200- μ A standby mode or 50-nA sleep mode	Adjustable	No	No
SN65HVD235D	200- μ A standby mode	Adjustable	No	Yes

(1) For the most current package and ordering information, see [机械、封装和可订购信息](#), or see the TI web site at www.ti.com.

7 Pin Configuration and Functions



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
D	1	I	CAN transmit data input (LOW for dominant and HIGH for recessive bus states), also called TXD, driver input
GND	2	GND	Ground connection
V _{CC}	3	Supply	Transceiver 3.3-V supply voltage
R	4	O	CAN receive data output (LOW for dominant and HIGH for recessive bus states), also called RXD, receiver output
LBK	5	I	SN65HVD233: Loopback mode input pin
EN		I	SN65HVD234: Enable input pin. Logic high for enabling a normal mode (high speed or slope control) mode. Logic low for sleep mode.
AB		I	SN65HVD235: Autobaud loopback mode input pin
CANL	6	I/O	Low level CAN bus line
CANH	7	I/O	High level CAN bus line
R _S	8	I	Mode select pin: strong pulldown to GND = high speed mode, strong pullup to V _{CC} = low power mode, 10-kΩ to 100-kΩ pulldown to GND = slope control mode

8 Specifications

8.1 Absolute Maximum Ratings⁽¹⁾⁽²⁾

over operating free-air temperature range unless otherwise noted

	MIN	MAX	UNIT
V _{CC} Supply voltage	−0.3	7	V
Voltage at any bus terminal (CANH or CANL)	−36	36	V
Voltage input, transient pulse, CANH and CANL, through 100 Ω (see Figure 18)	−100	100	V
V _I Input voltage, (D, R _S , EN, LBK, AB)	−0.5	7	V
V _O Output voltage	−0.5	7	V
I _O Receiver output current	−10	10	mA
Continuous total power dissipation	See Power Dissipation Ratings		
T _J Operating junction temperature		150	°C
T _{stg} Storage temperature		125	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltages, are with respect to network ground pin.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	CANH, CANL and GND	±16000	V
		All pins	3000	
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾		±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		3	3.6	V
	Voltage at any bus terminal (separately or common mode)		–7	12	
V_{IH}	High-level input voltage	D, EN, AB, LBK	2	5.5	
V_{IL}	Low-level input voltage	D, EN, AB, LBK	0	0.8	
V_{ID}	Differential input voltage between CANH and CANL		–6	6	kΩ
	Resistance from R_S to ground		0	100	
$V_{I(RS)}$	Input Voltage at R_S for standby		0.75 V_{CC}	5.5	V
I_{OH}	High-level output current	Driver	–50		mA
		Receiver	–10		
I_{OL}	Low-level output current	Driver		50	mA
		Receiver		10	
T_J	Operating junction temperature	HVD233, HVD234, HVD235		150	°C
T_A	Operating free-air temperature ⁽¹⁾	HVD233, HVD234, HVD235	–40	125	°C

(1) Maximum free-air temperature operation is allowed as long as the device maximum junction temperature is not exceeded.

8.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	VALUE	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽¹⁾	Low-K ⁽²⁾ board, no air flow	185	°C/W
		High-K ⁽³⁾ board, no air flow	101	
$R_{\theta JB}$	Junction-to-board thermal resistance	High-K ⁽³⁾ board, no air flow	82.8	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance		26.5	°C/W
$P_{(AVG)}$	Average power dissipation	$R_L = 60\ \Omega$, R_S at 0 V, input to D a 1-MHz 50% duty cycle square wave V_{CC} at 3.3 V, $T_A = 25^\circ\text{C}$	36.4	mW
$T_{(SD)}$	Thermal shutdown junction temperature		170	°C

(1) See [SZZA003](#) for an explanation of this parameter.

(2) JESD51-3 low effective thermal conductivity test board for leaded surface mount packages.

(3) JESD51-7 high effective thermal conductivity test board for leaded surface mount packages.

8.5 Power Dissipation Ratings

PACKAGE	CIRCUIT BOARD	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ⁽¹⁾ ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D	Low-K	596.6 mW	5.7 mW/°C	255.7 mW	28.4 mW
D	High-K	1076.9 mW	10.3 mW/°C	461.5 mW	51.3 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

8.6 Electrical Characteristics: Driver

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
$V_{O(D)}$	Bus output voltage (Dominant)	CANH	D at 0 V, R_S at 0 V, See Figure 12 and Figure 13	2.45		V_{CC}	V
		CANL		0.5		1.25	
V_O	Bus output voltage (Recessive)	CANH	D at 3 V, R_S at 0 V, See Figure 12 and Figure 13		2.3		V
		CANL			2.3		
$V_{OD(D)}$	Differential output voltage (Dominant)		D at 0 V, R_S at 0 V, See Figure 12 and Figure 13	1.5	2	3	V
			D at 0 V, R_S at 0 V, See Figure 13 and Figure 14	1.2	2	3	
V_{OD}	Differential output voltage (Recessive)		D at 3 V, R_S at 0 V, See Figure 12 and Figure 13	–120		12	mV
			D at 3 V, R_S at 0 V, No Load	–0.5		0.05	V
$V_{OC(pp)}$	Peak-to-peak common-mode output voltage		See Figure 21		1		V
I_{IH}	High-level input current	D, EN, LBK, AB	D = 2 V or EN = 2 V or LBK = 2 V or AB = 2 V	–30		30	μ A
I_{IL}	Low-level input current	D, EN, LBK, AB	D = 0.8 V or EN = 0.8 V or LBK = 0.8 V or AB = 0.8 V	–30		30	μ A
I_{OS}	Short-circuit output current		$V_{CANH} = -7$ V, CANL Open, See Figure 26	–250			mA
			$V_{CANH} = 12$ V, CANL Open, See Figure 26			1	
			$V_{CANL} = -7$ V, CANH Open, See Figure 26	–1			
			$V_{CANL} = 12$ V, CANH Open, See Figure 26			250	
C_O	Output capacitance		See receiver input capacitance				
$I_{IRS(s)}$	R_S input current for standby		R_S at 0.75 V_{CC}	–10			μ A
I_{CC}	Supply current	Sleep	EN at 0 V, D at V_{CC} , R_S at 0 V or V_{CC}		0.05	2	μ A
		Standby	R_S at V_{CC} , D at V_{CC} , AB at 0 V, LBK at 0 V, EN at V_{CC}		200	600	
		Dominant	D at 0 V, No Load, AB at 0 V, LBK at 0 V, R_S at 0 V, EN at V_{CC}			6	mA
		Recessive	D at V_{CC} , No Load, AB at 0 V, LBK at 0 V, R_S at 0 V, EN at V_{CC}			6	

(1) All typical values are at 25°C and with a 3.3-V supply.

8.7 Electrical Characteristics: Receiver

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IT+}	Positive-going input threshold voltage	AB at 0 V, LBK at 0 V, EN at V _{CC} , See Table 1		750	900	mV
V _{IT-}	Negative-going input threshold voltage		500	650		
V _{hys}	Hysteresis voltage (V _{IT+} – V _{IT-})			100		
V _{OH}	High-level output voltage	I _O = –4 mA, See Figure 17	2.4			V
V _{OL}	Low-level output voltage	I _O = 4 mA, See Figure 17			0.4	
I _I	Bus input current	CANH or CANL at 12 V	150		500	μA
		CANH or CANL at 12 V, V _{CC} at 0 V	200		600	
		CANH or CANL at –7 V	–610		–150	
		CANH or CANL at –7 V, V _{CC} at 0 V	–450		–130	
C _I	Input capacitance (CANH or CANL)	Pin-to-ground, V _I = 0.4 sin (4E6πt) + 0.5 V, D at 3 V, AB at 0 V, LBK at 0 V, EN at V _{CC}		40		pF
C _{ID}	Differential input capacitance	Pin-to-pin, V _I = 0.4 sin (4E6πt) + 0.5 V, D at 3 V, AB at 0 V, LBK at 0 V, EN at V _{CC}		20		
R _{ID}	Differential input resistance	D at 3 V, AB at 0 V, LBK at 0 V, EN at V _{CC}	40		100	kΩ
R _{IN}	Input resistance (CANH or CANL) to ground		20		50	
I _{CC}	Supply current	Sleep EN at 0 V, D at V _{CC} , R _S at 0 V or V _{CC}		0.05	2	μA
		Standby R _S at V _{CC} , D at V _{CC} , AB at 0 V, LBK at 0 V, EN at V _{CC}		200	600	
		Dominant D at 0 V, No Load, R _S at 0 V, LBK at 0 V, AB at 0 V, EN at V _{CC}			6	mA
		Recessive D at V _{CC} , No Load, R _S at 0 V, LBK at 0 V, AB at 0 V, EN at V _{CC}			6	

(1) All typical values are at 25°C and with a 3.3-V supply.

8.8 Switching Characteristics: Driver

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high-level output	R _S at 0 V, See Figure 15		35	85	ns
		R _S with 10 kΩ to ground, See Figure 15		70	125	
		R _S with 100 kΩ to ground, See Figure 15		500	870	
t _{PHL}	Propagation delay time, high-to-low-level output	R _S at 0 V, See Figure 15		70	120	ns
		R _S with 10 kΩ to ground, See Figure 15		130	180	
		R _S with 100 kΩ to ground, See Figure 15		870	1200	
t _{sk(p)}	Pulse skew (t _{PHL} – t _{PLH})	R _S at 0 V, See Figure 15		35		ns
		R _S with 10 kΩ to ground, See Figure 15		60		
		R _S with 100 kΩ to ground, See Figure 15		370		
t _r	Differential output signal rise time	R _S at 0 V, See Figure 15	20		70	ns
t _f	Differential output signal fall time		20		70	
t _r	Differential output signal rise time	R _S with 10 kΩ to ground, See Figure 15	30		135	ns
t _f	Differential output signal fall time		30		135	
t _r	Differential output signal rise time	R _S with 100 kΩ to ground, See Figure 15	350		1400	ns
t _f	Differential output signal fall time		350		1400	
t _{en(s)}	Enable time from standby to dominant	See Figure 19 and Figure 20		0.6	1.5	μs
t _{en(z)}	Enable time from sleep to dominant			1	5	

(1) All typical values are at 25°C and with a 3.3-V supply.

8.9 Switching Characteristics: Receiver

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 17		35	60	ns
t_{PHL}	Propagation delay time, high-to-low-level output			35	60	
$t_{sk(p)}$	Pulse skew ($ t_{PHL} - t_{PLH} $)			7		
t_r	Output signal rise time			2	5	
t_f	Output signal fall time			2	5	

(1) All typical values are at 25°C and with a 3.3-V supply.

8.10 Switching Characteristics: Device

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
$t_{(LBK)}$	Loopback delay, driver input to receiver output	HVD233	See Figure 23		7.5	12	ns
$t_{(AB1)}$	Loopback delay, driver input to receiver output	HVD235	See Figure 24		10	20	ns
$t_{(AB2)}$	Loopback delay, bus input to receiver output		See Figure 25		35	60	ns
$t_{(loop1)}$	Total loop delay, driver input to receiver output, recessive to dominant		R_S at 0 V, See Figure 22		70	135	ns
			R_S with 10 k Ω to ground, See Figure 22		105	190	
			R_S with 100 k Ω to ground, See Figure 22		535	1000	
$t_{(loop2)}$	Total loop delay, driver input to receiver output, dominant to recessive		R_S at 0 V, See Figure 22		70	135	ns
			R_S with 10 k Ω to ground, See Figure 22		105	190	
			R_S with 100 k Ω to ground, See Figure 22		535	1000	

(1) All typical values are at 25°C and with a 3.3-V supply.

8.11 Typical Characteristics

R_S , LBK , $AB = 0\text{ V}$; $EN = V_{CC}$

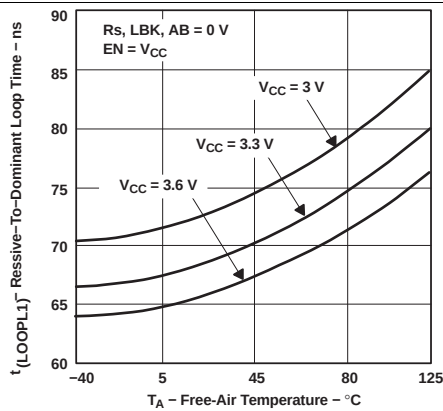


Figure 1. Recessive-to-Dominant Loop Time vs Free-Air Temperature

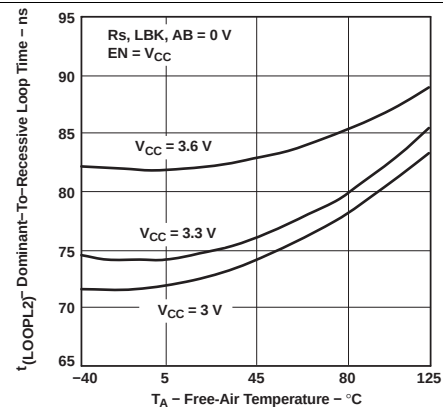


Figure 2. Dominant-to-Recessive Loop Time vs Free-Air Temperature

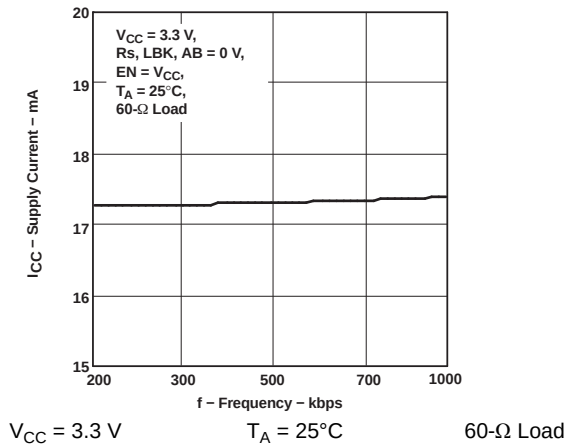


Figure 3. Supply Current vs Frequency

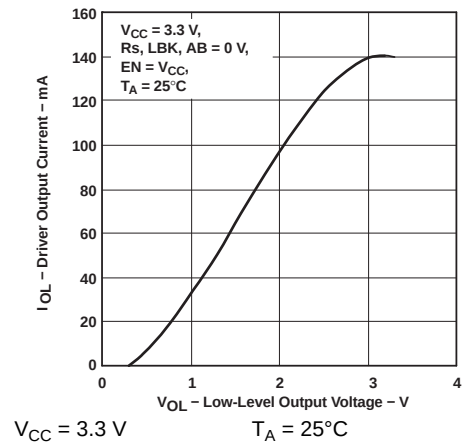


Figure 4. Driver Low-Level Output Current vs Low-Level Output Voltage

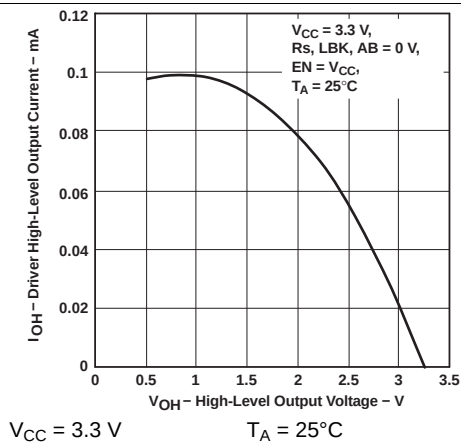


Figure 5. Driver High-Level Output Current vs High-Level Output Voltage

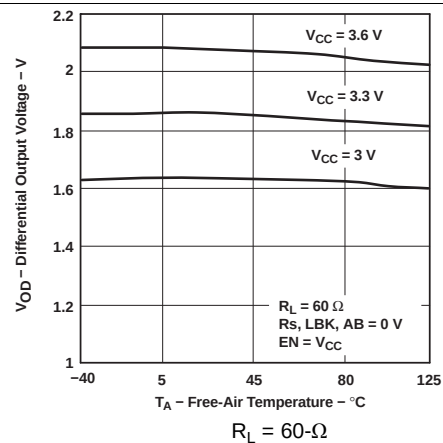
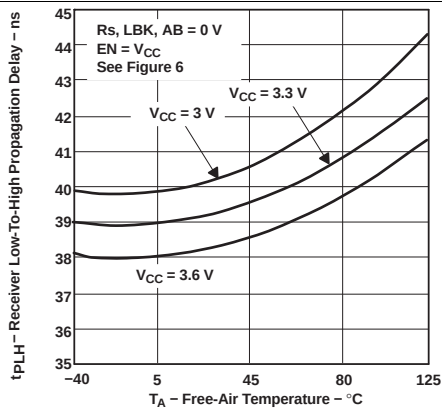


Figure 6. Differential Output Voltage vs Free-Air Temperature

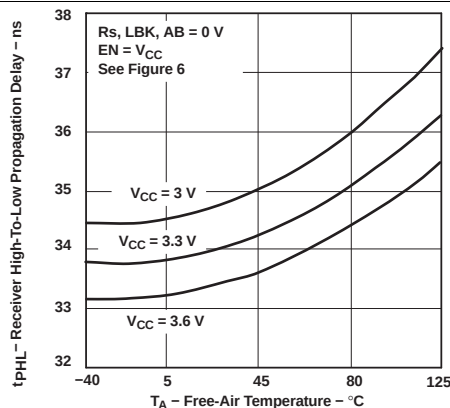
Typical Characteristics (continued)

$R_s, L_{BK}, AB = 0\text{ V}; EN = V_{CC}$



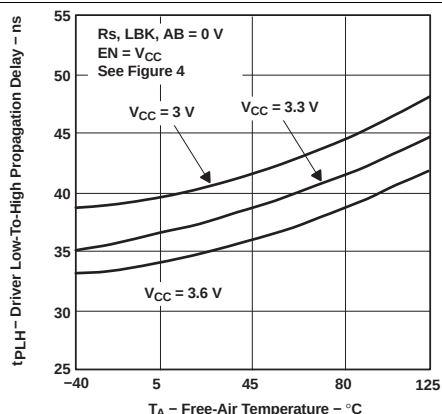
See Figure 3

Figure 7. Receiver Low-to-High Propagation Delay vs Free-Air Temperature



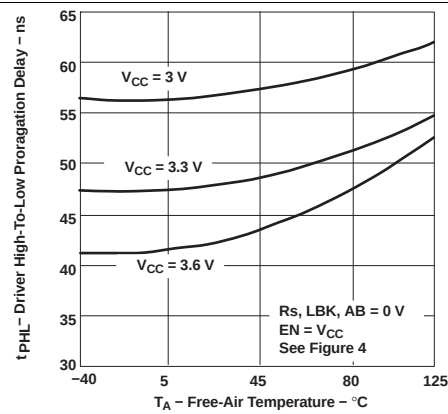
See Figure 3

Figure 8. Receiver High-to-Low Propagation Delay vs Free-Air Temperature



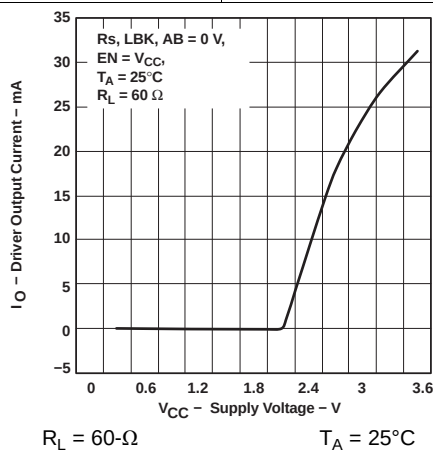
See Figure 1

Figure 9. Driver Low-to-High Propagation Delay vs Free-Air Temperature



See Figure 1

Figure 10. Driver High-to-Low Propagation Delay vs Free-Air Temperature



$R_L = 60\text{-}\Omega$

$T_A = 25^\circ\text{C}$

Figure 11. Driver Output Current vs Supply Voltage

9 Parameter Measurement Information

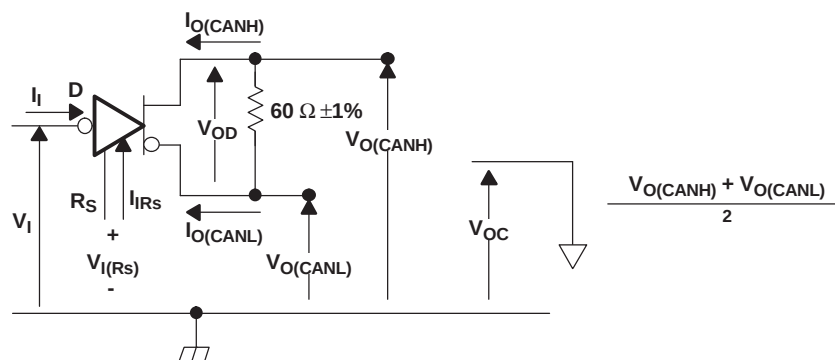


Figure 12. Driver Voltage, Current, and Test Definition

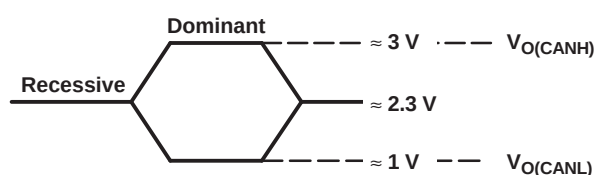


Figure 13. Bus Logic State Voltage Definitions

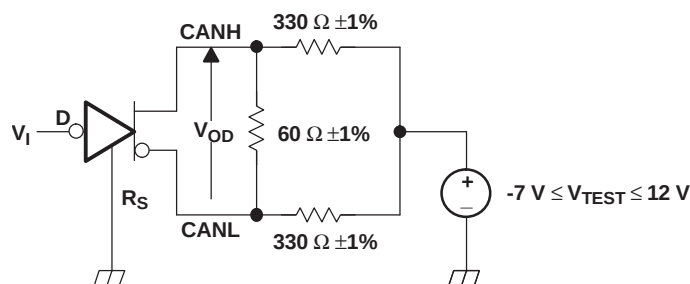
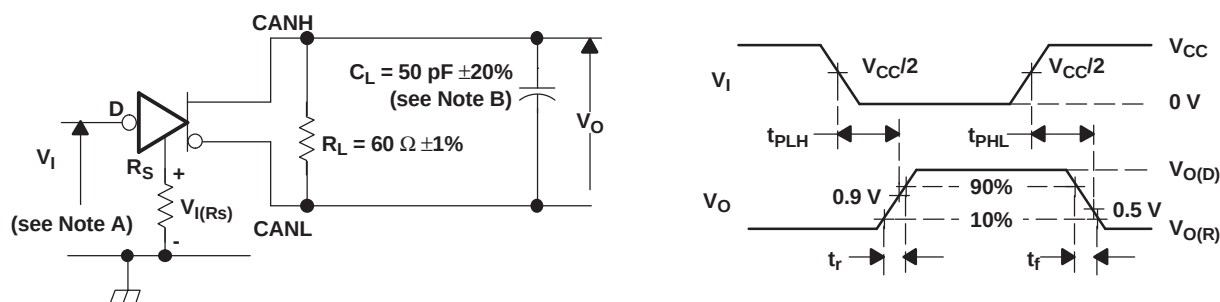


Figure 14. Driver V_{OD}



- The input pulse is supplied by a generator having the following characteristics: Pulse repetition rate (PRR) ≤ 125 kHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
- C_L includes fixture and instrumentation capacitance.

Figure 15. Driver Test Circuit and Voltage Waveforms

Parameter Measurement Information (continued)

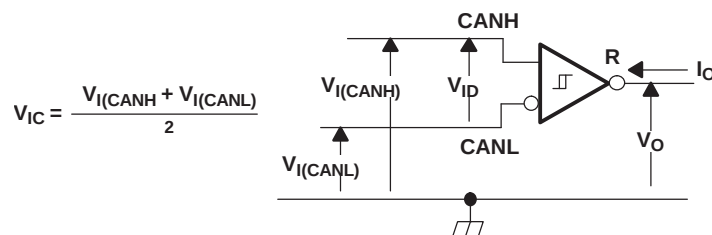
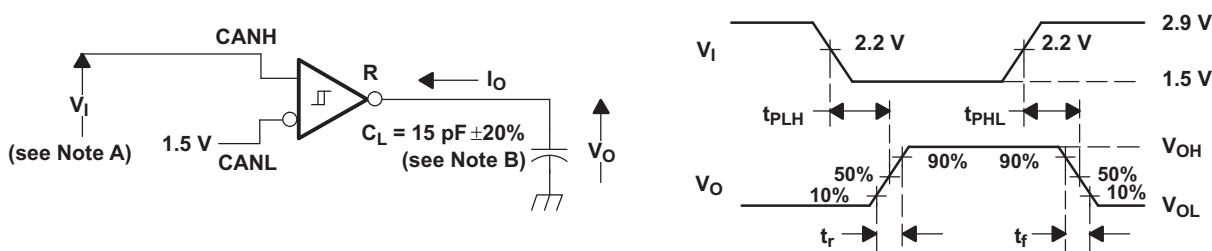


Figure 16. Receiver Voltage and Current Definitions

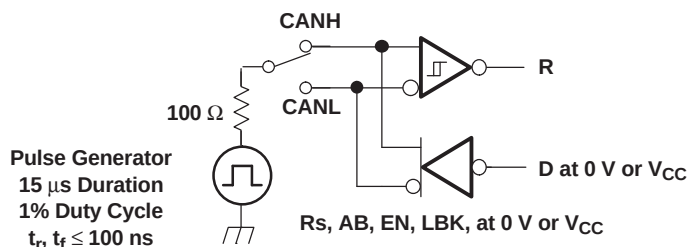


- A. The input pulse is supplied by a generator having the following characteristics: Pulse repetition rate (PRR) ≤ 125 kHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
- B. C_L includes fixture and instrumentation capacitance.

Figure 17. Receiver Test Circuit and Voltage Waveforms

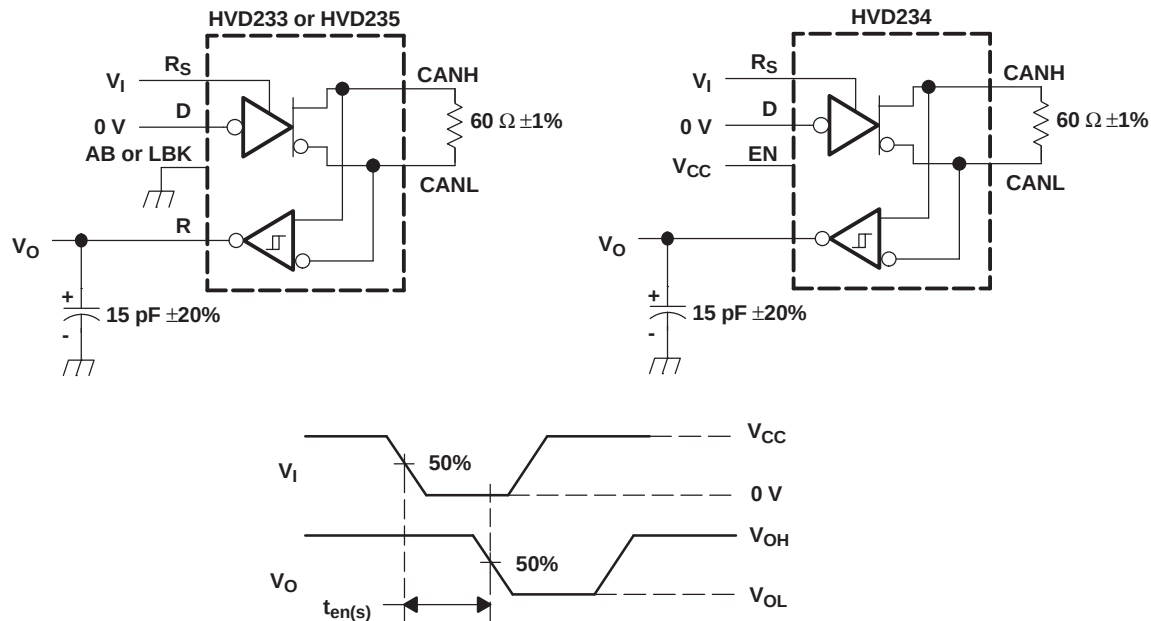
Table 1. Differential Input Voltage Threshold Test

INPUT		OUTPUT		MEASURED
V _{CANH}	V _{CANL}	R		V _{ID}
−6.1 V	−7 V	L	V _{OL}	900 mV
12 V	11.1 V	L		900 mV
−1 V	−7 V	L		6 V
12 V	6 V	L		6 V
−6.5 V	−7 V	H	V _{OH}	500 mV
12 V	11.5 V	H		500 mV
−7 V	−1 V	H		6 V
6 V	12 V	H		6 V
Open	Open	H		X



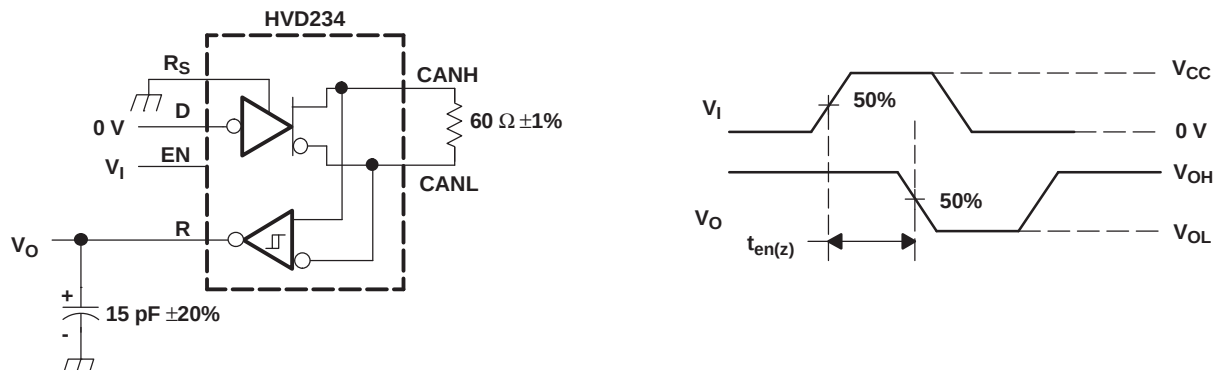
NOTE: This test is conducted to test survivability only. Data stability at the R output is not specified.

Figure 18. Test Circuit, Transient Overvoltage Test



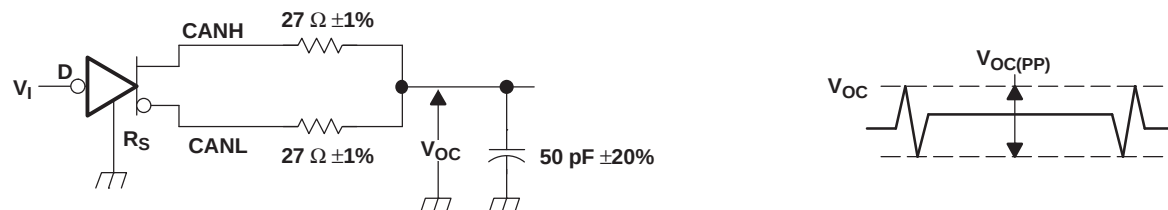
NOTE: All V_I input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 6$ ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 19. $T_{en(s)}$ Test Circuit and Voltage Waveforms



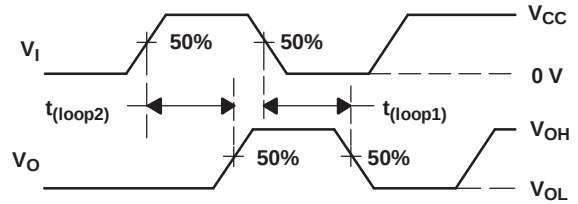
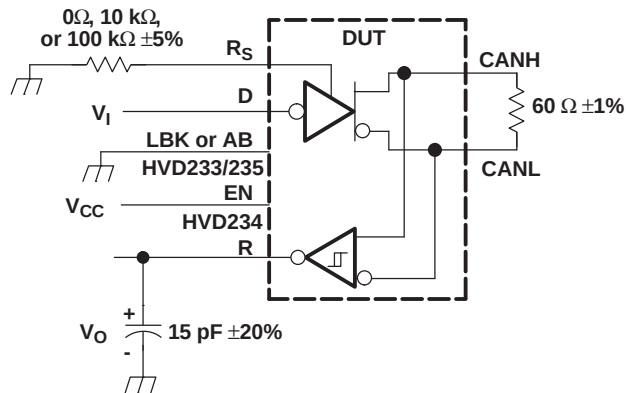
NOTE: All V_I input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 6$ ns, pulse repetition rate (PRR) = 50 kHz, 50% duty cycle.

Figure 20. $T_{en(z)}$ Test Circuit and Voltage Waveforms



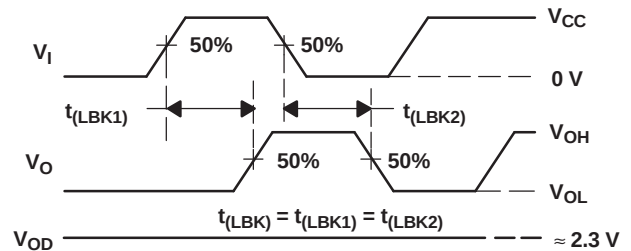
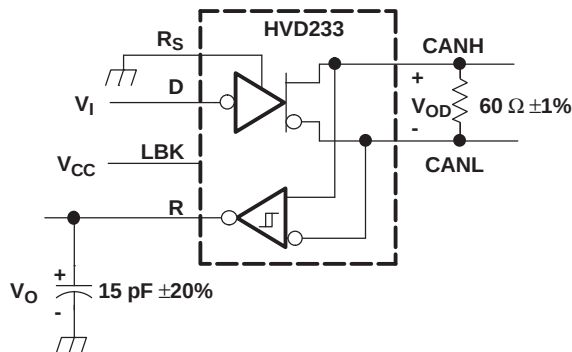
NOTE: All V_I input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 6$ ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 21. $V_{OC(pp)}$ Test Circuit and Voltage Waveforms



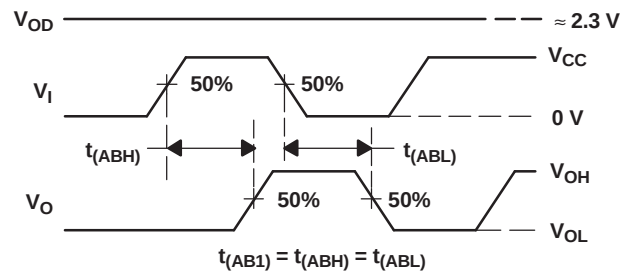
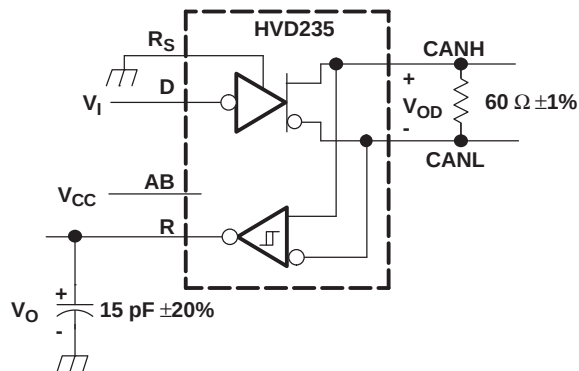
NOTE: All V_I input pulses are supplied by a generator having the following characteristics:
 t_r or $t_f \leq 6$ ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 22. $T_{(loop)}$ Test Circuit and Voltage Waveforms



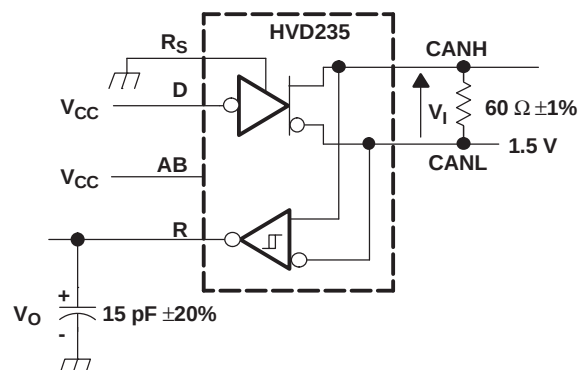
NOTE: All V_1 input pulses are supplied by a generator having the following characteristics:
 t_r or $t_f \leq 6$ ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 23. $T_{(LBK)}$ Test Circuit and Voltage Waveforms



NOTE: All V_1 input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 6$ ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 24. $T_{(AB1)}$ Test Circuit and Voltage Waveforms



NOTE: All V_1 input pulses are supplied by a generator having the following characteristics:
 t_r or $t_f \leq 6$ ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 25. $T_{(AB2)}$ Test Circuit and Voltage Waveforms

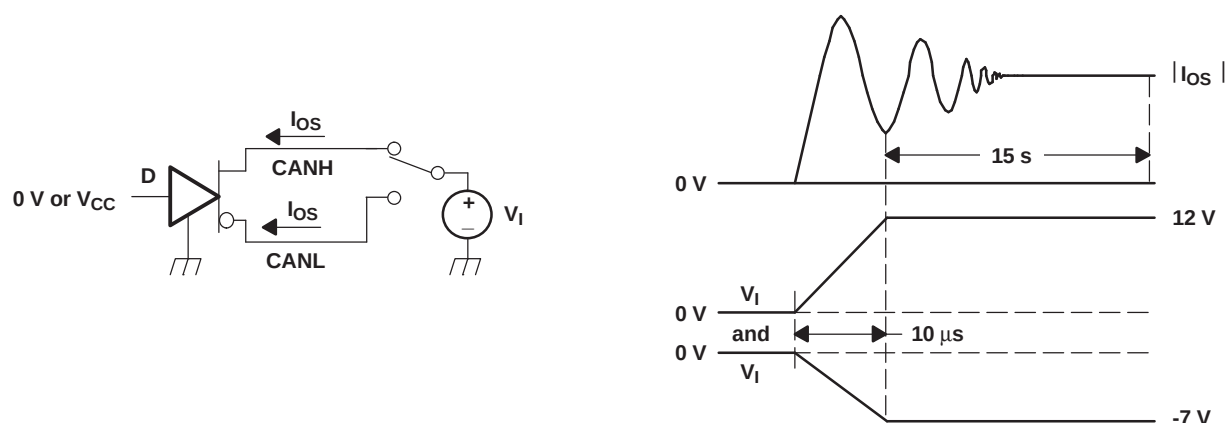
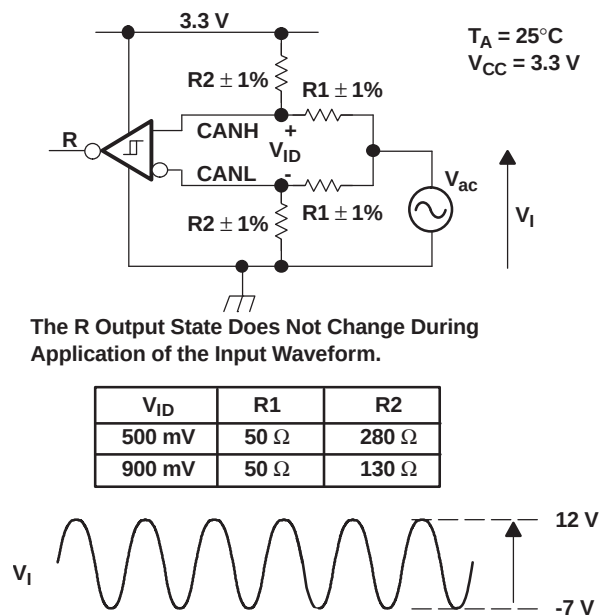


Figure 26. I_{OS} Test Circuit and Waveforms



NOTE: All input pulses are supplied by a generator with $f \leq 1.5\text{ MHz}$.

Figure 27. Common-Mode Voltage Rejection

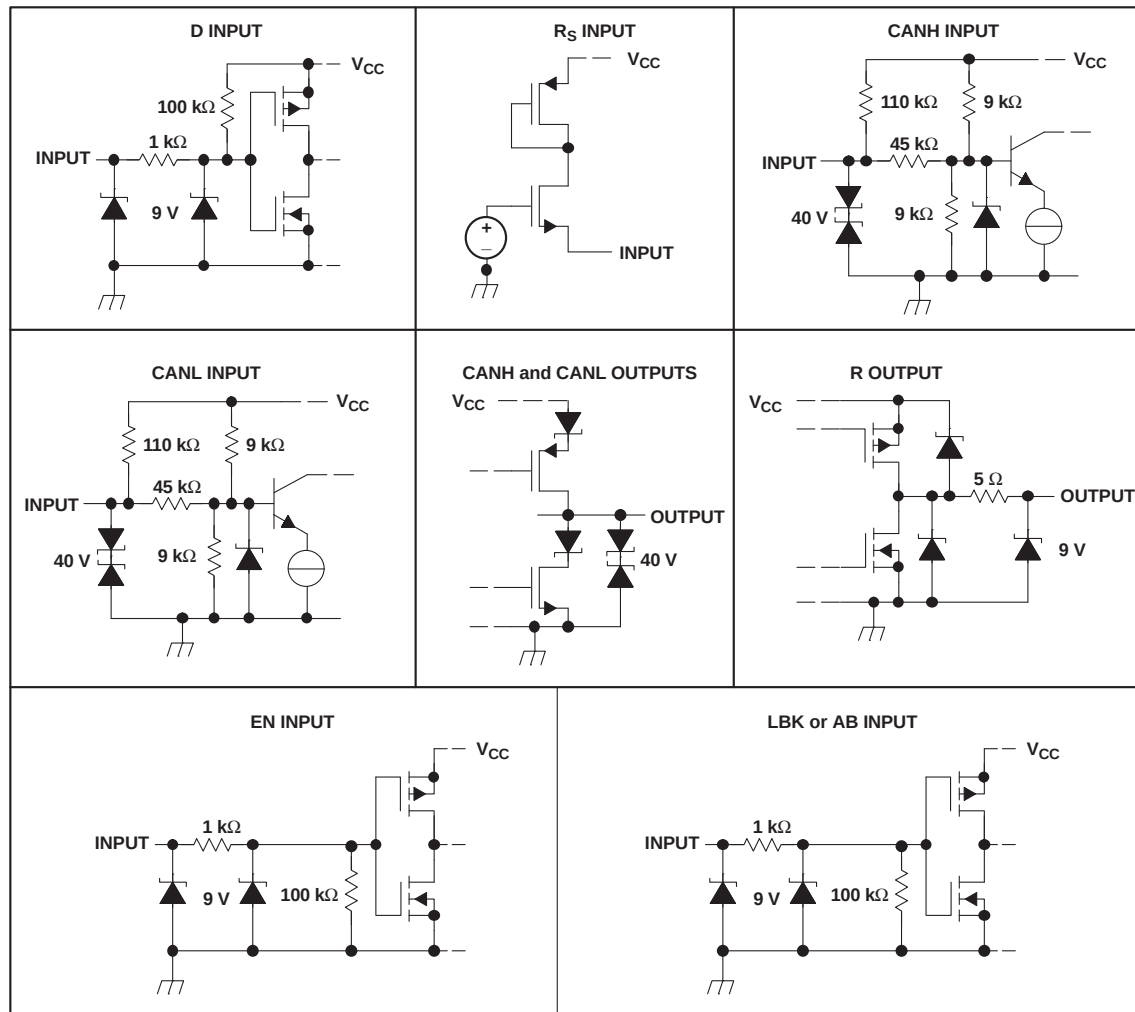


Figure 28. Equivalent Input and Output Schematic Diagrams

10 Detailed Description

10.1 Overview

This family of CAN transceivers is compatible with the ISO11898-2 High-Speed CAN (controller area network) physical layer standard. They are designed to interface between the differential bus lines in CAN and the CAN protocol controller at data rates up to 1 Mbps.

10.2 Functional Block Diagrams

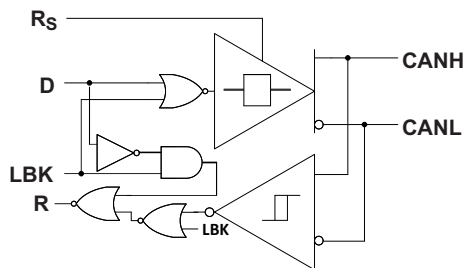


Figure 29. SN65HVD233 Functional Block Diagram

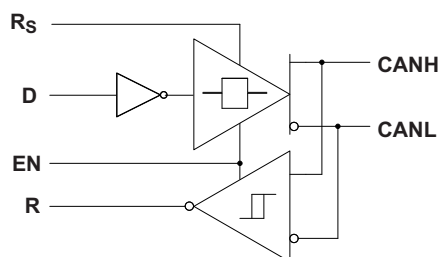


Figure 30. SN65HVD34 Functional Block Diagram

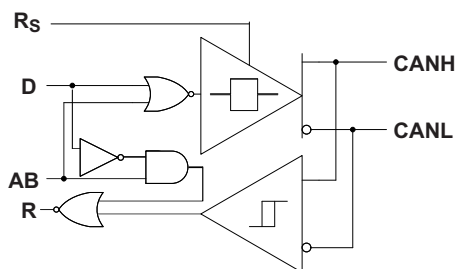


Figure 31. SN65HVD35 Functional Block Diagram

10.3 Feature Description

10.3.1 Diagnostic Loopback (SN65HVD233)

The diagnostic loopback or internal loopback function of the SN65HVD233 is enabled with a high-level input on pin 5, LBK. This mode disables the driver output while keeping the bus pins biased to the recessive state. This mode also redirects the D data input (transmit data) through logic to the received data output pin), thus creating an internal loopback of the transmit to receive data path. This mimics the loopback that occurs normally with a CAN transceiver because the receiver loops back the driven output to the R (receive data) pin. This mode allows the host protocol controller to input and read back a bit sequence or CAN messages to perform diagnostic routines without disturbing the CAN bus. A typical CAN bus application is displayed in [Figure 36](#).

Feature Description (continued)

If the LBK pin is not used it may be tied to ground (GND). However, it is pulled low internally (defaults to a low-level input) and may be left open if not in use.

10.3.2 Autobaud Loopback (SN65HVD235)

The autobaud loopback mode of the SN65HVD235 is enabled by placing a high level input on pin 5, AB. In autobaud mode, the driver output is disabled, thus blocking the D pin to bus path and the bus transmit function of the transceiver. The bus pins remain biased to recessive. The receiver to R pin path or the bus receive function of the device remains operational, allowing bus activity to be monitored. In addition, the autobaud mode adds an internal logic loopback path from the D pin to R pin so the local node may transmit to itself in sync with bus traffic while not disturbing messages on the bus. Thus if the local node's CAN controller generates an error frame, it is not transmitted to the bus, but is detected only by the local CAN controller. This is especially helpful to determine if the local node is set to the same baud rate as the network, and if not adjust it to the network baud rate (autobaud detection).

Autobaud detection is best suited to applications that have a known selection of baud rates. For example, a popular industrial application has optional settings of 125 kbps, 250 kbps, or 500 kbps. Once the SN65HVD235 is placed into autobaud loopback mode the application software could assume the first baud rate of 125 kbps. It then waits for a message to be transmitted by another node on the bus. If the wrong baud rate has been selected, an error message is generated by the local CAN controller because the sample times will not be at the correct time. However, because the bus-transmit function of the device has been disabled, no other nodes receive the error frame generated by this node's local CAN controller.

The application would then make use of the status register indications of the local CAN controller for message received and error warning status to determine if the set baud rate is correct or not. The warning status indicates that the CAN controller error counters have been incremented. A message received status indicates that a good message has been received. If an error is generated, the application would then set the CAN controller with the next possibly valid baud rate, and wait to receive another message. This pattern is repeated until an error free message has been received, thus the correct baud rate has been selected. At this point the application would place the SN65HVD235 in a normal transmitting mode by setting pin 5 to a low-level, thus enabling bus-transmit and bus-receive functions to normal operating states for the transceiver.

If the AB pin is not used it may be tied to ground (GND). However, it is pulled low internally (defaults to a low-level input) and may be left open if not in use.

10.3.3 Slope Control

The rise and fall slope of the SN65HVD233, SN65HVD234, and SN65HVD235 driver output can be adjusted by connecting a resistor from the Rs (pin 8) to ground (GND), or to a low-level input voltage as shown in [Figure 32](#).

The slope of the driver output signal is proportional to the pin's output current. This slope control is implemented with an external resistor value of 10 k Ω to achieve a ~ 15 V/ μ s slew rate, and up to 100 k Ω to achieve a ~ 2.0 V/ μ s slew rate. A typical slew rate versus pulldown resistance graph is shown in [Figure 33](#). Typical driver output waveforms with slope control are displayed in [Figure 39](#).

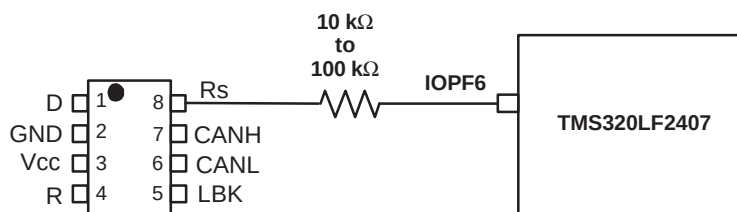


Figure 32. Slope Control/Standby Connection to a DSP

Feature Description (continued)

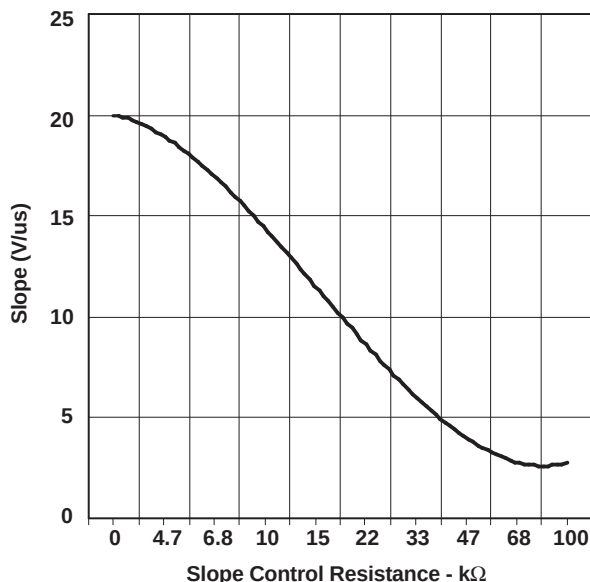


Figure 33. HVD233 Driver Output Signal Slope vs Slope Control Resistance Value

10.3.4 Standby

If a high-level input ($> 0.75 V_{CC}$) is applied to R_S (pin 8), the circuit enters a low-current, *listen only* standby mode during which the driver is switched off and the receiver remains active. If using this mode to save system power while waiting for bus traffic, the local controller can monitor the R output pin for a falling edge which indicates that a dominant signal was driven onto the CAN bus. The local controller can then drive the R_S pin low to return to slope control mode or high-speed mode.

10.3.5 Thermal Shutdown

If the junction temperature of the device exceeds the thermal shut down threshold the device turns off the CAN driver circuits thus blocking the D pin to bus transmission path. The shutdown condition is cleared when the junction temperature drops below the thermal shutdown temperature of the device. The CAN bus pins are high impedance biased to recessive level during a thermal shutdown, and the receiver to R pin path remains operational.

10.4 Device Functional Modes

10.4.1 Driver and Receiver

Table 2. Driver (SN65HVD233 or SN65HVD235)

INPUTS			OUTPUTS		
D	LBK/AB	R_S	CANH	CANL	BUS STATE
X	X	$> 0.75 V_{CC}$	Z	Z	Recessive
L	L or open	$\leq 0.33 V_{CC}$	H	L	Dominant
H or open	X		Z	Z	Recessive
X	H	$\leq 0.33 V_{CC}$	Z	Z	Recessive

Table 3. Receiver (SN65HVD233)

INPUTS				OUTPUT
BUS STATE	$V_{ID} = V_{(CANH)} - V_{(CANL)}$	LBK	D	R
Dominant	$V_{ID} \geq 0.9 \text{ V}$	L or open	X	L
Recessive	$V_{ID} \leq 0.5 \text{ V}$ or open	L or open	H or open	H
?	$0.5 \text{ V} < V_{ID} < 0.9 \text{ V}$	L or open	H or open	?
X	X	H	L	L
X	X		H	H

Table 4. Receiver (SN65HVD235)⁽¹⁾

INPUTS				OUTPUT
BUS STATE	$V_{ID} = V_{(CANH)} - V_{(CANL)}$	AB	D	R
Dominant	$V_{ID} \geq 0.9 \text{ V}$	L or open	X	L
Recessive	$V_{ID} \leq 0.5 \text{ V}$ or open	L or open	H or open	H
?	$0.5 \text{ V} < V_{ID} < 0.9 \text{ V}$	L or open	H or open	?
Dominant	$V_{ID} \geq 0.9 \text{ V}$	H	X	L
Recessive	$V_{ID} \leq 0.5 \text{ V}$ or open	H	H	H
Recessive	$V_{ID} \leq 0.5 \text{ V}$ or open	H	L	L
?	$0.5 \text{ V} < V_{ID} < 0.9 \text{ V}$	H	L	L

(1) H = high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate

Table 5. Driver (SN65HVD234)

INPUTS			OUTPUTS		
D	EN	R_s	CANH	CANL	BUS STATE
L	H	$\leq 0.33 V_{CC}$	H	L	Dominant
H	X	$\leq 0.33 V_{CC}$	Z	Z	Recessive
Open	X	X	Z	Z	Recessive
X	X	$> 0.75 V_{CC}$	Z	Z	Recessive
X	L or open	X	Z	Z	Recessive

Table 6. Receiver (SN65HVD234)⁽¹⁾

INPUTS			OUTPUT
BUS STATE	$V_{ID} = V_{(CANH)} - V_{(CANL)}$	EN	R
Dominant	$V_{ID} \geq 0.9 \text{ V}$	H	L
Recessive	$V_{ID} \leq 0.5 \text{ V}$ or open	H	H
?	$0.5 \text{ V} < V_{ID} < 0.9 \text{ V}$	H	?
X	X	L or open	H

(1) H = high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate

11 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

The CAN bus has two states during powered operation of the device; *dominant* and *recessive*. A dominant bus state is when the bus is driven differentially, corresponding to a logic low on the D and R pin. A recessive bus state is when the bus is biased to $V_{CC} / 2$ via the high-resistance internal resistors R_{IN} and R_{ID} of the receiver, corresponding to a logic high on the D and R pins. See [Figure 34](#) and [Figure 35](#).

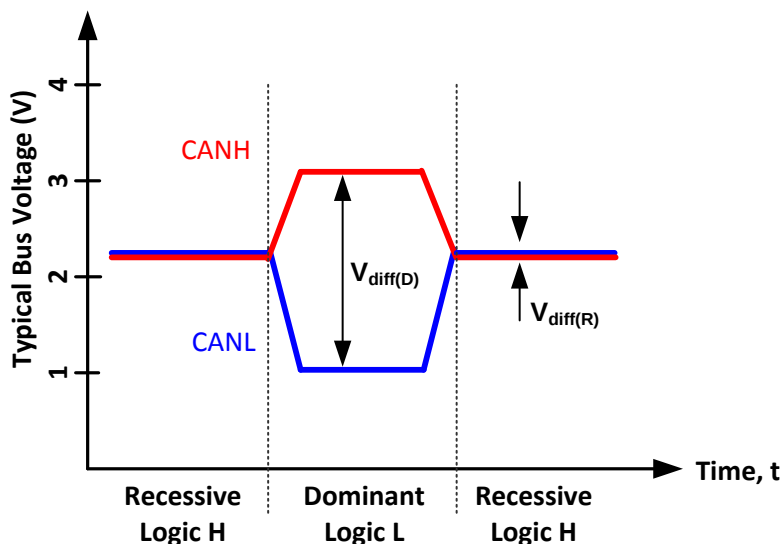


Figure 34. Bus States (Physical Bit Representation)

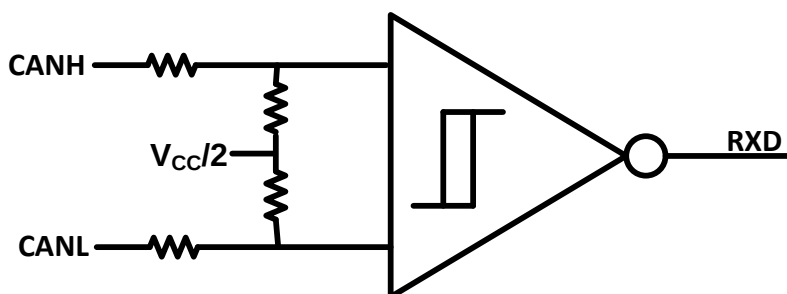


Figure 35. Simplified Recessive Common Mode Bias and Receiver

These CAN transceivers are typically used in applications with a host microprocessor or FPGA that includes the link layer portion of the CAN protocol. The different nodes on the network are typically connected through the use of a 120-Ω characteristic impedance twisted-pair cable with termination on both ends of the bus.

11.2 Typical Application

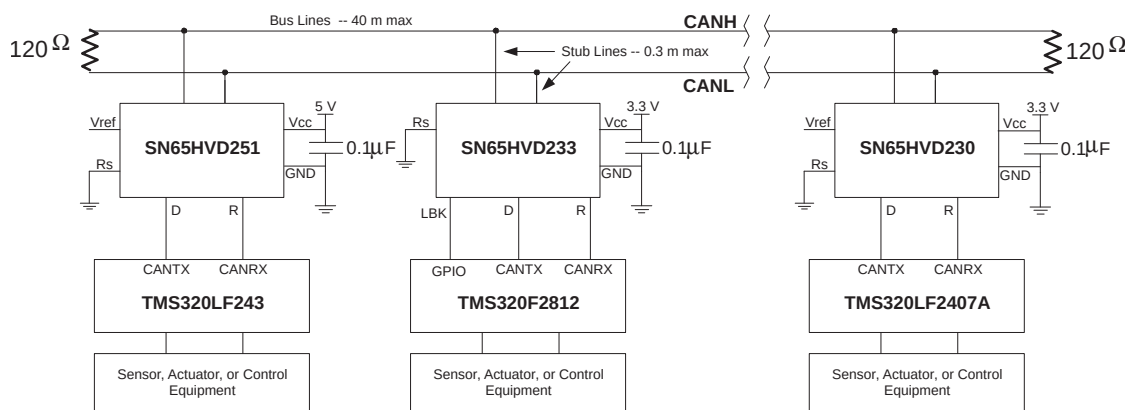


Figure 36. Typical HVD233 Application

11.2.1 Design Requirements

11.2.1.1 Bus Loading, Length and Number of Nodes

The ISO 11898 Standard specifies up to a data rate of 1 Mbps, maximum CAN bus cable length of 40 m, maximum drop line (stub) length of 0.3 m and a maximum of 30 nodes. However, with careful network design, the system may have longer cables, longer stub lengths, and many more nodes to a bus. Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898 standard. They have made system level trade-offs for data rate, cable length, and parasitic loading of the bus. Examples of some of these specifications are ARINC825, CANopen, CAN Kingdom, DeviceNet and NMEA200.

A high number of nodes requires a transceiver with high input impedance and wide common mode range such as the SN65HVD23x CAN family. ISO 11898-2 specifies the driver differential output with a 60- Ω load (two 120- Ω termination resistors in parallel) and the differential output must be greater than 1.5 V. The SN65HVD23x devices are specified to meet the 1.5-V requirement with a 60- Ω load, and additionally specified with a differential output voltage minimum of 1.2 V across a common mode range of -2 V to 7 V through a 330- Ω coupling network. This network represents the bus loading of 120 SN65HVD23x transceivers based on their minimum differential input resistance of 40 k Ω . Therefore, the SN65HVD23x supports up to 120 transceivers on a single bus segment with margin to the 1.2-V minimum differential input voltage requirement at each node.

For CAN network design, margin must be given for signal loss across the system and cabling, parasitic loadings, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes may be lower. Bus length may also be extended beyond the original ISO 11898 standard of 40 m by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1 km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898 CAN standard.

11.2.1.2 CAN Termination

The ISO 11898 standard specifies the interconnect to be a twisted-pair cable (shielded or unshielded) with 120- Ω characteristic impedance (Z_0). Resistors equal to the characteristic impedance of the line should be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop lines (stubs) connecting nodes to the bus should be kept as short as possible to minimize signal reflections. The termination may be on the cable or in a node, but if nodes may be removed from the bus the termination must be carefully placed so that it is not removed from the bus.

Typical Application (continued)

11.2.2 Detailed Design Procedure

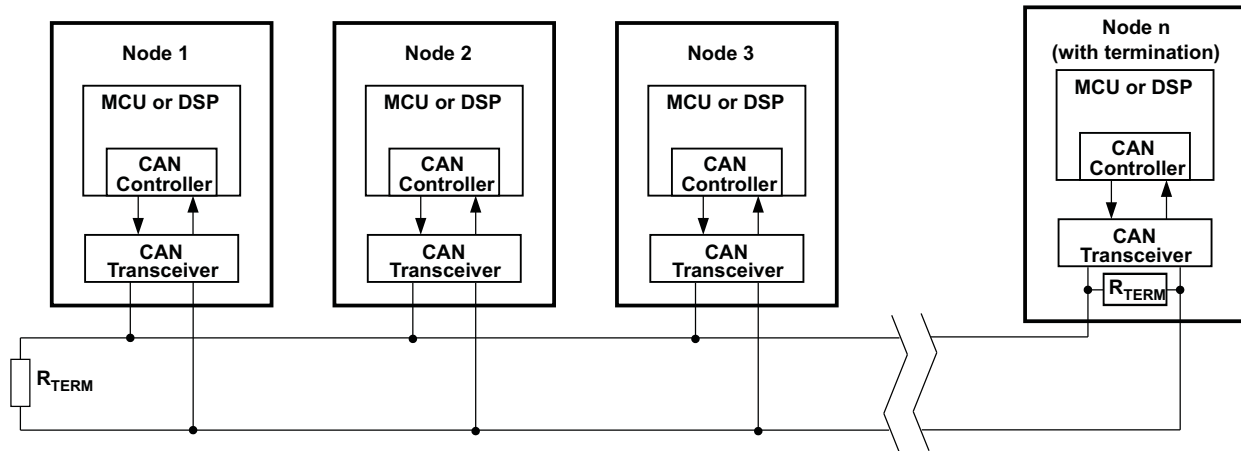


Figure 37. Typical CAN Bus

Termination is typically a 120- Ω resistor at each end of the bus. If filtering and stabilization of the common mode voltage of the bus is desired, then split termination may be used (see Figure 38). Split termination uses two 60- Ω resistors with a capacitor in the middle of these resistors to ground. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common mode voltages at the start and end of message transmissions.

Care should be taken in the power ratings of the termination resistors used. Typically the worst case condition would be if the system power supply was shorted across the termination resistance to ground. In most cases the current flow through the resistor in this condition would be much higher than the transceiver's current limit.

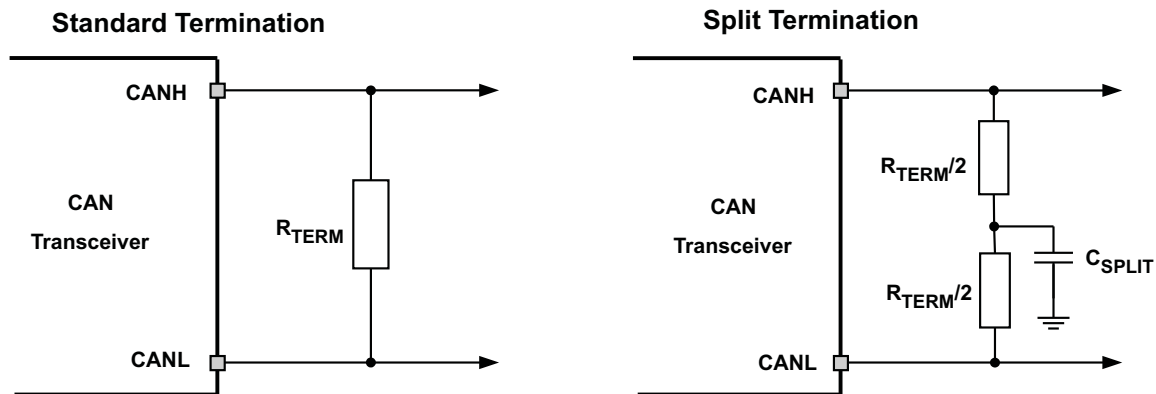


Figure 38. CAN Bus Termination Concepts

11.2.3 Application Curve

Figure 39 shows 3 typical output waveforms for the SN65HVD233 device with three different connections made to the R_S pin. The top waveform shows the typical differential signal when transitioning from a recessive level to a dominant level on the CAN bus with R_S tied to GND through a 0- Ω resistor. The second waveform shows the same signal for the condition with a 10-k Ω resistor tied from R_S to ground. The bottom waveform shows the typical differential signal for the case where a 100-k Ω resistor is tied from the R_S pin to ground.

Typical Application (continued)

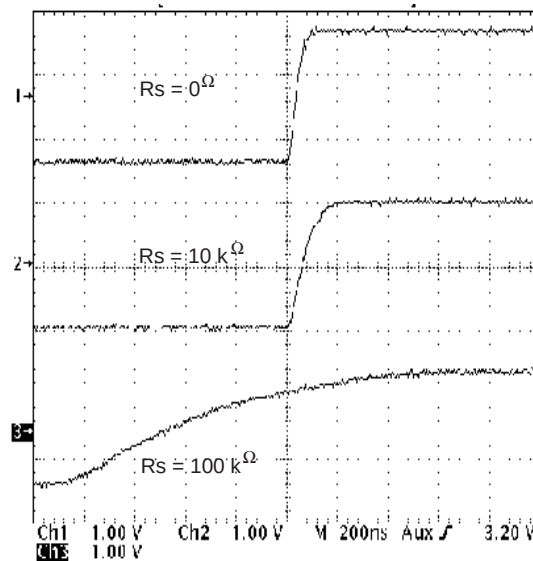


Figure 39. Typical SN65HVD233 Output Waveforms With Different Slope Control Resistor Values

11.3 System Example

11.3.1 ISO 11898 Compliance of SN65HVD23x Family of 3.3-V CAN Transceivers

11.3.1.1 Introduction

Many users value the low power consumption of operating their CAN transceivers from a 3.3-V supply. However, some are concerned about the interoperability with 5 V supplied transceivers on the same bus. This report analyzes this situation to address those concerns.

11.3.1.2 Differential Signal

CAN is a differential bus where complementary signals are sent over two wires and the voltage difference between the two wires defines the logical state of the bus. The differential CAN receiver monitors this voltage difference and outputs the bus state with a single ended logic level output signal.

System Example (continued)

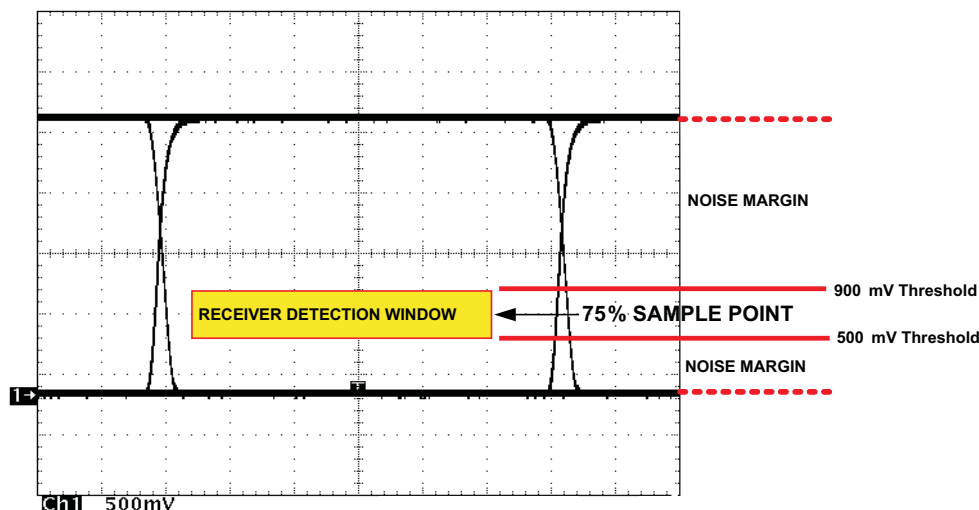


Figure 40. Typical SN65HVD230 Differential Output Voltage Waveform

The CAN driver creates the differential voltage between CANH and CANL in the dominant state. The dominant differential output of the SN65HVD23x is greater than 1.5 V and less than 3 V across a 60 ohm load as defined by the ISO 11898 standard. These are the same limiting values for 5 V supplied CAN transceivers. The bus termination resistors drive the recessive bus state and not the CAN driver.

A CAN receiver is required to output a recessive state when less than 500 mV of differential voltage exists on the bus, and a dominant state when more than 900 mV of differential voltage exists on the bus. The CAN receiver must do this with common-mode input voltages from –2 V to 7 V. The SN65HVD23x family receivers meet these same input specifications as 5 V supplied receivers.

11.3.1.3 Common-Mode Signal

A common-mode signal is an average voltage of the two signal wires that the differential receiver rejects. The common-mode signal comes from the CAN driver, ground noise, and coupled bus noise. Since the bias voltage of the recessive state of the device is dependent on V_{CC} , any noise present or variation of V_{CC} will have an effect on this bias voltage seen by the bus. The SN65HVD23x family has the recessive bias voltage set higher than $0.5 \cdot V_{CC}$ to comply with the ISO 11898-2 CAN standard. The caveat to this is that the common mode voltage will drop by a couple hundred millivolts when driving a dominant bit on the bus. This means that there is a common mode shift between the dominant bit and recessive bit states of the device. While this is not ideal, this small variation in the driver common-mode output is rejected by differential receivers and does not effect data, signal noise margins or error rates.

11.3.1.4 Interoperability of 3.3-V CAN in 5-V CAN Systems

The 3.3-V supplied SN65HVD23x family of CAN transceivers are fully compatible with 5-V CAN transceivers. The differential output voltage is the same, the recessive common mode output bias is the same, and the receivers have the same input specifications. The only slight difference is in the dominant common mode output voltage which is a couple hundred millivolts lower for 3.3-V CAN transceiver than 5-V supplied transceiver.

To help ensure the widest interoperability possible, the SN65HVD23x family has successfully passed the internationally recognized GIFT/ICT conformance and interoperability testing for CAN transceivers. Electrical interoperability does not always assure interchangeability however. Most implementers of CAN buses recognize that ISO 11898 does not sufficiently specify the electrical layer and that strict standard compliance alone does not ensure full interchangeability. This comes only with thorough equipment testing.

12 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100-nF ceramic capacitor located as close to the V_{CC} supply pins as possible. The TPS76333 is a linear voltage regulator suitable for the 3.3 V supply.

13 Layout

13.1 Layout Guidelines

In order for the PCB design to be successful, start with design of the protection and filtering circuitry. Because ESD and EFT transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high frequency layout techniques must be applied during PCB design. On chip IEC ESD protection is good for laboratory and portable equipment but is usually not sufficient for EFT and surge transients occurring in industrial environments. Therefore robust and reliable bus node design requires the use of external transient protection devices at the bus connectors. Placement at the connector also prevents these harsh transient events from propagating further into the PCB and system.

Use V_{CC} and ground planes to provide low inductance.

NOTE

High frequency current follows the path of least inductance and not the path of least resistance.

Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device.

An example placement of the Transient Voltage Suppression (TVS) device indicated as D1 (either bi-directional diode or varistor solution) and bus filter capacitors C8 and C9 are shown in [Figure 41](#).

The bus transient protection and filtering components should be placed as close to the bus connector, J1, as possible. This prevents transients, ESD and noise from penetrating onto the board and disturbing other devices.

Bus termination: [Figure 41](#) shows split termination. This is where the termination is split into two resistors, R5 and R6, with the center or split tap of the termination connected to ground via capacitor C7. Split termination provides common mode filtering for the bus. When termination is placed on the board instead of directly on the bus, care must be taken to ensure the terminating node is not removed from the bus as this will cause signal integrity issues of the bus is not properly terminated on both ends. See the application section for information on power ratings needed for the termination resistor(s).

Bypass and bulk capacitors should be placed as close as possible to the supply pins of transceiver, examples C2, C3 (V_{CC}).

Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.

To limit current of digital lines, serial resistors may be used. Examples are R1, R2, R3 and R4.

To filter noise on the digital IO lines, a capacitor may be used close to the input side of the IO as shown by C1 and C4.

Since the internal pullup and pulldown biasing of the device is weak for floating pins, an external 1-k Ω to 10-k Ω pullup or pulldown resistor should be used to bias the state of the pin more strongly against noise during transient events.

Pin 1: If an open drain host processor is used to drive the D pin of the device an external pull-up resistor between 1 k Ω and 10 k Ω and V_{CC} should be used to drive the recessive input state of the device.

Pin 8: is shown assuming the mode pin, RS, will be used. If the device will only be used in normal mode or slope control mode, R3 is not needed and the pads of C4 could be used for the pulldown resistor to GND.

13.2 Layout Example

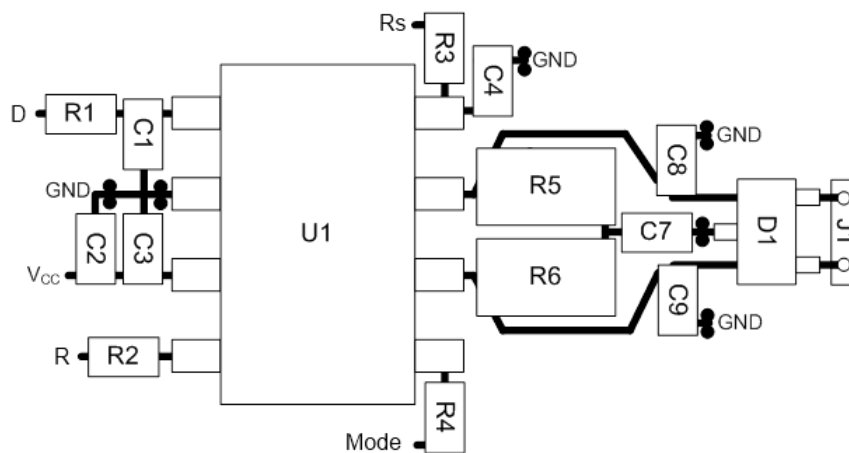


Figure 41. Layout Example Schematic

14 器件和文档支持

14.1 相关链接

下表列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 7. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持和社区
SN65HVD233	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
SN65HVD234	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
SN65HVD235	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

14.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的 [通知我](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

14.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

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设计支持 *TI 参考设计支持* 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

14.4 商标

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14.5 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

14.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

15 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65HVD233D	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-40 to 125	VP233
SN65HVD233DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VP233
SN65HVD234D	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-40 to 125	VP234
SN65HVD234DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VP234
SN65HVD235D	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-40 to 125	VP235
SN65HVD235DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VP235

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN65HVD233, SN65HVD234, SN65HVD235 :

- Automotive : [SN65HVD233-Q1](#), [SN65HVD234-Q1](#), [SN65HVD235-Q1](#)
- Enhanced Product : [SN65HVD233-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD233DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD234DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD235DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD233DR	SOIC	D	8	2500	353.0	353.0	32.0
SN65HVD234DR	SOIC	D	8	2500	353.0	353.0	32.0
SN65HVD235DR	SOIC	D	8	2500	353.0	353.0	32.0



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



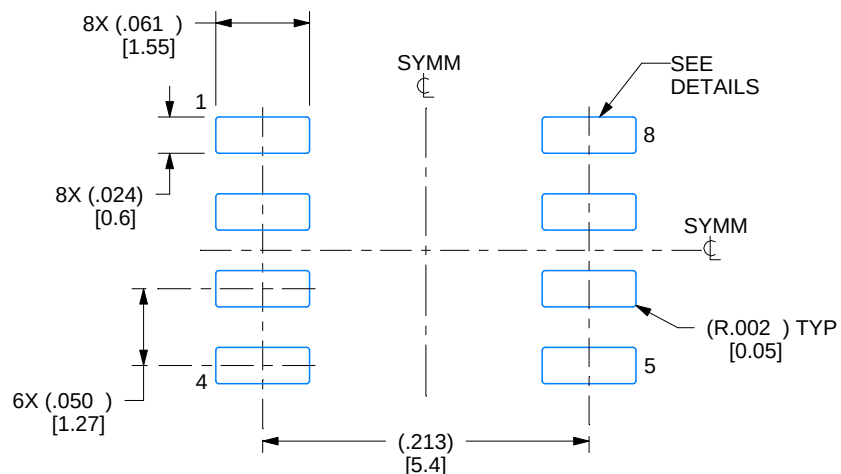
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

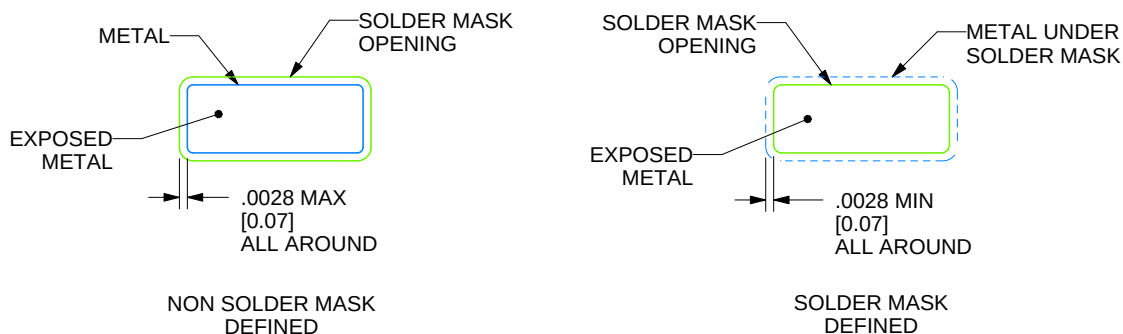
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

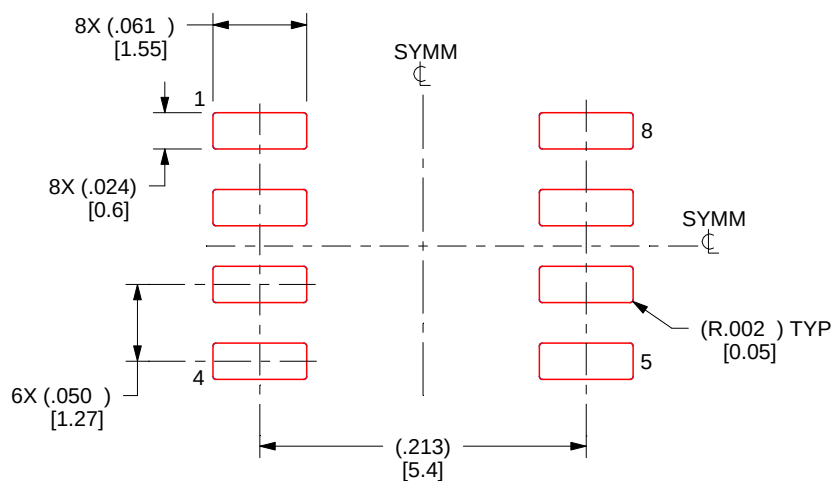
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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