74LVC4T3144

4-bit dual supply buffer/line driver; 3-state

Rev. 3 — 22 February 2024 Product data sheet

1. General description

The 74LVC4T3144 is a 4-bit, dual-supply level translating buffer with 3-state outputs. It features four data inputs (An and B4), four data outputs (YBn and YA4), and an output enable input ($\overline{OE}$). The device is configured to translate three inputs from $V_{CC(A)}$ to $V_{CC(B)}$ and one input from $V_{CC(B)}$ to $V_{CC(A)}$. $\overline{OE}$, An and YA4 are referenced to $V_{CC(A)}$ and YBn and B4 are referenced to $V_{CC(B)}$. A HIGH on $\overline{OE}$ causes the outputs to assume a high-impedance OFF-state.

The device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables outputs, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either $V_{CC(A)}$ or $V_{CC(B)}$ are at GND level, all outputs are in the high-impedance OFF-state.

2. Features and benefits

- Wide supply voltage range:
  - $V_{CC(A)}$: 1.2 V to 5.5 V
  - $V_{CC(B)}$: 1.2 V to 5.5 V
- High noise immunity
- Maximum data rates:
  - 200 Mbps (3.3 V to 5.0 V translation)
  - 140 Mbps (translate to 3.3 V))
  - 100 Mbps (translate to 2.5 V)
  - 75 Mbps (translate to 1.8 V)
  - 60 Mbps (translate to 1.5 V)
- Suspend mode
- Latch-up performance exceeds 100 mA per JESD 78B Class II
- ±24 mA output drive (V_{CC} = 3.0 V)
- Inputs accept voltages up to 5.5 V
- Low power consumption: 30 μA maximum I_{CC}
- I_{OFF} circuitry provides partial Power-down mode operation
- Complies with JEDEC standards:
  - JESD8-11A (1.4 V to 1.6 V)
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8C (3.0 V to 3.6 V)
  - JESD12-6 (4.5 V to 5.5 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC4T3144PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

4. Functional diagram

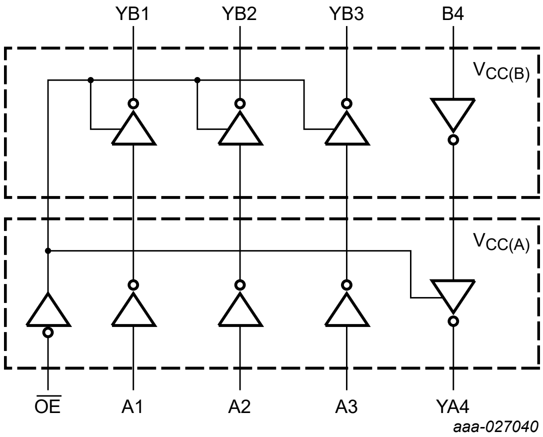
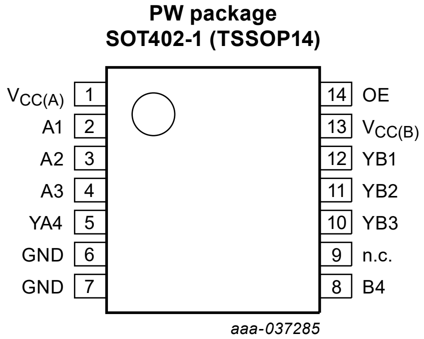


Fig. 1. Logic symbol

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$V_{CC(A)}$	1	supply voltage A (An inputs, YA4 output and $\overline{OE}$ input are referenced to $V_{CC(A)}$)
A1, A2, A3	2, 3, 4	data input
YA4	5	data output
GND	6, 7	ground (0 V)
B4	8	data input
n.c.	9	not connected
YB3, YB2, YB1	10, 11, 12	data output
$V_{CC(B)}$	13	supply voltage B (YBn outputs and B4 input are referenced to $V_{CC(B)}$)
$\overline{OE}$	14	output enable input (active LOW)

6. Functional description

Table 3. Function table [1]

Supply voltage	Control	Input	Output
$V_{CC(A)}$, $V_{CC(B)}$	**$\overline{OE}$ [2]**	**An, B4[2]**	**YBn, YA4[2]**
1.2 V to 5.5 V	L	L	L
1.2 V to 5.5 V	L	H	H
1.2 V to 5.5 V	H	X	Z
GND[3]	X	X	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.
[2] The An inputs, YA4 output and $\overline{OE}$ input are referenced to $V_{CC(A)}$; The YBn outputs and B4 input are referenced to $V_{CC(B)}$.
[3] If at least one of $V_{CC(A)}$ or $V_{CC(B)}$ is at GND level, the device goes into suspend mode.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CC(A)}$	supply voltage A			-0.5	+6.5	V
$V_{CC(B)}$	supply voltage B			-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V		-50	-	mA
V_I	input voltage		[1]	-0.5	+6.5	V
I_{OK}	output clamping current	$V_O < 0$ V		-50	-	mA
V_O	output voltage	Active mode	[1] [2] [3]	-0.5	V_{CCO} + 0.5	V
		Suspend or 3-state mode	[1]	-0.5	+6.5	V
I_O	output current	V_O = 0 V to V_{CCO}	[2]	-	±50	mA
I_{CC}	supply current	$I_{CC(A)}$ or $I_{CC(B)}$; per V_{CC} pin		-	100	mA
I_{GND}	ground current	per GND pin		-100	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[4]	-	500	mW

[1] The minimum input voltage ratings and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] V_{CCO} is the supply voltage associated with the output port.
[3] V_{CCO} + 0.5 V should not exceed 6.5 V.
[4] For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CC(A)}$	supply voltage A			1.2	5.5	V
$V_{CC(B)}$	supply voltage B			1.2	5.5	V
V_I	input voltage			0	5.5	V
V_O	output voltage	Active mode	[1]	0	V_{CCO}	V
		Suspend or 3-state mode		0	5.5	V
T_{amb}	ambient temperature			-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CCI} = 1.2 V	[2]	-	20	ns/V
		V_{CCI} = 1.4 V to 1.95 V		-	20	ns/V
		V_{CCI} = 2.3 V to 2.7 V		-	20	ns/V
		V_{CCI} = 3 V to 3.6 V		-	10	ns/V
		V_{CCI} = 4.5 V to 5.5 V		-	5	ns/V

[1] V_{CCO} is the supply voltage associated with the output port.
[2] V_{CCI} is the supply voltage associated with the input port.

9. Static characteristics

Table 6. Typical static characteristics at T_{amb} = 25 °C

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	YBn, YA4; V_I = V_{IH} or V_{IL}	[1]				
		I_O = -3 mA; V_{CCO} = 1.2 V		-	1.09	-	V
V_{OL}	LOW-level output voltage	YBn, YA4; V_I = V_{IH} or V_{IL}					
		I_O = 3 mA; V_{CCO} = 1.2 V	[1]	-	0.07	-	V
I_I	input leakage current	An, B4 and $\overline{OE}$ input; V_I = 0 V to 5.5 V; V_{CCI} = 1.2 V to 5.5 V	[2]	-	-	±1	µA
I_{OZ}	OFF-state output current	YBn, YA4; V_O = 0 V or V_{CCO}; V_{CCO} = 1.2 V to 5.5 V	[1]	-	-	±1	µA
		YBn, YA4; suspend mode; V_O = 0 V or V_{CCO}; $V_{CC(A)}$ = 5.5 V; $V_{CC(B)}$ = 0 V	[1]	-	-	±1	µA
		YBn, YA4; suspend mode; V_O = 0 V or V_{CCO}; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 5.5 V	[1]	-	-	±1	µA
I_{OFF}	power-off leakage current	A port; V_I or V_O = 0 V to 5.5 V; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 1.2 V to 5.5 V		-	-	±1	µA
		B port; V_I or V_O = 0 V to 5.5 V; $V_{CC(B)}$ = 0 V; $V_{CC(A)}$ = 1.2 V to 5.5 V		-	-	±1	µA
C_I	input capacitance	An, B4 and $\overline{OE}$ input; V_I = 0 V or 3.3 V; $V_{CC(A)}$ = 3.3 V; $V_{CC(B)}$ = 3.3 V		-	3	-	pF
C_O	output capacitance	YBn, YA4 output; V_O = 0 V or 3.3 V; $\overline{OE}$ input = 3.3 V; $V_{CC(A)}$ = 3.3 V; $V_{CC(B)}$ = 3.3 V		-	6.5	-	pF

[1] V_{CCO} is the supply voltage associated with the output port.
[2] V_{CCI} is the supply voltage associated with the input port.

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		-40 °C to +85 °C		-40 °C to +125 °C		Unit
				Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	data input	[1]					
		V_{CCI} = 1.2 V		$0.8V_{CCI}$	-	$0.8V_{CCI}$	-	V
		V_{CCI} = 1.4 V to 1.95 V		$0.65V_{CCI}$	-	$0.65V_{CCI}$	-	V
		V_{CCI} = 2.3 V to 2.7 V		1.7	-	1.7	-	V
		V_{CCI} = 3.0 V to 3.6 V		2.0	-	2.0	-	V
		V_{CCI} = 4.5 V to 5.5 V		$0.7V_{CCI}$	-	$0.7V_{CCI}$	-	V
		$\overline{OE}$ input						
		V_{CCI} = 1.2 V		$0.8V_{CC(A)}$	-	$0.8V_{CC(A)}$	-	V
		V_{CCI} = 1.4 V to 1.95 V		$0.65V_{CC(A)}$	-	$0.65V_{CC(A)}$	-	V
		V_{CCI} = 2.3 V to 2.7 V		1.7	-	1.7	-	V
		V_{CCI} = 3.0 V to 3.6 V		2.0	-	2.0	-	V
		V_{CCI} = 4.5 V to 5.5 V		$0.7V_{CC(A)}$	-	$0.7V_{CC(A)}$	-	V

Symbol	Parameter	Conditions		-40 °C to +85 °C		-40 °C to +125 °C		Unit
				Min	Max	Min	Max	
V_{IL}	LOW-level input voltage	data input	[1]					
		V_{CCI} = 1.2 V		-	$0.2V_{CCI}$	-	$0.2V_{CCI}$	V
		V_{CCI} = 1.4 V to 1.95 V		-	$0.35V_{CCI}$	-	$0.35V_{CCI}$	V
		V_{CCI} = 2.3 V to 2.7 V		-	0.7	-	0.7	V
		V_{CCI} = 3.0 V to 3.6 V		-	0.8	-	0.8	V
		V_{CCI} = 4.5 V to 5.5 V		-	$0.3V_{CCI}$	-	$0.3V_{CCI}$	V
		$\overline{OE}$ input						
		V_{CCI} = 1.2 V		-	$0.2V_{CC(A)}$	-	$0.2V_{CC(A)}$	V
		V_{CCI} = 1.4 V to 1.95 V		-	$0.35V_{CC(A)}$	-	$0.35V_{CC(A)}$	V
		V_{CCI} = 2.3 V to 2.7 V		-	0.7	-	0.7	V
		V_{CCI} = 3.0 V to 3.6 V		-	0.8	-	0.8	V
		V_{CCI} = 4.5 V to 5.5 V		-	$0.3V_{CC(A)}$	-	$0.3V_{CC(A)}$	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$						
		I_O = -100 μA; V_{CCO} = 1.2 V to 4.5 V	[2]	V_{CCO} - 0.1	-	V_{CCO} - 0.1	-	V
		I_O = -6 mA; V_{CCO} = 1.4 V		1.0	-	1.0	-	V
		I_O = -8 mA; V_{CCO} = 1.65 V		1.2	-	1.2	-	V
		I_O = -12 mA; V_{CCO} = 2.3 V		1.9	-	1.9	-	V
		I_O = -24 mA; V_{CCO} = 3.0 V		2.4	-	2.4	-	V
		I_O = -24 mA; V_{CCO} = 4.5 V		3.85	-	3.85	-	V
		I_O = -32 mA; V_{CCO} = 4.5 V		3.8	-	3.8	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IL}$	[2]					
		I_O = 100 μA; V_{CCO} = 1.2 V to 4.5 V		-	0.1	-	0.1	V
		I_O = 6 mA; V_{CCO} = 1.4 V		-	0.3	-	0.3	V
		I_O = 8 mA; V_{CCO} = 1.65 V		-	0.45	-	0.45	V
		I_O = 12 mA; V_{CCO} = 2.3 V		-	0.3	-	0.3	V
		I_O = 24 mA; V_{CCO} = 3.0 V		-	0.55	-	0.55	V
		I_O = 24 mA; V_{CCO} = 4.5 V		-	0.50	-	0.50	V
		I_O = 32 mA; V_{CCO} = 4.5 V		-	0.55	-	0.55	V
I_I	input leakage current	V_I = 0 V to 5.5 V; V_{CCI} = 1.2 V to 5.5 V		-	±2	-	±10	μA
I_{OZ}	OFF-state output current	V_O = 0 V or V_{CCO}; V_{CCO} = 1.2 V to 5.5 V	[2]	-	±2	-	±10	μA
		suspend mode; V_O = 0 V or V_{CCO}; $V_{CC(A)}$ = 5.5 V; $V_{CC(B)}$ = 0 V	[2]	-	±2	-	±10	μA
		suspend mode; V_O = 0 V or V_{CCO}; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 5.5 V	[2]	-	±2	-	±10	μA
I_{OFF}	power-off leakage current	A port; V_I or V_O = 0 V to 5.5 V; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 1.2 V to 5.5 V		-	±2	-	±10	μA
		B port; V_I or V_O = 0 V to 5.5 V; $V_{CC(B)}$ = 0 V; $V_{CC(A)}$ = 1.2 V to 5.5 V		-	±2	-	±10	μA

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
I_{CC}	supply current	A port; V_I = 0 V or V_{CCI}; I_O = 0 A [1]					
		$V_{CC(A)}$, $V_{CC(B)}$ = 1.2 V to 5.5 V	-	15	-	20	µA
		$V_{CC(A)}$ = 5.5 V; $V_{CC(B)}$ = 0 V	-	15	-	20	µA
		$V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 5.5 V	-2	-	-4	-	µA
		B port; V_I = 0 V or V_{CCI}; I_O = 0 A					
		$V_{CC(A)}$, $V_{CC(B)}$ = 1.2 V to 5.5 V	-	15	-	20	µA
		$V_{CC(B)}$ = 0 V; $V_{CC(A)}$ = 5.5 V	-2	-	-4	-	µA
		$V_{CC(B)}$ = 5.5 V; $V_{CC(A)}$ = 0 V	-	15	-	20	µA
		A plus B port ($I_{CC(A)}$ + $I_{CC(B)}$); I_O = 0 A; V_I = 0 V or V_{CCI}					
		$V_{CC(A)}$, $V_{CC(B)}$ = 1.2 V to 5.5 V	-	25	-	30	µA
ΔI_{CC}	additional supply current	per input; $V_{CC(A)}$, $V_{CC(B)}$ = 3.0 V to 5.5 V					
		$\overline{OE}$ input; $\overline{OE}$ input at $V_{CC(A)}$ - 0.6 V; A port at $V_{CC(A)}$ or GND; B port = open	-	50	-	75	µA
		A port; A port at $V_{CC(A)}$ - 0.6 V; B port = open	-	50	-	75	µA
		B port; B port at $V_{CC(B)}$ - 0.6 V; A port = open	-	50	-	75	µA

[1] V_{CCI} is the supply voltage associated with the input port.
[2] V_{CCO} is the supply voltage associated with the output port.

10. Dynamic characteristics

Table 8. Typical dynamic characteristics at $V_{CC(A)}$ = 1.2 V and T_{amb} = 25 °C [1]
Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 4; for waveforms see Fig. 2 and Fig. 3.

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	
t_{pd}	propagation delay	An to YBn	15.6	11.6	9.8	7.8	6.9	6.3	ns
		B4 to YA4	15.6	14.5	14.0	13.5	13.3	13.8	ns
t_{dis}	disable time	$\overline{OE}$ to YA4	8.7	8.7	8.7	8.7	8.7	8.7	ns
		$\overline{OE}$ to YBn	11.9	9.2	8.7	7.4	7.7	6.8	ns
t_{en}	enable time	$\overline{OE}$ to YA4	17.5	17.5	17.5	17.5	17.5	17.5	ns
		$\overline{OE}$ to YBn	18.3	13.6	11.5	9.5	8.8	8.5	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.

Table 9. Typical dynamic characteristics at $V_{CC(B)}$ = 1.2 V and T_{amb} = 25 °C [1]
Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 4; for waveforms see Fig. 2 and Fig. 3.

Symbol	Parameter	Conditions	$V_{CC(A)}$						Unit
			1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	
t_{pd}	propagation delay	An to YBn	15.6	14.5	14.0	13.5	13.3	13.1	ns
		B4 to YA4	15.6	11.6	9.8	7.8	6.9	6.3	ns
t_{dis}	disable time	$\overline{OE}$ to YA4	8.7	6.1	5.5	3.9	4.1	2.9	ns
		$\overline{OE}$ to YBn	11.9	10.5	9.9	9.2	8.9	8.4	ns
t_{en}	enable time	$\overline{OE}$ to YA4	17.5	11.6	9.0	5.7	4.6	3.8	ns
		$\overline{OE}$ to YBn	18.3	17.0	16.4	15.8	15.6	15.4	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.

Table 10. Typical power dissipation capacitance at $V_{CC(A)}$ = $V_{CC(B)}$ and T_{amb} = 25 °C [1] [2]
Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	$V_{CC(A)}$ and $V_{CC(B)}$						Unit
			1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	
C_{PD}	power dissipation capacitance	inputs An, B4	0.5	0.5	0.5	0.7	0.9	1.3	pF
		outputs YBn, YA4	12	12	12	12	12	12	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}{}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}{}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}{}^2 \times f_o)$ = sum of the outputs.
[2] f_i = 10 MHz; V_I = GND to V_{CC}; $t_r = t_f$ = 1 ns; C_L = 0 pF; $R_L = \infty\ \Omega$.

Table 11. Dynamic characteristics for temperature range -40 °C to +85 °C [1]

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 4; for waveforms see Fig. 2 and Fig. 3.

Symbol	Parameter	Conditions	$V_{CC(B)}$										Unit
			1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 1.5 V ± 0.1 V													
t_{pd}	propagation delay	An to YBn	1.7	20.7	1.6	17.1	1.3	12.9	1.1	11.1	1.0	9.5	ns
		B4 to YA4	1.7	20.7	1.6	19.8	1.6	19.0	1.5	18.5	1.5	18.3	ns
t_{dis}	disable time	$\overline{OE}$ to YA4	1.3	11.6	1.3	11.6	1.3	11.6	1.3	11.6	1.3	11.6	ns
		$\overline{OE}$ to YBn	1.5	14.4	1.6	13.2	1.3	10.4	1.5	10.7	1.2	9.4	ns
t_{en}	enable time	$\overline{OE}$ to YA4	2.1	21.8	2.1	21.8	2.1	21.8	2.1	21.8	2.1	21.8	ns
		$\overline{OE}$ to YBn	2.1	22.2	1.8	18.4	1.5	14.2	1.3	12.5	1.2	11.4	ns
$V_{CC(A)}$ = 1.8 V ± 0.15 V													
t_{pd}	propagation delay	An to YBn	1.6	19.8	1.4	16.2	1.2	11.9	1.0	10.2	0.9	8.5	ns
		B4 to YA4	1.6	17.1	1.4	16.2	1.3	15.3	1.2	14.9	1.2	14.5	ns
t_{dis}	disable time	$\overline{OE}$ to YA4	1.4	10.1	1.4	10.1	1.4	10.1	1.4	10.1	1.4	10.1	ns
		$\overline{OE}$ to YBn	1.4	13.7	1.5	12.3	1.2	9.5	1.4	9.7	1.1	8.2	ns
t_{en}	enable time	$\overline{OE}$ to YA4	1.8	17.2	1.8	17.2	1.8	17.2	1.8	17.2	1.8	17.2	ns
		$\overline{OE}$ to YBn	2.0	21.4	1.7	17.4	1.4	12.9	1.2	11.1	1.1	9.8	ns
$V_{CC(A)}$ = 2.5 V ± 0.2 V													
t_{pd}	propagation delay	An to YBn	1.6	19.0	1.3	15.3	1.0	11.0	0.9	9.1	0.7	7.2	ns
		B4 to YA4	1.3	12.9	1.2	11.9	1.0	11.0	0.9	10.6	0.9	10.2	ns
t_{dis}	disable time	$\overline{OE}$ to YA4	0.9	7.2	0.9	7.2	0.9	7.2	0.9	7.2	0.9	7.2	ns
		$\overline{OE}$ to YBn	1.3	12.8	1.4	11.3	1.1	8.4	1.3	8.5	1.0	6.9	ns
t_{en}	enable time	$\overline{OE}$ to YA4	1.4	11.7	1.4	11.7	1.4	11.7	1.4	11.7	1.4	11.7	ns
		$\overline{OE}$ to YBn	2.0	20.8	1.6	16.6	1.3	11.9	1.2	9.9	1.0	8.2	ns
$V_{CC(A)}$ = 3.3 V ± 0.3 V													
t_{pd}	propagation delay	An to YBn	1.5	18.5	1.2	14.9	0.9	10.6	0.8	8.5	0.7	6.6	ns
		B4 to YA4	1.1	11.1	1.0	10.2	0.9	9.1	0.8	8.5	0.7	8.1	ns
t_{dis}	disable time	$\overline{OE}$ to YA4	1.1	7.2	1.1	7.2	1.1	7.2	1.1	7.2	1.1	7.2	ns
		$\overline{OE}$ to YBn	1.2	12.3	1.3	10.9	1.0	8.0	1.2	8.0	0.9	6.3	ns
t_{en}	enable time	$\overline{OE}$ to YA4	1.2	9.3	1.2	9.3	1.2	9.3	1.2	9.3	1.2	9.3	ns
		$\overline{OE}$ to YBn	2.0	20.4	1.7	16.5	1.4	11.5	1.2	9.4	1.0	7.5	ns
$V_{CC(A)}$ = 5.0 V ± 0.5 V													
t_{pd}	propagation delay	An to YBn	1.5	18.3	1.2	14.5	0.9	10.2	0.7	8.1	0.6	6.3	ns
		B4 to YA4	1.0	9.5	0.9	8.5	0.7	7.2	0.7	6.6	0.6	6.3	ns
t_{dis}	disable time	$\overline{OE}$ to YA4	0.7	5.3	0.7	5.3	0.7	5.3	0.7	5.3	0.7	5.3	ns
		$\overline{OE}$ to YBn	1.2	12.0	1.3	10.5	0.9	7.6	1.2	7.6	0.8	5.8	ns
t_{en}	enable time	$\overline{OE}$ to YA4	1.1	7.0	1.1	7.0	1.1	7.0	1.1	7.0	1.1	7.0	ns
		$\overline{OE}$ to YBn	2.0	20.5	1.7	16.4	1.4	11.4	1.2	9.2	1.0	7.2	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.

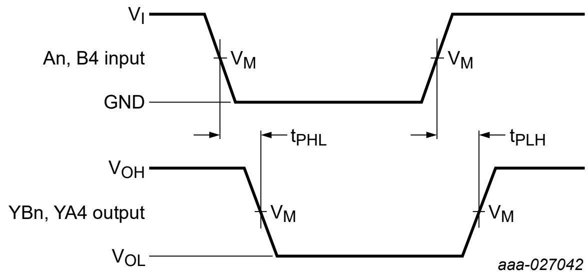
Table 12. Dynamic characteristics for temperature range -40 °C to +125 °C [1]

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 4; for waveforms see Fig. 2 and Fig. 3.

Symbol	Parameter	Conditions	$V_{CC(B)}$										Unit
			1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 1.5 V ± 0.1 V													
t_{pd}	propagation delay	An to YBn	1.7	22.0	1.6	18.3	1.3	14.0	1.1	12.2	1.0	10.5	ns
		B4 to YA4	1.7	22.0	1.6	21.0	1.6	20.1	1.5	19.5	1.5	19.4	ns
t_{dis}	disable time	$\overline{OE}$ to YA4	1.3	12.8	1.3	12.8	1.3	12.8	1.3	12.8	1.3	12.8	ns
		$\overline{OE}$ to YBn	1.5	15.8	1.6	14.5	1.3	11.5	1.5	11.1	1.2	9.7	ns
t_{en}	enable time	$\overline{OE}$ to YA4	2.1	23.2	2.1	23.2	2.1	23.2	2.1	23.2	2.1	23.2	ns
		$\overline{OE}$ to YBn	2.1	23.6	1.8	19.6	1.5	15.4	1.3	13.7	1.2	12.6	ns
$V_{CC(A)}$ = 1.8 V ± 0.15 V													
t_{pd}	propagation delay	An to YBn	1.6	21.0	1.4	17.4	1.2	13.0	1.0	11.2	0.9	9.3	ns
		B4 to YA4	1.6	18.3	1.4	17.4	1.3	16.4	1.2	16.0	1.2	15.6	ns
t_{dis}	disable time	$\overline{OE}$ to YA4	1.4	11.2	1.4	11.2	1.4	11.2	1.4	11.2	1.4	11.2	ns
		$\overline{OE}$ to YBn	1.4	15.2	1.5	13.5	1.2	10.5	1.4	10.0	1.1	8.5	ns
t_{en}	enable time	$\overline{OE}$ to YA4	1.8	18.4	1.8	18.4	1.8	18.4	1.8	18.4	1.8	18.4	ns
		$\overline{OE}$ to YBn	2.0	22.7	1.7	18.7	1.4	14.1	1.2	12.2	1.1	10.8	ns
$V_{CC(A)}$ = 2.5 V ± 0.2 V													
t_{pd}	propagation delay	An to YBn	1.6	20.1	1.3	16.4	1.0	11.9	0.9	9.9	0.7	7.9	ns
		B4 to YA4	1.3	14.0	1.2	13.0	1.0	11.9	0.9	11.5	0.9	11.1	ns
t_{dis}	disable time	$\overline{OE}$ to YA4	0.9	8.0	0.9	8.0	0.9	8.0	0.9	8.0	0.9	8.0	ns
		$\overline{OE}$ to YBn	1.3	14.0	1.4	12.5	1.1	9.3	1.3	9.3	1.0	7.5	ns
t_{en}	enable time	$\overline{OE}$ to YA4	1.4	12.7	1.4	12.7	1.4	12.7	1.4	12.7	1.4	12.7	ns
		$\overline{OE}$ to YBn	2.0	22.0	1.6	17.9	1.3	13.0	1.2	10.8	1.0	9.0	ns
$V_{CC(A)}$ = 3.3 V ± 0.3 V													
t_{pd}	propagation delay	An to YBn	1.5	19.5	1.2	16.0	0.9	11.5	0.8	9.3	0.7	7.3	ns
		B4 to YA4	1.1	12.2	1.0	11.2	0.9	9.9	0.8	9.3	0.7	8.8	ns
t_{dis}	disable time	$\overline{OE}$ to YA4	1.1	7.8	1.1	7.8	1.1	7.8	1.1	7.8	1.1	7.8	ns
		$\overline{OE}$ to YBn	1.2	13.6	1.3	12.1	1.0	8.8	1.2	8.3	0.9	6.5	ns
t_{en}	enable time	$\overline{OE}$ to YA4	1.2	10.1	1.2	10.1	1.2	10.1	1.2	10.1	1.2	10.1	ns
		$\overline{OE}$ to YBn	2.0	21.6	1.7	17.5	1.4	12.6	1.2	10.3	1.0	8.3	ns
$V_{CC(A)}$ = 5.0 V ± 0.5 V													
t_{pd}	propagation delay	An to YBn	1.5	19.4	1.2	15.6	0.9	11.1	0.7	8.8	0.6	6.8	ns
		B4 to YA4	1.0	10.5	0.9	9.3	0.7	7.9	0.7	7.3	0.6	6.8	ns
t_{dis}	disable time	$\overline{OE}$ to YA4	0.7	5.7	0.7	5.7	0.7	5.7	0.7	5.7	0.7	5.7	ns
		$\overline{OE}$ to YBn	1.2	13.3	1.3	11.7	0.9	8.4	1.2	7.9	0.8	6.0	ns
t_{en}	enable time	$\overline{OE}$ to YA4	1.1	7.7	1.1	7.7	1.1	7.7	1.1	7.7	1.1	7.7	ns
		$\overline{OE}$ to YBn	2.0	21.7	1.7	17.4	1.4	12.5	1.2	10.1	1.0	7.9	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.

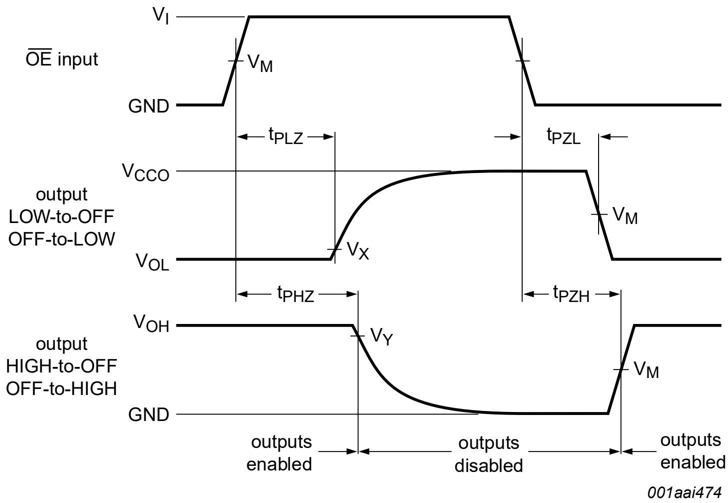
10.1. Waveforms and test circuit



Measurement points are given in Table 13.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 2. The data input (An, B4) to output (YBn, YA4) propagation delay times



Measurement points are given in Table 13.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

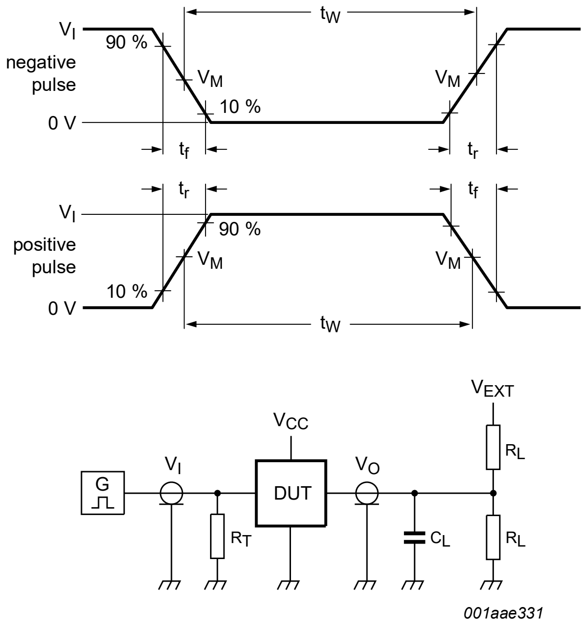
Fig. 3. Enable and disable times

Table 13. Measurement points

Supply voltage	Input [1]	Output [2]		
$V_{CC(A)}$, $V_{CC(B)}$	V_M	V_M	V_X	V_Y
1.2 V to 1.6 V	0.5 × V_{CCI}	0.5 × V_{CCO}	V_{OL} + 0.1 V	V_{OH} - 0.1 V
1.65 V to 2.7 V	0.5 × V_{CCI}	0.5 × V_{CCO}	V_{OL} + 0.15 V	V_{OH} - 0.15 V
3.0 V to 5.5 V	0.5 × V_{CCI}	0.5 × V_{CCO}	V_{OL} + 0.3 V	V_{OH} - 0.3 V

[1] V_{CCI} is the supply voltage associated with the input port.

[2] V_{CCO} is the supply voltage associated with the output port.



Test data is given in Table 14.

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance;

V_{EXT} = External voltage for measuring switching times.

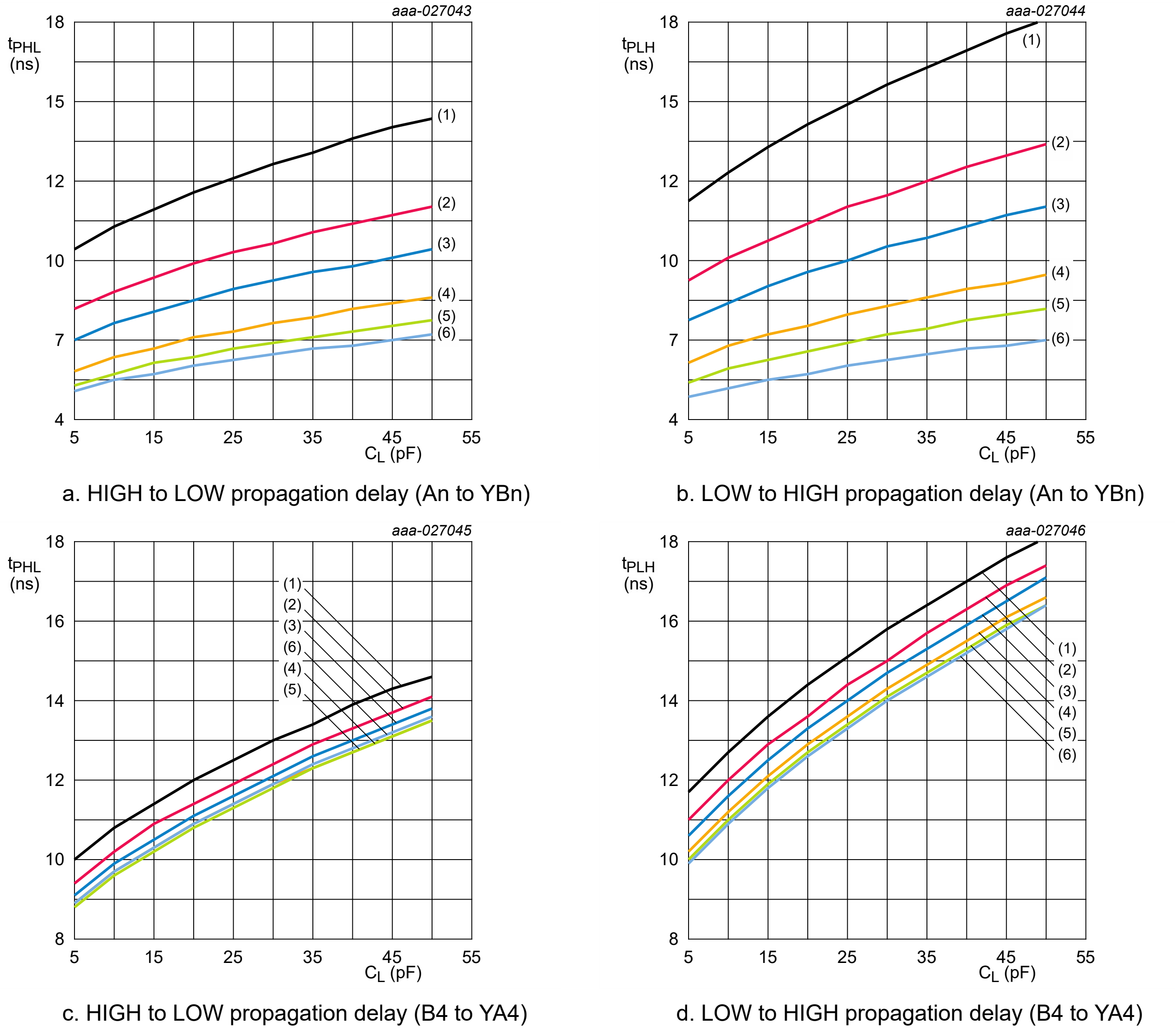
Fig. 4. Test circuit for measuring switching times

Table 14. Test data

Supply voltage	Input		Load		V_{EXT}		
$V_{CC(A)}$, $V_{CC(B)}$	V_I [1]	$\Delta t/\Delta V$ [2]	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ} [3]
1.2 V to 5.5 V	V_{CCI}	≤ 1.0 ns/V	15 pF	2 kΩ	open	GND	2 × V_{CCO}

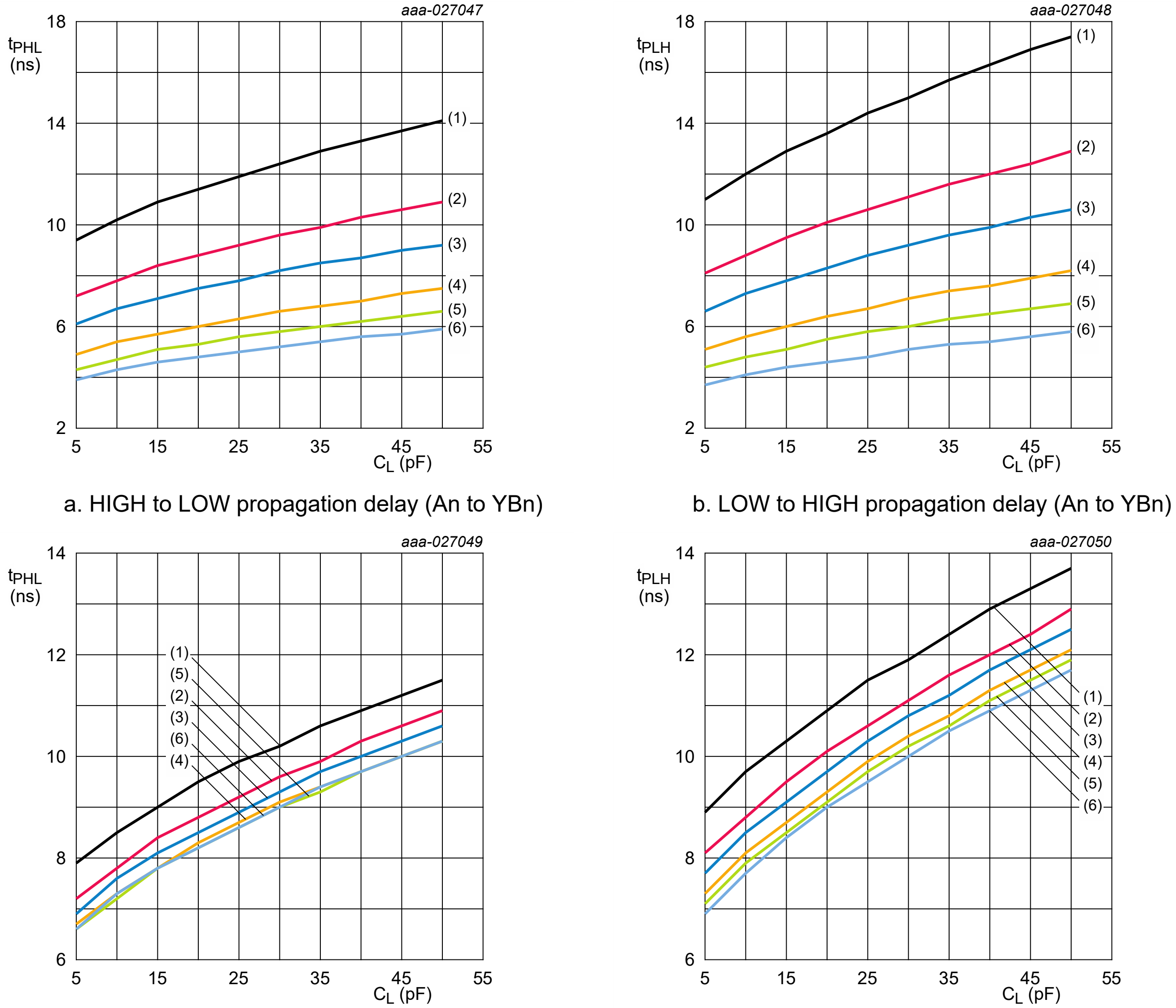
[1] V_{CCI} is the supply voltage associated with the input port.
[2] dV/dt ≥ 1.0 V/ns.
[3] V_{CCO} is the supply voltage associated with the output port.

10.2. Typical propagation delay characteristics



(1) $V_{CC(B)}$ = 1.2 V
(2) $V_{CC(B)}$ = 1.5 V
(3) $V_{CC(B)}$ = 1.8 V
(4) $V_{CC(B)}$ = 2.5 V
(5) $V_{CC(B)}$ = 3.3 V
(6) $V_{CC(B)}$ = 5.0 V

Fig. 5. Typical propagation delay versus load capacitance; T_{amb} = 25 °C; $V_{CC(A)}$ = 1.2 V



a. HIGH to LOW propagation delay (An to YBn)

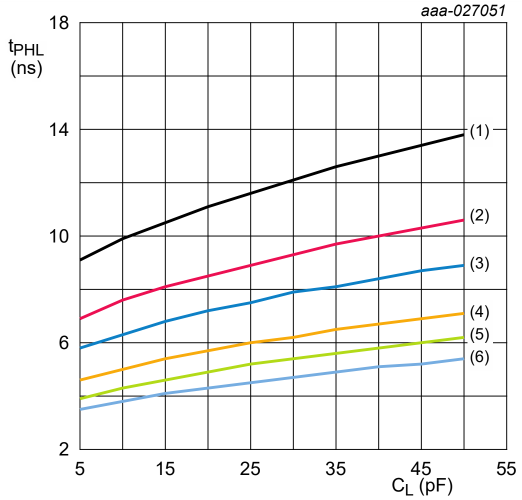
b. LOW to HIGH propagation delay (An to YBn)

c. HIGH to LOW propagation delay (B4 to YA4)

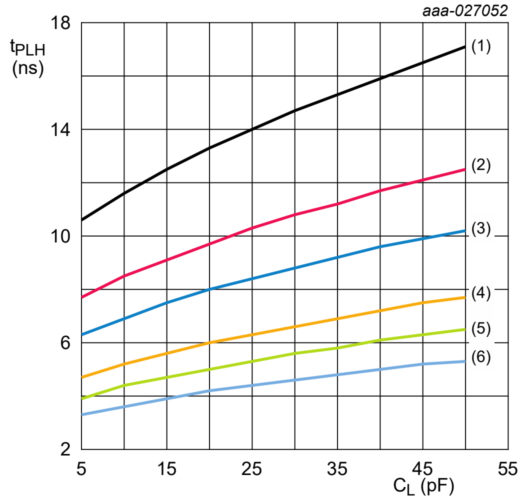
d. LOW to HIGH propagation delay (B4 to YA4)

(1) $V_{CC(B)}$ = 1.2 V
(2) $V_{CC(B)}$ = 1.5 V
(3) $V_{CC(B)}$ = 1.8 V
(4) $V_{CC(B)}$ = 2.5 V
(5) $V_{CC(B)}$ = 3.3 V
(6) $V_{CC(B)}$ = 5.0 V

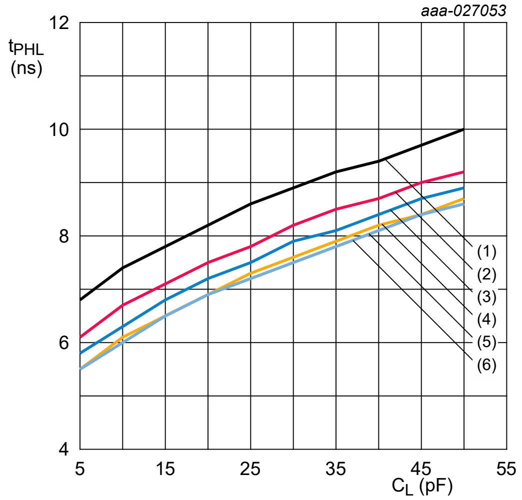
Fig. 6. Typical propagation delay versus load capacitance; T_{amb} = 25 °C; $V_{CC(A)}$ = 1.5 V



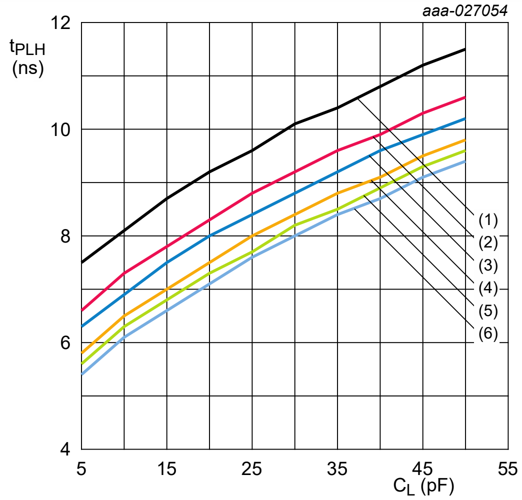
a. HIGH to LOW propagation delay (An to YBn)



b. LOW to HIGH propagation delay (An to YBn)



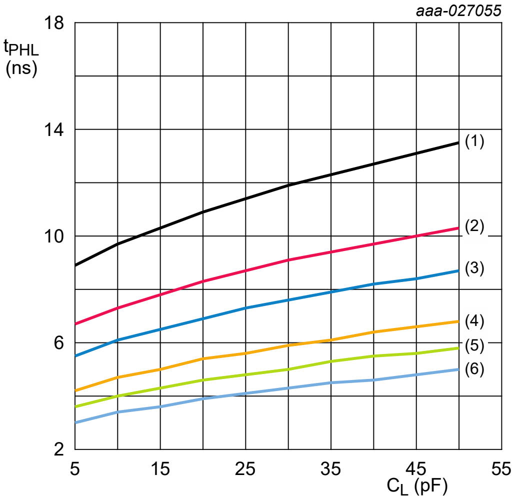
c. HIGH to LOW propagation delay (B4 to YA4)



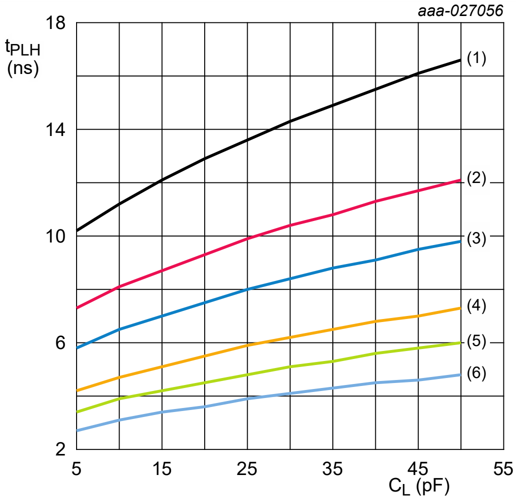
d. LOW to HIGH propagation delay (B4 to YA4)

(1) $V_{CC(B)}$ = 1.2 V
(2) $V_{CC(B)}$ = 1.5 V
(3) $V_{CC(B)}$ = 1.8 V
(4) $V_{CC(B)}$ = 2.5 V
(5) $V_{CC(B)}$ = 3.3 V
(6) $V_{CC(B)}$ = 5.0 V

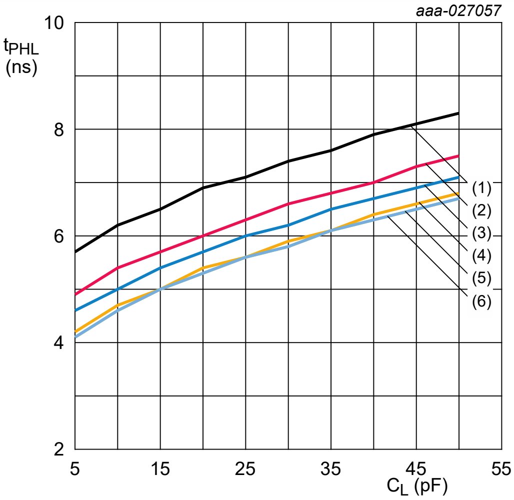
Fig. 7. Typical propagation delay versus load capacitance; T_{amb} = 25 °C; $V_{CC(A)}$ = 1.8 V



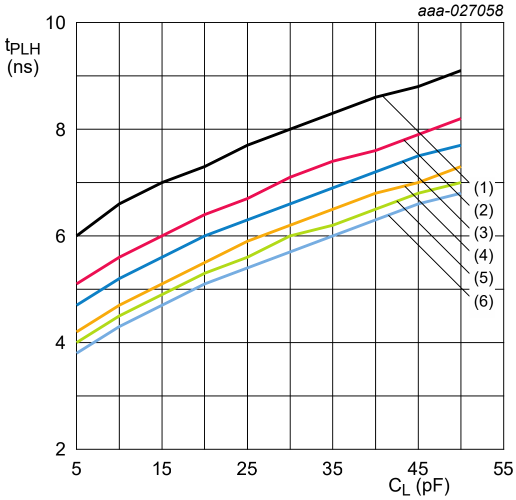
a. HIGH to LOW propagation delay (An to YBn)



b. LOW to HIGH propagation delay (An to YBn)



c. HIGH to LOW propagation delay (B4 to YA4)



d. LOW to HIGH propagation delay (B4 to YA4)

(1) $V_{CC(B)}$ = 1.2 V

(2) $V_{CC(B)}$ = 1.5 V

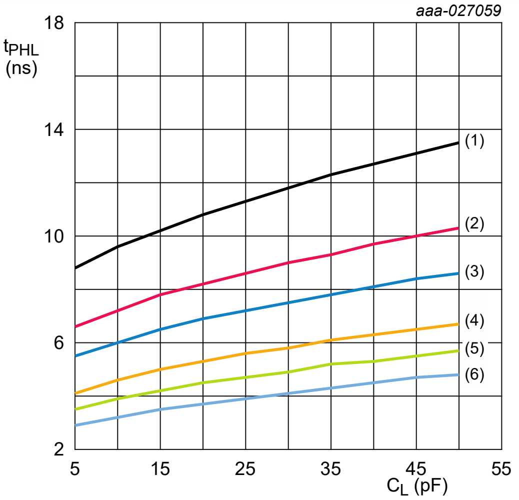
(3) $V_{CC(B)}$ = 1.8 V

(4) $V_{CC(B)}$ = 2.5 V

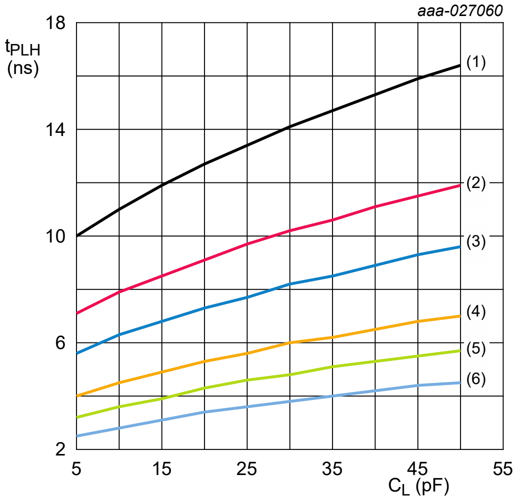
(5) $V_{CC(B)}$ = 3.3 V

(6) $V_{CC(B)}$ = 5.0 V

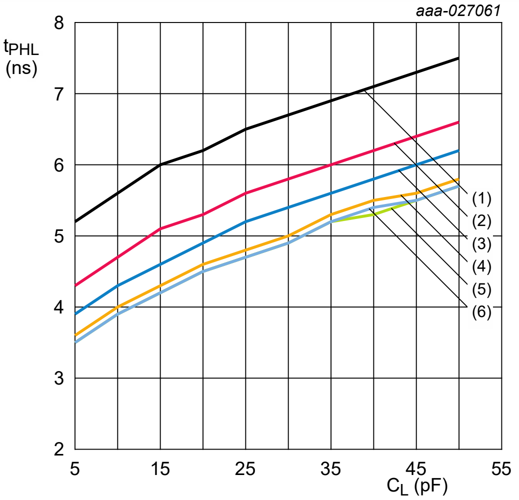
Fig. 8. Typical propagation delay versus load capacitance; T_{amb} = 25 °C; $V_{CC(A)}$ = 2.5 V



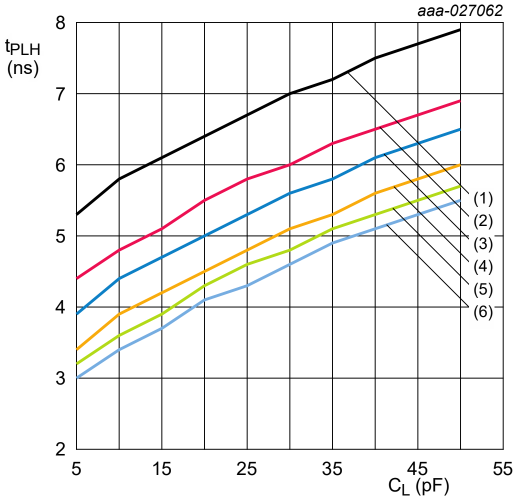
a. HIGH to LOW propagation delay (An to YBn)



b. LOW to HIGH propagation delay (An to YBn)



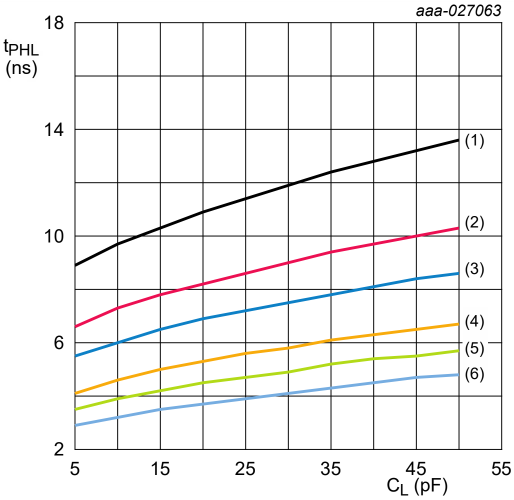
c. HIGH to LOW propagation delay (B4 to YA4)



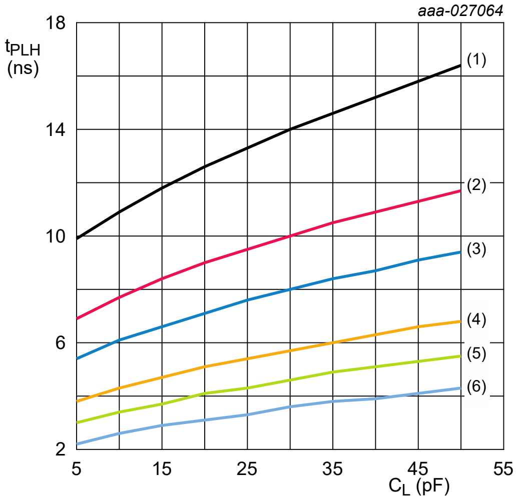
d. LOW to HIGH propagation delay (B4 to YA4)

(1) $V_{CC(B)}$ = 1.2 V
(2) $V_{CC(B)}$ = 1.5 V
(3) $V_{CC(B)}$ = 1.8 V
(4) $V_{CC(B)}$ = 2.5 V
(5) $V_{CC(B)}$ = 3.3 V
(6) $V_{CC(B)}$ = 5.0 V

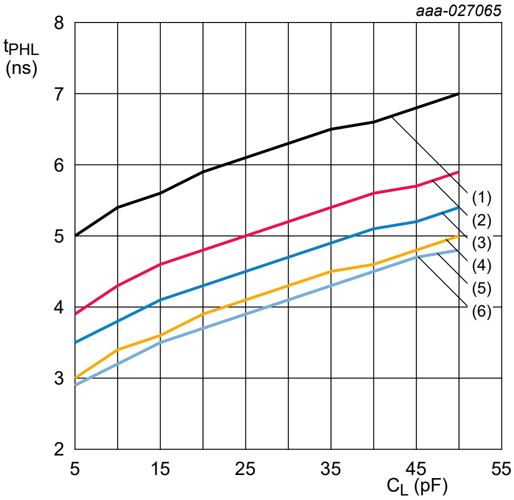
Fig. 9. Typical propagation delay versus load capacitance; T_{amb} = 25 °C; $V_{CC(A)}$ = 3.3 V



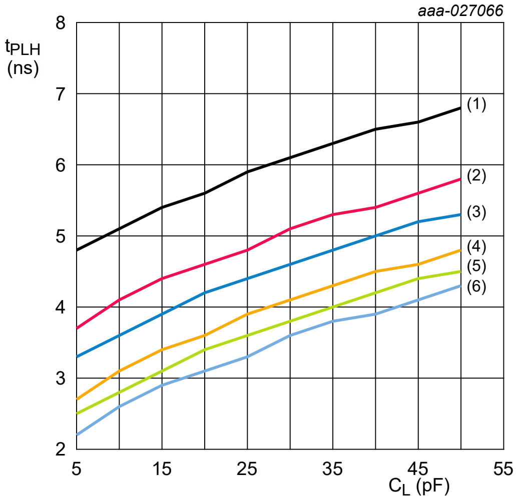
a. HIGH to LOW propagation delay (An to YBn)



b. LOW to HIGH propagation delay (An to YBn)



c. HIGH to LOW propagation delay (B4 to YA4)



d. LOW to HIGH propagation delay (B4 to YA4)

(1) $V_{CC(B)}$ = 1.2 V
(2) $V_{CC(B)}$ = 1.5 V
(3) $V_{CC(B)}$ = 1.8 V
(4) $V_{CC(B)}$ = 2.5 V
(5) $V_{CC(B)}$ = 3.3 V
(6) $V_{CC(B)}$ = 5.0 V

Fig. 10. Typical propagation delay versus load capacitance; T_{amb} = 25 °C; $V_{CC(A)}$ = 5 V

11. Application information

11.1. Unidirectional logic level-shifting application

The circuit given in Fig. 11 is an example of the 74LVC4T3144 being used in an unidirectional logic level-shifting application.

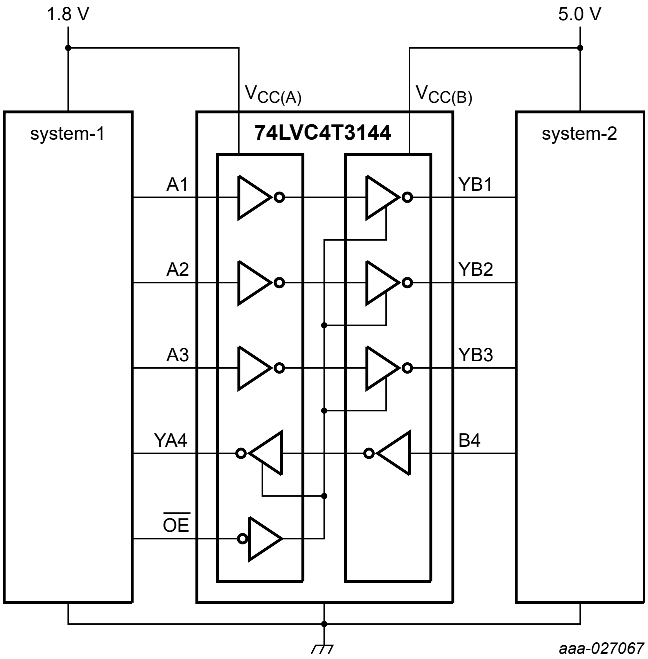


Fig. 11. Unidirectional logic level-shifting application

Table 15. Description unidirectional logic level-shifting application

Name	Description
$V_{CC(A)}$	supply voltage of system-1 (1.2 V to 5.5 V)
$V_{CC(B)}$	supply voltage of system-2 (1.2 V to 5.5 V)
A1, A2, A3	input level depends on $V_{CC(A)}$ voltage
YA4	output level depends on $V_{CC(A)}$ voltage
YB1, YB2, YB3	output level depends on $V_{CC(B)}$ voltage
B4	input level depends on $V_{CC(B)}$ voltage
$\overline{OE}$	input level depends on $V_{CC(A)}$ voltage
GND	device GND

11.2. Power-up considerations

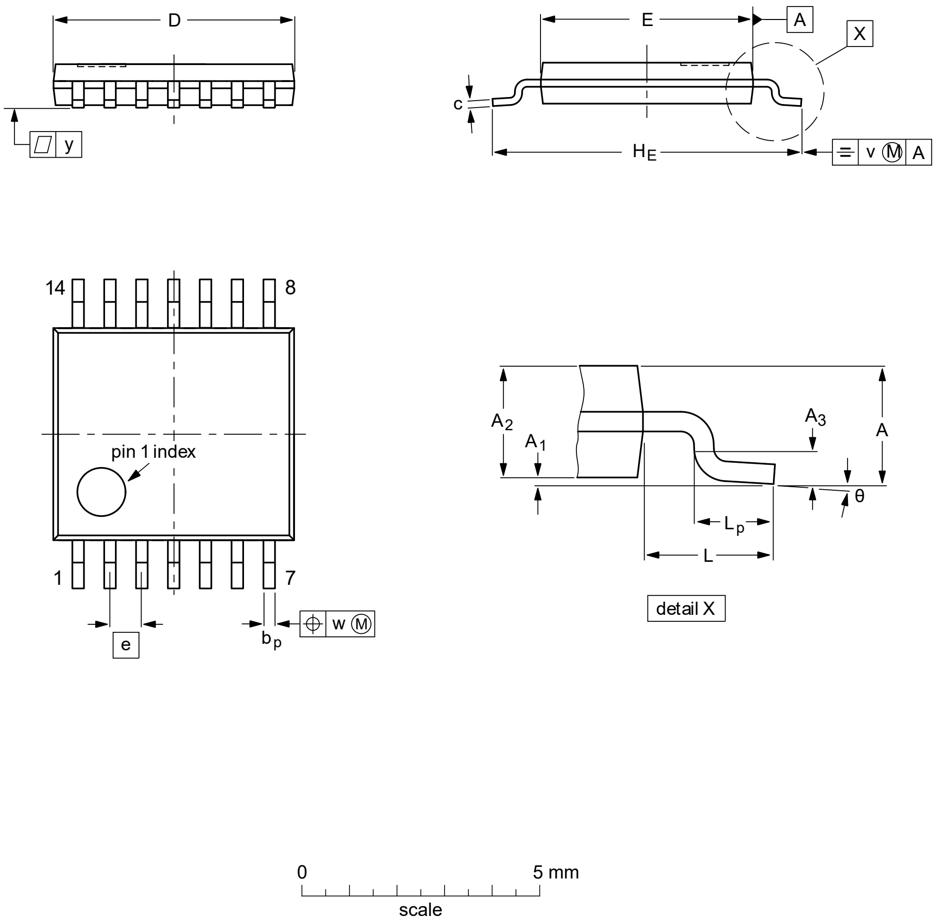
The device is designed such that no special power-up sequence is required other than GND being applied first.

Table 16. Typical total supply current ($I_{CC(A)}$ + $I_{CC(B)}$)

$V_{CC(A)}$	$V_{CC(B)}$							Unit
	0 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	
0 V	0	< 1	< 1	< 1	< 1	< 1	< 1	μA
1.2 V	< 1	< 1	< 1	< 1	< 1	< 1	1	μA
1.5 V	< 1	< 1	< 1	< 1	< 1	< 1	< 1	μA
1.8 V	< 1	< 1	< 1	< 1	< 1	< 1	< 1	μA
2.5 V	< 1	< 1	< 1	< 1	< 1	< 1	< 1	μA
3.3 V	< 1	< 1	< 1	< 1	< 1	< 1	< 1	μA
5.0 V	< 1	1	< 1	< 1	< 1	< 1	< 1	μA

12. Package outline

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.20	0.15	1.05		0.30	0.2	5.1	4.5		6.6		0.75				8°
	nom				0.25					0.65		1		0.2	0.1	0.1	
	min		0.05	0.80		0.19	0.09	4.9	4.3		6.2		0.45				0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot402-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~03-02-18~~ 23-10-27

Fig. 12. Package outline SOT402-1 (TSSOP14)

13. Abbreviations

Table 17. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

14. Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC4T3144 v.3	20240222	Product data sheet	-	74LVC4T3144 v.2
Modifications:	• Fig. 12: Aligned TSSOP package outline drawing to JEDEC MO-153.			
74LVC4T3144 v.2	20230803	Product data sheet	-	74LVC4T3144 v.1
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard. • Section 7: Derating values for P_{tot} total power dissipation updated.			
74LVC4T3144 v.1	20170814	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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