TS5A23159 1-Ω 2-Channel SPDT Analog Switch 5-V / 3.3-V 2-Channel 2:1 Multiplexer / Demultiplexer

1 Features

- Isolation in Power-Down Mode, $V_{CC} = 0$
- Specified Break-Before-Make Switching
- Low ON-State Resistance (1 Ω)
- Control Inputs are 5.5-V Tolerant
- Low Charge Injection
- Excellent ON-State Resistance Matching
- Low Total Harmonic Distortion (THD)
- Supports Analog and Digital Signals
- 1.65-V to 5.5-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Cell Phones
- PDAs
- Portable Instrumentation
- Audio and Video Signal Routing
- Low-Voltage Data-Acquisition Systems
- Communication Circuits
- Modems
- Hard Drives
- Computer Peripherals
- Wireless Terminals and Peripherals

3 Description

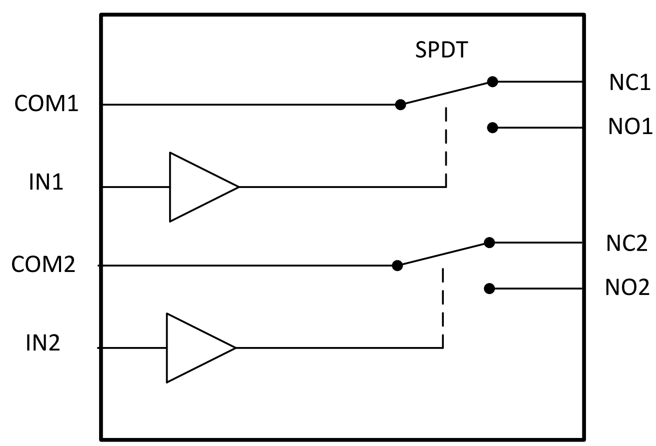
The TS5A23159 is a bidirectional 2-channel single-pole double-throw (SPDT) switch that is designed to operate from 1.65 V to 5.5 V. The device offers low ON-state resistance and excellent ON-state resistance matching with the break-before-make feature which prevents signal distortion during the transferring of a signal from one channel to another. The device has an excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for a wide variety of portable applications including cell phones, audio devices, and instrumentation.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS5A23159	VSSOP (10)	3.00 mm × 3.00 mm
	UQFN (10)	1.50 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (August 2013) to Revision H — **Page**

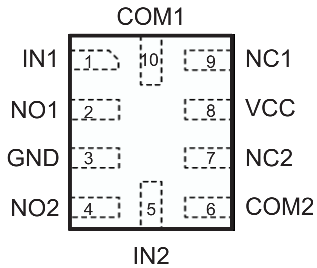
- Added *ESD Ratings* table, *Recommended Operating Conditions* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision F (September 2010) to Revision G — **Page**

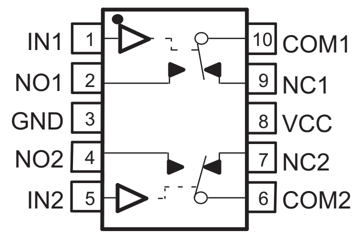
- Aligned package description throughout datasheet ... 1
- Removed *Ordering Information* table. ... 1

5 Pin Configuration and Functions

RSE Package
10-Pin UQFN
Top View



DGS Package
10-Pin VSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	IN1	I	Digital control to connect COM to NO or NC
2	NO1	I/O	Normally open
3	GND	—	Ground
4	NO2	I/O	Normally open
5	IN2	I	Digital control to connect COM to NO or NC
6	COM2	I/O	Common
7	NC2	I/O	Normally closed
8	VCC	—	Power supply
9	NC1	I/O	Normally closed
10	COM1	I/O	Common

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)(2)]

			MIN	MAX	UNIT
V_{CC}	Supply voltage[(3)]		–0.5	6.5	V
V_{NC} V_{NO} V_{COM}	Analog voltage[(3) (4) (5)]		–0.5	V_{CC} + 0.5	V
I_K	Analog port diode current	V_{NC}, V_{NO}, V_{COM} < 0	–50		mA
I_{NC} I_{NO} I_{COM}	On-state switch current	V_{NC}, V_{NO}, V_{COM} = 0 to V_{CC}	–200	200	mA
	On-state peak switch current[(6)]		–400	400	
V_{IN}	Digital input voltage[(3) (4)]		–0.5	6.5	V
I_{IK}	Digital input clamp current	V_I < 0	–50		mA
I_{CC}	Continuous current through V_{CC}			100	mA
I_{GND}	Continuous current through GND		–100	100	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) This value is limited to 5.5 V maximum.
(6) Pulse at 1-ms duration < 10% duty cycle

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply LC Voltage	0	5.5	V
V_{NC} V_{NO} V_{COM}	Analog voltage	0	V_{CC}	
V_{IN}	Digital input voltage range	0	V_{CC}	

6.4 Thermal Information

THERMAL METRIC[1]		TS5A23159		UNIT
		DGS (VSSOP)	RSE (UQFN)	
		10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	203.9	180.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	88.3	117.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	123.9	98.6	
ψ_{JT}	Junction-to-top characterization parameter	2.1	6.8	
ψ_{JB}	Junction-to-board characterization parameter	122.5	98.4	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics for 5-V Supply

V_{CC} = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
V_{COM}, V_{NO}, V_{NC}	Analog signal range					0		V_{CC}	V
R_{peak}	Peak ON resistance	0 ≤ (V_{NO} or V_{NC}) ≤ V_{CC}, I_{COM} = –100 mA,	Switch ON, See Figure 14	25°C	4.5 V		0.8	1.1	Ω
				Full				1.5	
R_{on}	ON-state resistance	V_{NO} or V_{NC} = 2.5 V, I_{COM} = –100 mA,	Switch ON, See Figure 14	25°C	4.5 V		0.7	0.9	Ω
				Full				1.1	
ΔR_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 2.5 V, I_{COM} = –100 mA,	Switch ON, See Figure 14	25°C	4.5 V		0.05	0.1	Ω
				Full				0.1	
$R_{on(flat)}$	ON-state resistance flatness	0 ≤ (V_{NO} or V_{NC}) ≤ V_{CC}, I_{COM} = –100 mA,	Switch ON, See Figure 14	25°C	4.5 V		0.15		Ω
		V_{NO} or V_{NC} = 1 V, 1.5 V, 2.5 V, I_{COM} = –100 mA,	Switch ON, See Figure 14	25°C			0.1	0.25	
				Full				0.25	
$I_{NO(OFF)}$, $I_{NC(OFF)}$	NC, NO OFF leakage current	V_{NC} or V_{NO} = 1 V, V_{COM} = 1 V to 4.5 V, or V_{NC} or V_{NO} = 4.5 V, V_{COM} = 1 V to 4.5 V,	Switch OFF, See Figure 15	25°C	5.5 V	–20	2	20	nA
				Full		–100		100	
$I_{NC(PWROFF)}$, $I_{NO(PWROFF)}$		V_{NC} or V_{NO} = 0 to 5.5 V, V_{COM} = 5.5 V to 0,	Switch OFF, See Figure 15	25°C	0 V	–1	0.2	1	µA
				Full		–20		20	
$I_{NO(ON)}$, $I_{NC(ON)}$	NC, NO ON leakage current	V_{NC} or V_{NO} = 1 V, V_{COM} = Open, or V_{NC} or V_{NO} = 4.5 V, V_{COM} = Open,	Switch ON, See Figure 16	25°C	5.5 V	–20	2	20	nA
				Full		–100		100	
$I_{COM(PWROFF)}$	COM OFF leakage current	V_{NC} or V_{NO} = 0 to 5.5 V, V_{COM} = 5.5 V to 0,	Switch OFF, See Figure 15	25°C	0 V	–1	0.1	1	µA
				Full		–20		20	
$I_{COM(ON)}$	COM ON leakage current	V_{NC} or V_{NO} = Open, V_{COM} = 1 V, or V_{NC} or V_{NO} = Open, V_{COM} = 4.5 V,	Switch ON, See Figure 16	25°C	5.5 V	–20	2	20	nA
				Full		–100		100	
DIGITAL CONTROL INPUTS (IN1, IN2)(2)									
V_{IH}	Input logic high			Full		2.4		5.5	V
V_{IL}	Input logic low			Full		0		0.8	V
I_{IH}, I_{IL}	Input leakage current	V_{IN} = 5.5 V or 0		25°C	5.5 V	–2		2	nA
				Full		–100		100	
DYNAMIC									
t_{ON}	Turnon time	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF, See Figure 18	25°C	5 V	1	8	13	ns
				Full	4.5 V to 5.5 V	1		16.5	
t_{OFF}	Turnoff time	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF, See Figure 18	25°C	5 V	1	5	8	ns
				Full	4.5 V to 5.5 V	1		8	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs,* SCBA004.

Electrical Characteristics for 5-V Supply (continued)

V_{CC} = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
t_{BBM}	Break-before-make time	$V_{NC} = V_{NO} = V_{CC}$, R_L = 50 Ω,	C_L = 35 pF, See Figure 19	25°C	5 V	1	5.5	13	ns
				Full	4.5 V to 5.5 V	1		14	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 23	25°C	5 V		–7		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	V_{NC} or V_{NO} = V_{CC} or GND, Switch OFF,	See Figure 17	25°C	5 V		18		pF
$C_{NC(ON)}$, $C_{NO(ON)}$	NC, NO ON capacitance	V_{NC} or V_{NO} = V_{CC} or GND, Switch ON,	See Figure 17	25°C	5 V		55		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_{CC} or GND, Switch ON,	See Figure 17	25°C	5 V		54.5		pF
C_I	Digital input capacitance	V_{IN} = V_{CC} or GND,	See Figure 17	25°C	5 V		2		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON,	See Figure 20	25°C	5 V		100		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 21	25°C	5 V		–64		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 22	25°C	5 V		–64		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 24	25°C	5 V		0.004%		
SUPPLY									
I_{CC}	Positive supply current	V_{IN} = V_{CC} or GND,	Switch ON or OFF	25°C	5.5 V		10	50	nA
				Full				750	

6.6 Electrical Characteristics for 3.3-V Supply

V_{CC} = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
V_{COM}, V_{NO}, V_{NC}	Analog signal range					0		V_{CC}	V
R_{peak}	Peak ON resistance	0 ≤ (V_{NO} or V_{NC}) ≤ V_{CC}, I_{COM} = –100 mA,	Switch ON, See Figure 14	25°C	3 V		1.3	1.6	Ω
				Full				2	
R_{on}	ON-state resistance	V_{NO} or V_{NC} = 2 V, I_{COM} = –100 mA,	Switch ON, See Figure 14	25°C	3 V		1.2	1.5	Ω
				Full				1.7	
ΔR_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 2 V, 0.8 V, I_{COM} = –100 mA,	Switch ON, See Figure 14	25°C	3 V		0.1	0.15	Ω
				Full			0.2		
$R_{on(flat)}$	ON-state resistance flatness	0 ≤ (V_{NO} or V_{NC}) ≤ V_{CC}, I_{COM} = –100 mA,	Switch ON, See Figure 14	25°C	3 V		0.15		Ω
		V_{NO} or V_{NC} = 2 V, 0.8 V, I_{COM} = –100 mA,	Switch ON, See Figure 14	25°C					
				Full					
$I_{NO(OFF)}$, $I_{NC(OFF)}$	NC, NO OFF leakage current	V_{NC} or V_{NO} = 1 V, V_{COM} = 1 V to 3 V, or V_{NC} or V_{NO} = 3 V, V_{COM} = 1 V to 3 V,	Switch OFF, See Figure 15	25°C	3.6 V	–20	2	20	nA
				Full		–50		50	
$I_{NC(PWROFF)}$, $I_{NO(PWROFF)}$		V_{NC} or V_{NO} = 0 to 3.6 V, V_{COM} = 3.6 V to 0,	Switch OFF, See Figure 15	25°C	0 V	–1	0.2	1	µA
				Full		–15		15	
$I_{NO(ON)}$, $I_{NC(ON)}$	NC, NO ON leakage current	V_{NC} or V_{NO} = 1 V, V_{COM} = Open, or V_{NC} or V_{NO} = 3 V, V_{COM} = Open,	Switch ON, See Figure 16	25°C	3.6 V	–10	2	10	nA
				Full		–20		20	
$I_{COM(PWROFF)}$	COM OFF leakage current	V_{NC} or V_{NO} = 3.6 V to 0, V_{COM} = 0 to 3.6 V,	Switch OFF, See Figure 15	25°C	0 V	–1	0.2	1	µA
				Full		–15		15	
$I_{COM(ON)}$	COM ON leakage current	V_{NC} or V_{NO} = Open, V_{COM} = 1 V, or V_{NC} or V_{NO} = Open, V_{COM} = 3 V,	Switch ON, See Figure 16	25°C	3.6 V	–10	2	10	nA
				Full		–20		20	
DIGITAL CONTROL INPUTS (IN1, IN2)(2)									
V_{IH}	Input logic high			Full		2		5.5	V
V_{IL}	Input logic low			Full		0		0.8	V
I_{IH}, I_{IL}	Input leakage current	V_{IN} = 5.5 V or 0		25°C	3.6 V	–2		2	nA
				Full		–20		20	
DYNAMIC									
t_{ON}	Turnon time	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF, See Figure 18	25°C	3.3 V	5	11	19	ns
				Full	3 V to 3.6 V	3		22	
t_{OFF}	Turnoff time	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF, See Figure 18	25°C	3.3 V	1	5	9	ns
				Full	3 V to 3.6 V	1		9	
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF, See Figure 19	25°C	3.3 V	1	7	17	ns
				Full	3 V to 3.6 V	1		20	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs,* SCBA004.

Electrical Characteristics for 3.3-V Supply (continued)

V_{CC} = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 23	25°C	3.3 V		–4		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	V_{NC} or V_{NO} = V_{CC} or GND, Switch OFF,	See Figure 17	25°C	3.3 V		18		pF
$C_{NC(ON)}$, $C_{NO(ON)}$	NC, NO ON capacitance	V_{NC} or V_{NO} = V_{CC} or GND, Switch ON,	See Figure 17	25°C	3.3 V		56		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_{CC} or GND, Switch ON,	See Figure 17	25°C	3.3 V		56		pF
C_I	Digital input capacitance	V_{IN} = V_{CC} or GND,	See Figure 17	25°C	3.3 V		2		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON,	See Figure 20	25°C	3.3 V		100		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 21	25°C	3.3 V		–64		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 22	25°C	3.3 V		–64		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 24	25°C	3.3 V		0.01%		
SUPPLY									
I_{CC}	Positive supply current	V_{IN} = V_{CC} or GND,	Switch ON or OFF	25°C	3.6 V			25	nA
				Full				150	

6.7 Electrical Characteristics for 2.5-V Supply(1)

V_{CC} = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
V_{COM}, V_{NO}, V_{NC}	Analog signal range					0		V_{CC}	V
R_{peak}	Peak ON resistance	0 ≤ (V_{NO} or V_{NC}) ≤ V_{CC}, I_{COM} = –8 mA,	Switch ON, See Figure 14	25°C	2.3 V		1.8	2.5	Ω
				Full				2.7	
R_{on}	ON-state resistance	V_{NO} or V_{NC} = 1.8 V, I_{COM} = –8 mA,	Switch ON, See Figure 14	25°C	2.3 V		1.5	2	Ω
				Full				2.4	
ΔR_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 1.8 V, 0.8 V, I_{COM} = –8 mA,	Switch ON, See Figure 14	25°C	2.3 V		0.15	0.2	Ω
				Full				0.2	
$R_{on(flat)}$	ON-state resistance flatness	0 ≤ (V_{NO} or V_{NC}) ≤ V_{CC}, I_{COM} = –8 mA,	Switch ON, See Figure 14	25°C	2.3 V		0.6		Ω
		V_{NO} or V_{NC} = 0.8 V, 1.8 V, I_{COM} = –8 mA,	Switch ON, See Figure 14	25°C			0.6	1	
				Full				1	
$I_{NO(OFF)}$, $I_{NC(OFF)}$	NC, NO OFF leakage current	V_{NC} or V_{NO} = 0.5 V, V_{COM} = 0.5 V to 2.3 V, or V_{NC} or V_{NO} = 2.2 V, V_{COM} = 0.5 V to 2.3 V,	Switch OFF, See Figure 15	25°C	2.3 V	–20	2	20	nA
				Full		–50		50	
$I_{NC(PWROFF)}$, $I_{NO(PWROFF)}$		V_{NC} or V_{NO} = 0 to 2.7 V, V_{COM} = 2.7 V to 0,	Switch OFF, See Figure 15	25°C	0 V	–1	0.1	1.0	µA
				Full		–10		10	
$I_{NO(ON)}$, $I_{NC(ON)}$	NC, NO ON leakage current	V_{NC} or V_{NO} = 0.5 V, V_{COM} = Open, or V_{NC} or V_{NO} = 2.2 V, V_{COM} = Open,	Switch ON, See Figure 16	25°C	2.7 V	–10	2	10	nA
				Full		–20		20	
$I_{COM(PWROFF)}$	COM OFF leakage current	V_{NC} or V_{NO} = 2.7 V to 0, V_{COM} = 0 to 2.7 V,	Switch OFF, See Figure 15	25°C	0 V	–1	0.1	1	µA
				Full		–10		10	
$I_{COM(ON)}$	COM ON leakage current	V_{NC} or V_{NO} = Open, V_{COM} = 0.5 V, or V_{NC} or V_{NO} = Open, V_{COM} = 2.2 V,	Switch ON, See Figure 16	25°C	2.7 V	–10	2	10	nA
				Full		–20		20	
DIGITAL CONTROL INPUTS (IN1, IN2)(2)									
V_{IH}	Input logic high			Full		1.8		5.5	V
V_{IL}	Input logic low			Full		0		0.6	V
I_{IH}, I_{IL}	Input leakage current	V_{IN} = 5.5 V or 0		25°C	2.7 V	–2		2	nA
				Full		–20		20	
DYNAMIC									
t_{ON}	Turnon time	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF, See Figure 18	25°C	2.5 V	5	15	28	ns
				Full	2.3 V to 2.7 V	5		32	
t_{OFF}	Turnoff time	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF, See Figure 18	25°C	2.5 V	2	6	9	ns
				Full	2.3 V to 2.7 V	2		10	
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF, See Figure 19	25°C	2.5 V	1	10	27	ns
				Full	2.3 V to 2.7 V	1		30	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs,* SCBA004.

Electrical Characteristics for 2.5-V Supply[1] (continued)

V_{CC} = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 23	25°C	2.5 V		–3		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	V_{NC} or V_{NO} = V_{CC} or GND, Switch OFF,	See Figure 17	25°C	2.5 V		18.5		pF
$C_{NC(ON)}$, $C_{NO(ON)}$	NC, NO ON capacitance	V_{NC} or V_{NO} = V_{CC} or GND, Switch ON,	See Figure 17	25°C	2.5 V		56.5		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_{CC} or GND, Switch ON,	See Figure 17	25°C	2.5 V		56.5		pF
C_I	Digital input capacitance	V_{IN} = V_{CC} or GND,	See Figure 17	25°C	2.5 V		2		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON,	See Figure 20	25°C	2.5 V		100		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 21	25°C	2.5 V		–64		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 22	25°C	2.5 V		–64		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 24	25°C	2.5 V		0.02%		
SUPPLY									
I_{CC}	Positive supply current	V_{IN} = V_{CC} or GND,	Switch ON or OFF	25°C	2.7 V		10	25	nA
				Full				100	

6.8 Electrical Characteristics for 1.8-V Supply

V_{CC} = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
V_{COM}, V_{NO}, V_{NC}	Analog signal range					0		V_{CC}	V
R_{peak}	Peak ON resistance	0 ≤ (V_{NO} or V_{NC}) ≤ V_{CC}, I_{COM} = –2 mA,	Switch ON, See Figure 14	25°C	1.65 V		5		Ω
				Full				15	
R_{on}	ON-state resistance	V_{NO} or V_{NC} = 1.5 V, I_{COM} = –2 mA,	Switch ON, See Figure 14	25°C	1.65 V		2	2.5	Ω
				Full				3.5	
ΔR_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 0.6 V, 1.5 V, I_{COM} = –2 mA,	Switch ON, See Figure 14	25°C	1.65 V		0.15	0.4	Ω
				Full				0.4	
$R_{on(flat)}$	ON-state resistance flatness	0 ≤ (V_{NO} or V_{NC}) ≤ V_{CC}, I_{COM} = –2 mA,	Switch ON, See Figure 14	25°C	1.65 V		5		Ω
		V_{NO} or V_{NC} = 0.6 V, 1.5 V, I_{COM} = –2 mA,	Switch ON, See Figure 14	25°C			4.5		
				Full					
$I_{NO(OFF)}$, $I_{NC(OFF)}$	NC, NO OFF leakage current	V_{NC} or V_{NO} = 0.3 V, V_{COM} = 0.3 V to 1.65 V, or V_{NC} or V_{NO} = 1.65 V, V_{COM} = 0.3 V to 1.65 V	Switch OFF, See Figure 15	25°C	1.65 V	–20	2	20	nA
				Full		–50		50	
$I_{NC(PWROFF)}$, $I_{NO(PWROFF)}$		V_{NC} or V_{NO} = 0 to 1.95 V, V_{COM} = 1.95 V to 0,	Switch OFF, See Figure 15	25°C	0 V	–1	0.1	1	μA
				Full		–5		5	
$I_{NO(ON)}$, $I_{NC(ON)}$	NC, NO ON leakage current	V_{NC} or V_{NO} = 0.3 V, V_{COM} = Open, or V_{NC} or V_{NO} = 1.65 V, V_{COM} = Open,	Switch ON, See Figure 16	25°C	1.95 V	–5	2	5	nA
				Full		–20		20	
$I_{COM(PWROFF)}$	COM OFF leakage current	V_{NC} or V_{NO} = 1.95 V to 0, V_{COM} = 0 to 1.95 V,	Switch OFF, See Figure 15	25°C	0 V	–1	0.1	1	μA
				Full		–5		5	
$I_{COM(ON)}$	COM ON leakage current	V_{NC} or V_{NO} = Open, V_{COM} = 0.3 V, or V_{NC} or V_{NO} = Open, V_{COM} = 1.65 V,	Switch ON, See Figure 16	25°C	1.95 V	–10	2	10	nA
				Full		–20		20	
DIGITAL CONTROL INPUTS (IN1, IN2)									
V_{IH}	Input logic high			Full		1.5		5.5	V
V_{IL}	Input logic low			Full		0		0.6	V
I_{IH}, I_{IL}	Input leakage current	V_{IN} = 5.5 V or 0		25°C	1.95 V	–2		2	nA
				Full		–20		20	
DYNAMIC									
t_{ON}	Turnon time	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF, See Figure 18	25°C	1.8 V	10	27.5	48.5	ns
				Full	1.65 V to 1.95 V	10		55	
t_{OFF}	Turnoff time	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF, See Figure 18	25°C	1.8 V	2	6.5	11	ns
				Full	1.65 V to 1.95 V	2		12	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

Electrical Characteristics for 1.8-V Supply (continued)

V_{CC} = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
t_{BBM}	Break-before-make time	$V_{NC} = V_{NO} = V_{CC}$, R_L = 50 Ω,	C_L = 35 pF, See Figure 19	25°C	1.8 V	1	18	50	ns
				Full	1.65 V to 1.95 V	1		55	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 23	25°C	1.8 V		2		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	V_{NC} or V_{NO} = V_{CC} or GND, Switch OFF,	See Figure 17	25°C	1.8 V		18.5		pF
$C_{NC(ON)}$, $C_{NO(ON)}$	NC, NO ON capacitance	V_{NC} or V_{NO} = V_{CC} or GND, Switch ON,	See Figure 17	25°C	1.8 V		56.5		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_{CC} or GND, Switch ON,	See Figure 17	25°C	1.8 V		56.5		pF
C_I	Digital input capacitance	V_{IN} = V_{CC} or GND,	See Figure 17	25°C	1.8 V		2		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON,	See Figure 20	25°C	1.8 V		105		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 21	25°C	1.8 V		–64		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 22	25°C	1.8 V		–64		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 24	25°C	1.8 V		0.06%		
SUPPLY									
I_{CC}	Positive supply current	V_{IN} = V_{CC} or GND,	Switch ON or OFF	25°C	1.95 V		10	25	nA
				Full				50	

6.9 Typical Characteristics

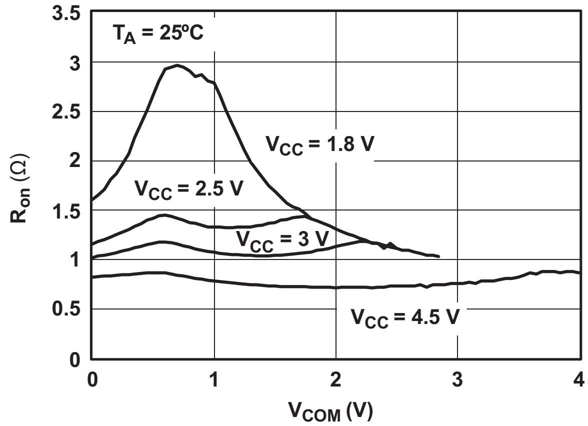


Figure 1. R_{on} vs V_{COM}

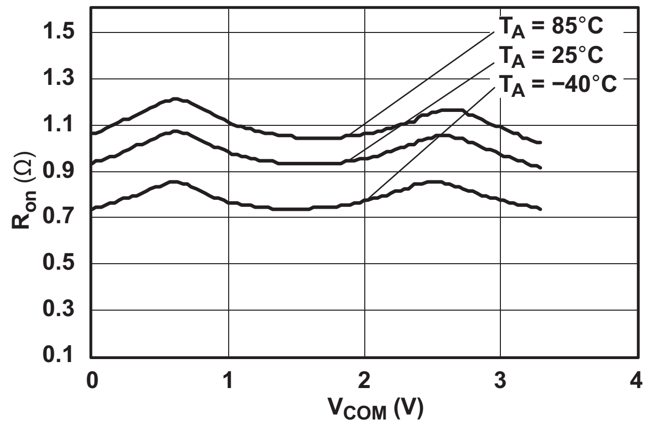


Figure 2. R_{on} vs V_{COM} (V_{CC} = 3.3 V)

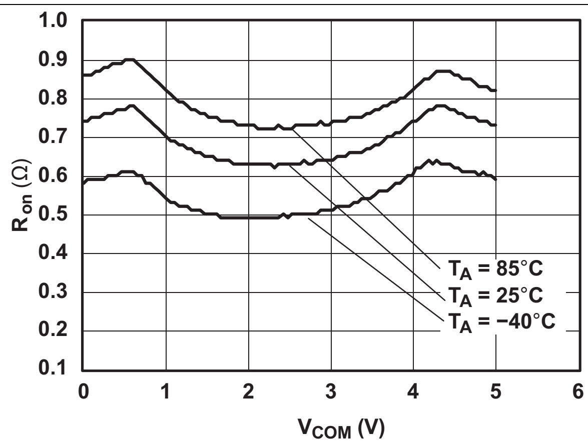


Figure 3. R_{on} vs V_{COM} (V_{CC} = 5 V)

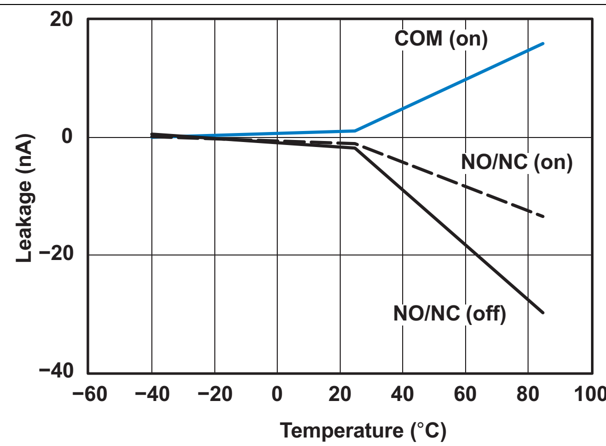


Figure 4. Leakage Current vs Temperature (V_{CC} = 3.3 V)

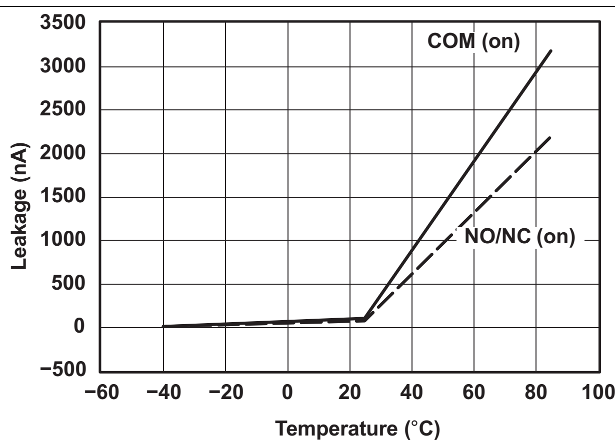


Figure 5. Leakage Current vs Temperature (V_{CC} = 5 V)

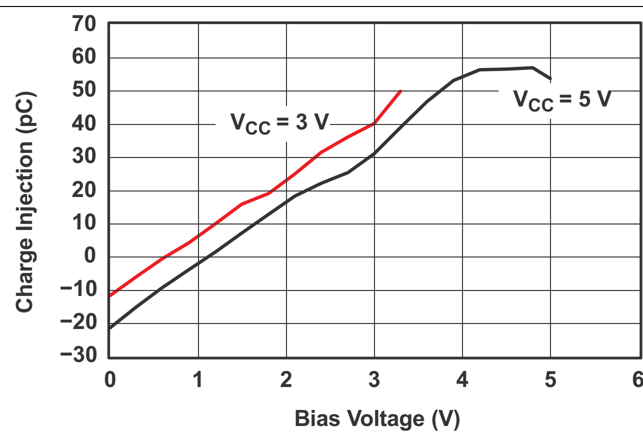


Figure 6. Charge Injection (Q_C) vs V_{COM}

Typical Characteristics (continued)

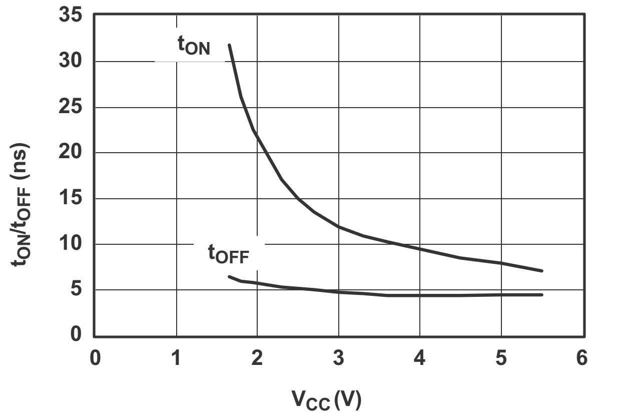


Figure 7. T_{ON} and T_{OFF} vs Supply Voltage

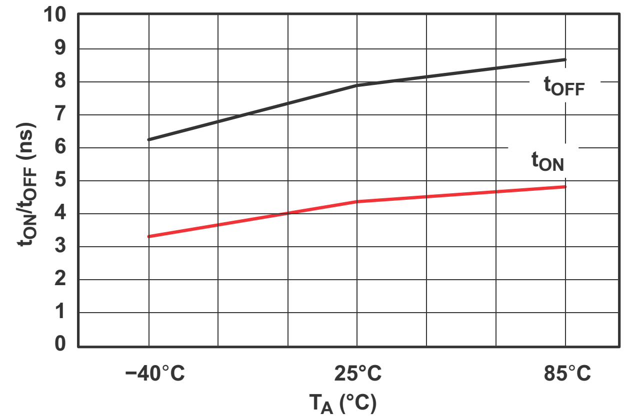


Figure 8. T_{ON} and T_{OFF} vs Temperature (5-V Supply)

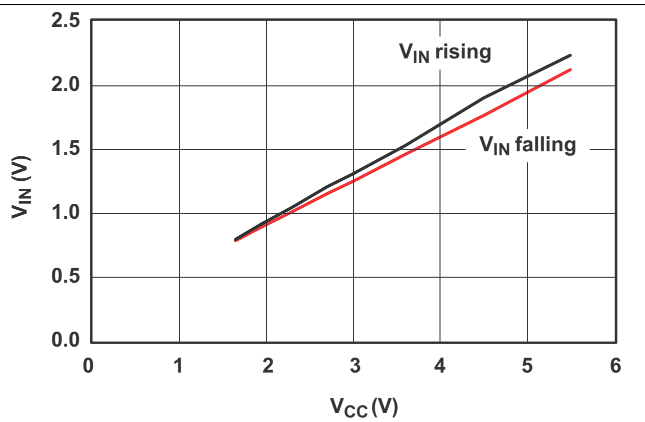


Figure 9. Logic-Level Threshold vs V_{CC}

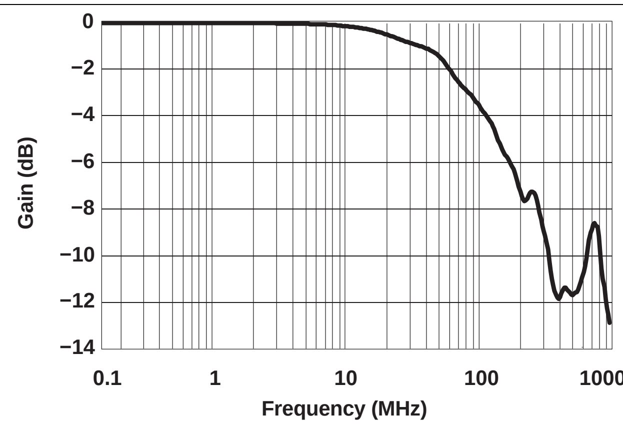


Figure 10. Bandwidth (V_{CC} = 5 V)

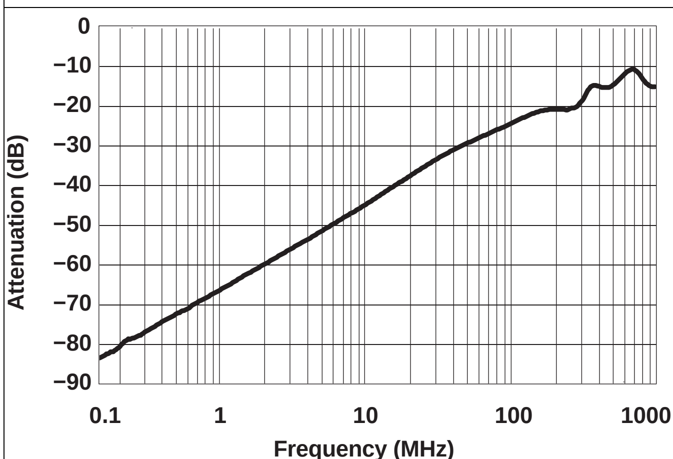


Figure 11. Off Isolation vs Frequency

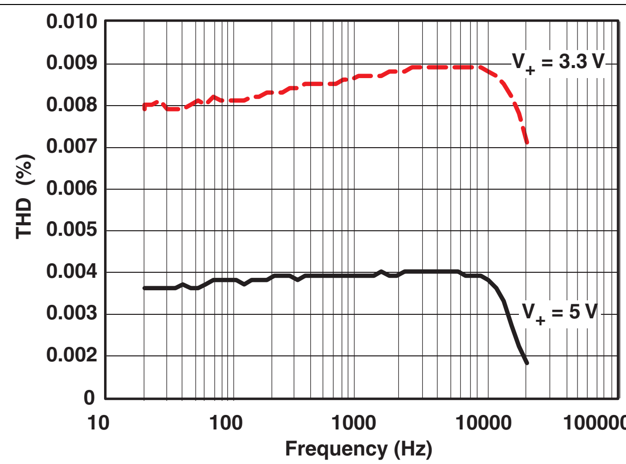


Figure 12. Total Harmonic Distortion vs Frequency

Typical Characteristics (continued)

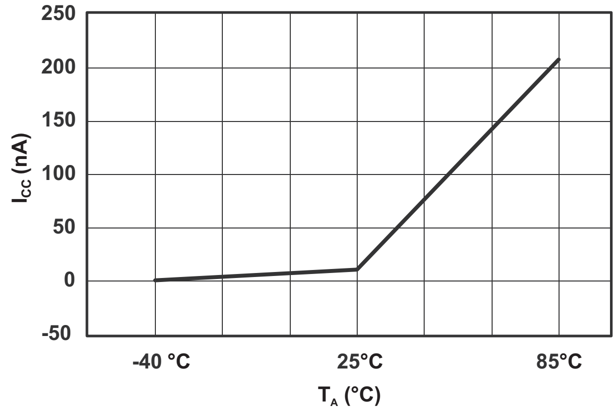


Figure 13. Power-Supply Current vs Temperature (V_{CC} = 5 V)

7 Parameter Measurement Information

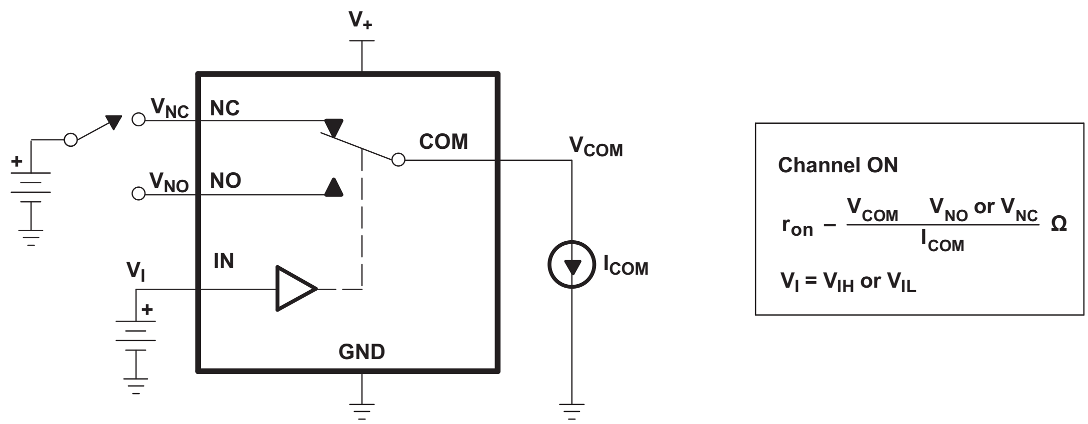


Figure 14. ON-State Resistance (R_{on})

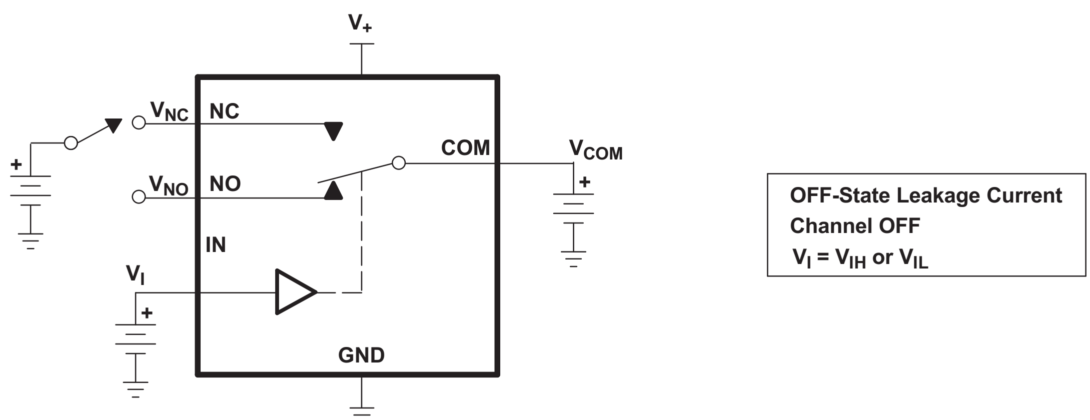


Figure 15. OFF-State Leakage Current ($I_{NC(OFF)}$, $I_{NC(PWROFF)}$, $I_{NO(OFF)}$, $I_{NO(PWROFF)}$, $I_{COM(OFF)}$, $Ic_{OM(PWROFF)}$)

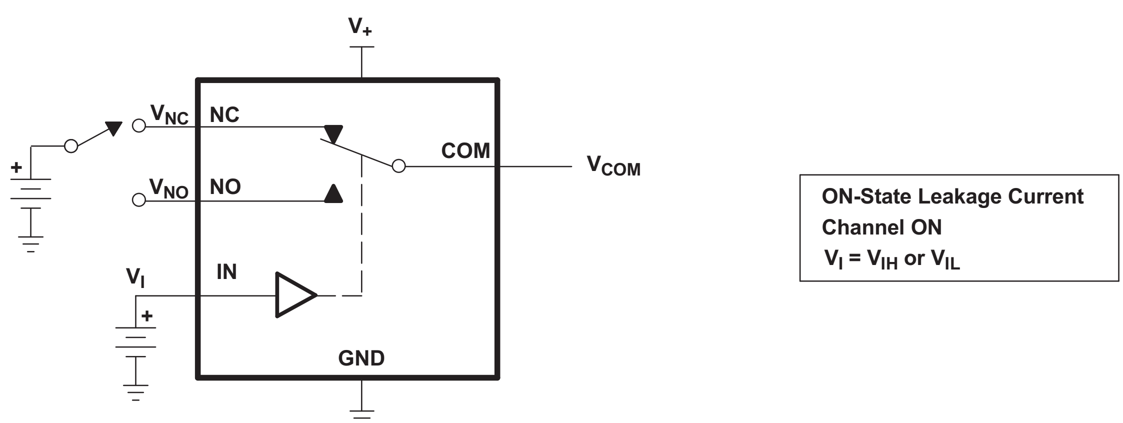


Figure 16. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)

Parameter Measurement Information (continued)

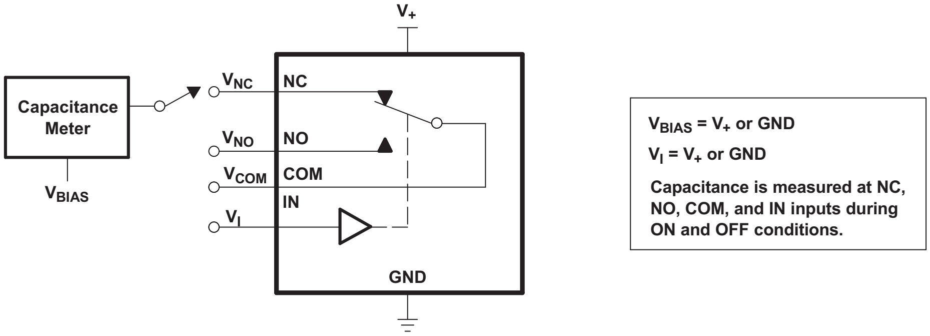
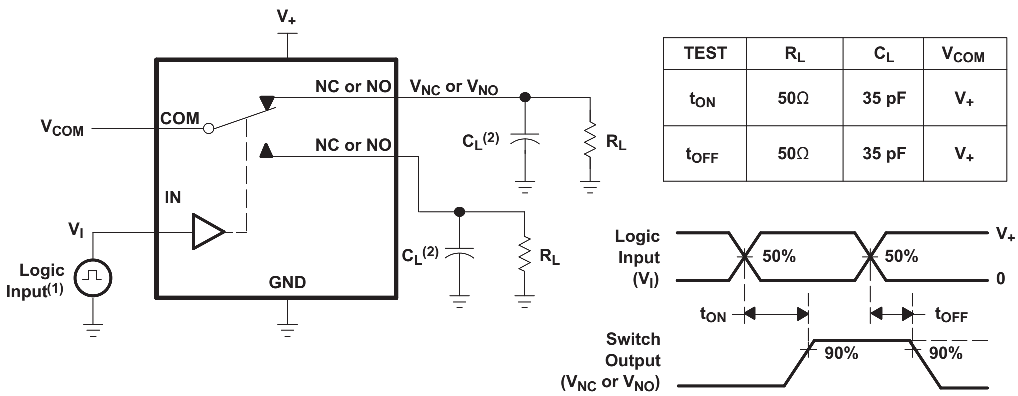


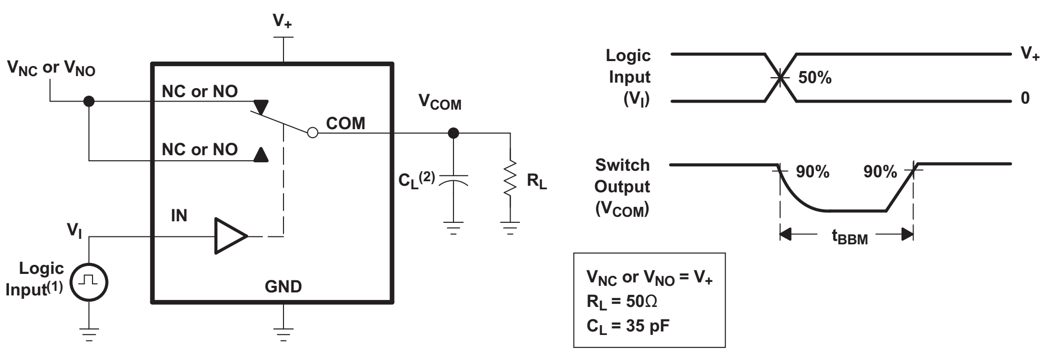
Figure 17. Capacitance (C_I, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$)



TEST	R_L	C_L	V_{COM}
t_{ON}	50Ω	35 pF	V_+
t_{OFF}	50Ω	35 pF	V_+

1. All input pulses are supplied by generators having the following characteristics:
PRR 3 10 MHz, Z_O = 50 Ω , t_r < 5 ns, t_f < 5 ns.
2. C_L includes probe and jig capacitance.

Figure 18. Turnon (T_{ON}) and Turnoff Time (T_{OFF})



1. All input pulses are supplied by generators having the following characteristics:
PRR 3 10 MHz, Z_O = 50 Ω , t_r < 5 ns, t_f < 5 ns.
2. C_L includes probe and jig capacitance.

Figure 19. Break-Before-Make Time (T_{BBM})

Parameter Measurement Information (continued)

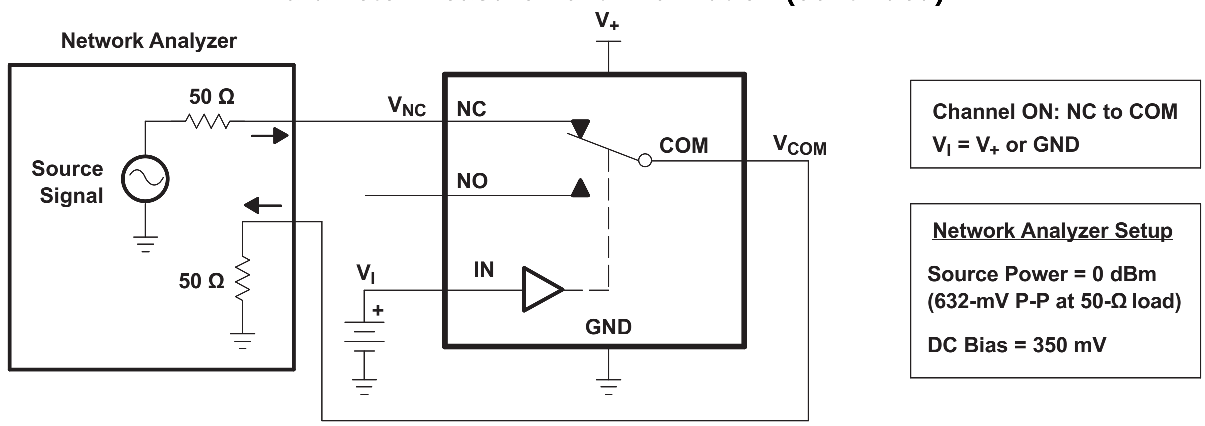


Figure 20. Bandwidth (Bw)

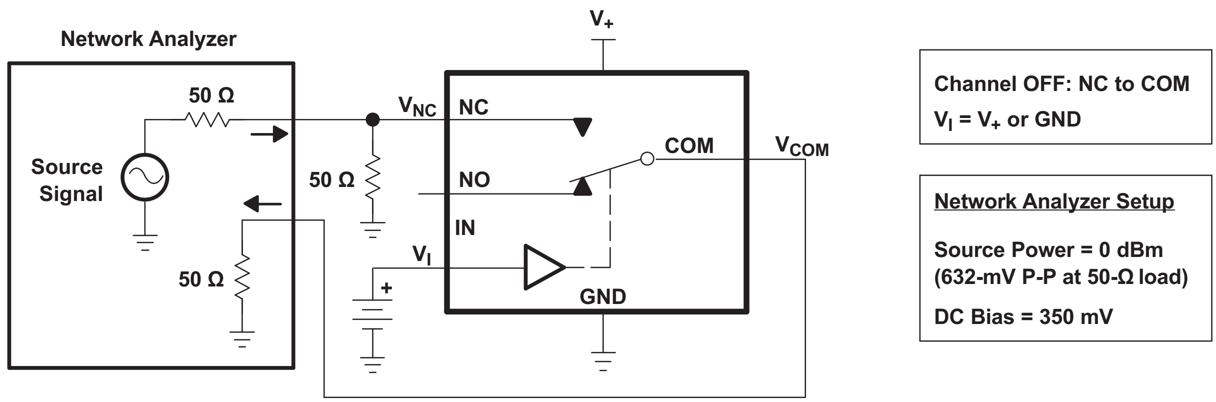


Figure 21. Off Isolation (O_{ISO})

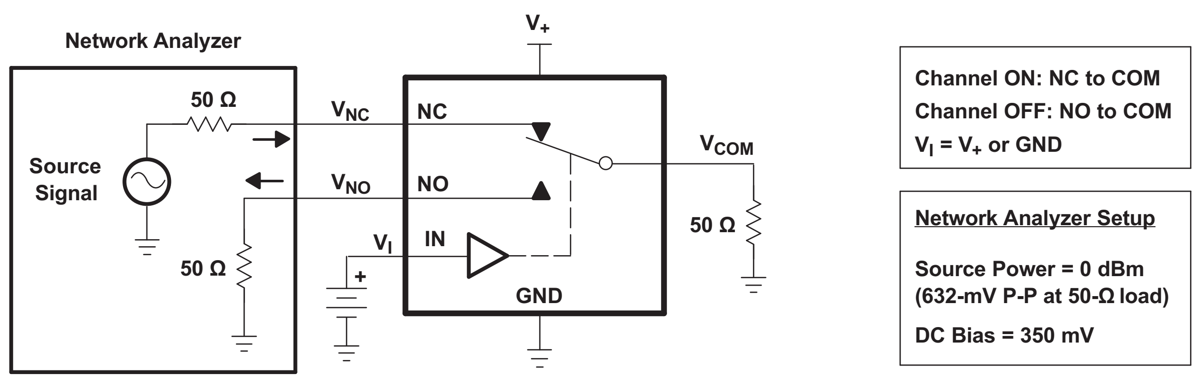
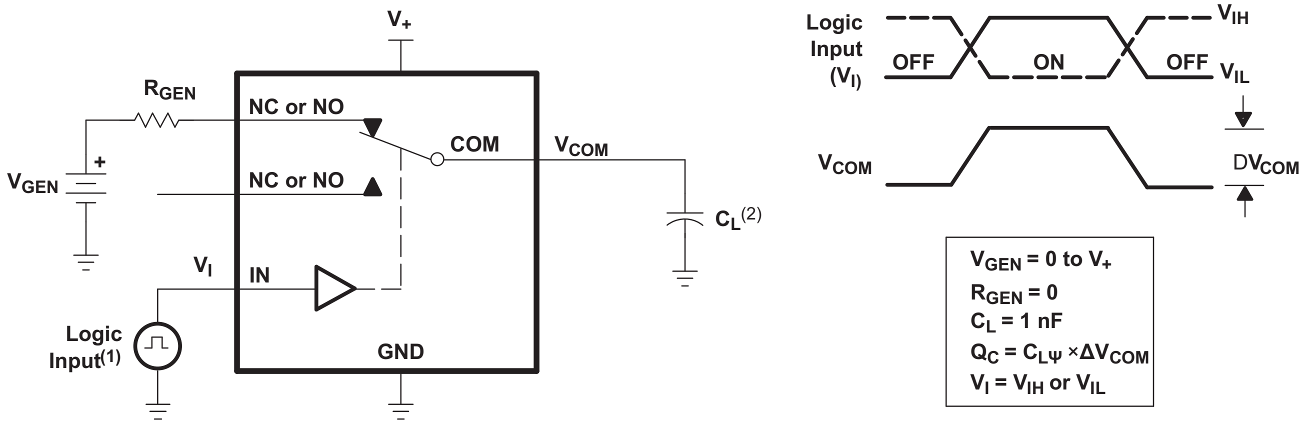


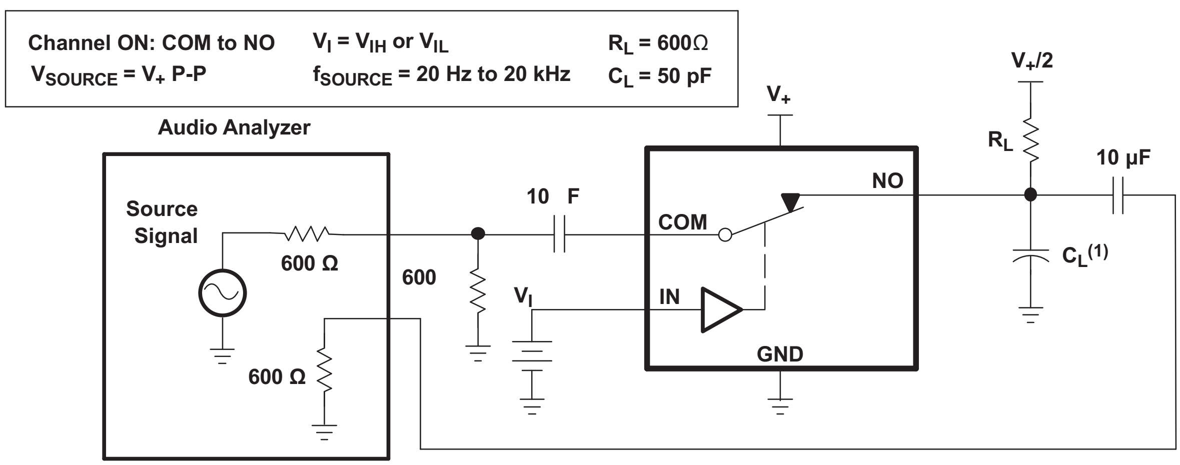
Figure 22. Crosstalk (X_{TALK})

Parameter Measurement Information (continued)



1. All input pulses are supplied by generators having the following characteristics:
PRR 3 10 MHz, Z_O = 50 Ω , t_r < 5 ns, t_f < 5 ns.
2. C_L includes probe and jig capacitance.

Figure 23. Charge Injection (Q_C)



1. C_L includes probe and jig capacitance.

Figure 24. Total Harmonic Distortion (THD)

Parameter Measurement Information (continued)

Table 1. Parameter Description

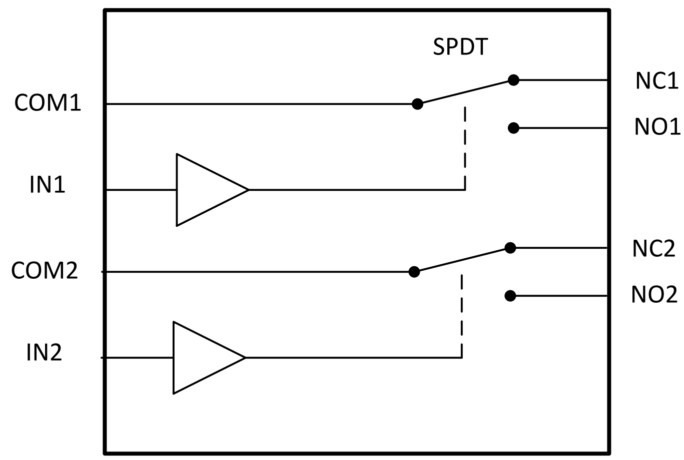
SYMBOL	DESCRIPTION
V_{COM}	Voltage at COM
V_{NC}	Voltage at NC
V_{NO}	Voltage at NO
R_{on}	Resistance between COM and NC or COM and NO ports when the channel is ON
R_{peak}	Peak on-state resistance over a specified voltage range
ΔR_{on}	Difference of R_{on} between channels in a specific device
$R_{on(flat)}$	Difference between the maximum and minimum value of R_{on} in a channel over the specified range of conditions
$I_{NC(OFF)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state under worst-case input and output conditions
$I_{NC(PWROFF)}$	Leakage current measured at the NC port during the power-down condition, $V_{CC} = 0$
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state under worst-case input and output conditions
$I_{NO(PWROFF)}$	Leakage current measured at the NO port during the power-down condition, $V_{CC} = 0$
$I_{NC(ON)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) open
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the ON state and the output (NC or NO) open
$I_{COM(PWROFF)}$	Leakage current measured at the COM port during the power-down condition, $V_{CC} = 0$
V_{IH}	Minimum input voltage for logic high for the control input (IN)
V_{IL}	Maximum input voltage for logic low for the control input (IN)
V_{IN}	Voltage at the control input (IN)
I_{IH}, I_{IL}	Leakage current measured at the control input (IN)
t_{ON}	Turnon time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM, NC, or NO) signal when the switch is turning ON.
t_{OFF}	Turnoff time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM, NC, or NO) signal when the switch is turning OFF.
t_{BBM}	Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO) when the control signal changes state.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NO or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$. C_L is the load capacitance and ΔV_{COM} is the change in analog output voltage.
$C_{NC(OFF)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
$C_{NO(OFF)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
$C_{NC(ON)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
$C_{NO(ON)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is ON
C_I	Capacitance of control input (IN)
O_{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state.
X_{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain.
THD	Total harmonic distortion is defined as the ratio of the root mean square (RMS) value of the second, third, and higher harmonics to the magnitude of fundamental harmonic.
I_{CC}	Static power-supply current with the control (IN) pin at V_{CC} or GND

8 Detailed Description

8.1 Overview

The TS5A23159 is a bidirectional 2-channel single-pole double-throw (SPDT) switch that is designed to operate from 1.65 V to 5.5 V. The device offers low ON-state resistance and excellent ON-state resistance matching with the break-before-make feature which prevents signal distortion during the transferring of a signal from one channel to another. The device has an excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for a wide variety of portable applications including cell phones, audio devices, and instrumentation.

8.2 Functional Block Diagram



8.3 Feature Description

The TS5A23159 is a bidirectional device that has two single-pole, double-throw switches. The two channels of the switch are contorled independantly by two digital signals; one digital control for each single-pole, double-throw switch.

8.4 Device Functional Modes

Table 2. Function Table

IN	NC to COM, COM to NC	NO to COM, COM to NO
L	ON	OFF
H	OFF	ON

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The switches are bidirectional, so the NO, NC, and COM pins can be used as either inputs or outputs.

9.2 Typical Application

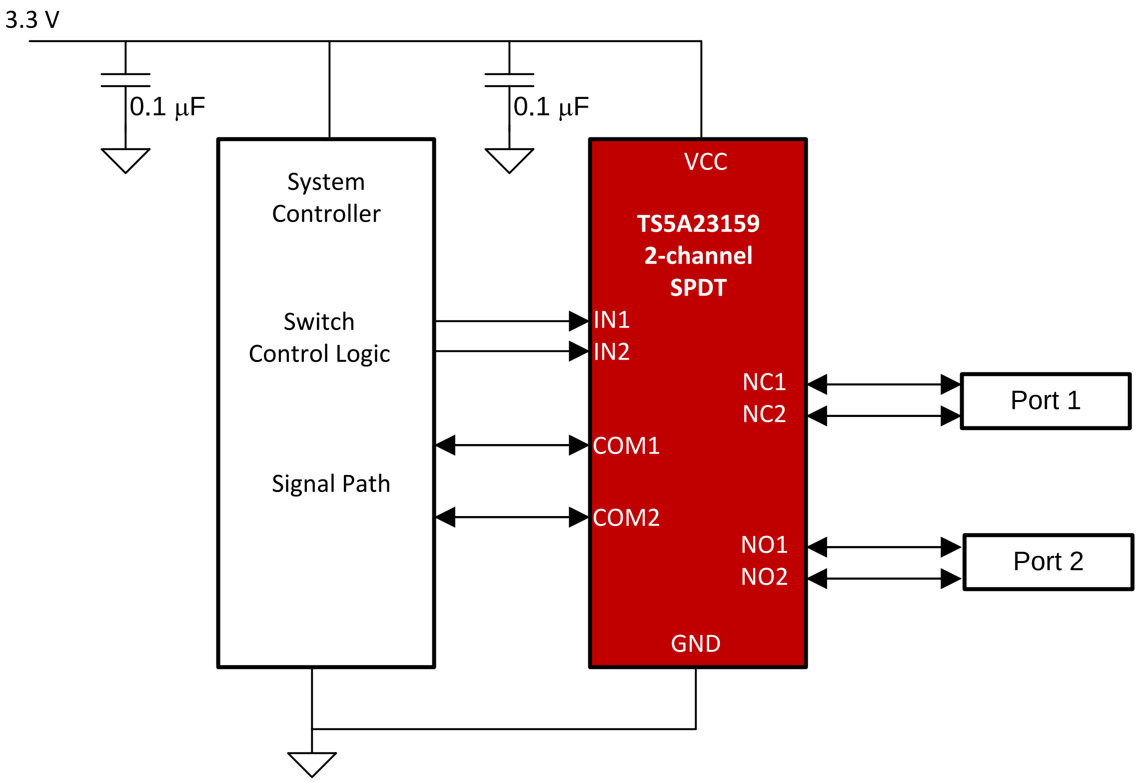


Figure 25. Typical Application Diagram

9.2.1 Design Requirements

Ensure that all of the signals passing through the switch are within the specified ranges in the recommended operating conditions to ensure proper performance.

9.2.2 Detailed Design Procedure

The TS5A23159 can be properly operated without any external components. However, TI recommends connecting unused pins to ground through a 50-Ω resistor to prevent signal reflections back into the device. TI also recommends that the digital control pins (INX) be pulled up to VCC or down to GND to avoid undesired switch positions that could result from the floating pin.

Typical Application (continued)

9.2.3 Application Curve

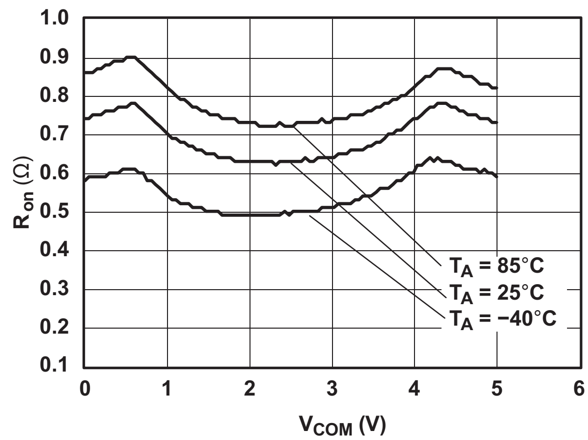


Figure 26. R_{on} vs V_{COM} (V_{CC} = 5 V)

10 Power Supply Recommendations

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the device. Always sequence VCC on first, followed by NO, NC, or COM. Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the VCC supply to other components. A 0.1-μF capacitor, connected from VCC to GND, is adequate for most applications.

11 Layout

11.1 Layout Guidelines

High-speed switches require proper layout and design procedures for optimum performance. Reduce stray inductance and capacitance by keeping traces short and wide. Ensure that bypass capacitors are as close to the device as possible. Use large ground planes where possible.

11.2 Layout Example

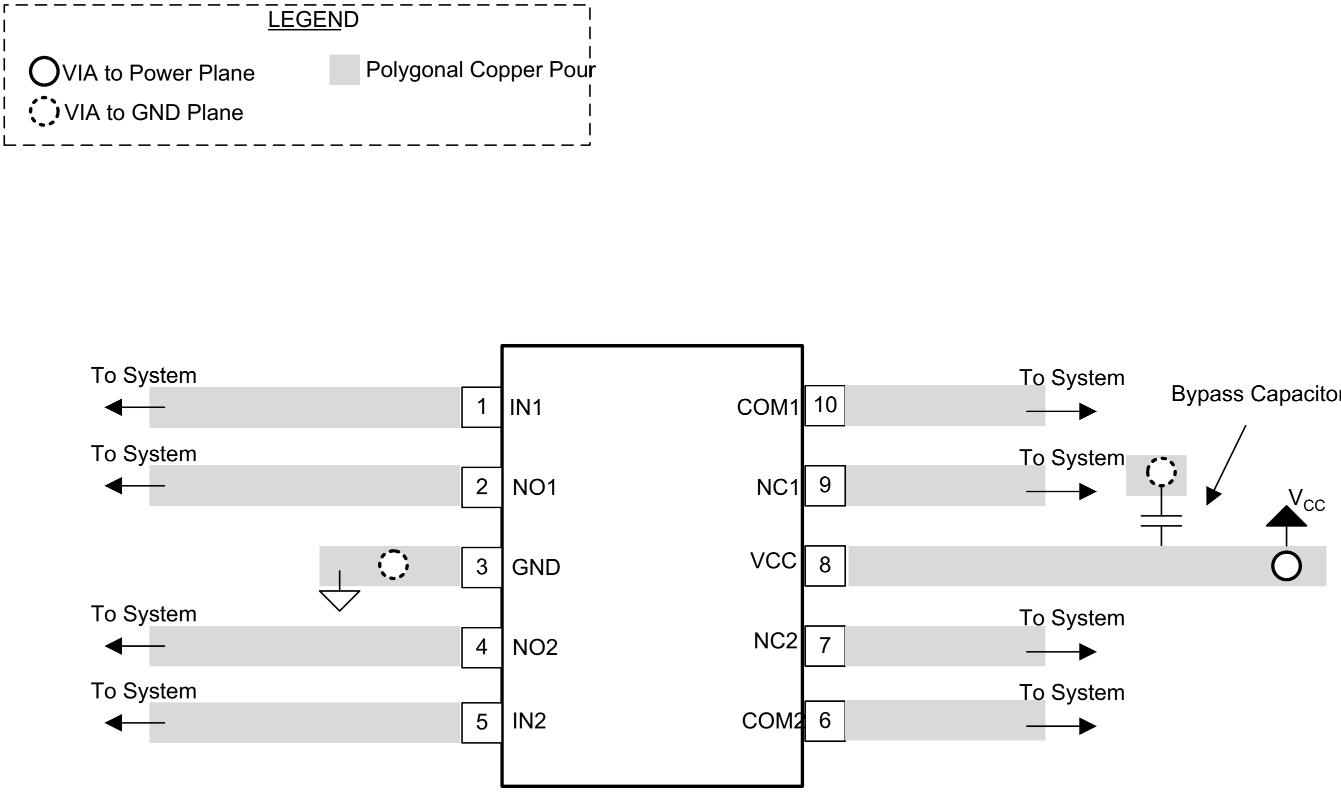


Figure 27. Layout Recommendation

12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS5A23159DGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JEQ, JER)
TS5A23159DGST	Obsolete	Production	VSSOP (DGS) | 10	-	-	Call TI	Call TI	-40 to 85	JER
TS5A23159RSER	Active	Production	UQFN (RSE) | 10	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(JE7, JEO, JER, JE V)

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

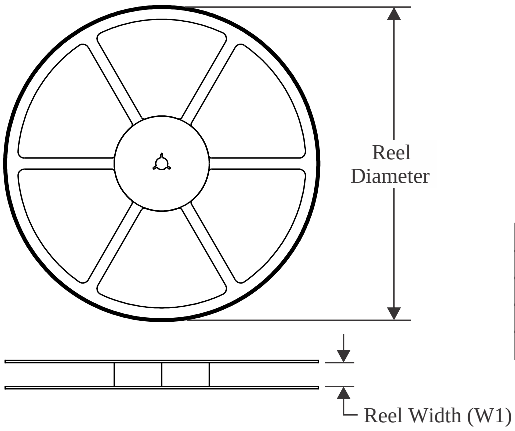
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

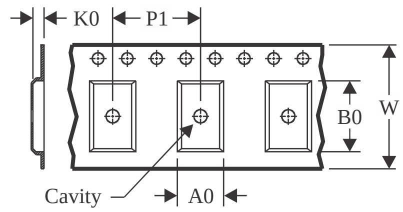
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

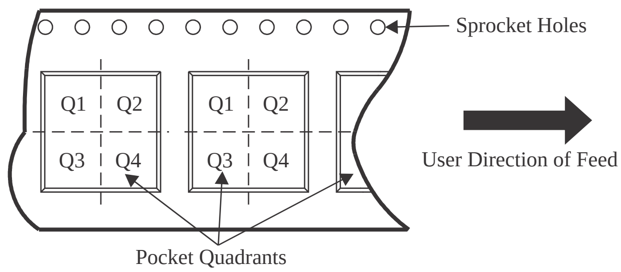


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

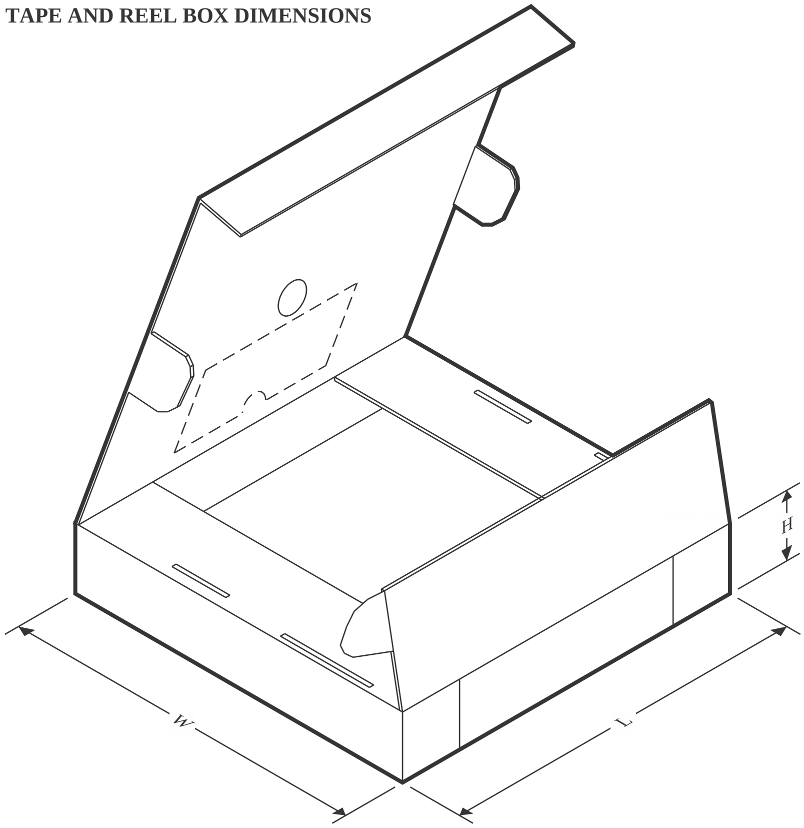
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

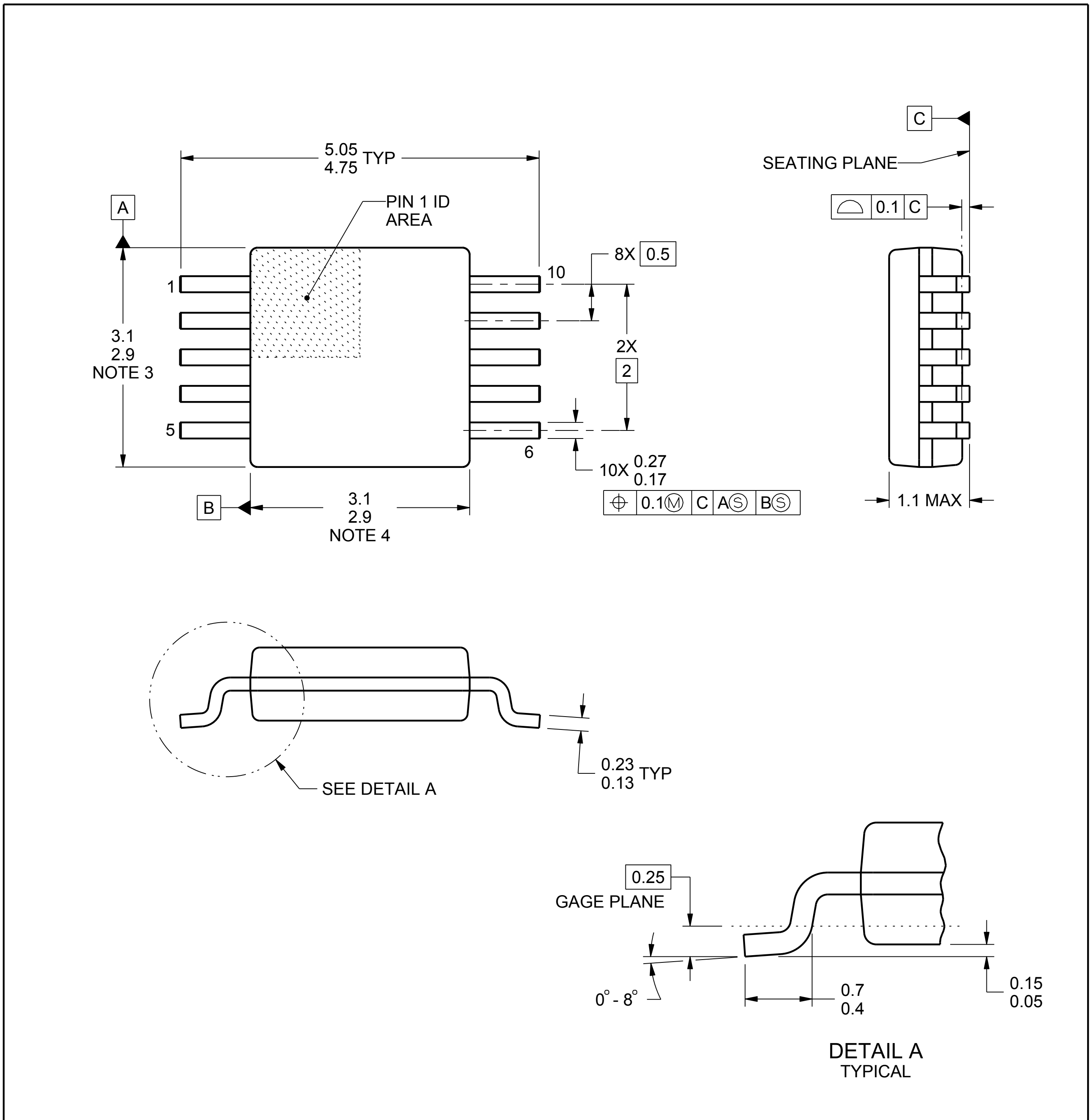
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A23159DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TS5A23159RSER	UQFN	RSE	10	3000	180.0	9.5	1.7	2.2	0.75	4.0	8.0	Q1
TS5A23159RSER	UQFN	RSE	10	3000	180.0	9.5	1.7	2.3	0.75	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

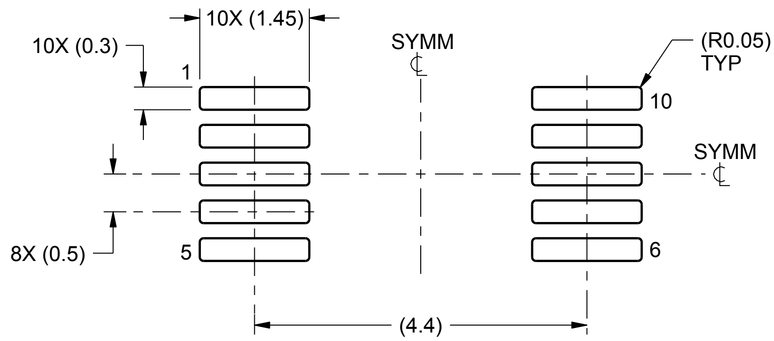
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A23159DGSR	VSSOP	DGS	10	2500	358.0	335.0	35.0
TS5A23159RSER	UQFN	RSE	10	3000	189.0	185.0	36.0
TS5A23159RSER	UQFN	RSE	10	3000	184.0	184.0	19.0



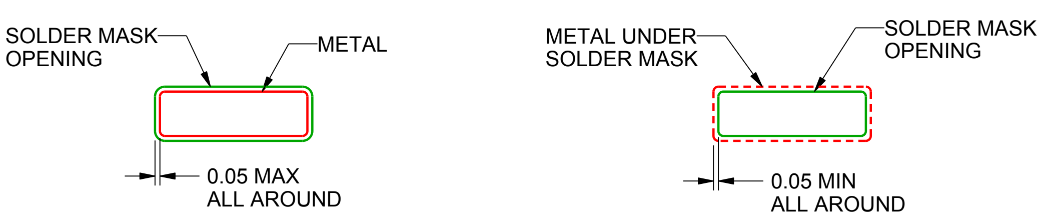
4221984/A 05/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X



NON SOLDER MASK DEFINED

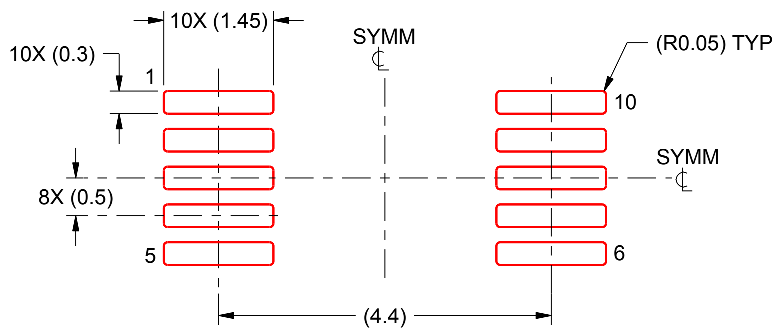
SOLDER MASK DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

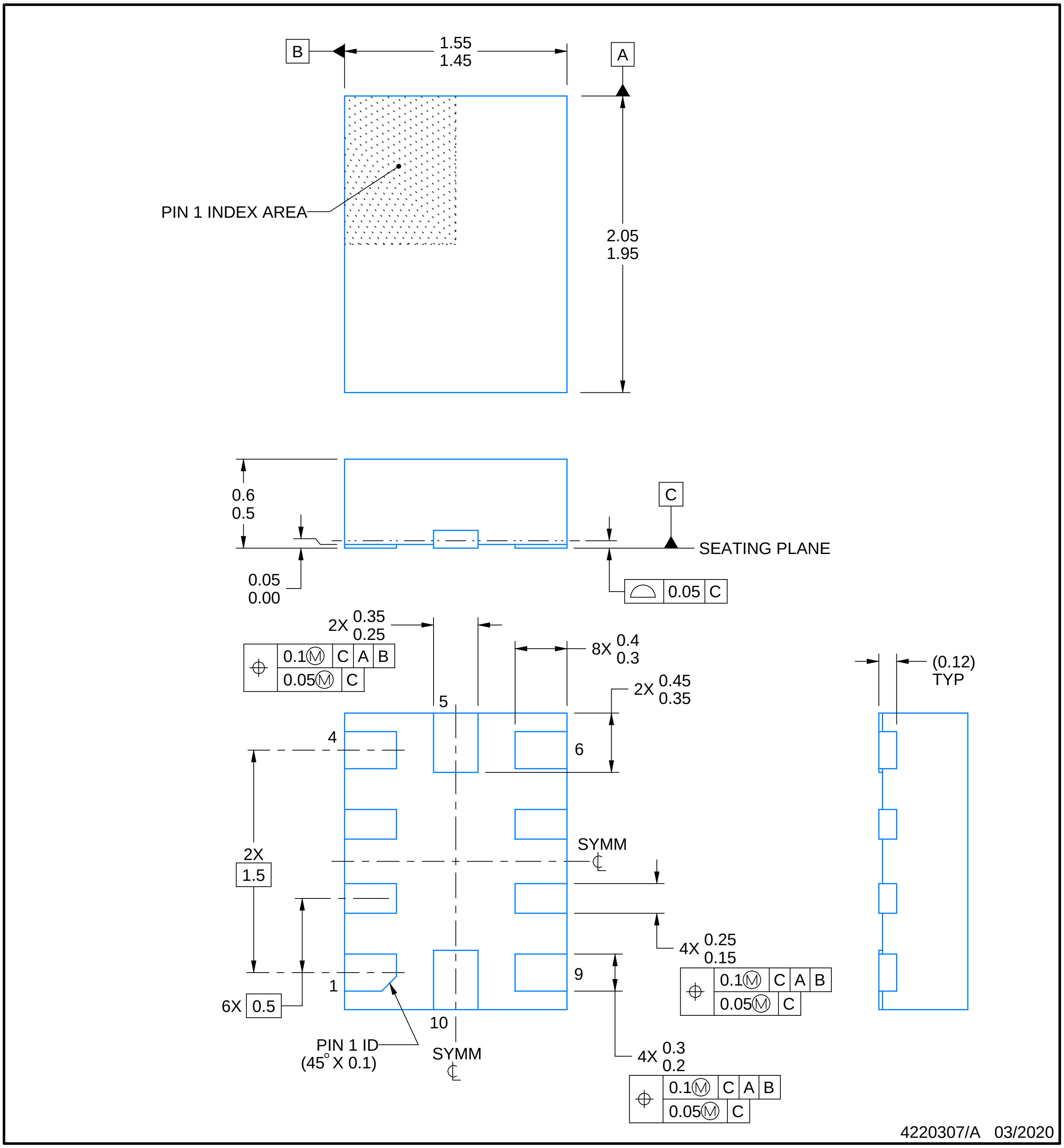


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

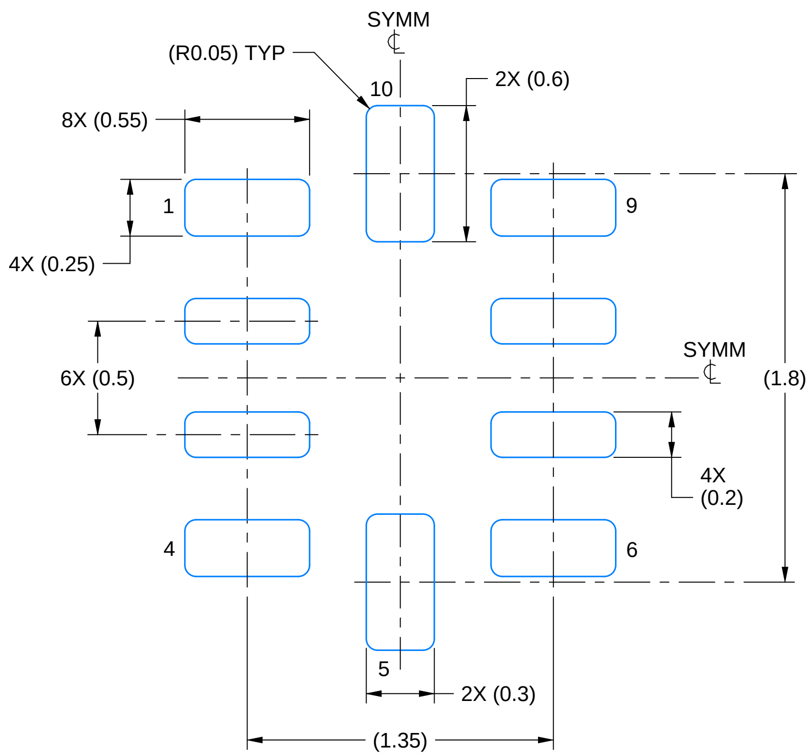
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

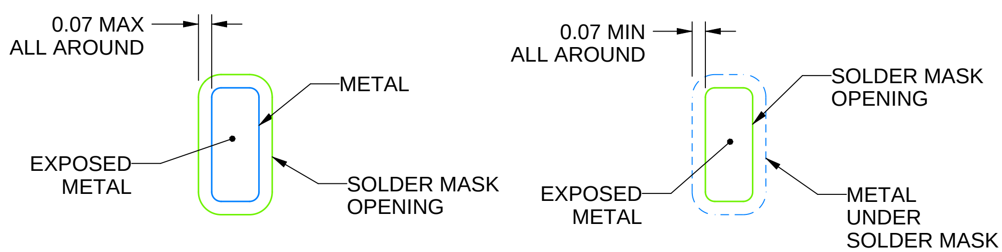


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



NON SOLDER MASK
DEFINED
(PREFERRED)

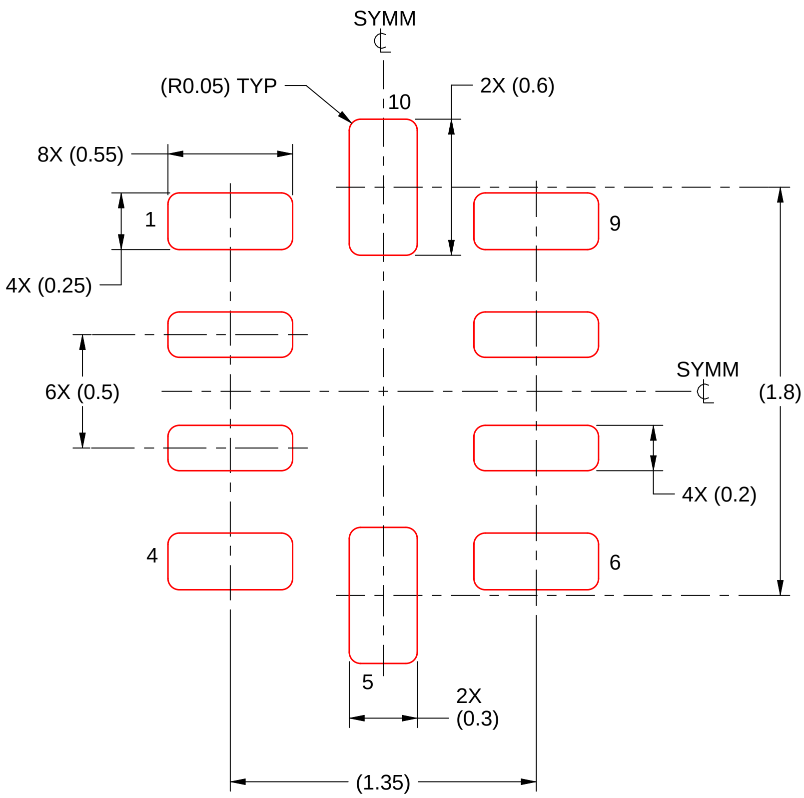
SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4220307/A 03/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICKNESS
SCALE: 30X

4220307/A 03/2020

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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