

SN54122, SN54123, SN54130, SN54LS122, SN54LS123, SN74122, SN74123, SN74130, SN74LS122, SN74LS123 RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

SDLS043 – DECEMBER 1983 – REVISED MARCH 1988

- D-C Triggered from Active-High or Active-Low Gated Logic Inputs
- Retriggerable for Very Long Output Pulses, Up to 100% Duty Cycle
- Overriding Clear Terminates Output Pulse
- '122 and 'LS122 Have Internal Timing Resistors

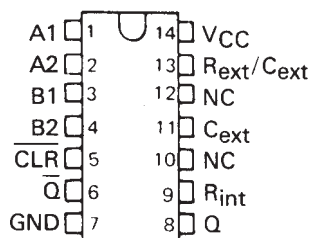
description

These d-c triggered multivibrators feature output pulse-duration control by three methods. The basic pulse time is programmed by selection of external resistance and capacitance values (see typical application data). The '122 and 'LS122 have internal timing resistors that allow the circuits to be used with only an external capacitor, if so desired. Once triggered, the basic pulse duration may be extended by retriggering the gated low-level-active (A) or high-level-active (B) inputs, or be reduced by use of the overriding clear. Figure 1 illustrates pulse control by retriggering and early clear.

The 'LS122 and 'LS123 are provided enough Schmitt hysteresis to ensure jitter-free triggering from the B input with transition rates as slow as 0.1 millivolt per nanosecond.

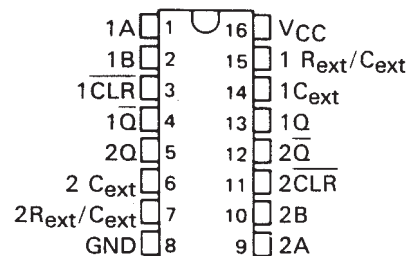
The R_{int} is nominally 10 k Ω for '122 and 'LS122.

SN54122, SN54LS122 . . . J OR W PACKAGE
SN74122 . . . N PACKAGE
SN74LS122 . . . D OR N PACKAGE
(TOP VIEW) (SEE NOTES 1 THRU 4)

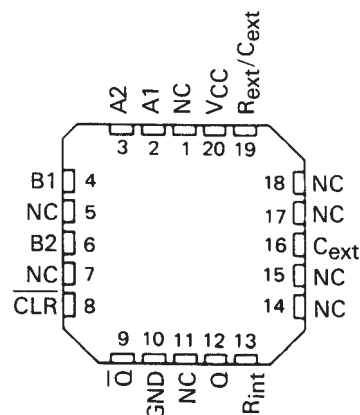


- NOTES: 1. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).
2. To use the internal timing resistor of '122 or 'LS122, connect R_{int} to VCC.
3. For improved pulse duration accuracy and repeatability, connect an external resistor between R_{ext}/C_{ext} and VCC with R_{int} open-circuited.
4. To obtain variable pulse durations, connect an external variable resistance between R_{int} or R_{ext}/C_{ext} and VCC.

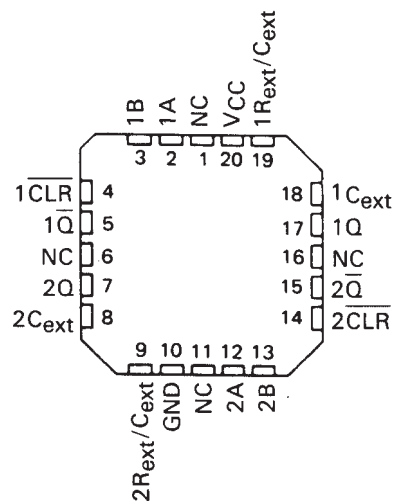
SN54123, SN54130, SN54LS123 . . . J OR W PACKAGE
SN74123, SN74130 . . . N PACKAGE
SN74LS123 . . . D OR N PACKAGE
(TOP VIEW) (SEE NOTES 1 THRU 4)



SN54LS122 . . . FK PACKAGE
(TOP VIEW) (SEE NOTES 1 THRU 4)



SN54LS123 . . . FK PACKAGE
(TOP VIEW) (SEE NOTES 1 THRU 4)

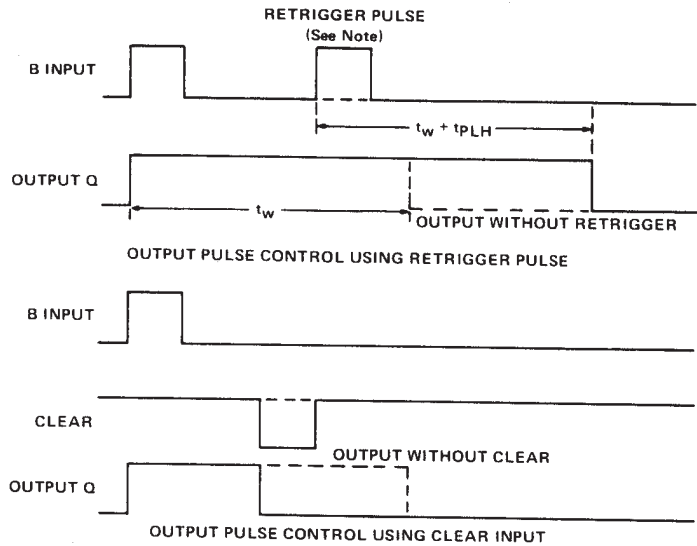


NC - No internal connection

SN54122, SN54123, SN54130, SN54LS122, SN54LS123,
SN74122, SN74123, SN74130, SN74LS122, SN74LS123
RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

SDLS043 – DECEMBER 1983 – REVISED MARCH 1988

description (continued)



NOTE: Retrigger pulses starting before 0.22 C_{ext} (in picofrads) nanoseconds after the initial trigger pulse will be ignored and the output duration will remain unchanged.

FIGURE 1—TYPICAL INPUT/OUTPUT PULSES

'122, 'LS122
FUNCTION TABLE

| INPUTS | | | | | OUTPUTS | |
|--------|----|----|----|----|---------|-----------|
| CLEAR | A1 | A2 | B1 | B2 | Q | \bar{Q} |
| L | X | X | X | X | L | H |
| X | H | H | X | X | L† | H† |
| X | X | X | L | X | L† | H† |
| X | X | X | X | L | L† | H† |
| H | L | X | ↑ | H | | |
| H | L | X | H | ↑ | | |
| H | X | L | ↑ | H | | |
| H | X | L | H | ↑ | | |
| H | H | ↓ | H | H | | |
| H | ↓ | ↓ | H | H | | |
| H | ↓ | H | H | H | | |
| ↑ | L | X | H | H | | |
| ↑ | X | L | H | H | | |

'123, '130, 'LS123
FUNCTION TABLE

| INPUTS | | | OUTPUTS | |
|--------|---|---|---------|-----------|
| CLEAR | A | B | Q | \bar{Q} |
| L | X | X | L | H |
| X | H | X | L† | H† |
| X | X | L | L† | H† |
| H | L | ↑ | | |
| H | ↓ | H | | |
| ↑ | L | H | | |

See explanation of function tables on page

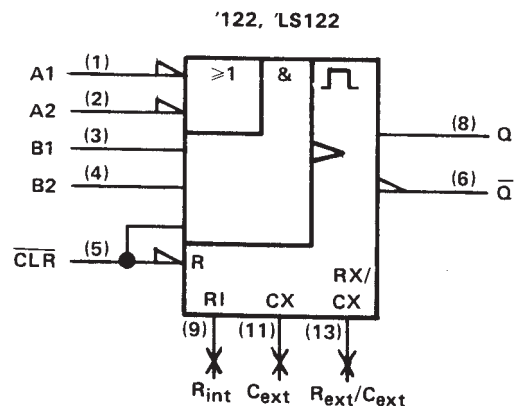
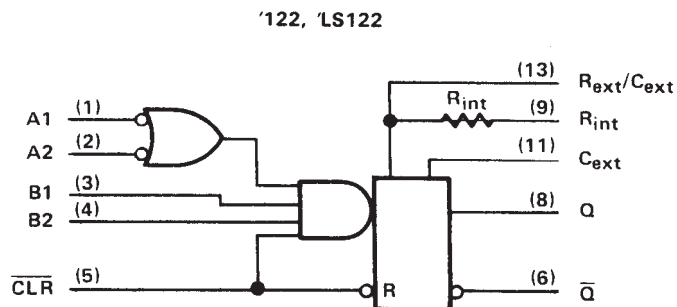
† These lines of the functional tables assume that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the set up.

SN54122, SN54123, SN54130, SN54LS122, SN54LS123, SN74122, SN74123, SN74130, SN74LS122, SN74LS123 RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

SDLS043 – DECEMBER 1983 – REVISED MARCH 1988

logic diagram (positive logic)

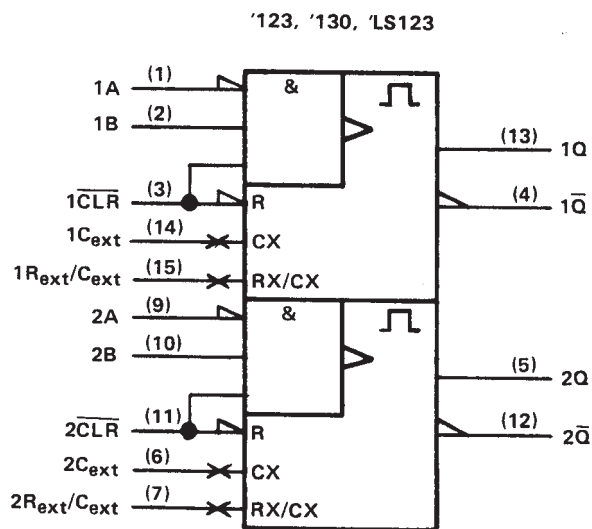
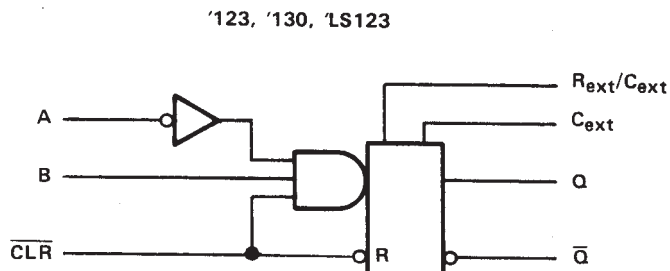
logic symbol†



R_{int} is nominally 10 k Ω for '122 and 'LS122

logic diagram (positive logic) (each multivibrator)

logic symbol†



Pin numbers shown are for D, J, N, and W packages.

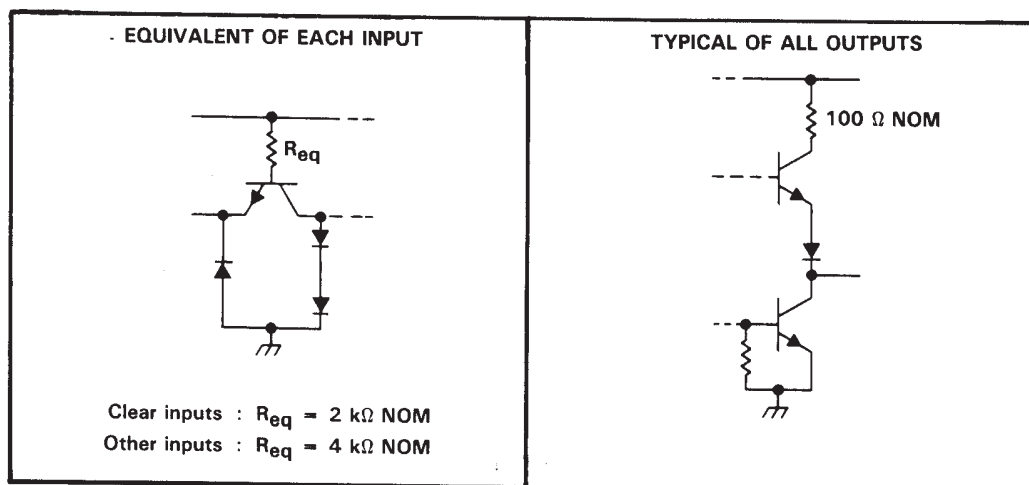
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54122, SN54123, SN54130, SN54LS122, SN54LS123, SN74122, SN74123, SN74130, SN74LS122, SN74LS123 RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

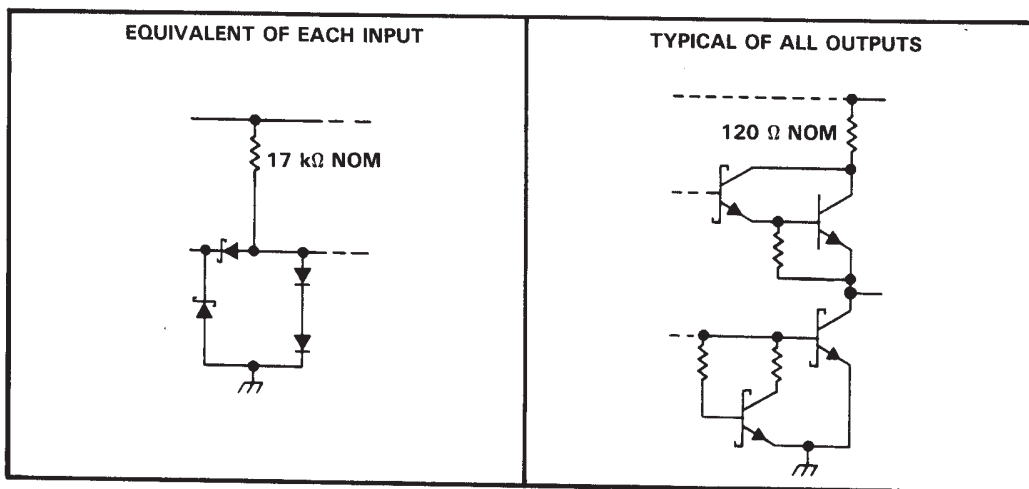
SDLS043 – DECEMBER 1983 – REVISED MARCH 1988

schematics of inputs and outputs

'122, '123, '130 CIRCUITS



'LS122, 'LS123 CIRCUITS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|---------------------------------------------|----------------|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage: '122, '123, '130 | 5.5 V |
| 'LS122, 'LS123 | 7 V |
| Operating free-air temperature range: SN54' | -55°C to 125°C |
| SN74' | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.

SN54122, SN54123, SN54130, SN74122, SN74123, SN74130 RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

SDLS043 – DECEMBER 1983 – REVISED MARCH 1988

recommended operating conditions

| | SN54' | | | SN74' | | | UNIT |
|--------------------------------------------------|----------------|-----|------|----------------|-----|------|-------------|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, V_{CC} | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level output current, I_{OH} | | | -800 | | | -800 | μA |
| Low-level output current, I_{OL} | | | 16 | | | 16 | mA |
| Pulse duration, t_W | 40 | | | 40 | | | ns |
| External timing resistance, R_{ext} | 5 | | 25 | 5 | | 50 | k Ω |
| External capacitance, C_{ext} | No restriction | | | No restriction | | | |
| Wiring capacitance at R_{ext}/C_{ext} terminal | | | 50 | | | 50 | pF |
| Operating free-air temperature, T_A | -55 | | 125 | 0 | | 70 | $^{\circ}C$ |

electrical characteristics over recommended free-air operating temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | '122 | | | '123, '130 | | | UNIT |
|-----------|-----------------------------------------|---------------------------------------------------------------|------|------|------|------------|------|------|---------|
| | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| V_{IH} | High-level input voltage | | 2 | | | 2 | | | V |
| V_{IL} | Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| V_{IK} | Input clamp voltage | $V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$ | | | -1.5 | | | -1.5 | V |
| V_{OH} | High-level output voltage | $V_{CC} = \text{MIN}, I_{OH} = -800 \mu A$, See Note 5 | 2.4 | 3.4 | | 2.4 | 3.4 | | V |
| V_{OL} | Low-level output voltage | $V_{CC} = \text{MIN}, I_{OL} = 16 \text{ mA}$, See Note 5 | | 0.2 | 0.4 | | 0.2 | 0.4 | V |
| I_I | Input current at maximum input voltage | $V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$ | | | 1 | | | 1 | mA |
| I_{IH} | High-level input current | Data inputs | | | 40 | | | 40 | μA |
| | | Clear input | | | 80 | | | 80 | |
| I_{IL} | Low-level input current | Data inputs | | | -1.6 | | | -1.6 | mA |
| | | Clear input | | | -3.2 | | | -3.2 | |
| I_{OS} | Short-circuit output current§ | $V_{CC} = \text{MAX}$, See Note 5 | -10 | | -40 | -10 | | -40 | mA |
| I_{CC} | Supply current (quiescent or triggered) | $V_{CC} = \text{MAX}$, See Notes 6 and 7 | 23 | 36 | | 46 | 66 | | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}C$.

§ Not more than one output should be shorted at a time.

NOTES: 5. Ground C_{ext} to measure V_{OH} at Q, V_{OL} at \bar{Q} , or I_{OS} at Q. C_{ext} is open to measure V_{OH} at \bar{Q} , V_{OL} at Q, or I_{OS} at \bar{Q} .

6. Quiescent I_{CC} is measured (after clearing) with 4.5 V applied to all clear and A inputs, B inputs grounded, all outputs open and $R_{ext} = 25 \text{ k}\Omega$. R_{int} of '122 is open.

7. I_{CC} is measured in the triggered state with 2.4 V applied to all clear and B inputs, A inputs grounded, all outputs open, $C_{ext} = 0.02 \mu F$, and $R_{ext} = 25 \text{ k}\Omega$. R_{int} of '122 is open.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}C$, see note 8

| PARAMETER¶ | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | '122, '130 | | | '123 | | | UNIT |
|----------------------|--------------|-------------|--------------------------------------------------------------------------------------------------------------|------------|------|------|------|------|------|---------|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| t_{PLH} | A | Q | $C_{ext} = 0$, $R_{ext} = 5 \text{ k}\Omega$, $C_L = 15 \text{ pF}$, $R_L = 400 \Omega$ | 22 | 33 | | 22 | 33 | | ns |
| | B | Q | | 19 | 28 | | 19 | 28 | | |
| t_{PHL} | A | \bar{Q} | | 30 | 40 | | 30 | 40 | | ns |
| | B | \bar{Q} | | 27 | 36 | | 27 | 36 | | |
| t_{PHL} | Clear | Q | | 18 | 27 | | 18 | 27 | | ns |
| t_{PLH} | Clear | \bar{Q} | | 30 | 40 | | 30 | 40 | | |
| $t_{WQ}(\text{min})$ | A or B | Q | | 45 | 65 | | 45 | 76 | | ns |
| t_{WQ} | A or B | Q | $C_{ext} = 1000 \text{ pF}$, $R_{ext} = 10 \text{ k}\Omega$, $C_L = 15 \text{ pF}$, $R_L = 400 \Omega$ | 3.08 | 3.42 | 3.76 | 2.76 | 3.03 | 3.37 | μs |

¶ t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

t_{WQ} = duration of pulse at output Q.

NOTE 8: Load circuits and voltage waveforms are shown in Section 1.



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SN54LS122, SN54LS123, SN74LS122, SN74LS123 RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

SDLS043 – DECEMBER 1983 – REVISED MARCH 1988

recommended operating conditions

| | SN54LS' | | | SN74LS' | | | UNIT |
|--------------------------------------------------|----------------|-----|------|----------------|-----|------|-------------|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, V_{CC} | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level output current, I_{OH} | | | -400 | | | -400 | μA |
| Low-level output current, I_{OL} | | | 4 | | | 8 | mA |
| Pulse duration, t_w | 40 | | | 40 | | | ns |
| External timing resistance, R_{ext} | 5 | | 180 | 5 | | 260 | k Ω |
| External capacitance, C_{ext} | No restriction | | | No restriction | | | |
| Wiring capacitance at R_{ext}/C_{ext} terminal | | | 50 | | | 50 | pF |
| Operating free-air temperature, T_A | -55 | | 125 | 0 | | 70 | $^{\circ}C$ |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS† | SN54LS' | | | SN74LS' | | | UNIT |
|--------------------------------------------------|-------------------------------------------------------------------------------------------------|---------|------|-------------|---------|------|-------------|---------|
| | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| V_{IH} High-level input voltage | | 2 | | | 2 | | | V |
| V_{IL} Low-level input voltage | | | | 0.7 | | | 0.8 | V |
| V_{IK} Input clamp voltage | $V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$ | | | -1.5 | | | -1.5 | V |
| V_{OH} High-level output voltage | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu A$ | 2.5 | 3.5 | | 2.7 | 3.5 | | V |
| V_{OL} Low-level output voltage | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 4 \text{ mA}$ | 0.25 | 0.4 | | 0.25 | 0.4 | | V |
| | | | | | | | 0.35 0.5 | |
| I_I Input current at maximum input voltage | $V_{CC} = \text{MAX}, V_I = 7 \text{ V}$ | | | 0.1 | | | 0.1 | mA |
| I_{IH} High-level input current | $V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$ | | | 20 | | | 20 | μA |
| I_{IL} Low-level input current | $V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$ | | | -0.4 | | | -0.4 | mA |
| I_{OS} Short-circuit output current§ | $V_{CC} = \text{MAX}$ | -20 | | -100 | -20 | | -100 | mA |
| I_{CC} Supply current (quiescent or triggered) | $V_{CC} = \text{MAX},$ See Note 13 | | | 'LS122 6 11 | | | 'LS123 6 11 | mA |
| | | | | | | | 12 20 | |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}C$.

§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

NOTES: 12. To measure V_{OH} at Q, V_{OL} at Q, or I_{OS} at Q, ground R_{ext}/C_{ext} , apply 2 V to B and clear, and pulse A from 2 V to 0 V.

13. With all outputs open and 4.5 V applied to all data and clear inputs. I_{CC} is measured after a momentary ground, then 4.5 V, is applied to A or B inputs.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}C$ (see note 8)

| PARAMETER¶ | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------|-----------------|----------------|-----------------------------------------------------------------------------------|----------------------------------------------------------------------|-----|-----|------|
| tPLH | A | Q | Cext = 0, Rext = 5 kΩ, CL = 15 pF, RL = 2 kΩ | | 23 | 33 | ns |
| | B | | | | 23 | 44 | |
| tPHL | A | Q̄ | | | 32 | 45 | ns |
| | B | | | | 34 | 56 | |
| tPHL | Clear | Q | | | 20 | 27 | ns |
| tPLH | | Q̄ | | | 28 | 45 | |
| twQ (min) | | Q | | | 116 | 200 | |
| twQ | A or B | Q | | Cext = 1000 pF, Rext = 10 kΩ, CL = 15 pF, RL = 2 kΩ | 4 | 4.5 | 5 |

¶ t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

t_{wQ} = duration of pulse at output Q.

NOTE 8: Load circuits and voltage waveforms are shown in Section 1.



SN54122, SN54123, SN54130, SN74122, SN74123, SN74130 RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

SDLS043 – DECEMBER 1983 – REVISED MARCH 1988

TYPICAL APPLICATION DATA FOR '122, '123, '130

For pulse durations when $C_{ext} \leq 1000$ pF, see Figure 4.

The output pulse duration is primarily a function of the external capacitor and resistor. For $C_{ext} > 1000$ pF, the output pulse duration (t_W) is defined as:

$$t_W = K \cdot R_T \cdot C_{ext} \left(1 + \frac{0.7}{R_T} \right)$$

where

K is 0.32 for '122, 0.28 for '123 and '130

R_T is in $k\Omega$ (internal or external timing resistance.)

C_{ext} is in pF

t_W is in ns

To prevent reverse voltage across C_{ext} , it is recommended that the method shown in Figure 2 be employed when using electrolytic capacitors and in applications utilizing the clear function. In all applications using the diode, the pulse duration is:

$$t_W = K_D \cdot R_T \cdot C_{ext} \left(1 + \frac{0.7}{R_T} \right)$$

K_D is 0.28 for '122, 0.25 for '123 and '130

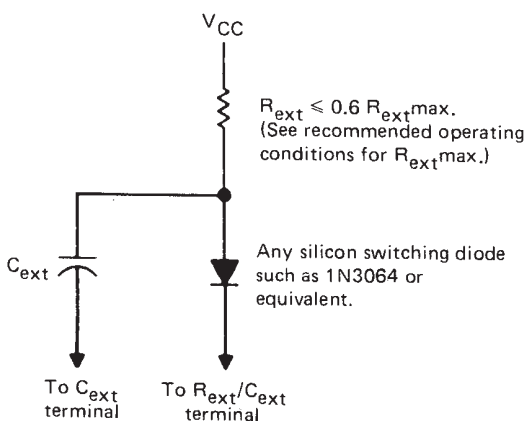


FIGURE 2

Applications requiring more precise pulse durations (up to 28 seconds) and not requiring the clear feature can best be satisfied with the '121.

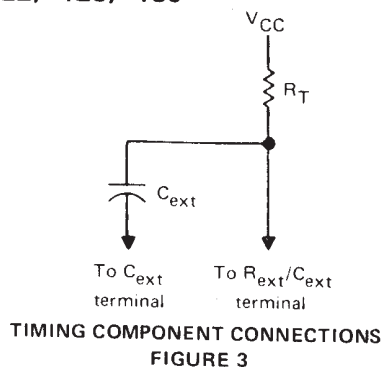


FIGURE 3

TYPICAL OUTPUT PULSE DURATION vs EXTERNAL TIMING CAPACITANCE

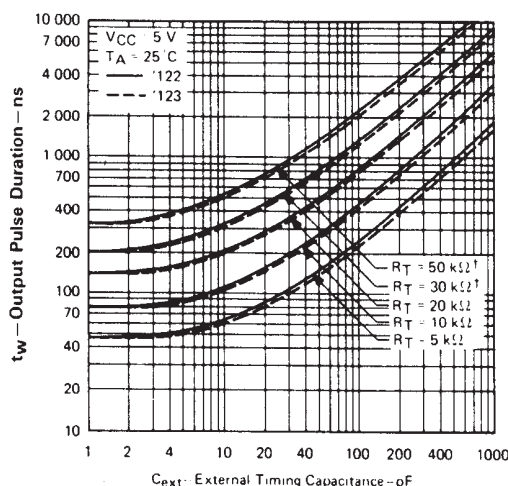


FIGURE 4

†These values of resistance exceed the maximum recommended for use over the full temperature range of the SN54' circuits.

SN54LS122, SN54LS123, SN74LS122, SN74LS123 RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

SDLS043 – DECEMBER 1983 – REVISED MARCH 1988

TYPICAL APPLICATION DATA FOR 'LS122, 'LS123

The basic output pulse duration is essentially determined by the values of external capacitance and timing resistance. For pulse durations when $C_{ext} \leq 1000$ pF, use Figure 6, or use Figure 7 where the pulse duration may be defined as:

$$t_w = K \cdot R_T \cdot C_{ext}$$

When $C_{ext} \geq 1 \mu F$, the output pulse width is defined as:

$$t_w = 0.33 \cdot R_T \cdot C_{ext}$$

For the above two equations, as applicable;

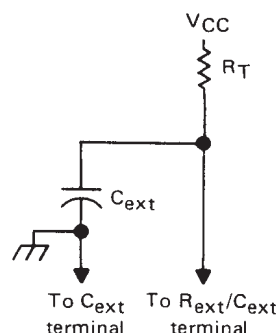
K is multiplier factor, see Figure 7

R_T is in $k\Omega$ (internal or external timing resistance)

C_{ext} is in pF

t_w is in ns

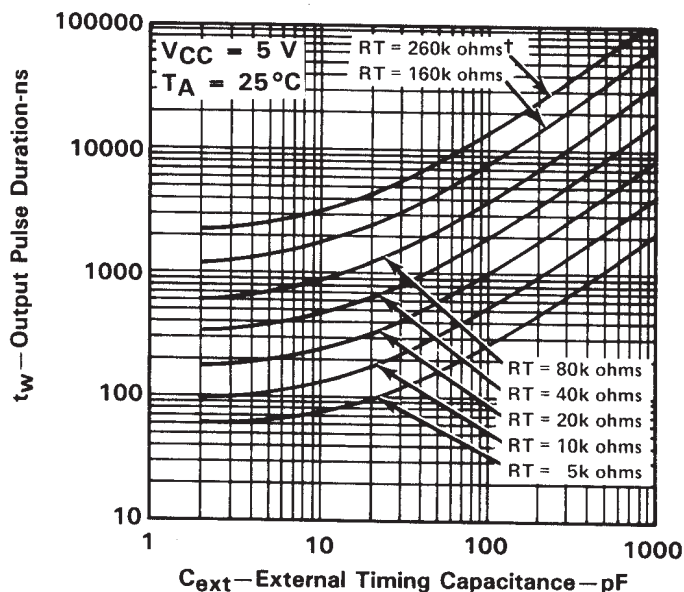
For maximum noise immunity, system ground should be applied to the C_{ext} node, even though the C_{ext} node is already tied to the ground lead internally. Due to the timing scheme used by the 'LS122 and 'LS123, a switching diode is not required to prevent reverse biasing when using electrolytic capacitors.



TIMING COMPONENT CONNECTIONS

FIGURE 5

'LS122, 'LS123 TYPICAL OUTPUT PULSE DURATION vs EXTERNAL TIMING CAPACITANCE



† This value of resistance exceeds the maximum recommended for use over the full temperature range of the SN54LS circuits.

FIGURE 6

SN54LS122, SN54LS123, SN74LS122, SN74LS123 RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

SDLS043 – DECEMBER 1983 – REVISED MARCH 1988

TYPICAL APPLICATION DATA FOR 'LS122, 'LS123†

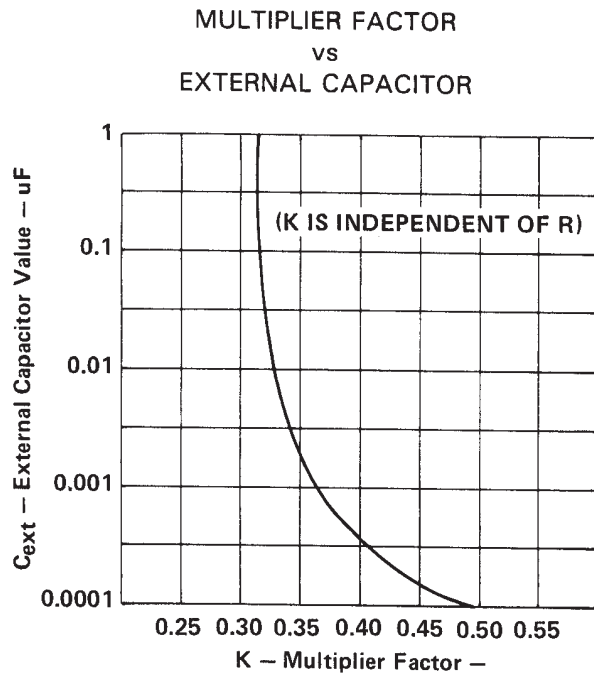


FIGURE 7

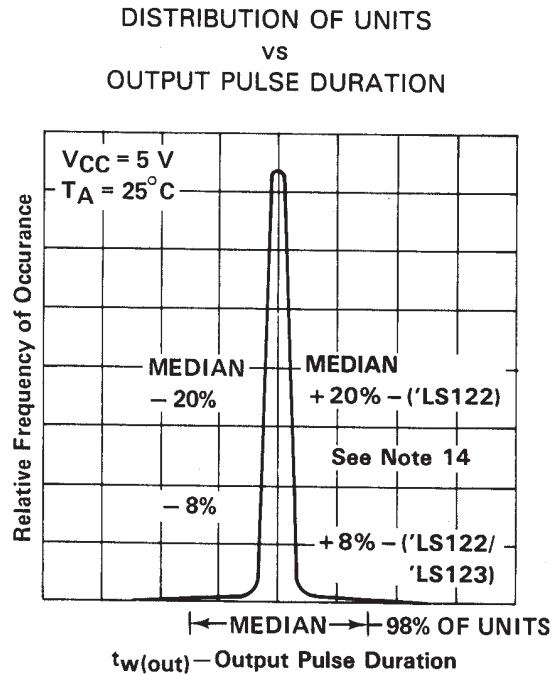


FIGURE 8

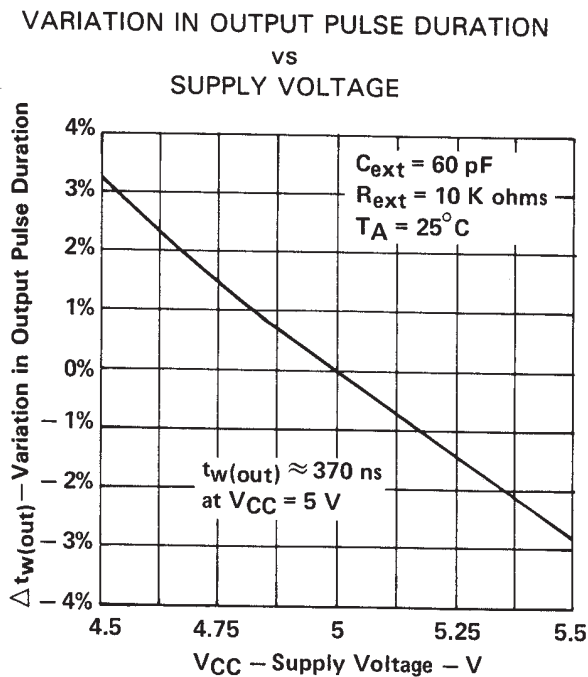


FIGURE 9

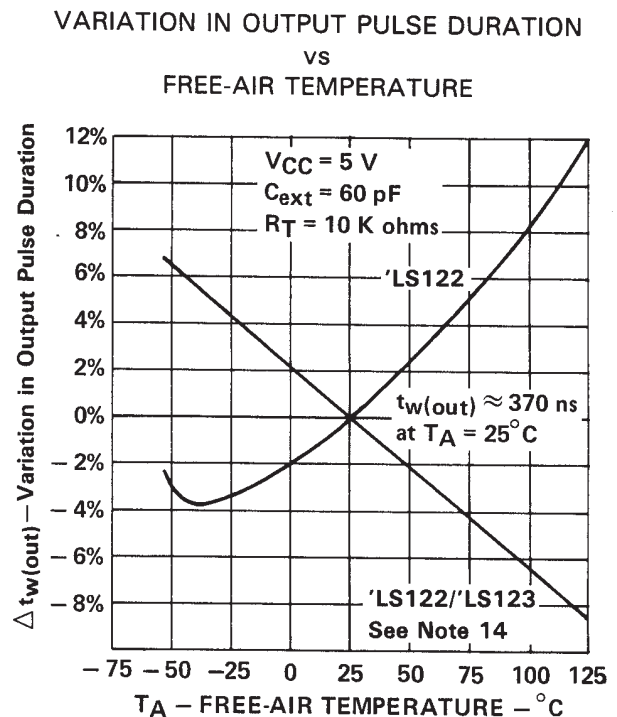


FIGURE 10

NOTE 14: For the 'LS122, the internal timing resistor, R_{int} was used. For the 'LS122/123, an external timing resistor was used for R_T .

†Data for temperatures below $0^\circ C$ and above $70^\circ C$ and for supply voltages below 4.75 V and above 5.25 V are applicable for SN54LS122 and SN54LS123 only.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|--------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|------------------------------------|
| 5962-7603901VEA | Active | Production | CDIP (J) 16 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-7603901VE A SNV54LS123J |
| 5962-7603901VFA | Active | Production | CFP (W) 16 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-7603901VF A SNV54LS123W |
| 7603901EA | Active | Production | CDIP (J) 16 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 7603901EA SNJ54LS123J |
| 7603901FA | Active | Production | CFP (W) 16 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 7603901FA SNJ54LS123W |
| JM38510/01203BEA | Active | Production | CDIP (J) 16 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 01203BEA |
| JM38510/31401B2A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 31401B2A |
| JM38510/31401BEA | Active | Production | CDIP (J) 16 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 31401BEA |
| JM38510/31401BFA | Active | Production | CFP (W) 16 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 31401BFA |
| SN54123J | Active | Production | CDIP (J) 16 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54123J |
| SN54LS123J | Active | Production | CDIP (J) 16 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54LS123J |
| SN74123N | Active | Production | PDIP (N) 16 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74123N |
| SN74LS122D | Obsolete | Production | SOIC (D) 14 | - | - | Call TI | Call TI | 0 to 70 | LS122 |
| SN74LS122DR | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS122 |
| SN74LS122N | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74LS122N |
| SN74LS122NSR | Active | Production | SOP (NS) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS122 |
| SN74LS123D | Active | Production | SOIC (D) 16 | 40 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS123 |
| SN74LS123DBR | Active | Production | SSOP (DB) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | - | LS123 |
| SN74LS123DR | Active | Production | SOIC (D) 16 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS123 |
| SN74LS123DRG4 | Active | Production | SOIC (D) 16 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS123 |
| SN74LS123N | Active | Production | PDIP (N) 16 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74LS123N |
| SN74LS123NSR | Active | Production | SOP (NS) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS123 |
| SN74LS123NSRG4 | Active | Production | SOP (NS) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS123 |

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|------------------------------|------------|-------------------|----------------|-----------------------|----------|--------------------------------|-----------------------------|--------------|--------------------------|
| SNJ54123J | Active | Production | CDIP (J) 16 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SNJ54123J |
| SNJ54123W | Active | Production | CFP (W) 16 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SNJ54123W |
| SNJ54LS123FK | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SNJ54LS123FK |
| SNJ54LS123J | Active | Production | CDIP (J) 16 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 7603901EA SNJ54LS123J |
| SNJ54LS123W | Active | Production | CFP (W) 16 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 7603901FA SNJ54LS123W |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54123, SN54LS123, SN54LS123-SP, SN74123, SN74LS123 :

- Catalog : [SN74123](#), [SN74LS123](#), [SN54LS123](#)
- Military : [SN54123](#), [SN54LS123](#)
- Space : [SN54LS123-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LS122DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LS122NSR | SOP | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LS123DBR | SSOP | DB | 16 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |
| SN74LS123DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LS123NSR | SOP | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LS123NSR | SOP | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LS122DR | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| SN74LS122NSR | SOP | NS | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LS123DBR | SSOP | DB | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LS123DR | SOIC | D | 16 | 2500 | 353.0 | 353.0 | 32.0 |
| SN74LS123NSR | SOP | NS | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LS123NSR | SOP | NS | 16 | 2000 | 353.0 | 353.0 | 32.0 |

TUBE



*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-7603901VFA | W | CFP | 16 | 25 | 506.98 | 26.16 | 6220 | NA |
| JM38510/31401B2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| JM38510/31401BFA | W | CFP | 16 | 25 | 506.98 | 26.16 | 6220 | NA |
| M38510/31401B2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| M38510/31401BFA | W | CFP | 16 | 25 | 506.98 | 26.16 | 6220 | NA |
| SN74123N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74123N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS122N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS122N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS123D | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| SN74LS123DE4 | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| SN74LS123N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS123NE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54123W | W | CFP | 16 | 25 | 506.98 | 26.16 | 6220 | NA |
| SNJ54LS123FK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



NON SOLDER MASK
DEFINED



SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

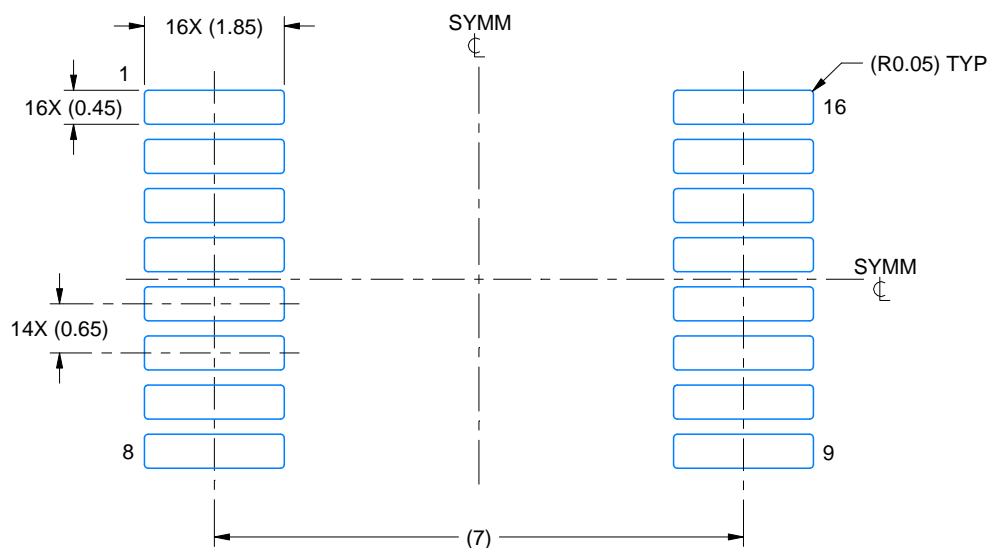
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

EXAMPLE BOARD LAYOUT

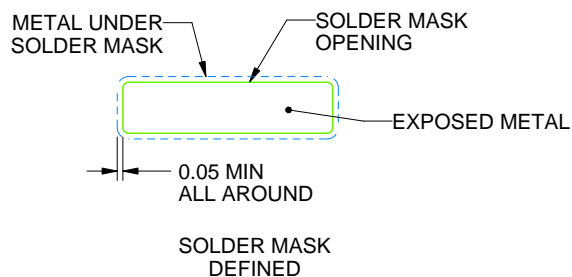
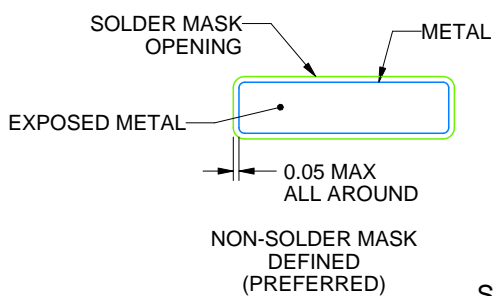
DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within MIL STD 1835 GDFP2-F16

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| PINS ** DIM | 14 | 16 | 18 | 20 |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



| PINS ** | 14 | 16 | 18 | 20 |
|---------------------|------------------|------------------|------------------|------------------|
| DIM | | | | |
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS-001 VARIATION | AA | BB | AC | AD |



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.



SOP - 2.00 mm max height

[illegible]

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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