CC1120 High-Performance RF Transceiver for Narrowband Systems

1 Device Overview

1.1 Features

- High-Performance, Single-Chip Transceiver
  - Adjacent Channel Selectivity: 64 dB at 12.5-kHz Offset
  - Blocking Performance: 91 dB at 10 MHz
  - Excellent Receiver Sensitivity:
    - –123 dBm at 1.2 kbps
    - –110 dBm at 50 kbps
    - –127 dBm Using Built-in Coding Gain
  - Very Low Phase Noise: –111 dBc/Hz at 10-kHz Offset
- Suitable for Systems Targeting ETSI Category 1 Compliance in 169-MHz and 433-MHz Bands
- High Spectral Efficiency (9.6 kbps in 12.5-kHz Channel in Compliance With FCC Narrowbanding Mandate)
- Separate 128-Byte RX and TX FIFOs
- Support for Seamless Integration With the CC1190 Device for Increased Range Giving up to 3-dB Improvement in Sensitivity and up to +27-dBm Output Power
- Power Supply
  - Wide Supply Voltage Range (2.0 V to 3.6 V)
  - Low Current Consumption:
    - RX: 2 mA in RX Sniff Mode
    - RX: 17 mA Peak Current in Low-Power Mode
    - RX: 22 mA Peak Current in High-Performance Mode
    - TX: 45 mA at +14 dBm
  - Power Down: 0.12 µA (0.5 µA With eWOR Timer Running)
- Programmable Output Power up to +16 dBm With 0.4-dB Step Size
- Automatic Output Power Ramping
- Configurable Data Rates: 0 to 200 kbps
- Supported Modulation Formats: 2-FSK, 2-GFSK, 4-FSK, 4-GFSK, MSK, OOK
- WaveMatch: Advanced Digital Signal Processing for Improved Sync Detect Performance
- RoHS-Compliant 5-mm × 5-mm No-Lead QFN 32-Pin Package (RHB)
- Regulations – Suitable for Systems Targeting Compliance With
  - **Europe:** ETSI EN 300 220, ETSI EN 54-25
  - **US:** FCC CFR47 Part 15, FCC CFR47 Part 90, 24, and 101
  - **Japan:** ARIB RCR STD-T30, ARIB STD-T67, ARIB STD-T108
- Peripherals and Support Functions
  - Enhanced Wake-On-Radio (eWOR) Functionality for Automatic Low-Power Receive Polling
  - Includes Functions for Antenna Diversity Support
  - Support for Retransmissions
  - Support for Automatic Acknowledge of Received Packets
  - TCXO Support and Control, Also in Power Modes
  - Automatic Clear Channel Assessment (CCA) for Listen-Before-Talk (LBT) Systems
  - Built-in Coding Gain Support for Increased Range and Robustness
  - Digital RSSI Measurement
  - Temperature Sensor

1.2 Applications

- Narrowband Ultra-Low-Power Wireless Systems With Channel Spacing Down to 12.5 kHz
- 169-, 315-, 433-, 868-, 915-, 920-, 950-MHz ISM/SRD Band
- Wireless Metering and Wireless Smart Grid (AMR and AMI)
- IEEE 802.15.4g Systems
- Home and Building Automation
- Wireless Alarm and Security Systems
- Industrial Monitoring and Control
- Wireless Healthcare Applications
- Wireless Sensor Networks and Active RFID
- Private Mobile Radios

1.3 Description

The CC1120 device is a fully integrated single-chip radio transceiver designed for high performance at very low-power and low-voltage operation in cost-effective wireless systems. All filters are integrated, thus removing the need for costly external SAW and IF filters. The device is mainly intended for Industrial, Scientific, and Medical (ISM) applications and Short Range Device (SRD) frequency bands at 164 to 192 MHz, 274 to 320 MHz, 410 to 480 MHz, and 820 to 960 MHz.

The CC1120 device provides extensive hardware support for packet handling, data buffering, burst transmissions, clear channel assessment, link quality indication, and wake-on-radio. The main operating parameters of the CC1120 device can be controlled through an SPI interface. In a typical system, the CC1120 device is used with a microcontroller and only a few external passive components.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CC1120	VQFN (32)	5.00 mm × 5.00 mm

(1) For more information, see Section 8, *Mechanical Packaging and Orderable Information*

1.4 Functional Block Diagram

Figure 1-1 shows the system block diagram of the CC1120 device.

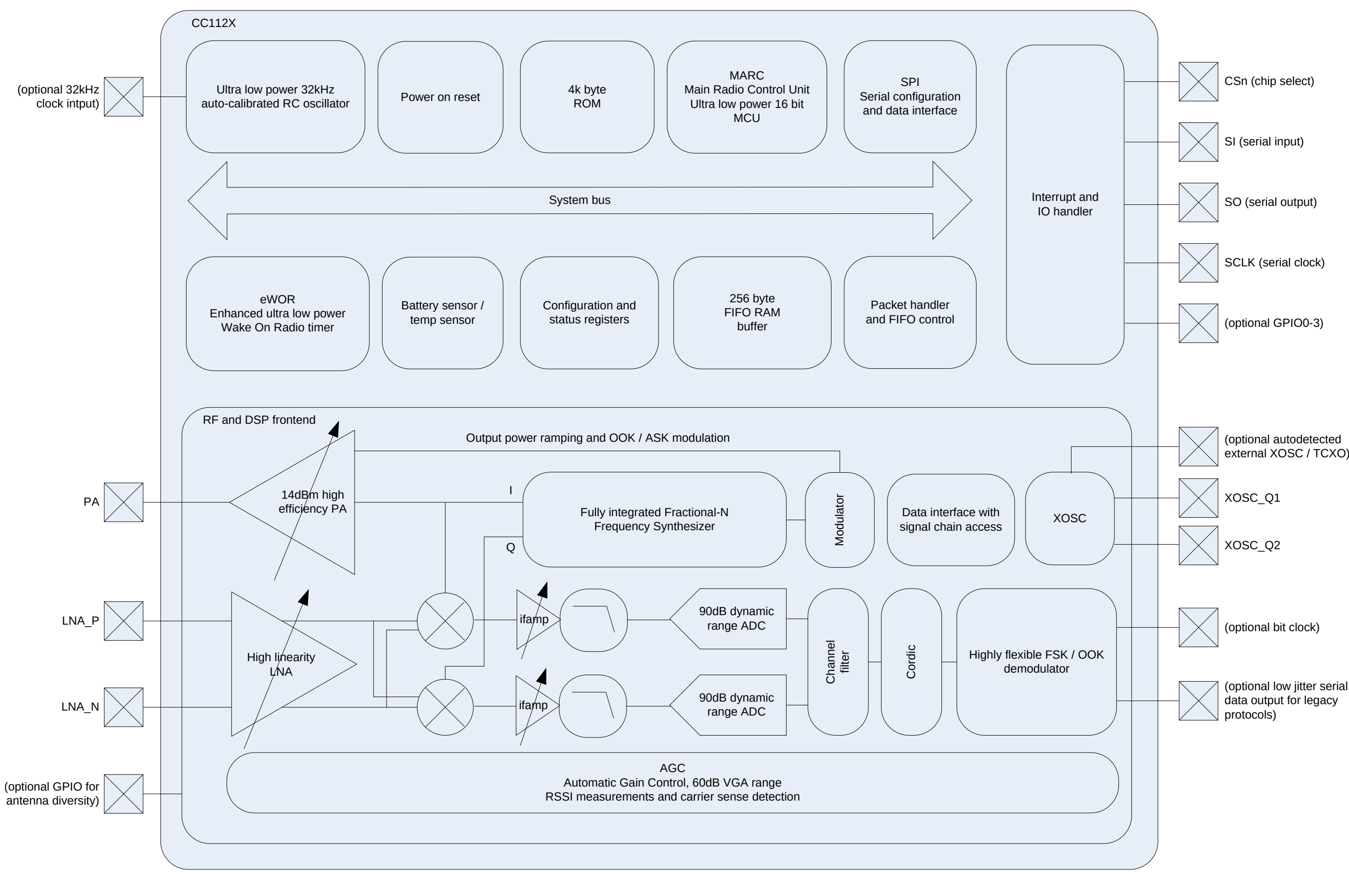

Figure 1-1. Functional Block Diagram

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2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (September 2014) to Revision H	Page
• Moved storage temperature range back to *Absolute Maximum Ratings* table	7
• Updated the formatting of the *Specifications* section	7
• Changed clock frequency minimum value FROM: 32 MHz TO: 31.25 MHz in *32-MHz Clock Input (TCXO)*	14
• Added clock frequency typical value of 32 MHz to *32-MHz Clock Input (TCXO)*	14
• Changed crystal frequency minimum value FROM: 32 MHz TO: 31.25 MHz in the *32-MHz Crystal Oscillator* table	14
• Added crystal frequency typical value of 32 MHz in the *32-MHz Crystal Oscillator* table	14
• Changed table title FROM: *Wakeup and Timing* TO: *Timing Requirements*	16

Changes from Revision F (July 2014) to Revision G	Page
• Added "Ambient" to the temperature range condition and removed Tj from Temperature range	7
• Added data to TCXO table	14

3 Terminal Configuration and Functions

3.1 Pin Diagram

Figure 3-1 shows pin names and locations for the CC1120 device.

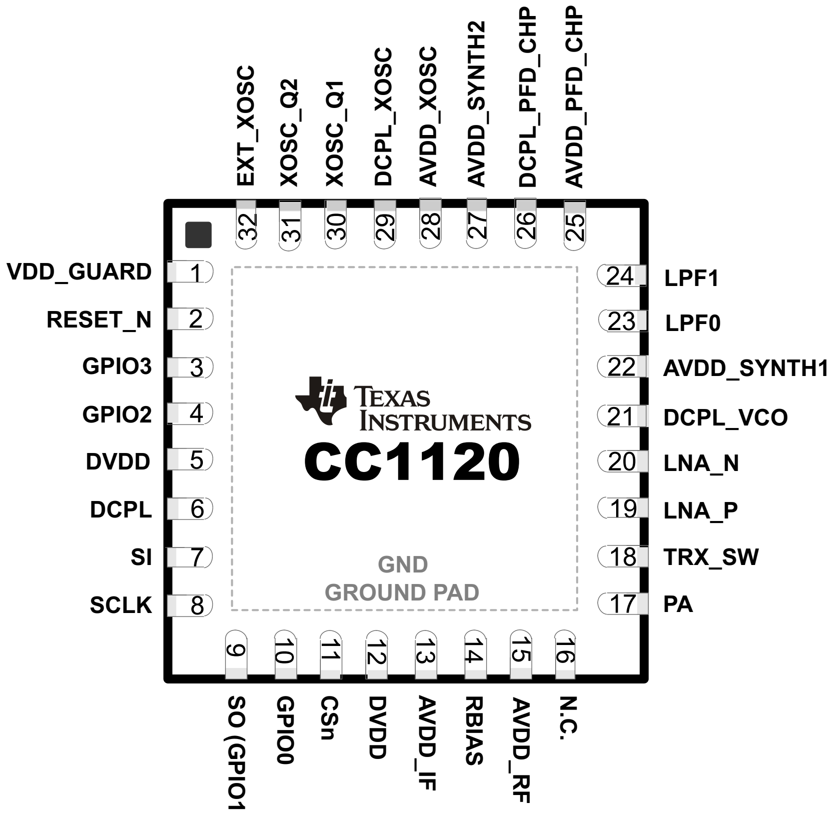


Figure 3-1. Package 5-mm × 5-mm QFN

3.2 Pin Configuration

The following table lists the pinout configuration for the CC1120 device.

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VDD_GUARD	Power	2.0–3.6 V VDD
2	RESET_N	Digital input	Asynchronous, active-low digital reset
3	GPIO3	Digital I/O	General-purpose I/O
4	GPIO2	Digital I/O	General-purpose I/O
5	DVDD	Power	2.0–3.6 VDD to internal digital regulator
6	DCPL	Power	Digital regulator output to external decoupling capacitor
7	SI	Digital input	Serial data in
8	SCLK	Digital input	Serial data clock
9	SO(GPIO1)	Digital I/O	Serial data out (general-purpose I/O)
10	GPIO0	Digital I/O	General-purpose I/O
11	CSn	Digital input	Active-low chip select
12	DVDD	Power	2.0–3.6 V VDD
13	AVDD_IF	Power	2.0–3.6 V VDD
14	RBIAS	Analog	External high-precision resistor
15	AVDD_RF	Power	2.0–3.6 V VDD
16	N.C.	—	Not connected
17	PA	Analog	Single-ended TX output (requires DC path to VDD)
18	TRX_SW	Analog	TX and RX switch. Connected internally to GND in TX and floating (high-impedance) in RX.
19	LNA_P	Analog	Differential RX input (requires DC path to ground)
20	LNA_N	Analog	Differential RX input (requires DC path to ground)
21	DCPL_VCO	Power	Pin for external decoupling of VCO supply regulator
22	AVDD_SYNTH1	Power	2.0–3.6 V VDD
23	LPF0	Analog	External loop filter components
24	LPF1	Analog	External loop filter components
25	AVDD_PFD_CHP	Power	2.0–3.6 V VDD
26	DCPL_PFD_CHP	Power	Pin for external decoupling of PFD and CHP regulator
27	AVDD_SYNTH2	Power	2.0–3.6 V VDD
28	AVDD_XOSC	Power	2.0–3.6 V VDD
29	DCPL_XOSC	Power	Pin for external decoupling of XOSC supply regulator
30	XOSC_Q1	Analog	Crystal oscillator pin 1 (must be grounded if a TCXO or other external clock connected to EXT_XOSC is used)
31	XOSC_Q2	Analog	Crystal oscillator pin 2 (must be left floating if a TCXO or other external clock connected to EXT_XOSC is used)
32	EXT_XOSC	Digital input	Pin for external clock input (must be grounded if a regular crystal connected to XOSC_Q1 and XOSC_Q2 is used)
—	GND	Ground pad	The ground pad must be connected to a solid ground plane.

4 Specifications

All measurements performed on CC1120EM_868_915 rev.1.0.1, CC1120EM_955 rev.1.2.1, CC1120EM_420_470 rev.1.0.1, or CC1120EM_169 rev.1.2.

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
Supply voltage (VDD, AVDD_x)	All supply pins must have the same voltage	–0.3	3.9	V
Input RF level			+10	dBm
Voltage on any digital pin	Max 3.9 V	–0.3	VDD + 0.3	V
Voltage on analog pins (including DCPL pins)		–0.3	2.0	V
Storage temperature, T_{stg}		–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under general characteristics is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS} unless otherwise noted.

4.1 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge (ESD) performance	Human body model (HBM), per ANSI/ESDA/JEDEC JS001(1)		±2	kV
		Charged device model (CDM), per JESD22-C101(2)	All pins	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V HBM allows safe manufacturing with a standard ESD control process.

4.2 Recommended Operating Conditions (General Characteristics)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Voltage supply range	All supply pins must have the same voltage	2.0		3.6	V
Voltage on digital inputs		0		VDD	V
Ambient temperature range		–40		85	°C

4.3 RF Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency bands		820		960	MHz
		410		480	
	See SWRA398, *Using the CC112x/CC1175 at 274 to 320 MHz,* for more information	(273.3)		(320)	
		164		192	
	Contact TI for more information about the use of these frequency bands	(205)		(240)	
		(136.7)		(160)	
Frequency resolution	In 820–950 MHz band		30		Hz
	In 410–480 MHz band		15		
	In 164–192 MHz band		6		
Data rate	Packet mode	0		200	kbps
	Transparent mode	0		100	
Data rate step size			1e-4		bps

4.4 Power Consumption Summary

T_A = 25°C, VDD = 3.0 V if nothing else stated

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT CONSUMPTION: STATIC MODES						
Power down with retention				0.12	1	µA
		Low-power RC oscillator running		0.5		
XOFF mode		Crystal oscillator / TCXO disabled		170		µA
IDLE mode		Clock running, system waiting with no radio activity		1.3		mA
CURRENT CONSUMPTION, TRANSMIT MODES						
TX current consumption +10 dBm		950-MHz band (high-performance mode)		37		mA
TX current consumption 0 dBm				26		mA
TX current consumption +14 dBm		868-, 915-, and 920-MHz bands (high-performance mode)		45		mA
TX current consumption +10 dBm				34		mA
TX current consumption +15 dBm		434-MHz band (high-performance mode)		50		mA
TX current consumption +14 dBm				45		mA
TX current consumption +10 dBm				34		mA
TX current consumption +15 dBm		169-MHz band (high-performance mode)		54		mA
TX current consumption +14 dBm				49		mA
TX current consumption +10 dBm				41		mA
LOW-POWER MODE(1)						
TX current consumption +10 dBm				32		mA
CURRENT CONSUMPTION, RECEIVE MODE (HIGH-PERFORMANCE MODE)(1)						
RX wait for sync	1.2 kbps, 4-byte preamble	Using RX sniff mode, where the receiver wakes up at regular intervals to look for an incoming packet(2)		2		mA
	38.4 kbps, 4-byte preamble			13.4		
RX peak current	433-, 868-, 915-, 920-, and 950–MHz bands	Peak current consumption during packet reception at the sensitivity threshold		22		mA
	169-MHz band			23		
Average current consumption Check for data packet every 1 second using Wake on Radio		50 kbps, 5-byte preamble, 40-kHz RC oscillator used as sleep timer		15		µA
CURRENT CONSUMPTION, RECEIVE MODE (LOW-POWER MODE)(1)						
RX peak current Low-power RX mode	1.2 kbps	Peak current consumption during packet reception at the sensitivity level		17		mA

(1) T_A = 25°C, VDD = 3.0 V, f_c = 869.5 MHz if nothing else stated.
(2) See the sniff mode design note for more information (SWRA428).

4.5 Receive Parameters

All RX measurements made at the antenna connector, to a bit error rate (BER) limit of 1%.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL RECEIVE PARAMETERS (HIGH-PERFORMANCE MODE)(1)						
Saturation				+10		dBm
Digital channel filter programmable bandwidth			8		200	kHz
IIP3, normal mode		At maximum gain		–14		dBm
IIP3, high linearity mode		Using 6-dB gain reduction in front end		–8		dBm
Data rate offset tolerance		With carrier sense detection enabled and assuming 4-byte preamble		±12%		
Data rate offset tolerance		With carrier sense detection disabled		±0.2%		
Spurious emissions	1–13 GHz (VCO leakage at 3.5 GHz)	Radiated emissions measured according to ETSI EN 300 220, f_c = 869.5 MHz		–56		dBm
Spurious emissions	30 MHz to 1 GHz	Radiated emissions measured according to ETSI EN 300 220, f_c = 869.5 MHz		< –57		dBm
Optimum source impedance	868-, 915-, and 920-MHz bands	(Differential or single-ended RX configurations)		60 + j60 / 30 + j30		Ω
Optimum source impedance	433-MHz band	(Differential or single-ended RX configurations)		100 + j60 / 50 + j30		Ω
Optimum source impedance	169-MHz band	(Differential or single-ended RX configurations)		140 + j40 / 70 + j20		Ω
RX PERFORMANCE IN 950-MHZ BAND (HIGH-PERFORMANCE MODE)(2)						
Sensitivity(3)		1.2 kbps, DEV = 4 kHz CHF = 10 kHz(4)		–120		dBm
Sensitivity(3)		1.2 kbps, DEV = 20 kHz CHF = 50 kHz(4)		–114		dBm
Sensitivity(3)		50 kbps 2GFSK, DEV = 25 kHz, CHF = 100 kHz(4)		–107		dBm
Sensitivity(3)		200 kbps, DEV = 83 kHz (outer symbols), CHF = 200 kHz(4), 4GFSK(5)		–100		dBm
Blocking and Selectivity	1.2 kbps 2FSK, 12.5-kHz channel separation, 4-kHz deviation, 10-kHz channel filter	± 12.5 kHz (adjacent channel)		51		dB
Blocking and Selectivity	1.2 kbps 2FSK, 12.5-kHz channel separation, 4-kHz deviation, 10-kHz channel filter	± 25 kHz (alternate channel)		52		dB
Blocking and Selectivity	1.2 kbps 2FSK, 12.5-kHz channel separation, 4-kHz deviation, 10-kHz channel filter	± 1 MHz		73		dB
Blocking and Selectivity	1.2 kbps 2FSK, 12.5-kHz channel separation, 4-kHz deviation, 10-kHz channel filter	± 2 MHz		76		dB
Blocking and Selectivity	1.2 kbps 2FSK, 12.5-kHz channel separation, 4-kHz deviation, 10-kHz channel filter	± 10 MHz		81		dB
Blocking and Selectivity	1.2 kbps 2FSK, 50-kHz channel separation, 20-kHz deviation, 50-kHz channel filter	± 50 kHz (adjacent channel)		47		dB
Blocking and Selectivity	1.2 kbps 2FSK, 50-kHz channel separation, 20-kHz deviation, 50-kHz channel filter	+ 100 kHz (alternate channel)		48		dB
Blocking and Selectivity	1.2 kbps 2FSK, 50-kHz channel separation, 20-kHz deviation, 50-kHz channel filter	± 1 MHz		69		dB
Blocking and Selectivity	1.2 kbps 2FSK, 50-kHz channel separation, 20-kHz deviation, 50-kHz channel filter	± 2 MHz		71		dB
Blocking and Selectivity	1.2 kbps 2FSK, 50-kHz channel separation, 20-kHz deviation, 50-kHz channel filter	± 10 MHz		78		dB
Blocking and Selectivity	50 kbps 2GFSK, 200-kHz channel separation, 25-kHz deviation, 100-kHz channel filter (Same modulation format as 802.15.4g Mandatory Mode)	± 200 kHz (adjacent channel)		43		dB
Blocking and Selectivity	50 kbps 2GFSK, 200-kHz channel separation, 25-kHz deviation, 100-kHz channel filter (Same modulation format as 802.15.4g Mandatory Mode)	± 400 kHz (alternate channel)		51		dB
Blocking and Selectivity	50 kbps 2GFSK, 200-kHz channel separation, 25-kHz deviation, 100-kHz channel filter (Same modulation format as 802.15.4g Mandatory Mode)	± 1 MHz		62		dB
Blocking and Selectivity	50 kbps 2GFSK, 200-kHz channel separation, 25-kHz deviation, 100-kHz channel filter (Same modulation format as 802.15.4g Mandatory Mode)	± 2 MHz		65		dB
Blocking and Selectivity	50 kbps 2GFSK, 200-kHz channel separation, 25-kHz deviation, 100-kHz channel filter (Same modulation format as 802.15.4g Mandatory Mode)	± 10 MHz		71		dB
Blocking and Selectivity	200 kbps 4GFSK, 83-kHz deviation (outer symbols), 200-kHz channel filter, zero IF	± 200 kHz (adjacent channel)		37		dB
Blocking and Selectivity	200 kbps 4GFSK, 83-kHz deviation (outer symbols), 200-kHz channel filter, zero IF	± 400 kHz (alternate channel)		44		dB
Blocking and Selectivity	200 kbps 4GFSK, 83-kHz deviation (outer symbols), 200-kHz channel filter, zero IF	± 1 MHz		55		dB
Blocking and Selectivity	200 kbps 4GFSK, 83-kHz deviation (outer symbols), 200-kHz channel filter, zero IF	± 2 MHz		58		dB
Blocking and Selectivity	200 kbps 4GFSK, 83-kHz deviation (outer symbols), 200-kHz channel filter, zero IF	± 10 MHz		64		dB

(1) T_A = 25°C, VDD = 3.0 V, f_c = 869.5 MHz if nothing else stated.
(2) T_A = 25°C, VDD = 3.0 V if nothing else stated.
(3) Sensitivity can be improved if the TX and RX matching networks are separated.
(4) DEV is short for deviation, CHF is short for Channel Filter Bandwidth
(5) BT = 0.5 is used in all GFSK measurements

Receive Parameters *(continued)*

All RX measurements made at the antenna connector, to a bit error rate (BER) limit of 1%.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RX PERFORMANCE IN 868-, 915-, AND 920-MHZ BANDS (HIGH-PERFORMANCE MODE) (2)						
Sensitivity		300 bps with coding gain (using a PN spreading sequence with 4 chips per data bit) DEV = 4 kHz CHF = 10 kHz (4)		–127		dBm
		1.2 kbps, DEV = 4 kHz CHF = 10 kHz (4)		–123		
		1.2 kbps, DEV = 10 kHz CHF = 42 kHz (4)		–120		
		1.2 kbps, DEV = 20 kHz CHF = 50 kHz (4)		–117		
		4.8 kbps OOK		–114		
		38.4 kbps, DEV = 20 kHz CHF = 100 kHz (4)		–110		
		50 kbps 2GFSK, DEV = 25 kHz, CHF = 100 kHz (4)		–110		
		200 kbps, DEV = 83 kHz (outer symbols), CHF = 200 kHz (4), 4GFSK		–103		
Blocking and Selectivity	1.2-kbps 2-FSK, 12.5-kHz channel separation, 4-kHz deviation, 10-kHz channel filter	± 12.5 kHz (adjacent channel)		54		dB
		± 25 kHz (alternate channel)		54		
		± 1 MHz		75		
		± 2 MHz		79		
		± 10 MHz		87		
	1.2-kbps 2-FSK, 12.5-kHz channel separation, using settings optimized for blocking performance (3-kHz deviation, 7.8-kHz channel filter, minimum loop bandwidth)	± 1 kHz		78		
		± 2 kHz		82		
		± 8 MHz		88		
		± 10 MHz		88		
	1.2-kbps 2-FSK, 50-kHz channel separation, 20-kHz deviation, 50-kHz channel filter	± 50 kHz (adjacent channel)		48		
		+ 100 kHz (alternate channel)		48		
		± 1 MHz		69		
		± 2 MHz		74		
		± 10 MHz		81		
	38.4-kbps 2-GFSK, 100-kHz channel separation, 20-kHz deviation, 100-kHz channel filter	+ 100 kHz (adjacent channel)		42		
		± 200 kHz (alternate channel)		43		
		± 1 MHz		62		
		± 2 MHz		66		
		± 10 MHz		74		
	50-kbps 2-GFSK, 200-kHz channel separation, 25-kHz deviation, 100-kHz channel filter (Same modulation format as 802.15.4g Mandatory Mode)	± 200 kHz (adjacent channel)		43		
		± 400 kHz (alternate channel)		50		
		± 1 MHz		61		
		± 2 MHz		65		
		± 10 MHz		74		
	200-kbps 4-GFSK, 83-kHz deviation (outer symbols), 200-kHz channel filter, zero IF	± 200 kHz (adjacent channel)		36		
		± 400 kHz (alternate channel)		44		
		± 1 MHz		55		
		± 2 MHz		59		
		± 10 MHz		67		
Image rejection (image compensation enabled)		1.2 kbps, DEV = 4 kHz CHF = 10 kHz (4), image at –125 kHz		54		dB

Receive Parameters *(continued)*

All RX measurements made at the antenna connector, to a bit error rate (BER) limit of 1%.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RX PERFORMANCE IN 434-MHZ BAND (HIGH-PERFORMANCE MODE)[2]						
Sensitivity		1.2 kbps, DEV = 4 kHz CHF = 10 kHz[4]		–123		dBm
		50 kbps 2GFSK, DEV = 25 kHz, CHF = 100 kHz		–109		
		1.2 kbps, DEV = 20 kHz CHF = 50 kHz[4]		–116		
Blocking and Selectivity	1.2 kbps 2FSK, 12.5-kHz channel separation, 4-kHz deviation, 10-kHz channel filter	± 12.5 kHz (adjacent channel)		60		dB
		± 25 kHz (alternate channel)		60		
		± 1 MHz		79		
		± 2 MHz		82		
		± 10 MHz		91		
	1.2 kbps 2FSK, 50-kHz channel separation, 20-kHz deviation, 50-kHz channel filter	± 50 kHz (adjacent channel)		54		
		+ 100 kHz (alternate channel)		54		
		± 1 MHz		74		
		± 2 MHz		78		
		± 10 MHz		86		
	38.4 kbps 2GFSK, 100-kHz channel separation, 20-kHz deviation, 100-kHz channel filter	+ 100 kHz (adjacent channel)		47		
		± 200 kHz (alternate channel)		50		
		± 1 MHz		67		
		± 2 MHz		71		
		± 10 MHz		78		
RX PERFORMANCE IN 169-MHZ BAND (HIGH-PERFORMANCE MODE)[2]						
Sensitivity		1.2 kbps, DEV = 4 kHz CHF = 10 kHz[4]		–123		dbm
		1.2 kbps, DEV = 20 kHz CHF = 50 kHz[4]		–117		
Blocking and Selectivity	1.2 kbps 2FSK, 12.5-kHz channel separation, 4-kHz deviation, 10-kHz channel filter	± 12.5 kHz (adjacent channel)		64		dB
		± 25 kHz (alternate channel)		66		
		± 1 MHz		82		
		± 2 MHz		83		
		± 10 MHz		89		
	1.2 kbps 2FSK, 50-kHz channel separation, 20-kHz deviation, 50-kHz channel filter	± 50 kHz (adjacent channel)		60		
		+ 100 kHz (alternate channel)		60		
		± 1 MHz		76		
		± 2 MHz		77		
		± 10 MHz		83		
Spurious response rejection	1.2 kbps 2FSK, 12.5-kHz channel separation, 4-kHz deviation, 10-kHz channel filter			70		dB
Image rejection (image compensation enabled)		1.2 kbps, DEV = 4 kHz CHF = 10 kHz[4], image at –125 kHz		66		dB

Receive Parameters *(continued)*

All RX measurements made at the antenna connector, to a bit error rate (BER) limit of 1%.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RX PERFORMANCE IN LOW-POWER MODE [1]						
Sensitivity		1.2 kbps, DEV = 4 kHz CHF = 10 kHz [4]		–111		dBm
		38.4 kbps, DEV = 50 kHz CHF = 100 kHz [4]		–99		
		50 kbps 2GFSK, DEV = 25 kHz, CHF = 100 kHz [4]		–99		
Blocking and Selectivity	1.2 kbps 2FSK, 12.5-kHz channel separation, 4-kHz deviation, 10-kHz channel filter	± 12.5 kHz (adjacent channel)		46		dB
		± 25 kHz (alternate channel)		46		
		± 1 MHz		73		
		± 2 MHz		78		
		± 10 MHz		79		
	1.2 kbps 2FSK, 50-kHz channel separation, 20-kHz deviation, 50-kHz channel filter	± 50 kHz (adjacent channel)		43		
		+ 100 kHz (alternate channel)		45		
		± 1 MHz		71		
		± 2 MHz		74		
		± 10 MHz		75		
	38.4 kbps 2GFSK, 100-kHz channel separation, 20-kHz deviation, 100-kHz channel filter	+ 100 kHz (adjacent channel)		37		
		+ 200 kHz (alternate channel)		43		
		± 1 MHz		58		
		± 2 MHz		62		
		+ 10 MHz		64		
	50 kbps 2GFSK, 200-kHz channel separation, 25-kHz deviation, 100-kHz channel filter (Same modulation format as 802.15.4g Mandatory Mode)	+ 200 kHz (adjacent channel)		43		
		+ 400 kHz (alternate channel)		52		
		± 1 MHz		60		
		± 2 MHz		64		
		± 10 MHz		65		
Saturation				+10		dBm

4.6 Transmit Parameters

T_A = 25°C, VDD = 3.0 V, f_c = 869.5 MHz if nothing else stated

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum output power	At 950 MHz		+12		dBm
	At 915- and 920-MHz		+14		
	At 915- and 920-MHz with VDD = 3.6 V		+15		
	At 868 MHz		+15		
	At 868 MHz with VDD = 3.6 V		+16		
	At 433 MHz		+15		
	At 433 MHz with VDD = 3.6 V		+16		
	At 169 MHz		+15		
	At 169 MHz with VDD = 3.6 V		+16		
Minimum output power	Within fine step size range		–11		dBm
	Within coarse step size range		–40		
Output power step size	Within fine step size range		0.4		dB
Adjacent channel power	4-GFSK 9.6 kbps in 12.5-kHz channel, measured in 100-Hz bandwidth at 434 MHz (FCC Part 90 Mask D compliant)		–75		dBc
	4-GFSK 9.6 kbps in 12.5-kHz channel, measured in 8.75-kHz bandwidth (ETSI EN 300 220 compliant)		–58		
	2-GFSK 2.4 kbps in 12.5-kHz channel, 1.2-kHz deviation		–61		
Spurious emissions (not including harmonics)			<–60		dBm

Transmit Parameters *(continued)*

T_A = 25°C, VDD = 3.0 V, f_c = 869.5 MHz if nothing else stated

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Harmonics	2nd Harm, 169 MHz	Transmission at +14 dBm (or maximum allowed in applicable band where this is less than +14 dBm) using TI reference design Emissions measured according to ARIB T-96 in 950-MHz band, ETSI EN 300-220 in 170-, 433-, and 868-MHz bands and FCC part 15.247 in 450- and 915-MHz band Fourth harmonic in 915-MHz band will require extra filtering to meet FCC requirements if transmitting for long intervals (>50-ms periods)		–39		dBm
	3rd Harm, 169 MHz			–58		
	2nd Harm, 433 MHz			–56		
	3rd Harm, 433 MHz			–51		
	2nd Harm, 450 MHz			–60		
	3rd Harm, 450 MHz			–45		
	2nd Harm, 868 MHz			–40		
	3rd Harm, 868 MHz			–42		
	2nd Harm, 915 MHz			56		dBµV/m
	3rd Harm, 915 MHz			52		
	4th Harm, 915 MHz			60		
	2nd Harm, 950 MHz			–58		dBm
	3rd Harm, 950 MHz			–42		
Optimum load impedance	868-, 915-, and 920-MHz bands			35 + j35		Ω
	433 MHz band			55 + j25		
	169 MHz band			80 + j0		

4.7 PLL Parameters

T_A = 25°C, VDD = 3.0 V if nothing else stated

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
HIGH-PERFORMANCE MODE					
Phase noise in 950-MHz band	± 10 kHz offset		–99		dBc/Hz
	± 100 kHz offset		–99		
	± 1 MHz offset		–123		
Phase noise in 868-, 915-, 920-MHz bands	± 10 kHz offset		–99		dBc/Hz
	± 100 kHz offset		–100		
	± 1 MHz offset		–122		
Phase noise in 433-MHz band	± 10 kHz offset		–106		dBc/Hz
	± 100 kHz offset		–107		
	± 1 MHz offset		–127		
Phase noise in 169-MHz band	± 10 kHz offset		–111		dBc/Hz
	± 100 kHz offset		–116		
	± 1 MHz offset		–135		

PLL Parameters *(continued)*

T_A = 25°C, VDD = 3.0 V if nothing else stated

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOW-POWER MODE (1)					
Phase noise in 950-MHz band	± 10 kHz offset		–90		dBc/Hz
	± 100 kHz offset		–92		
	± 1 MHz offset		–124		
Phase noise in 868-, 915-, 920-MHz bands	± 10 kHz offset		–95		dBc/Hz
	± 100 kHz offset		–95		
	± 1 MHz offset		–124		
Phase noise in 433-MHz band	± 10 kHz offset		–98		dBc/Hz
	± 100 kHz offset		–102		
	± 1 MHz offset		–129		
Phase noise in 169-MHz band	± 10 kHz offset		–106		dBc/Hz
	± 100 kHz offset		–110		
	± 1 MHz offset		–136		

(1) T_A = 25°C, VDD = 3.0 V, f_c = 869.5 MHz if nothing else stated

4.8 32-MHz Clock Input (TCXO)

T_A = 25°C, VDD = 3.0 V if nothing else stated

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Clock frequency			31.25	32	33.6	MHz
TCXO with CMOS output (1)	High input voltage	TCXO with CMOS output directly coupled to pin EXT_OSC	1.4		VDD	V
	Low input voltage		0		0.6	
Clipped sine output	Clock input amplitude (peak-to-peak)	TCXO clipped sine output connected to pin EXT_OSC through series capacitor	0.8		1.5	V

(1) For TCXO with CMOS output rise and fall time, see Section 4.15.

4.9 32-MHz Crystal Oscillator

T_A = 25°C, VDD = 3.0 V if nothing else stated

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Crystal frequency	It is expected that there be will degraded sensitivity at multiples of XOSC/2 in RX, and an increase in spurious emissions when the RF channel is close to multiples of XOSC in TX. We recommend that the RF channel is kept RX_BW/2 away from XOSC/2 in RX, and that the level of spurious emissions be evaluated if the RF channel is closer than 1 MHz to multiples of XOSC in TX.	31.25	32	33.6	MHz
Load capacitance (C_L)			10		pF
ESR	Simulated over operating conditions			60	Ω

4.10 32-kHz Clock Input

T_A = 25°C, VDD = 3.0 V if nothing else stated

PARAMETER	MIN	TYP	MAX	UNIT
Clock frequency		32		kHz
32-kHz clock input pin input high voltage	0.8 × VDD			V
32-kHz clock input pin input high voltage			0.2 × VDD	V

4.11 32-kHz RC Oscillator

T_A = 25°C, VDD = 3.0 V if nothing else stated

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency	After calibration		32		kHz
Frequency accuracy after calibration	Relative to frequency reference (32-MHz crystal or TCXO)		±0.1%		
Initial calibration time(1)					

(1) For Initial calibration time of the 32-kHz RC Oscillator, see Section 4.15.

4.12 I/O and Reset

T_A = 25°C, VDD = 3.0 V if nothing else stated

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Logic input high voltage		0.8 × VDD			V
Logic input low voltage				0.2 × VDD	V
Logic output high voltage	At 4-mA output load or less	0.8 × VDD			V
Logic output low voltage	At 4-mA output load or less			0.2 × VDD	V
Power-on reset threshold	Voltage on DVDD pin		1.3		V

4.13 Temperature Sensor

T_A = 25°C, VDD = 3.0 V if nothing else stated(1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Temperature sensor range		–40		85	°C
Temperature coefficient	Change in sensor output voltage versus change in temperature		2.66		mV/°C
Typical output voltage	Typical sensor output voltage at T_A = 25°C, VDD = 3.0 V		794		mV
VDD coefficient	Change in sensor output voltage versus change in VDD		1.17		mV/V

(1) The CC1120 device can be configured to provide a voltage proportional to temperature on GPIO1. The temperature can be estimated by measuring this voltage (see Section 4.13, *Temperature Sensor*). For more information, refer to *CC112X/CC120X On-Chip Temperature Sensor* (SWRA415).

4.14 Thermal Resistance Characteristics for RHB Package

NAME	DESCRIPTION	°C/W(1)
$R\Theta_{JC(top)}$	Junction-to-case (top)	21.1
$R\Theta_{JB}$	Junction-to-board	5.3
$R\Theta_{JA}$	Junction-to-free air	31.3
Psi_{JT}	Junction-to-package top	0.2
Psi_{JB}	Junction-to-board	5.3
$R\Theta_{JC(bot)}$	Junction-to-case (bottom)	0.8

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

Power dissipation of 40 mW and an ambient temperature of 25ºC is assumed.

4.15 Timing Requirements

T_A = 25°C, VDD = 3.0 V, f_c = 869.5 MHz if nothing else stated

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
Power down to IDLE		Depends on crystal		0.4		ms
IDLE to RX/TX		Calibration disabled		166		µs
		Calibration enabled		461		µs
RX/TX turnaround				50		µs
RX/TX to IDLE time		Calibrate when leaving RX/TX enabled		296		µs
		Calibrate when leaving RX/TX disabled		0		µs
Frequency synthesizer calibration		When using SCAL strobe		391		µs
Time from start RX until valid RSSI Including gain settling (function of channel bandwidth. Programmable for trade-off between speed and accuracy)		12.5-kHz channels		4.6		ms
		200-kHz channels		0.3		ms
32-MHz CLOCK INPUT (TCXO)(1)						
TCXO with CMOS output	Rise and fall time				2	ns
32-kHz RC OSCILLATOR(2)						
Initial calibration time				1.6		ns

(1) See Section 4.8 for more information about the 32-MHz Clock Input (TCXO).
(2) See Section 4.11 for more information about the 32-kHz RC Oscillator.

4.16 Regulatory Standards

PERFORMANCE MODE	FREQUENCY BAND	SUITABLE FOR COMPLIANCE WITH
High-performance mode	820–960 MHz(1)	ARIB T-96 ARIB T-108 ETSI EN 300 220 category 2 ETSI EN 54-25 FCC PART 101 FCC PART 24 SUBMASK D FCC PART 15.247 FCC PART 15.249 FCC PART 90 MASK G FCC PART 90 MASK J
	410–480 MHz(2)	ARIB T-67 ARIB RCR STD-30 ETSI EN 300 220 category 1 FCC PART 90 MASK D FCC PART 90 MASK G
	164–192 MHz(2)	ETSI EN 300 220 category 1 FCC PART 90 MASK D
Low-power mode	820–960 MHz	ETSI EN 300 220 category 2 FCC PART 15.247 FCC PART 15.249
	410–480 MHz	ETSI EN 300 220 category 2
	164–192 MHz	ETSI EN 300 220 category 2

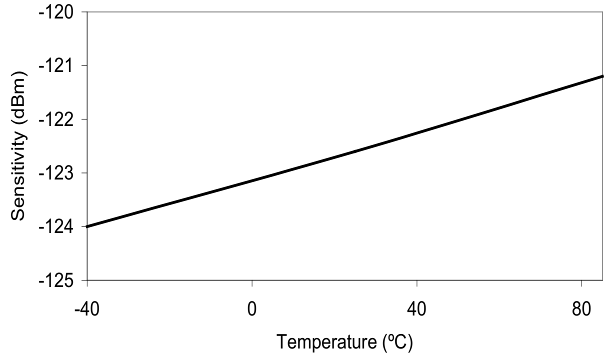
(1) Performance also suitable for systems targeting maximum allowed output power in the respective bands, using a range extender such as the CC1190 device
(2) Performance also suitable for systems targeting maximum allowed output power in the respective bands, using a range extender

4.17 Typical Characteristics

T_A = 25°C, VDD = 3.0 V, f_c = 869.5 MHz if nothing else stated.

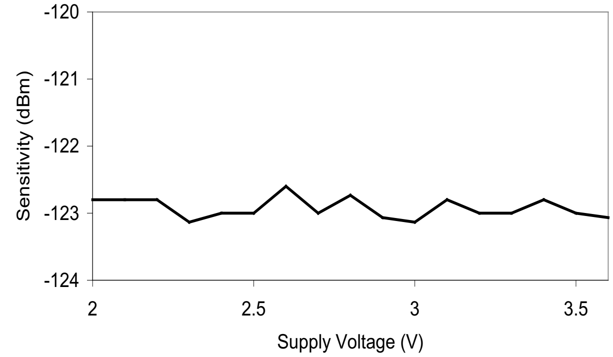
All measurements performed on CC1120EM_868_915 rev.1.0.1, CC1120EM_955 rev.1.2.1, CC1120EM_420_470 rev.1.0.1, or CC1120EM_169 rev.1.2.

Figure 4-17 was measured at the 50-Ω antenna connector.



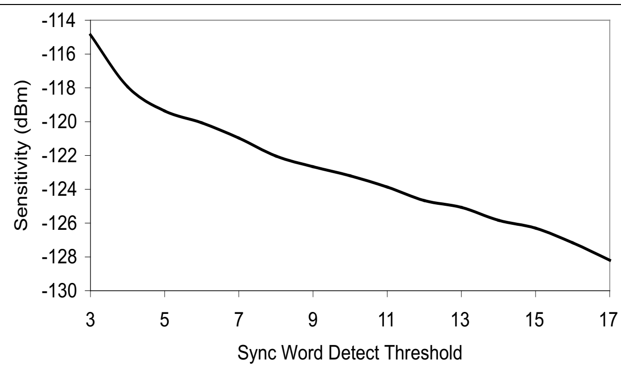
1.2 kbps, 4-kHz Deviation, 10-kHz Channel Filter Bandwidth

Figure 4-1. Sensitivity vs Temperature



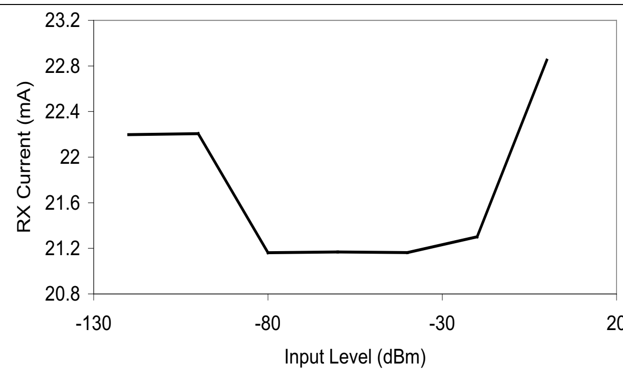
1.2 kbps, 4-kHz Deviation, 10-kHz Channel Filter Bandwidth

Figure 4-2. Sensitivity vs Voltage



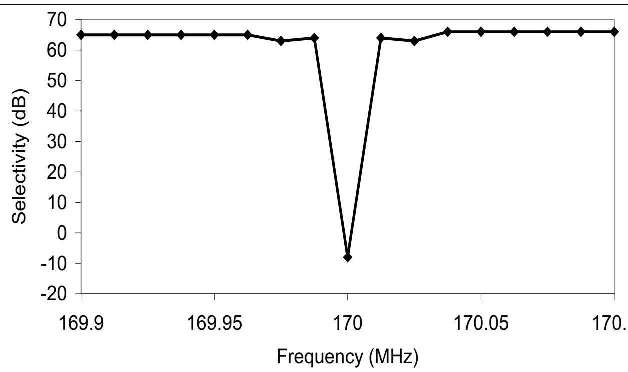
1.2 kbps, 4-kHz Deviation, 10-kHz Channel Filter Bandwidth

Figure 4-3. Sync Word Sensitivity vs Voltage



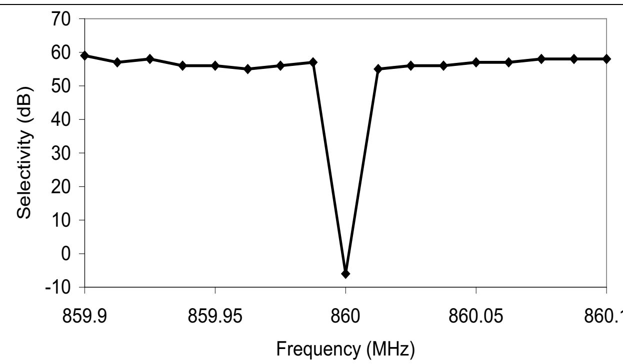
1.2 kbps, 4-kHz Deviation, 10-kHz Channel Filter Bandwidth

Figure 4-4. RX Current vs Input Level



1.2 kbps, 4-kHz Deviation, 10-kHz Channel Filter Bandwidth

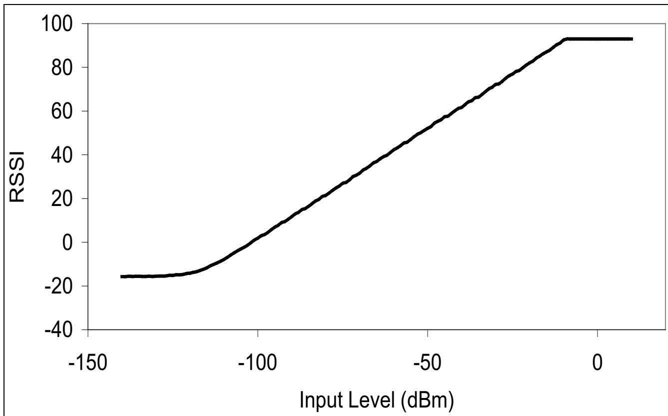
Figure 4-5. Selectivity vs Offset Frequency (12.5-kHz Channels)



1.2 kbps, 4-kHz Deviation, 10-kHz Channel Filter Bandwidth

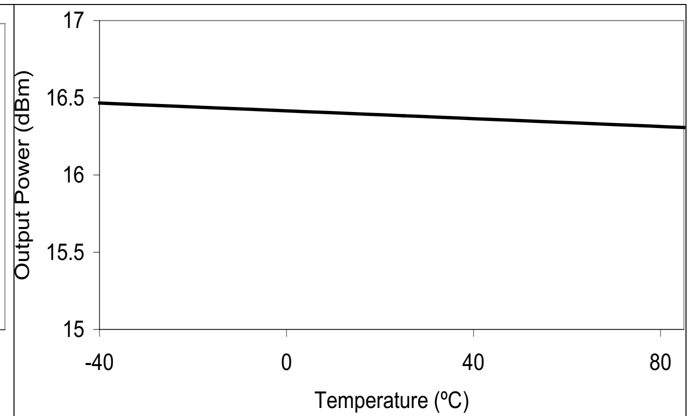
Figure 4-6. Selectivity vs Offset Frequency (12.5-kHz Channels)

Typical Characteristics *(continued)*



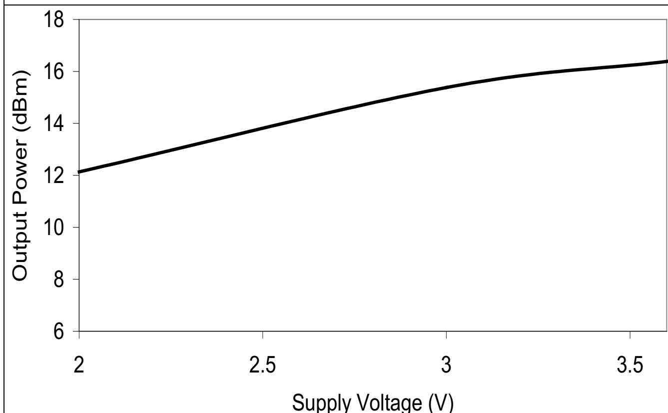
1.2 kbps, 4-kHz Deviation, 10-kHz Channel Filter Bandwidth

Figure 4-7. RSSI vs Input Level



Max Setting, 170 MHz, 3.6 V

Figure 4-8. Output Power vs Temperature



Max Setting, 170 MHz,

Figure 4-9. Output Power vs Voltage

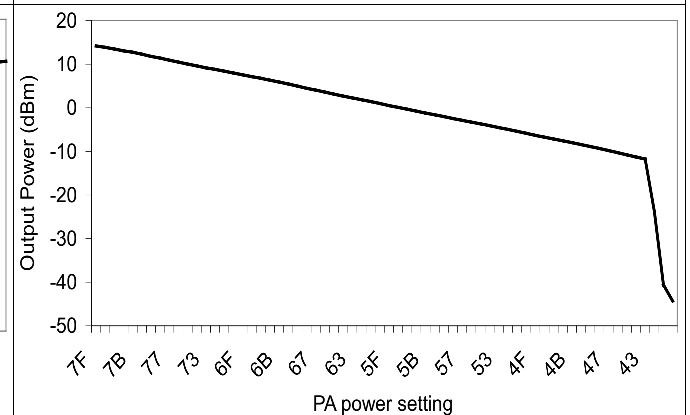


Figure 4-10. Output Power at 868 MHz vs PA Power Setting

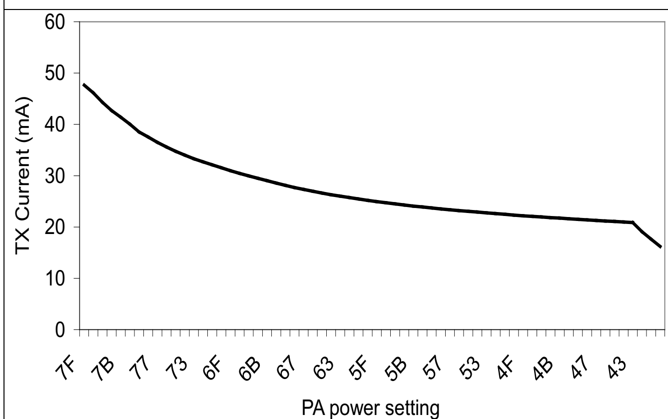


Figure 4-11. TX Current at 868 MHz vs PA Power Setting

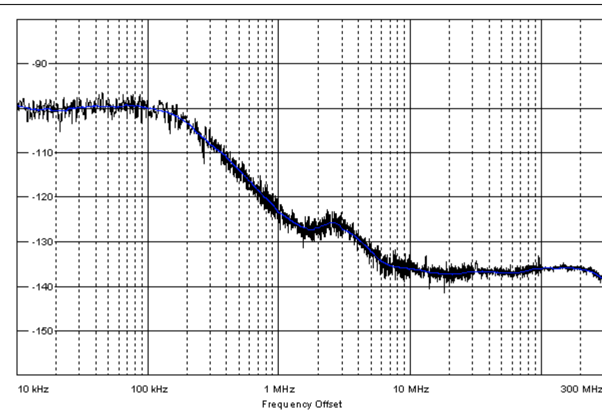
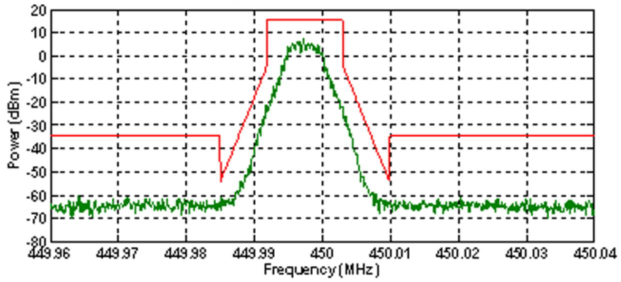


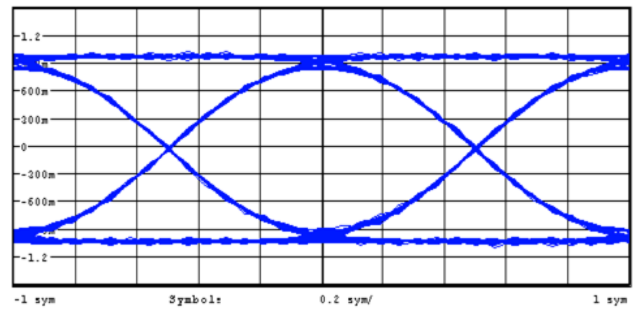
Figure 4-12. Phase Noise in 868-MHz Band

Typical Characteristics (continued)



9.6 kbps in 12.5-kHz Channel

Figure 4-13. FCC Part 90 Mask D



1.2 kbps 2-FSK, DEV = 4 kHz

Figure 4-14. Eye Diagram

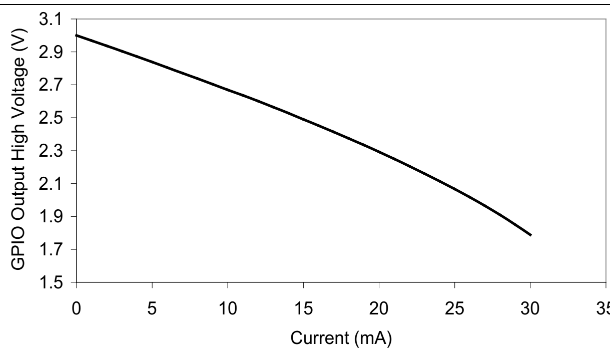


Figure 4-15. GPIO Output High Voltage vs Current Being Sourced

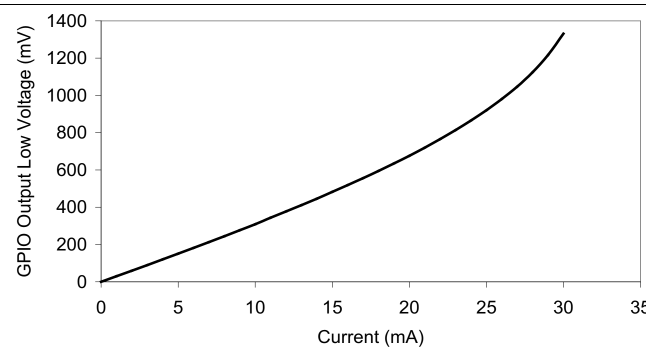


Figure 4-16. GPIO Output Low Voltage vs Current Being Sinked

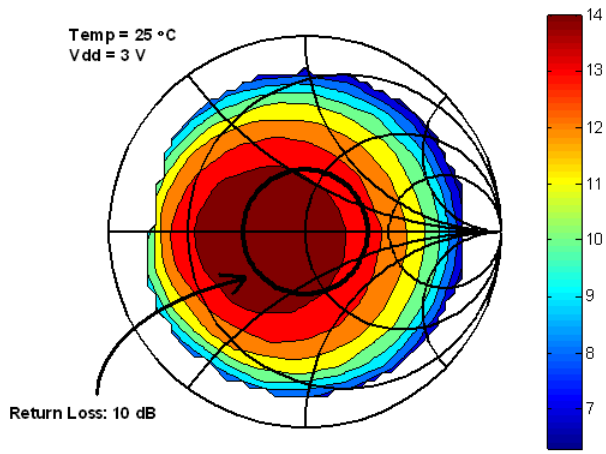


Figure 4-17. Output Power vs Load Impedance (+14-dBm Setting)

5 Detailed Description

5.1 Block Diagram

Figure 5-1 shows the system block diagram of the CC1120 devices.

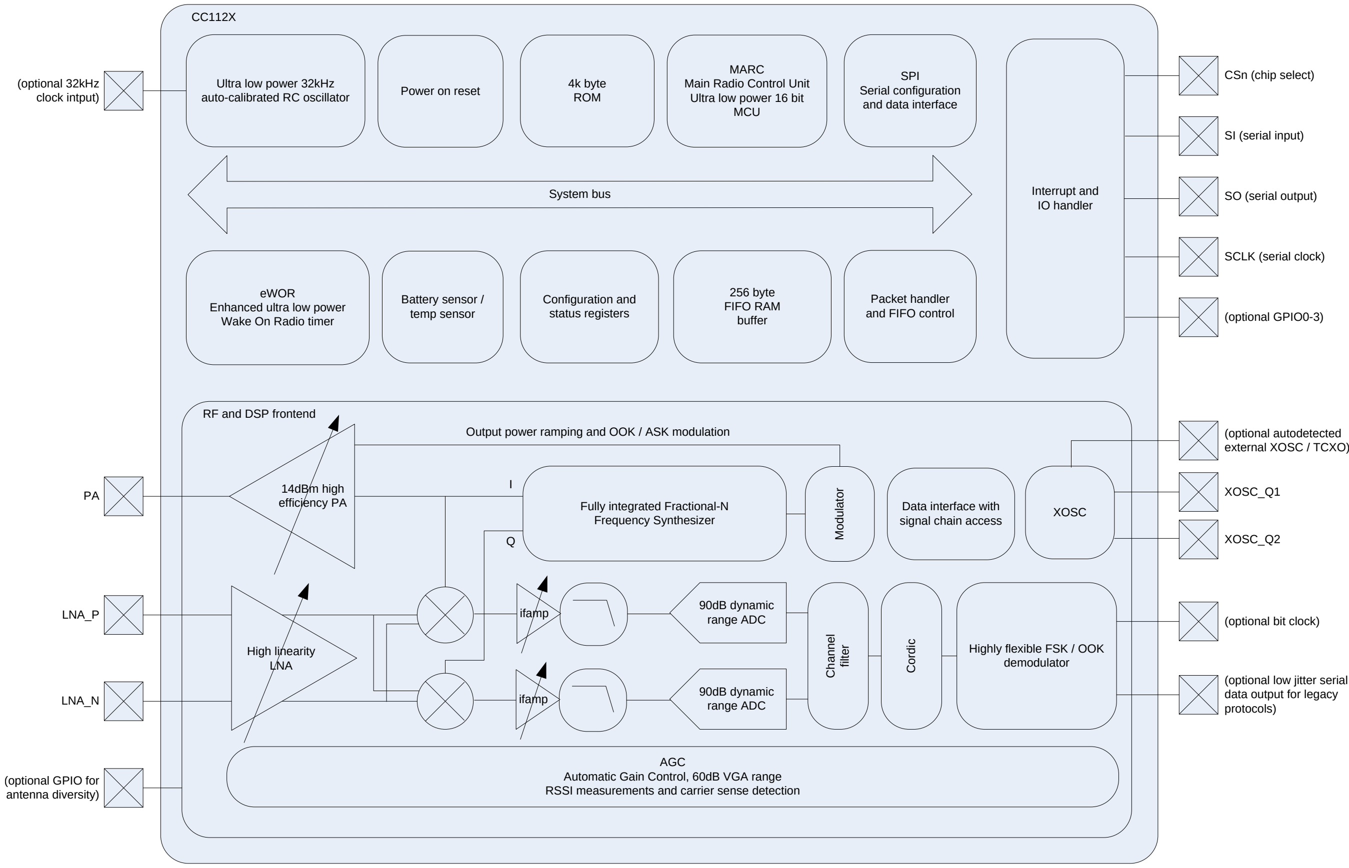


Figure 5-1. System Block Diagram

5.2 Frequency Synthesizer

At the center of the CC1120 device there is a fully integrated, fractional-N, ultra-high-performance frequency synthesizer. The frequency synthesizer is designed for excellent phase noise performance, providing very high selectivity and blocking performance. The system is designed to comply with the most stringent regulatory spectral masks at maximum transmit power.

Either a crystal can be connected to XOSC_Q1 and XOSC_Q2, or a TCXO can be connected to the EXT_XOSC input. The oscillator generates the reference frequency for the synthesizer, as well as clocks for the analog-to-digital converter (ADC) and the digital part. To reduce system cost, CC1120 device has high-accuracy frequency estimation and compensation registers to measure and compensate for crystal inaccuracies. This compensation enables the use of lower cost crystals. If a TCXO is used, the CC1120 device automatically turns on and off the TCXO when needed to support low-power modes and Wake-On-Radio operation.

5.3 Receiver

The CC1120 device features a highly flexible receiver. The received RF signal is amplified by the low-noise amplifier (LNA) and is down-converted in quadrature (I/Q) to the intermediate frequency (IF). At IF, the I/Q signals are digitized by the high dynamic-range ADCs.

An advanced automatic gain control (AGC) unit adjusts the front-end gain, and enables the CC1120 device to receive strong and weak signals, even in the presence of strong interferers. High-attenuation channels and data filtering enable reception with strong neighbor channel interferers. The I/Q signal is converted to a phase and magnitude signal to support the FSK and OOK modulation schemes.

NOTE

A unique I/Q compensation algorithm removes any problem of I/Q mismatch, thus avoiding time-consuming and costly I/Q image calibration steps.

The CC1120 device only requires preamble to settle the AGC. The minimum number of preamble required is 0.5 byte.

5.4 Transmitter

The CC1120 transmitter is based on direct synthesis of the RF frequency (in-loop modulation). To use the spectrum effectively, the CC1120 device has extensive data filtering and shaping in TX mode to support high throughput data communication in narrowband channels. The modulator also controls power ramping to remove issues such as spectral splattering when driving external high-power RF amplifiers.

5.5 Radio Control and User Interface

The CC1120 digital control system is built around the main radio control (MARC), which is implemented using an internal high-performance, 16-bit ultra-low-power processor. MARC handles power modes, radio sequencing, and protocol timing.

A 4-wire SPI serial interface is used for configuration and data buffer access. The digital baseband includes support for channel configuration, packet handling, and data buffering. The host MCU can stay in power-down mode until a valid RF packet is received. This greatly reduces power consumption. When the host MCU receives a valid RF packet, it burst-reads the data. This reduces the required computing power.

The CC1120 radio control and user interface are based on the widely used CC1101 transceiver. This relationship enables an easy transition between the two platforms. The command strobes and the main radio states are the same for the two platforms.

For legacy formats, the CC1120 device also supports two serial modes.

- Synchronous serial mode: The CC1120 device performs bit synchronization and provides the MCU with a bit clock with associated data.
- Transparent mode: The CC1120 device outputs the digital baseband signal using a digital interpolation filter to eliminate jitter introduced by digital filtering and demodulation.

5.6 Enhanced Wake-On-Radio (eWOR)

eWOR, using a flexible integrated sleep timer, enables automatic receiver polling with no intervention from the MCU. When the CC1120 device enters RX mode, it listens and then returns to sleep if a valid RF packet is not received. The sleep interval and duty cycle can be configured to make a trade-off between network latency and power consumption. Incoming messages are time-stamped to simplify timer re-synchronization.

The eWOR timer runs off an ultra-low-power 32-kHz RC oscillator. To improve timing accuracy, the RC oscillator can be automatically calibrated to the RF crystal in configurable intervals.

5.7 Sniff Mode

The CC1120 device supports quick start up times, and requires few preamble bits. Sniff mode uses these conditions to dramatically reduce the current consumption while the receiver is waiting for data.

Because the CC1120 device can wake up and settle much faster than the duration of most preambles, it is not required to be in RX mode continuously while waiting for a packet to arrive. Instead, the enhanced Wake-On-Radio feature can be used to put the device into sleep mode periodically. By setting an appropriate sleep time, the CC1120 device can wake up and receive the packet when it arrives with no performance loss. This sequence removes the need for accurate timing synchronization between transmitter and receiver, and lets the user trade off current consumption between the transmitter and receiver.

For more information, see the sniff mode design note (SWRA428).

5.8 Antenna Diversity

Antenna diversity can increase performance in a multipath environment. An external antenna switch is required. The CC1201 device uses one of the GPIO pins to automatically control the switch. This device also supports differential output control signals typically used in RF switches.

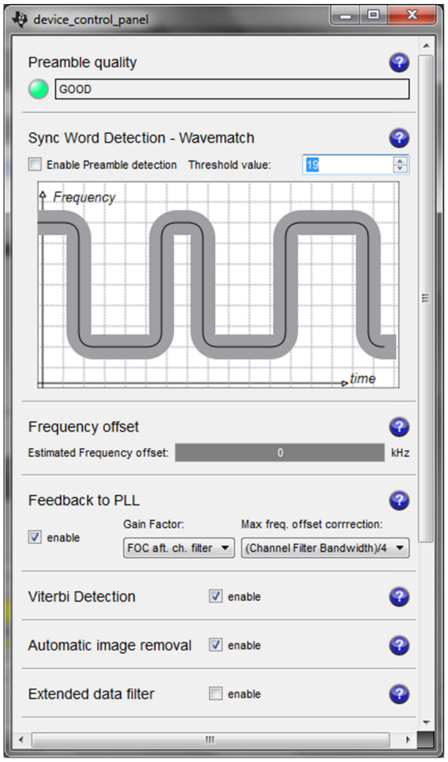
If antenna diversity is enabled, the GPIO alternates between high and low states until a valid RF input signal is detected. An optional acknowledge packet can be transmitted without changing the state of the GPIO.

An incoming RF signal can be validated by received signal strength or by using the automatic preamble detector. Using the automatic preamble detector ensures a more robust system and avoids the need to set a defined signal strength threshold (such a threshold sets the sensitivity limit of the system).

5.9 WaveMatch

Advanced capture logic locks onto the synchronization word and does not require preamble settling bytes. Therefore, receiver settling time is reduced to the settling time of the AGC, typically 4 bits.

The WaveMatch feature also greatly reduces false sync triggering on noise, further reducing the power consumption and improving sensitivity and reliability. The same logic can also be used as a high-performance preamble detector to reliably detect a valid preamble in the channel.



See SWRC046 for more information.

Figure 5-2. Receiver Configurator in SmartRF™ Studio

6 Application, Implementation, and Layout

NOTE

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

6.1 Application Information

6.1.1 Typical Application Circuit

NOTE

This section is intended only as an introduction. The reference designs listed in Section 6.1.2 show everything required.

Very few external components are required for the operation of the CC1120 device. Figure 6-1 shows a typical application circuit. The board layout will greatly influence the RF performance of the CC1120 device. Figure 6-1 does not show decoupling capacitors for power pins.

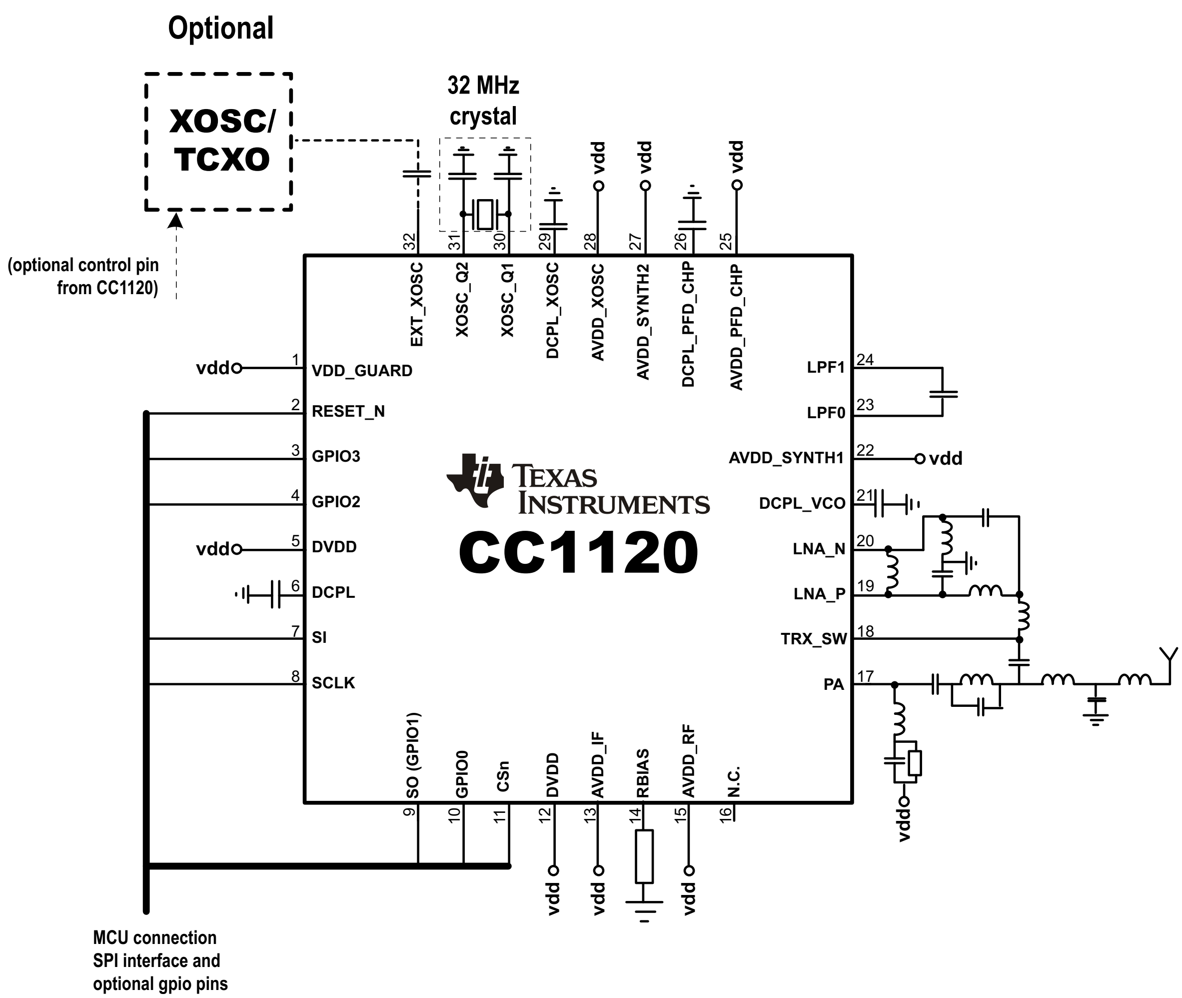


Figure 6-1. Typical Application Circuit

6.1.2 TI Reference Designs

The following reference designs are available for the CC1120 device:

CC1120EM-868-915-RD *CC1120EM 868- to 915-MHz Reference Design*
This RF Layout Reference Design demonstrates good decoupling and layout techniques for a low power RF device operating in the 868-MHz and 915-MHz frequency bands.

CC1120EM 868/915 MHz Reference Design (SWRC222)

CC112x IPC 868- and 915-MHz 2-layer Reference Design (SWRR106)

CC112x IPC 868- and 915-MHz 4-layer Reference Design (SWRR107)

CC1120EM-169-RD *CC1120EM 169-MHz Reference Design*
This RF Layout Reference Design demonstrates good decoupling and layout techniques for a low power RF device operating in the 169-MHz frequency band. (SWRC220)

CC1120EM-420-470-RD *CC1120EM 420- to 470-MHz Reference Design*
This RF Layout Reference Design demonstrates good decoupling and layout techniques for a low power RF device operating in the 420-470 MHz frequency band. (SWRC221)

7 Device and Documentation Support

7.1 Device Support

7.1.1 Development Support

7.1.1.1 Configuration Software

The CC1120 device can be configured using the SmartRF Studio software (SWRC046). The SmartRF Studio software is highly recommended for obtaining optimum register settings, and for evaluating performance and functionality.

7.1.2 Device and Development-Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, CC1120). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, RHB) and the temperature range (for example, blank is the default commercial temperature range) provides a legend for reading the complete device name for any CC1120 device.

For orderable part numbers of CC1120 devices in the QFN package types, see the Package Option Addendum of this document, the TI website (www.ti.com), or contact your TI sales representative.

7.2 Documentation Support

The following documents supplement the CC1120 transceiver. Copies of these documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided at www.ti.com.

SWRU295 *CC112X/CC1175 Low-Power High Performance Sub-1 GHz RF Transceivers/Transmitter User's Guide*

SWRA398 *Using the CC112x/CC1175 at 274 to 320 MHz*

SWRC046 *SmartRF Studio Software*

SWRA428 *CC112x/CC120x Sniff Mode Application Note*

SWRZ039 *CC112x, CC1175 Silicon Errata*

SWRR106 *CC112x IPC 868- and 915-MHz 2-layer Reference Design*

SWRR107 *CC112x IPC 868- and 915-MHz 4-layer Reference Design*

SWRC220 *CC1120EM 169-MHz Reference Design*

SWRC221 *CC1120EM 420- to 470-MHz Reference Design*

SWRC222 *CC1120EM 868- to 915-MHz Reference Design*

7.2.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

7.3 Trademarks

SmartRF, E2E are trademarks of Texas Instruments.

7.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

8 Mechanical Packaging and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CC1120RHBR	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 85	CC1120
CC1120RHBT	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 85	CC1120

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

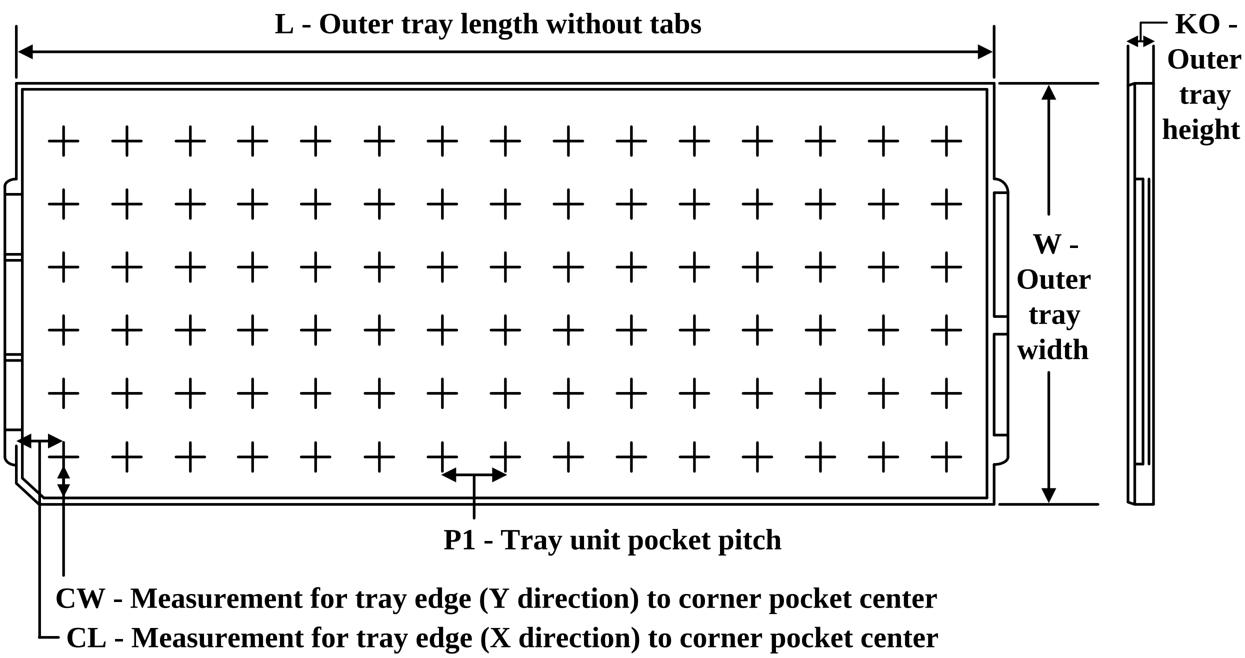
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

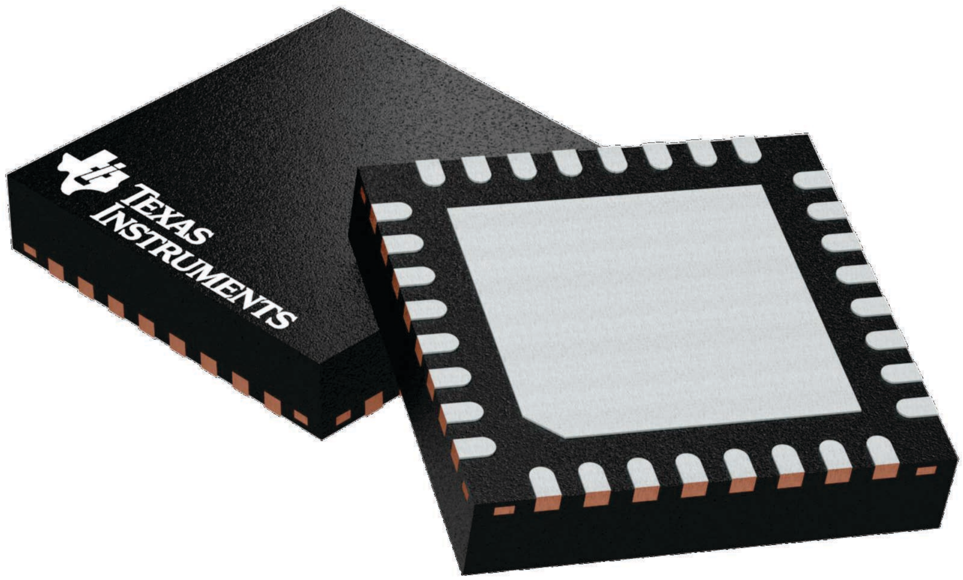
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
CC1120RHBR	RHB	VQFN	32	3000	14 x 35	150	315	135.9	7620	8.8	7.9	8.15
CC1120RHBT	RHB	VQFN	32	250	35 x 14	150	315	135.9	7620	8.8	7.9	8.15
CC1120RHBT	RHB	VQFN	32	250	35 x 14	150	315	135.9	7620	8.8	7.9	8.15

GENERIC PACKAGE VIEW

RHB 32 | **VQFN - 1 mm max height**

5 x 5, 0.5 mm pitch | PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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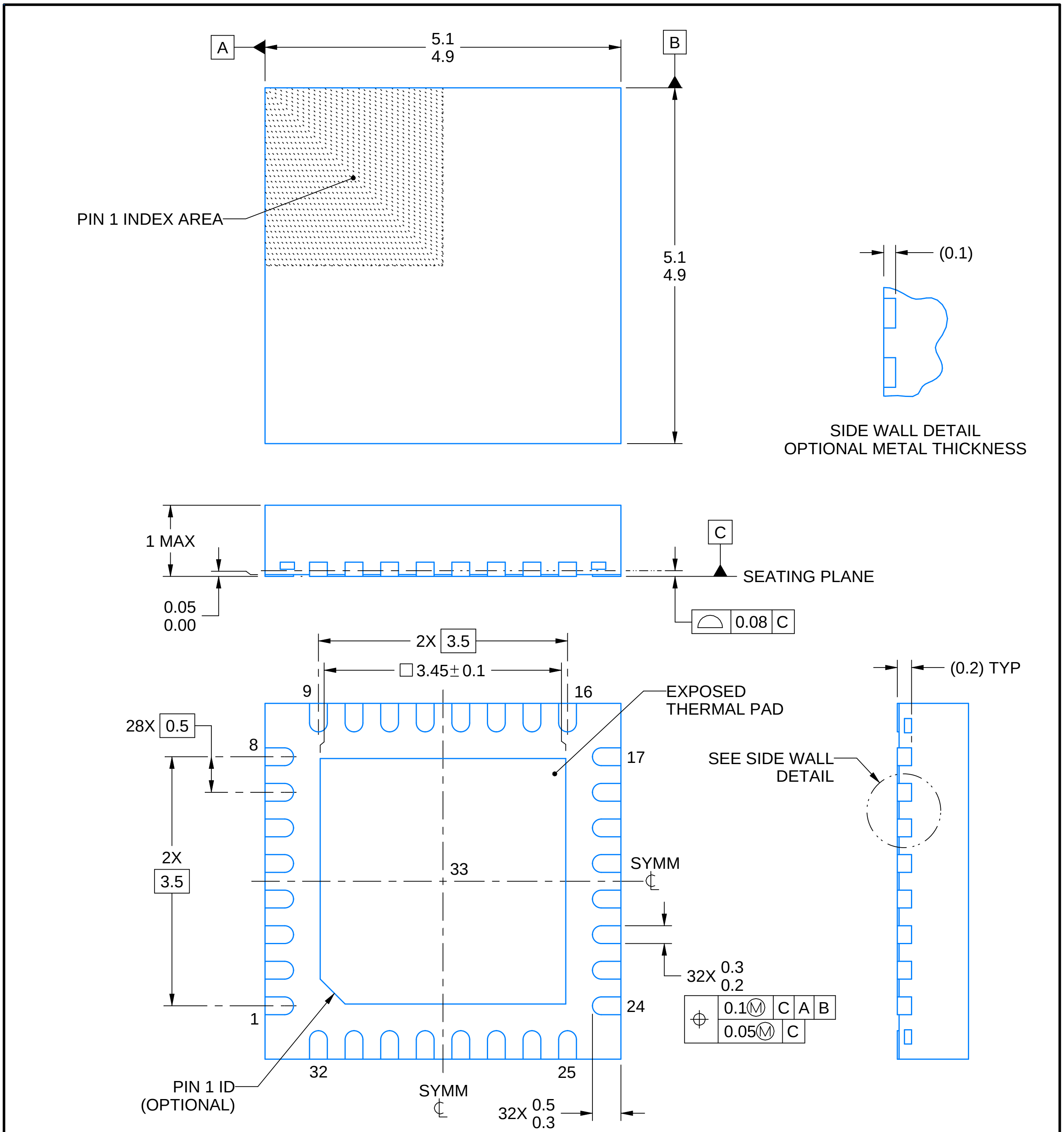
PACKAGE OUTLINE

VQFN - 1 mm max height

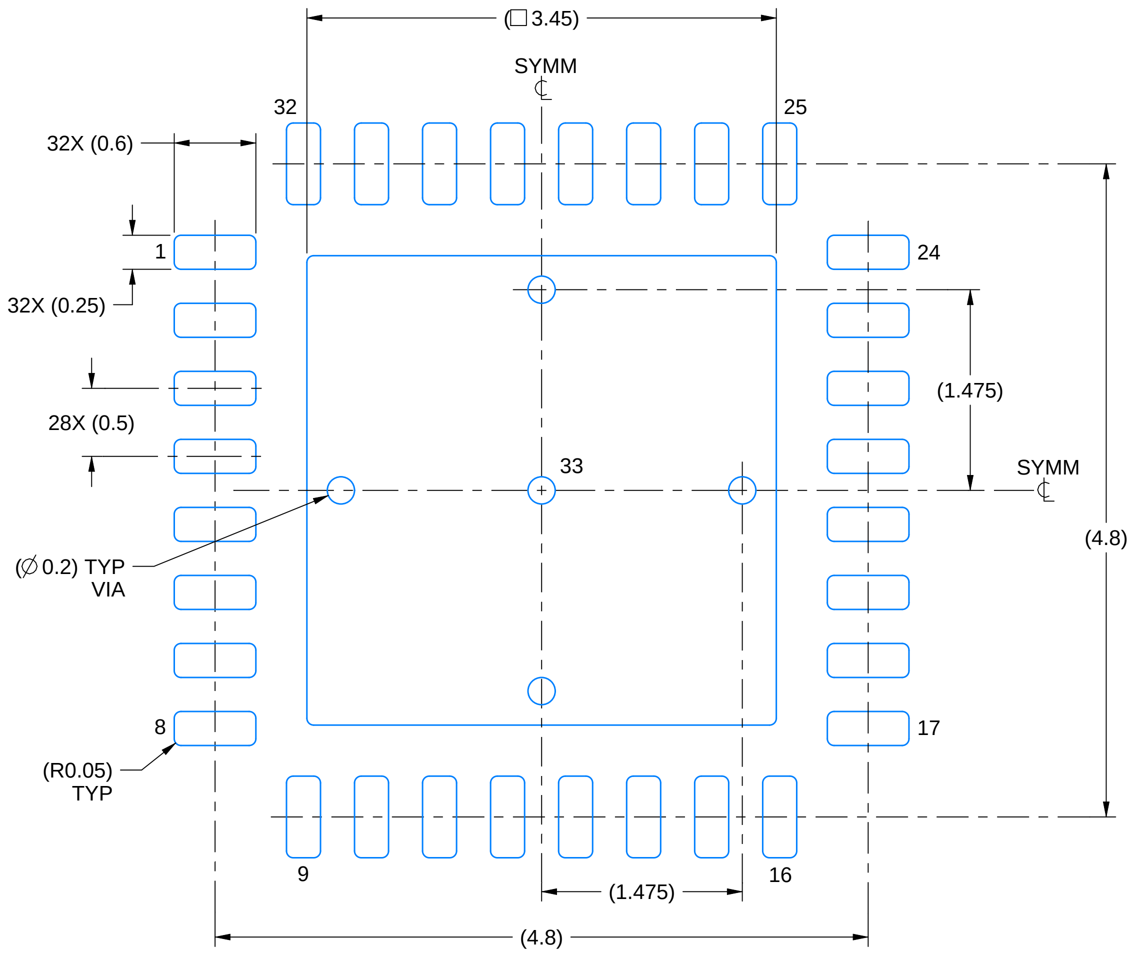
PLASTIC QUAD FLATPACK - NO LEAD



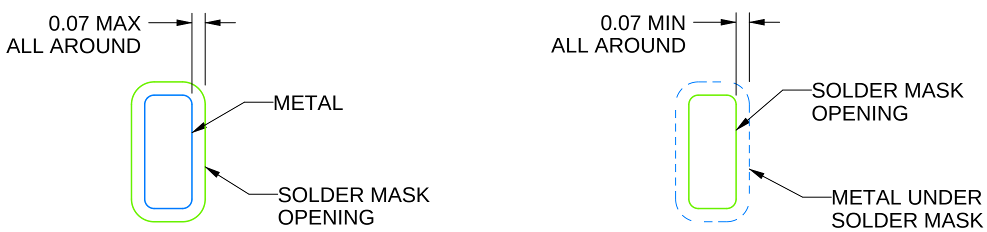
4223442/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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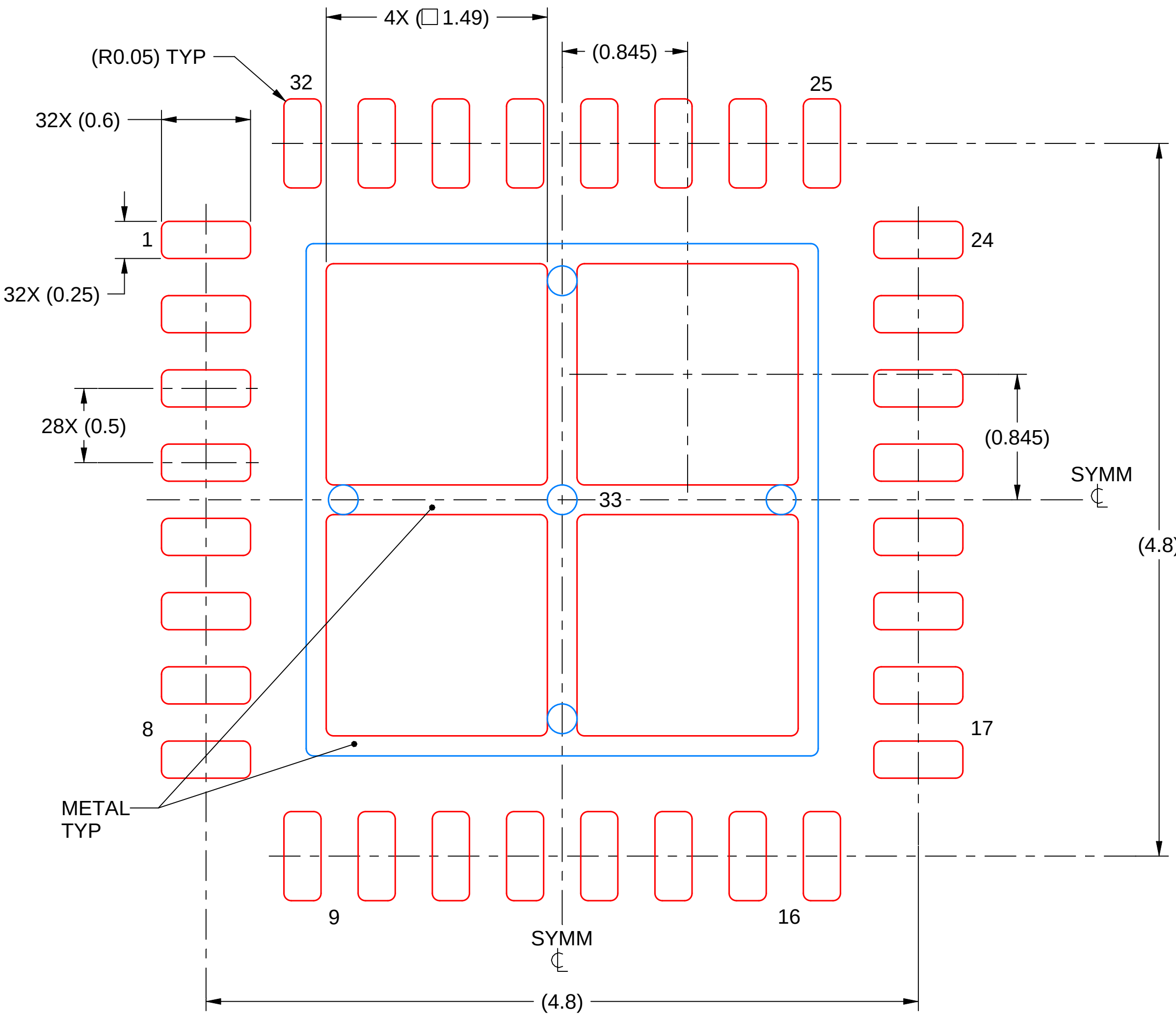
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.