

## SN74AHC1G08 单路双输入正与门

## 1 特性

- 工作电压范围：2V 至 5.5V
- 5V 时  $t_{pd}$  最大值为 7ns
- 低功耗， $I_{CC}$  最大值为 10 $\mu$ A
- 电压为 5V 时，输出驱动为  $\pm 8$ mA
- 所有输入支持施密特触发操作，使得电路允许输入缓慢上升和下降
- 闩锁性能超过 250mA，符合 JESD 17 规范的要求

## 2 应用

- 条形码扫描器
- 电缆解决方案
- 电子书
- 嵌入式个人电脑 (PC)
- 现场变送器：温度或压力传感器
- 指纹识别
- HVAC：暖通空调
- 网络附属存储 (NAS)
- 服务器主板和电源装置 (PSU)
- 软件定义的无线电 (SDR)
- 电视：高清电视 (HDTV)、LCD 电视和数字电视
- 视频通信系统
- 无线数据访问卡、耳机、键盘、鼠标和局域网 (LAN) 卡

## 3 说明

SN74AHC1G08 器件是一个单通道双输入正与门。该器件以正逻辑执行布尔函数  $Y = A \bullet B$  或  $Y = \overline{A + B}$ 。

## 封装信息

| 器件型号        | 封装 <sup>(1)</sup>  | 封装尺寸 <sup>(2)</sup> | 封装尺寸 <sup>(3)</sup> |
|-------------|--------------------|---------------------|---------------------|
| SN74AHC1G08 | DBV ( SOT-23 , 5 ) | 2.9mm x 2.8mm       | 2.9mm x 1.6mm       |
|             | DCK ( SC-70 , 5 )  | 2mm x 2.1mm         | 2mm x 1.25mm        |
|             | DRL (SOT, 5)       | 1.6mm x 1.6mm       | 1.6mm x 1.2mm       |

- (1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
- (2) 封装尺寸 (长 x 宽) 为标称值，并包括引脚 (如适用)。
- (3) 封装尺寸 (长 x 宽) 为标称值，不包括引脚。



逻辑图 (正逻辑)



## Table of Contents

|                                                                               |          |                                                                  |           |
|-------------------------------------------------------------------------------|----------|------------------------------------------------------------------|-----------|
| <b>1 特性</b> .....                                                             | <b>1</b> | 7.3 Feature Description.....                                     | <b>8</b>  |
| <b>2 应用</b> .....                                                             | <b>1</b> | 7.4 Device Functional Modes.....                                 | <b>8</b>  |
| <b>3 说明</b> .....                                                             | <b>1</b> | <b>8 Application and Implementation</b> .....                    | <b>9</b>  |
| <b>4 Pin Configuration and Functions</b> .....                                | <b>3</b> | 8.1 Application Information.....                                 | <b>9</b>  |
| <b>5 Specifications</b> .....                                                 | <b>4</b> | 8.2 Typical Application.....                                     | <b>9</b>  |
| 5.1 Absolute Maximum Ratings.....                                             | <b>4</b> | 8.3 Power Supply Recommendations.....                            | <b>10</b> |
| 5.2 ESD Ratings.....                                                          | <b>4</b> | 8.4 Layout.....                                                  | <b>10</b> |
| 5.3 Recommended Operating Conditions.....                                     | <b>4</b> | <b>9 Device and Documentation Support</b> .....                  | <b>12</b> |
| 5.4 Thermal Information.....                                                  | <b>5</b> | 9.1 Documentation Support (Analog).....                          | <b>12</b> |
| 5.5 Electrical Characteristics.....                                           | <b>5</b> | 9.2 接收文档更新通知.....                                                | <b>12</b> |
| 5.6 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ..... | <b>5</b> | 9.3 支持资源.....                                                    | <b>12</b> |
| 5.7 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ .....   | <b>6</b> | 9.4 Trademarks.....                                              | <b>12</b> |
| 5.8 Operating Characteristics.....                                            | <b>6</b> | 9.5 静电放电警告.....                                                  | <b>12</b> |
| 5.9 Typical Characteristics.....                                              | <b>6</b> | 9.6 术语表.....                                                     | <b>12</b> |
| <b>6 Parameter Measurement Information</b> .....                              | <b>7</b> | <b>10 Revision History</b> .....                                 | <b>12</b> |
| <b>7 Detailed Description</b> .....                                           | <b>8</b> | <b>11 Mechanical, Packaging, and Orderable Information</b> ..... | <b>12</b> |
| 7.1 Overview.....                                                             | <b>8</b> |                                                                  |           |
| 7.2 Functional Block Diagram.....                                             | <b>8</b> |                                                                  |           |

## 4 Pin Configuration and Functions

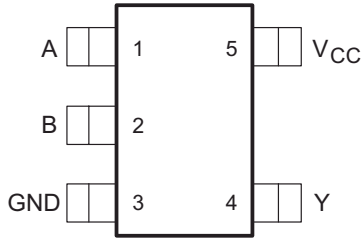


图 4-1. DBV Package 5-Pin SOT-23 Top View

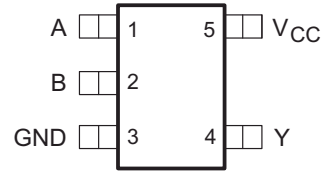
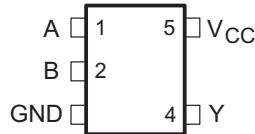


图 4-2. DCK Package 5-Pin SC70 Top View



See mechanical drawings for dimensions (in 节 11).

图 4-3. DRL Package 5-Pin SOT Top View

表 4-1. Pin Functions

| PIN |      | TYPE <sup>(1)</sup> | DESCRIPTION |
|-----|------|---------------------|-------------|
| NO. | NAME |                     |             |
| 1   | A    | I                   | Data Input  |
| 2   | B    | I                   | Data Input  |
| 3   | GND  | —                   | Ground      |
| 4   | Y    | O                   | Data Output |
| 5   | VCC  | —                   | Power       |

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|           |                                            | MIN                         | MAX            | UNIT   |
|-----------|--------------------------------------------|-----------------------------|----------------|--------|
| $V_{CC}$  | Supply voltage                             | −0.5                        | 7              | V      |
| $V_I$     | Input voltage <sup>(2)</sup>               | −0.5                        | 7              | V      |
| $V_O$     | Output voltage <sup>(2)</sup>              | −0.5                        | $V_{CC} + 0.5$ | V      |
| $I_{IK}$  | Input clamp current                        | $V_I < 0$                   |                | −20 mA |
| $I_{OK}$  | Output clamp current                       | $V_O < 0$ or $V_O > V_{CC}$ |                | ±20 mA |
| $I_O$     | Continuous output current                  | $V_O = 0$ to $V_{CC}$       |                | ±25 mA |
|           | Continuous current through $V_{CC}$ or GND |                             |                | ±50 mA |
| $T_J$     | Junction temperature                       |                             |                | 150 °C |
| $T_{stg}$ | Storage temperature                        | −65                         | 150            | °C     |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 5.2 ESD Ratings

|             |                         | VALUE                                                                                    | UNIT  |
|-------------|-------------------------|------------------------------------------------------------------------------------------|-------|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>              | ±2000 |
|             |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup> | ±1000 |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                     |                                    | MIN                                      | MAX      | UNIT |
|---------------------|------------------------------------|------------------------------------------|----------|------|
| $V_{CC}$            | Supply voltage                     | 2                                        | 5.5      | V    |
| $V_{IH}$            | High-level input voltage           | $V_{CC} = 2\text{ V}$                    | 1.5      | V    |
|                     |                                    | $V_{CC} = 3\text{ V}$                    | 2.1      |      |
|                     |                                    | $V_{CC} = 5.5\text{ V}$                  | 3.85     |      |
| $V_{IL}$            | Low-level input voltage            | $V_{CC} = 2\text{ V}$                    | 0.5      | V    |
|                     |                                    | $V_{CC} = 3\text{ V}$                    | 0.9      |      |
|                     |                                    | $V_{CC} = 5.5\text{ V}$                  | 1.65     |      |
| $V_I$               | Input voltage                      | 0                                        | 5.5      | V    |
| $V_O$               | Output voltage                     | 0                                        | $V_{CC}$ | V    |
| $I_{OH}$            | High-level output current          | $V_{CC} = 2\text{ V}$                    | −50      | μA   |
|                     |                                    | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | −4       | mA   |
|                     |                                    | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$   | −8       |      |
| $I_{OL}$            | Low-level output current           | $V_{CC} = 2\text{ V}$                    | 50       | μA   |
|                     |                                    | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 4        | mA   |
|                     |                                    | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$   | 8        |      |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 100      | ns/V |
|                     |                                    | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$   | 20       |      |

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                                               | MIN | MAX | UNIT |
|-----------------------------------------------|-----|-----|------|
| T <sub>A</sub> Operating free-air temperature | –55 | 125 | °C   |

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

## 5.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup>                           | SN74AHC1G08  |            |           | UNIT |
|---------------------------------------------------------|--------------|------------|-----------|------|
|                                                         | DBV (SOT-23) | DCK (SC70) | DRL (SOT) |      |
|                                                         | 5 PINS       | 5 PINS     | 5 PINS    |      |
| R <sub>θJA</sub> Junction-to-ambient thermal resistance | 278          | 289.2      | 142       | °C/W |

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                                 | TEST CONDITIONS                                             | V <sub>CC</sub> | T <sub>A</sub> = 25°C |     |      | T <sub>A</sub> = –55°C to 125°C |      | UNIT |
|-------------------------------------------|-------------------------------------------------------------|-----------------|-----------------------|-----|------|---------------------------------|------|------|
|                                           |                                                             |                 | MIN                   | TYP | MAX  | MIN                             | MAX  |      |
| V <sub>OH</sub> High level output voltage | I <sub>OH</sub> = –50 μA                                    | 2 V             | 1.9                   | 2   |      | 1.9                             |      | V    |
|                                           |                                                             | 3 V             | 2.9                   | 3   |      | 2.9                             |      |      |
|                                           |                                                             | 4.5 V           | 4.4                   | 4.5 |      | 4.4                             |      |      |
|                                           | I <sub>OH</sub> = –4 mA                                     | 3 V             | 2.58                  |     |      | 2.48                            |      |      |
|                                           | I <sub>OH</sub> = –8 mA                                     | 4.5 V           | 3.94                  |     |      | 3.8                             |      |      |
| V <sub>OL</sub> Low level output voltage  | I <sub>OL</sub> = 50 μA                                     | 2 V             |                       |     | 0.1  |                                 | 0.1  | V    |
|                                           |                                                             | 3 V             |                       |     | 0.1  |                                 | 0.1  |      |
|                                           |                                                             | 4.5 V           |                       |     | 0.1  |                                 | 0.1  |      |
|                                           | I <sub>OL</sub> = 4 mA                                      | 3 V             |                       |     | 0.36 |                                 | 0.44 |      |
|                                           | I <sub>OL</sub> = 8 mA                                      | 4.5 V           |                       |     | 0.36 |                                 | 0.44 |      |
| I <sub>I</sub> Input leakage current      | V <sub>I</sub> = 5.5 V or GND                               | 0 V to 5.5 V    |                       |     | ±0.1 |                                 | ±1   | μA   |
| I <sub>CC</sub> Supply current            | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0 | 5.5 V           |                       |     | 1    |                                 | 10   | μA   |
| C <sub>i</sub> Input Capacitance          | V <sub>I</sub> = V <sub>CC</sub> or GND                     | 5 V             |                       | 4   | 10   |                                 | 10   | pF   |

## 5.6 Switching Characteristics, V<sub>CC</sub> = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

| PARAMETER        | FROM<br>(INPUT) | TO<br>(OUTPUT) | OUTPUT<br>CAPACITANCE  | T <sub>A</sub> = 25°C |     |      | T <sub>A</sub> = –40°C to 85°C |     | T <sub>A</sub> = –55°C to 125°C |     | UNIT |    |
|------------------|-----------------|----------------|------------------------|-----------------------|-----|------|--------------------------------|-----|---------------------------------|-----|------|----|
|                  |                 |                |                        | MIN                   | TYP | MAX  | MIN                            | MAX | MIN                             | MAX |      |    |
| t <sub>PLH</sub> | A or B          | Y              | C <sub>L</sub> = 15 pF |                       | 6.2 | 8.8  |                                | 1   | 10.5                            | 1   | 11   | ns |
| t <sub>PHL</sub> |                 |                |                        |                       | 6.2 | 8.8  |                                | 1   | 10.5                            | 1   | 11   |    |
| t <sub>PLH</sub> | A or B          | Y              | C <sub>L</sub> = 50 pF |                       | 8.7 | 12.3 |                                | 1   | 14                              | 1   | 14.5 | ns |
| t <sub>PHL</sub> |                 |                |                        |                       | 8.7 | 12.3 |                                | 1   | 14                              | 1   | 14.5 |    |

## 5.7 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | OUTPUT CAPACITANCE   | $T_A = 25^\circ\text{C}$ |     |     | $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ |     | $T_A = -55^\circ\text{C to } 125^\circ\text{C}$ |     | UNIT |
|-----------|--------------|-------------|----------------------|--------------------------|-----|-----|------------------------------------------------|-----|-------------------------------------------------|-----|------|
|           |              |             |                      | MIN                      | TYP | MAX | MIN                                            | MAX | MIN                                             | MAX |      |
| $t_{PLH}$ | A or B       | Y           | $C_L = 15\text{ pF}$ |                          | 4.3 | 5.9 | 1                                              | 7   | 1                                               | 7.5 | ns   |
| $t_{PHL}$ |              |             |                      |                          | 4.3 | 5.9 | 1                                              | 7   | 1                                               | 7.5 |      |
| $t_{PLH}$ | A or B       | Y           | $C_L = 50\text{ pF}$ |                          | 5.8 | 7.9 | 1                                              | 9   | 1                                               | 9.5 | ns   |
| $t_{PHL}$ |              |             |                      |                          | 5.8 | 7.9 | 1                                              | 9   | 1                                               | 9.5 |      |

## 5.8 Operating Characteristics

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

| PARAMETER |                               | TEST CONDITIONS             | TYP | UNIT |
|-----------|-------------------------------|-----------------------------|-----|------|
| $C_{pd}$  | Power dissipation capacitance | No load, $f = 1\text{ MHz}$ | 18  | pF   |

## 5.9 Typical Characteristics

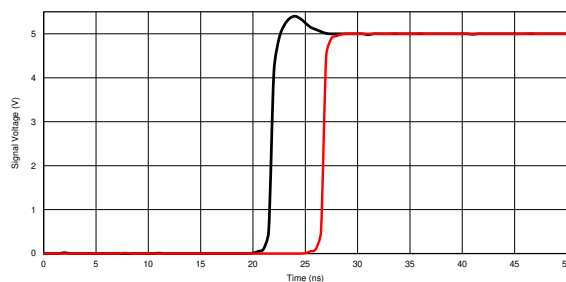
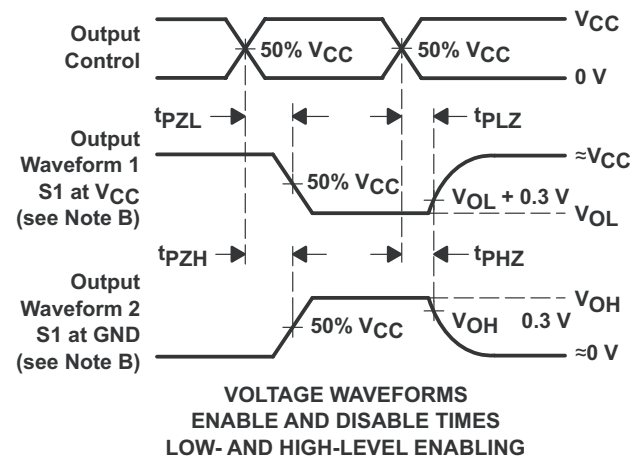
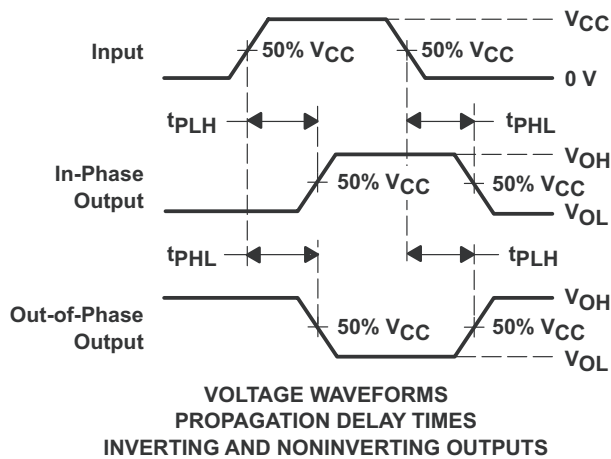
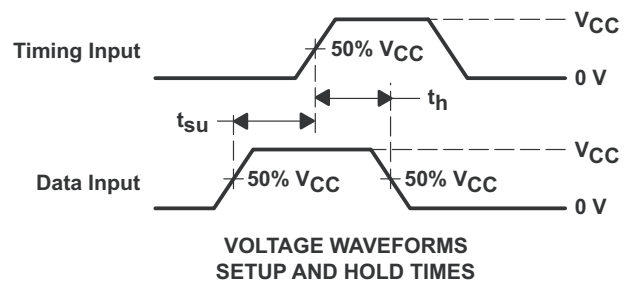
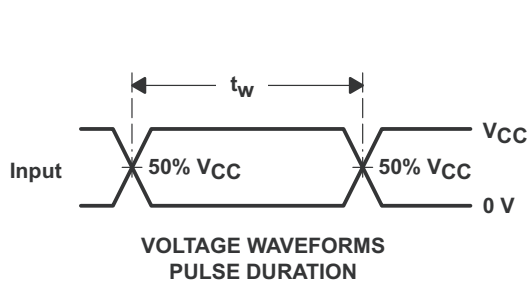
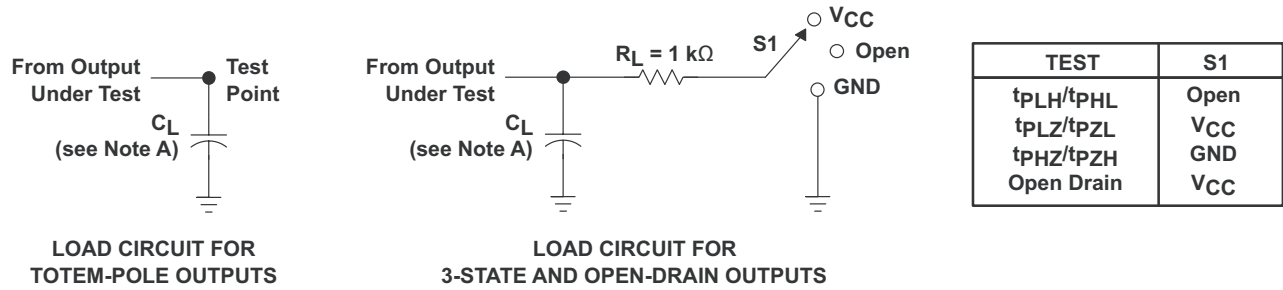


图 5-1. Response Time vs Output Voltage ( $T_A = 25^\circ\text{C}$ ,  $V_A = 5\text{ V}$ )

## 6 Parameter Measurement Information



- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
- The outputs are measured one at a time with one input transition per measurement.
- All parameters and waveforms are not applicable to all devices.

图 6-1. Load Circuit and Voltage Waveforms

## 7 Detailed Description

### 7.1 Overview

The SN74AHC1G08 device is a single 2-input positive-AND gate. The device performs the Boolean function  $Y = A \bullet B$  or  $Y = \overline{A + B}$  in positive logic.

### 7.2 Functional Block Diagram



图 7-1. Logic Diagram (Positive Side)

### 7.3 Feature Description

The SN74AHC1G08 device has a wide operating  $V_{CC}$  range of 2 V to 5.5 V, which allows it to be used in a broad range of systems. The low propagation delay allows fast switching and higher operation speeds. In addition, the low-power consumption makes this device a good choice for portable and battery power-sensitive applications.

### 7.4 Device Functional Modes

表 7-1 lists the functional modes for SN74AHC1G08.

表 7-1. Function Table

| INPUTS <sup>(1)</sup> |   | OUTPUT <sup>(2)</sup> |
|-----------------------|---|-----------------------|
| A                     | B | Y                     |
| H                     | H | H                     |
| L                     | X | L                     |
| X                     | L | L                     |

- (1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care
- (2) H = Driving High, L = Driving Low, Z = High Impedance State

## 8 Application and Implementation

### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 8.1 Application Information

A common application for AND gates is their use in power sequencing. Power sequencing is often employed in applications that require a processor or other delicate device with specific voltage timing requirements in order to protect the device from malfunctioning. Using the SN74AHC1G08 to verify that the processor has turned on can protect it from any harmful signals.

### 8.2 Typical Application

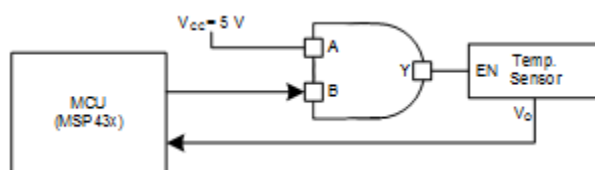


图 8-1. Power Sequencing Application

#### 8.2.1 Design Requirements

The SN74AHC1G08 device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits.

The SN74AHC1G08 allows switching control of analog and digital signals with a digital control signal. All input signals should remain as close to either 0 V or  $V_{CC}$  as possible for optimal operation.

#### 8.2.2 Detailed Design Procedure

- Recommended input conditions:
  - For rise time and fall time specifications, see  $\Delta t/\Delta v$  in the [§ 5.3](#) table.
  - For specified high and low levels, see  $V_{IH}$  and  $V_{IL}$  in the [§ 5.3](#) table.
  - Inputs and outputs are overvoltage tolerant and can therefore go as high as 5.5 V at any valid  $V_{CC}$ .
- Recommended output conditions:
  - Load currents should not exceed  $\pm 50$  mA.
- Frequency selection criterion:
  - The effects of frequency upon the device's power consumption should be studied in *CMOS Power Consumption and CPD Calculation*, [SCAA035](#).
  - Added trace resistance and capacitance can reduce maximum frequency capability; follow the layout practices listed in the [§ 8.4](#) section.

## 8.2.3 Application Curves

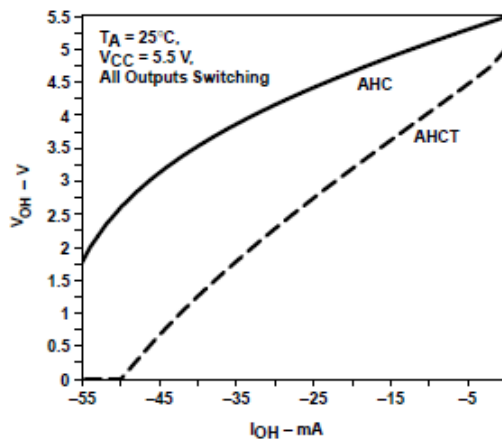


图 8-2. AHC Family  $V_{OH}$  vs  $I_{OH}$  at  $V_{CC} = 5.5$  V

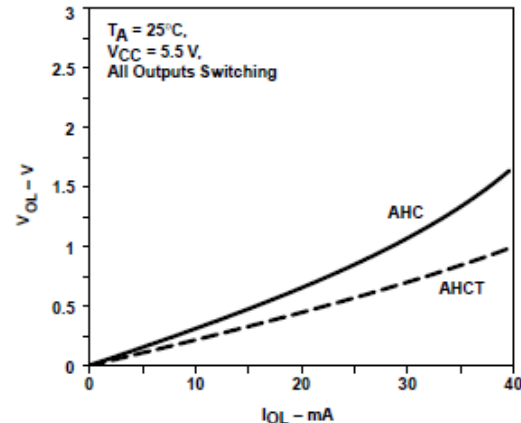


图 8-3. AHC Family  $V_{OL}$  vs  $I_{OL}$  at  $V_{CC} = 5.5$  V

## 8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the [节 5.3](#) table.

Each  $V_{CC}$  terminal should have a bypass capacitor to prevent power disturbance. A 0.1- $\mu$ F bypass capacitor is recommended for devices with a single supply. If multiple pins are labeled  $V_{CC}$ , then a 0.01- $\mu$ F or 0.022- $\mu$ F capacitor is recommended for each  $V_{CC}$  because the  $V_{CC}$  pins are tied together internally. For devices with dual-supply pins operating at different voltages, for example  $V_{CC}$  and  $V_{DD}$ , a 0.1- $\mu$ F bypass capacitor is recommended for each supply pin. Use multiple bypass capacitors in parallel to reject different frequencies of noise. Capacitors with values of 0.1  $\mu$ F and 1  $\mu$ F are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 8.4 Layout

### 8.4.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. [图 8-4](#) shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

#### 8.4.1.1 Layout Example

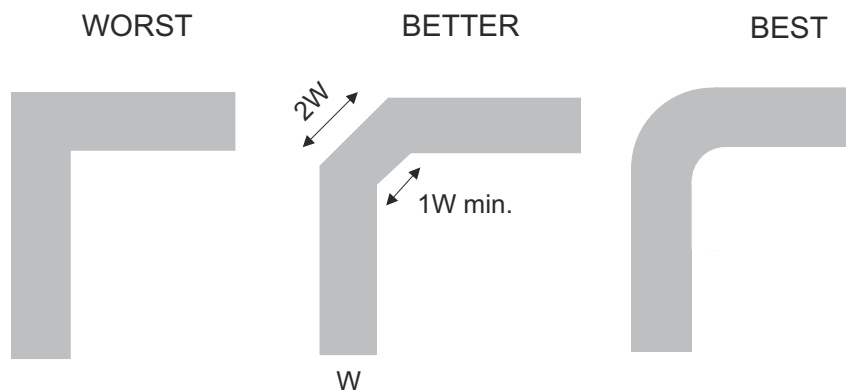


图 8-4. Trace Example

## 9 Device and Documentation Support

### 9.1 Documentation Support (Analog)

#### 9.1.1 Related Documentation

For related documentation see the following:

- *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#)
- *CMOS Power Consumption and CPD Calculation*, [SCAA035](#)
- *Selecting the Right Texas Instruments Signal Switch*, [SZZA030](#)

### 9.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 9.3 支持资源

**TI E2E™ 中文支持论坛** 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

### 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

### 9.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 9.6 术语表

#### TI 术语表

本术语表列出并解释了术语、首字母缩略词和定义。

## 10 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision Q (October 2023) to Revision R (January 2024) | Page |
|---------------------------------------------------------------------|------|
| • Updated RθJA values: DBV = 206 to 278, all values in °C/W .....   | 5    |

| Changes from Revision P (March 2016) to Revision Q (October 2023)   | Page |
|---------------------------------------------------------------------|------|
| • Updated RθJA values: DCK = 252 to 289.2, all values in °C/W ..... | 5    |

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

## PACKAGING INFORMATION

| Orderable part number             | Status<br>(1) | Material type<br>(2) | Package   Pins    | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)                        |
|-----------------------------------|---------------|----------------------|-------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|--------------------------------------------|
| <a href="#">SN74AHC1G08DBV3</a>   | Active        | Production           | SOT-23 (DBV)   5  | 3000   LARGE T&R      | Yes         | SNBI                                 | Level-1-260C-UNLIM                | -55 to 125   | A08Y                                       |
| <a href="#">SN74AHC1G08DBVR</a>   | Active        | Production           | SOT-23 (DBV)   5  | 3000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -55 to 125   | (38EH, 3BVF, A083, A08G, A08J, A08L, A08S) |
| <a href="#">SN74AHC1G08DBVRE4</a> | Active        | Production           | SOT-23 (DBV)   5  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | A08G                                       |
| <a href="#">SN74AHC1G08DBVRG4</a> | Active        | Production           | SOT-23 (DBV)   5  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | A08G                                       |
| <a href="#">SN74AHC1G08DBVT</a>   | Obsolete      | Production           | SOT-23 (DBV)   5  | -                     | -           | Call TI                              | Call TI                           | -55 to 125   | (A083, A08G, A08J, A08S)                   |
| <a href="#">SN74AHC1G08DBVTG4</a> | Active        | Production           | SOT-23 (DBV)   5  | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | A08G                                       |
| <a href="#">SN74AHC1G08DCK3</a>   | Active        | Production           | SC70 (DCK)   5    | 3000   LARGE T&R      | Yes         | SNBI                                 | Level-1-260C-UNLIM                | -55 to 125   | AEY                                        |
| <a href="#">SN74AHC1G08DCKR</a>   | Active        | Production           | SC70 (DCK)   5    | 3000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -55 to 125   | (1B9, AE3, AEG, AEJ, AEL, AES)             |
| <a href="#">SN74AHC1G08DCKRE4</a> | Active        | Production           | SC70 (DCK)   5    | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | AE3                                        |
| <a href="#">SN74AHC1G08DCKRG4</a> | Active        | Production           | SC70 (DCK)   5    | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | AE3                                        |
| <a href="#">SN74AHC1G08DCKT</a>   | Obsolete      | Production           | SC70 (DCK)   5    | -                     | -           | Call TI                              | Call TI                           | -55 to 125   | (AE3, AEG, AEJ, AES)                       |
| <a href="#">SN74AHC1G08DCKTE4</a> | Active        | Production           | SC70 (DCK)   5    | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | AE3                                        |
| <a href="#">SN74AHC1G08DCKTG4</a> | Active        | Production           | SC70 (DCK)   5    | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | AE3                                        |
| <a href="#">SN74AHC1G08DRLR</a>   | Active        | Production           | SOT-5X3 (DRL)   5 | 4000   LARGE T&R      | Yes         | NIPDAU   NIPDAUAG                    | Level-1-260C-UNLIM                | -55 to 125   | (AEB, AES)                                 |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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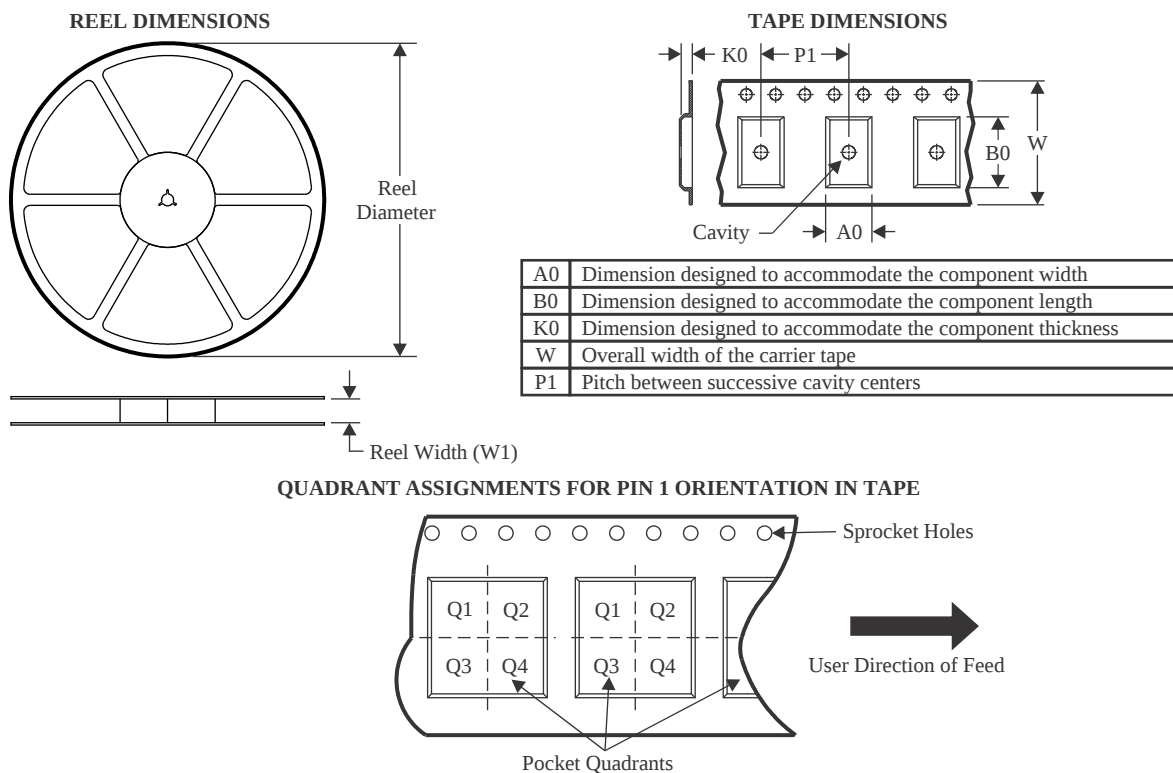
**OTHER QUALIFIED VERSIONS OF SN74AHC1G08 :**

- Automotive : [SN74AHC1G08-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

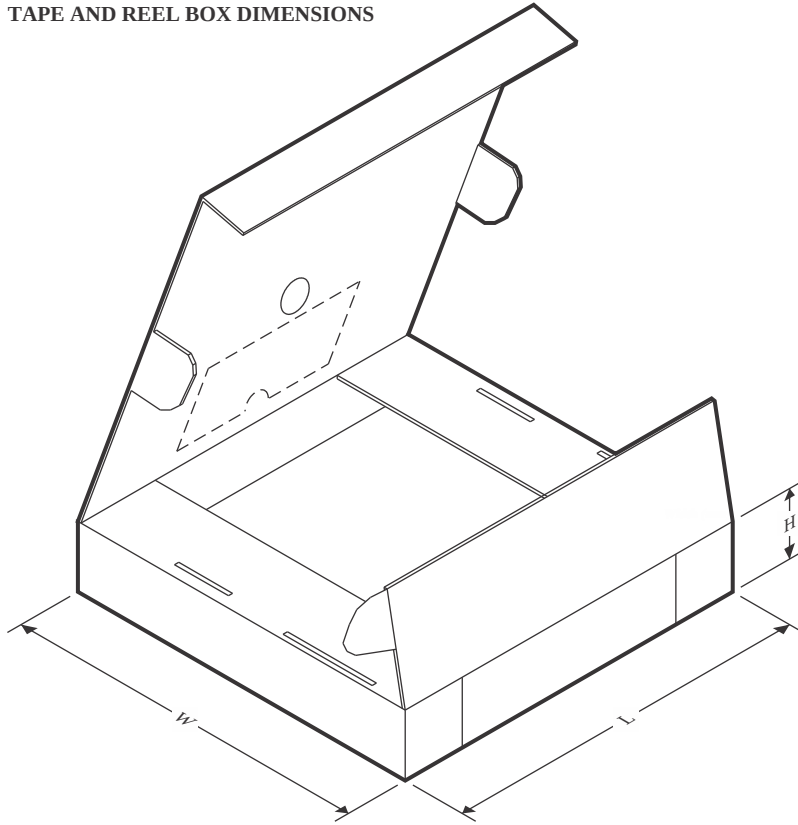
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AHC1G08DBVR   | SOT-23       | DBV             | 5    | 3000 | 180.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| SN74AHC1G08DBVRG4 | SOT-23       | DBV             | 5    | 3000 | 178.0              | 9.0                | 3.23    | 3.17    | 1.37    | 4.0     | 8.0    | Q3            |
| SN74AHC1G08DBVTG4 | SOT-23       | DBV             | 5    | 250  | 178.0              | 9.0                | 3.23    | 3.17    | 1.37    | 4.0     | 8.0    | Q3            |
| SN74AHC1G08DCKR   | SC70         | DCK             | 5    | 3000 | 180.0              | 8.4                | 2.3     | 2.5     | 1.2     | 4.0     | 8.0    | Q3            |
| SN74AHC1G08DCKRG4 | SC70         | DCK             | 5    | 3000 | 178.0              | 9.2                | 2.4     | 2.4     | 1.22    | 4.0     | 8.0    | Q3            |
| SN74AHC1G08DCKTG4 | SC70         | DCK             | 5    | 250  | 178.0              | 9.2                | 2.4     | 2.4     | 1.22    | 4.0     | 8.0    | Q3            |
| SN74AHC1G08DRLR   | SOT-5X3      | DRL             | 5    | 4000 | 180.0              | 8.4                | 1.98    | 1.78    | 0.69    | 4.0     | 8.0    | Q3            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AHC1G08DBVR   | SOT-23       | DBV             | 5    | 3000 | 210.0       | 185.0      | 35.0        |
| SN74AHC1G08DBVRG4 | SOT-23       | DBV             | 5    | 3000 | 180.0       | 180.0      | 18.0        |
| SN74AHC1G08DBVTG4 | SOT-23       | DBV             | 5    | 250  | 180.0       | 180.0      | 18.0        |
| SN74AHC1G08DCKR   | SC70         | DCK             | 5    | 3000 | 210.0       | 185.0      | 35.0        |
| SN74AHC1G08DCKRG4 | SC70         | DCK             | 5    | 3000 | 180.0       | 180.0      | 18.0        |
| SN74AHC1G08DCKTG4 | SC70         | DCK             | 5    | 250  | 180.0       | 180.0      | 18.0        |
| SN74AHC1G08DRLR   | SOT-5X3      | DRL             | 5    | 4000 | 202.0       | 201.0      | 28.0        |

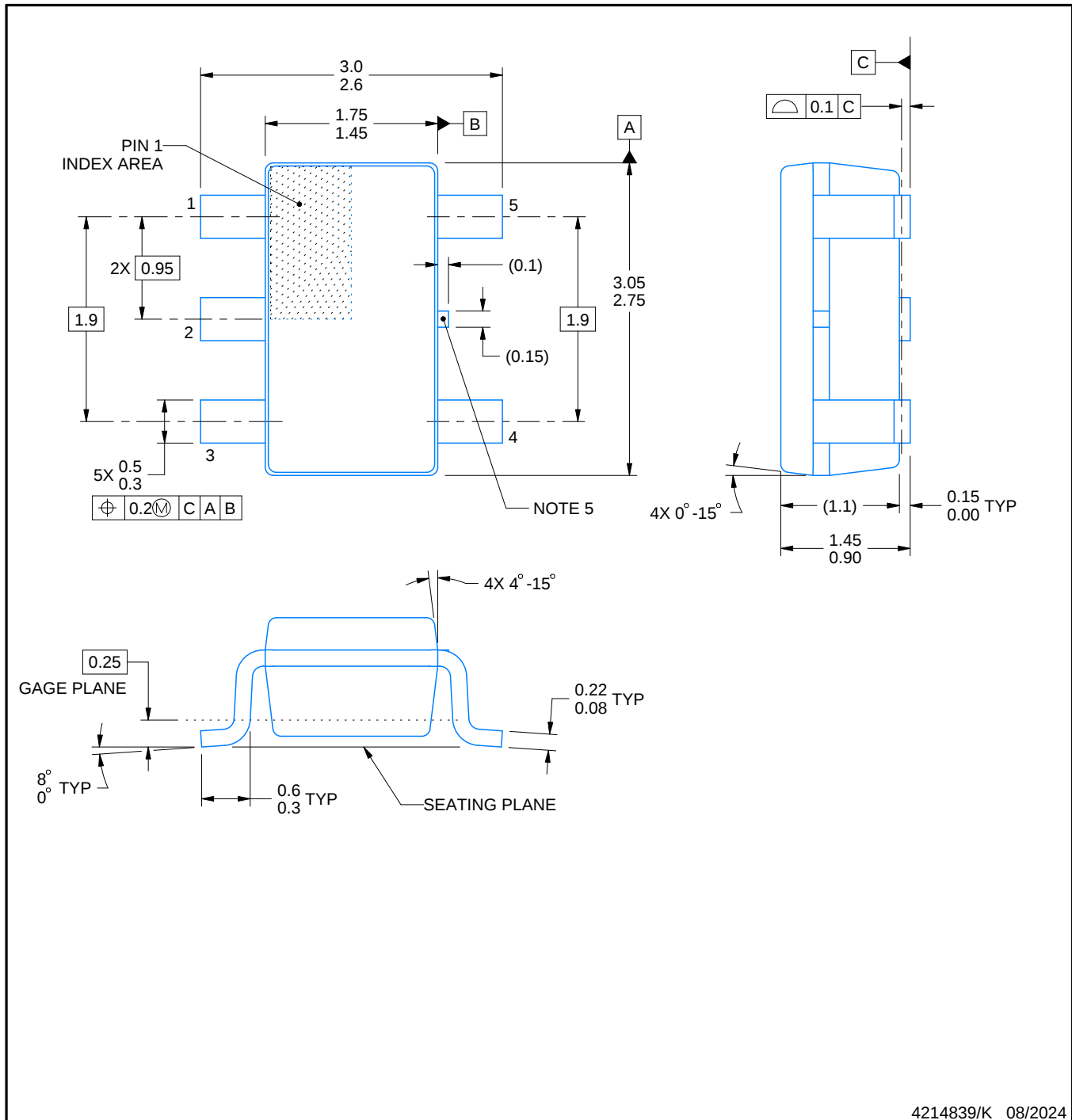
DBV0005A



## PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/K 08/2024

### NOTES:

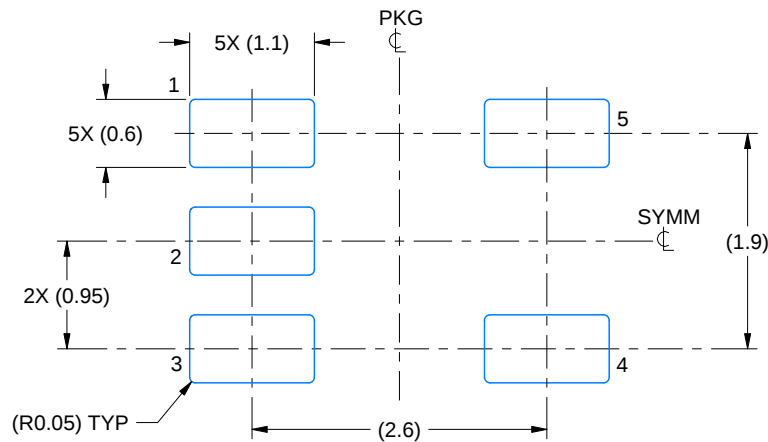
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

# EXAMPLE BOARD LAYOUT

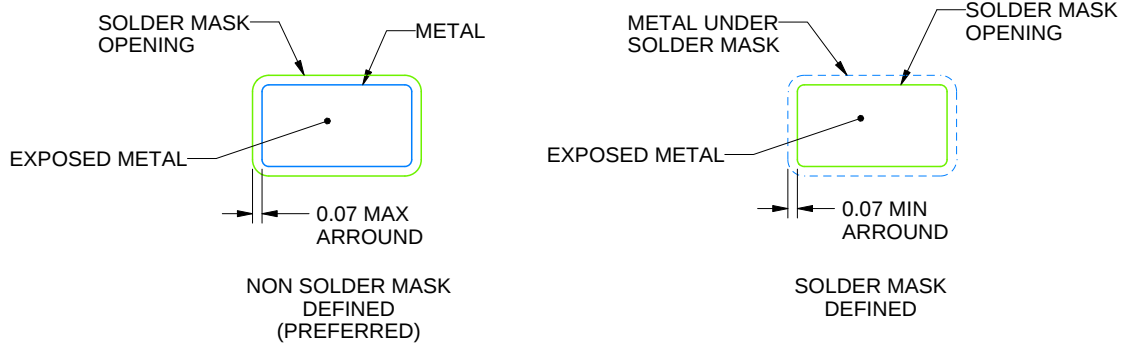
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

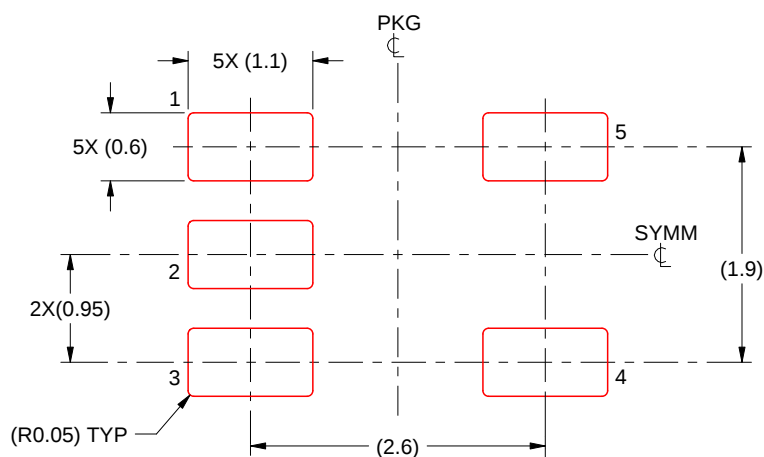
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



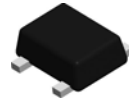
SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

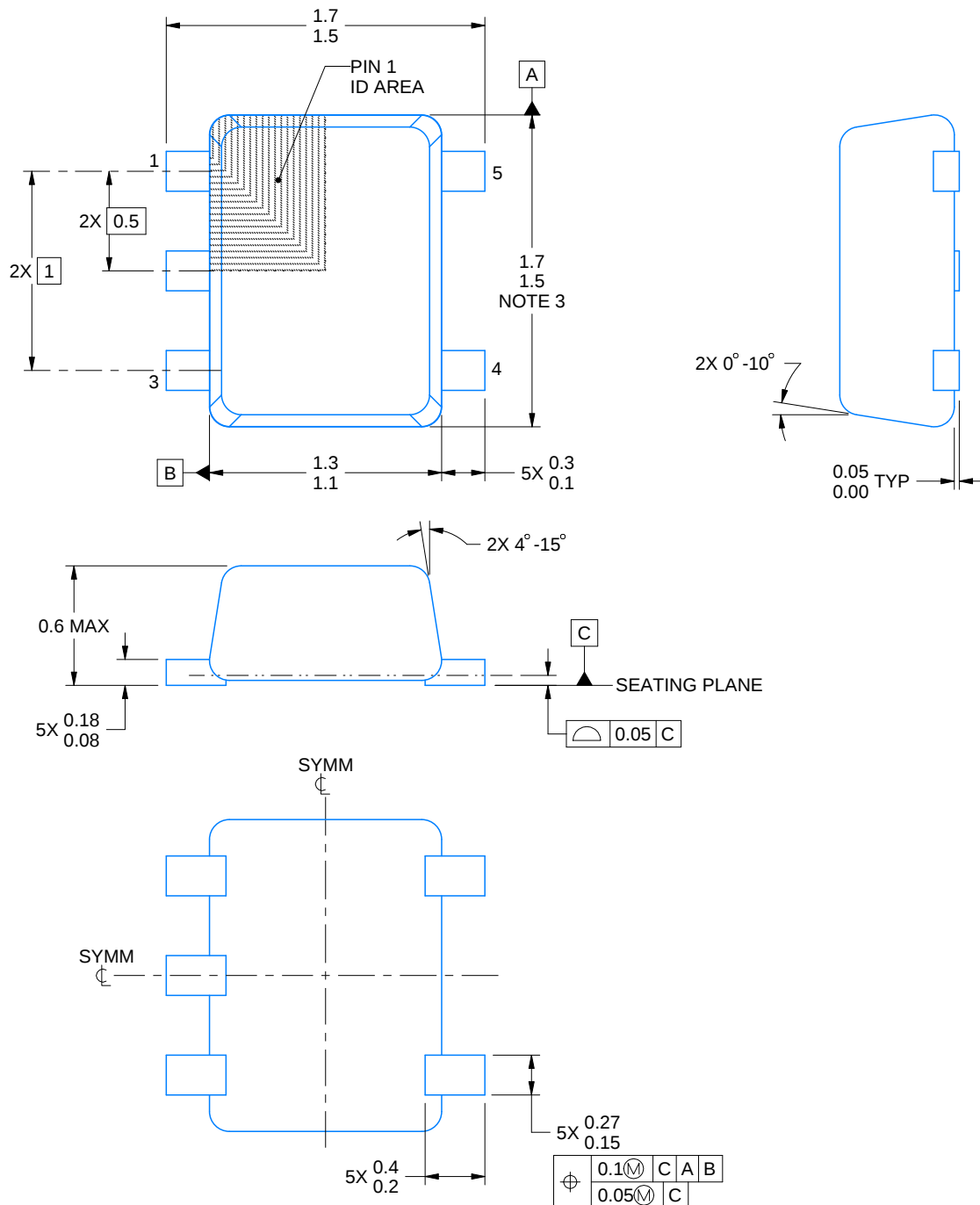
DRL0005A



## PACKAGE OUTLINE

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



4220753/E 11/2024

### NOTES:

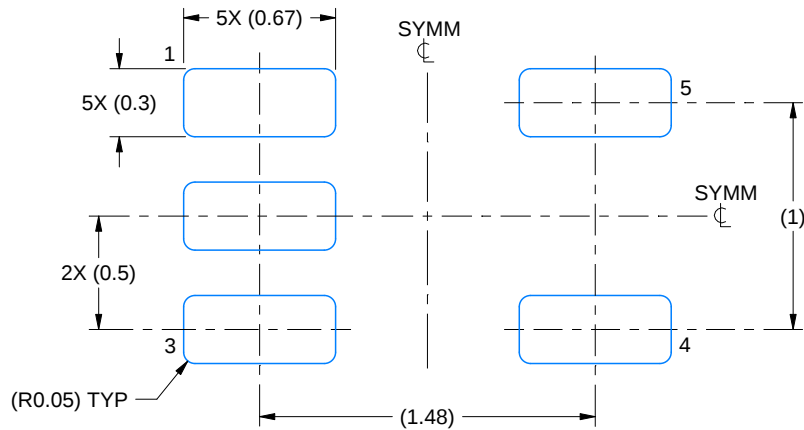
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1

# EXAMPLE BOARD LAYOUT

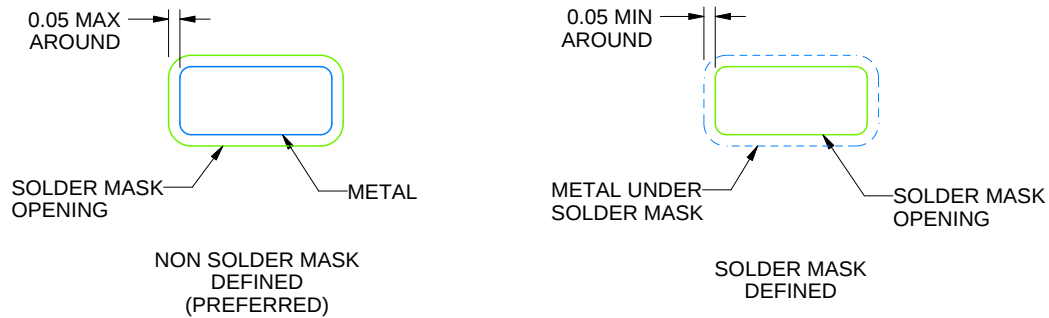
DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
SCALE:30X



SOLDERMASK DETAILS

4220753/E 11/2024

NOTES: (continued)

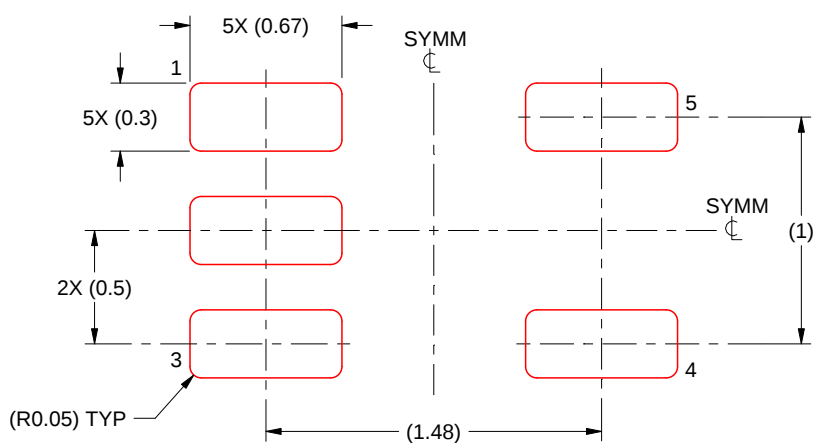
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



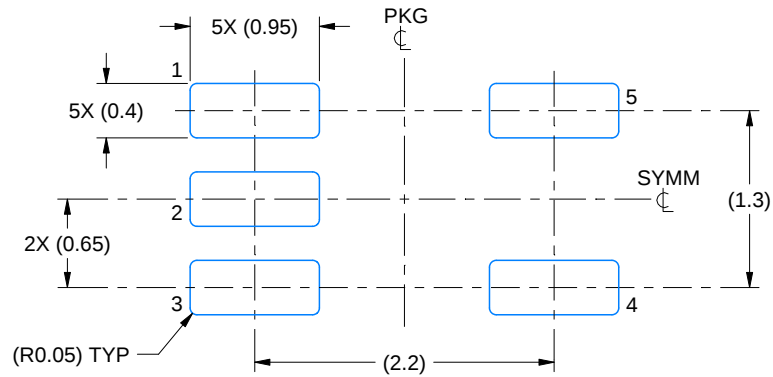
SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:30X

4220753/E 11/2024

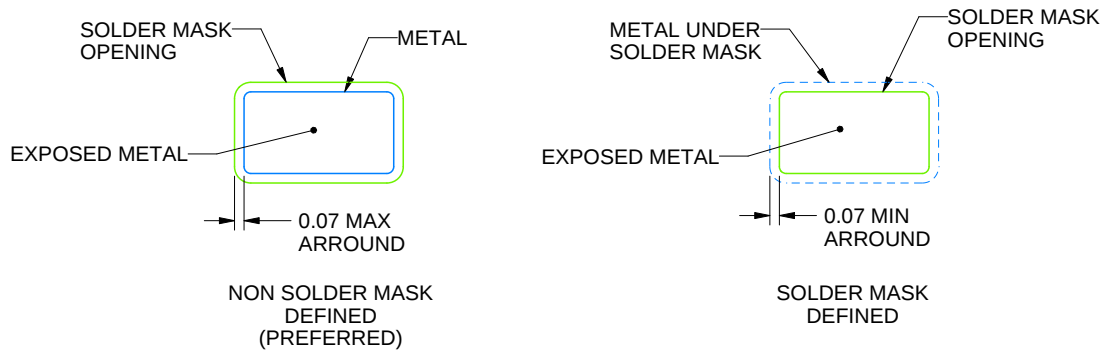
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.





LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X

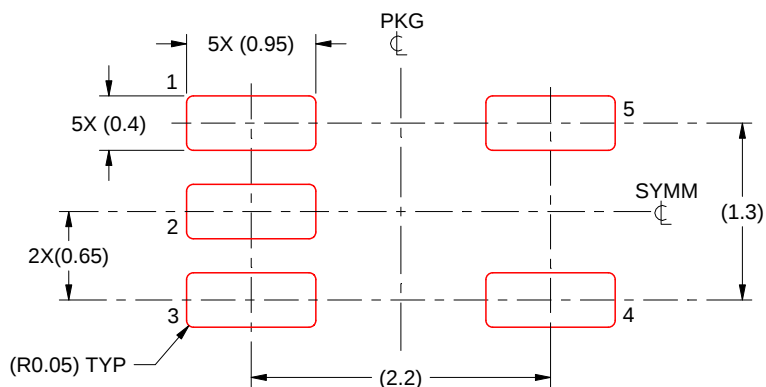


## SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.  
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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