

LM321LV、LM358LV、LM324LV 行业标准低电压运算放大器

1 特性

- 适用于成本敏感型系统的行业标准放大器
- 低输入失调电压： $\pm 1\text{mV}$
- 共模电压范围包括接地
- 单位增益带宽： 1MHz
- 低宽带噪声： $40\text{nV}/\sqrt{\text{Hz}}$
- 低静态电流： $90\mu\text{A}/\text{通道}$
- 单位增益稳定
- 可在 2.7V 至 5.5V 的电源电压范围内工作
- 提供单通道、双通道和四通道型号
- 严格的 ESD 规格： 2kV HBM
- 工作温度范围： -40°C 至 125°C

2 应用

- 无线电器
- 不间断电源
- 电池组、充电器和测试设备
- 电源模块
- 环境传感器信号调节
- 现场变送器：温度传感器
- 示波器、数字万用表、测试设备
- 机架式服务器
- HVAC：暖通空调
- 直流电机控制
- 低侧电流感测

3 说明

LM3xxLV 系列包括单路 LM321LV、双路 LM358LV 和四路 LM324LV 运算放大器。这些器件由 2.7V 至 5.5V 的低电压供电。

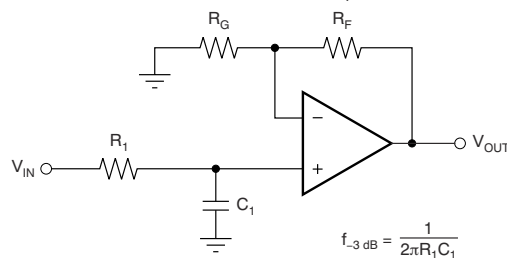
在成本敏感型低压应用中，这些运算放大器可作为 LM321、LM358 和 LM324 的替代产品。部分应用为大型电器、烟雾探测器和个人电子产品。LM3xxLV 器件在低电压下可提供比 LM3xx 器件更佳的性能，并且功耗更低。这些运算放大器具有单位增益稳定性，并且在过驱情况下不会出现相位反转。ESD 设计为 LM3xxLV 系列提供了至少 2kV 的 HBM 规格。

LM3xxLV 系列采用行业标准封装。这些封装包括 SOT-23、SOIC、VSSOP 和 TSSOP 封装。

器件信息

器件型号 ⁽¹⁾	封装	封装尺寸 (标称值)
LM321LV	SOT-23 (5)	$1.60\text{mm} \times 2.90\text{mm}$
	SC70 (5)	$1.25\text{mm} \times 2.00\text{mm}$
LM358LV	SOIC (8)	$3.91\text{mm} \times 4.90\text{mm}$
	SOT-23 (8)	$1.60\text{mm} \times 2.90\text{mm}$
	TSSOP (8)	$3.00\text{mm} \times 4.40\text{mm}$
	VSSOP (8)	$3.00\text{mm} \times 3.00\text{mm}$
LM324LV	SOIC (14)	$8.65\text{mm} \times 3.91\text{mm}$
	TSSOP (14)	$4.40\text{mm} \times 5.00\text{mm}$
	SOT-23 (14)	$4.20\text{mm} \times 2.00\text{mm}$

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right) \left(\frac{1}{1 + sR_1C_1}\right)$$

单极低通滤波器



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4 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (September 2019) to Revision E (February 2022)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• 向器件信息表中添加了 SOT-23 (DYY) 封装.....	1
• 向引脚配置和功能部分中添加了 DYY (SOT-23) 信息.....	3
• 向热性能信息：LM324LV 表中添加了 DYY (SOT-23).....	7
Changes from Revision C (May 2019) to Revision D (September 2019)	Page
• 删除了数据表中 SOT-23 (DDF) 封装的全部预发布说明.....	1
Changes from Revision B (February 2019) to Revision C (May 2019)	Page
• 向器件信息表中添加了 SOT-23 (DDF) 封装.....	1
• 向引脚配置和功能部分中添加了 DDF (SOT-23) 信息.....	3
• 向热性能信息：LM358LV 表中添加了 DDF (SOT-23).....	7
Changes from Revision A (January 2019) to Revision B (February 2019)	Page
• 更改了 LM321LVIDBV (SOT-23) 引脚图以匹配 LM321LVIDCK (SC70) 引脚排列.....	3
Changes from Revision * (September 2018) to Revision A (January 2019)	Page
• 将数据表标题从 LM3xxLV... 更改为 LM321LV、LM358LV、LM324LV... ..	1

5 引脚配置和功能

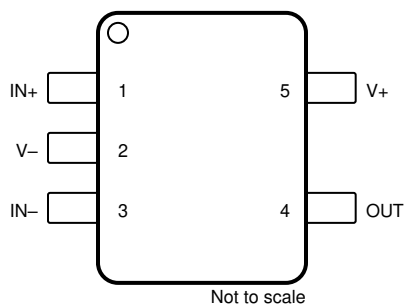
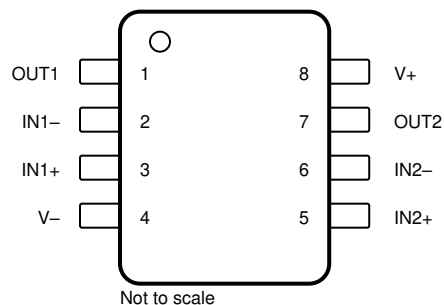


图 5-1. LM321LV DBV 和 DCK 封装
 5 引脚 SOT-23 和 SC70
 (顶视图)

表 5-1. 引脚功能 : LM321LV

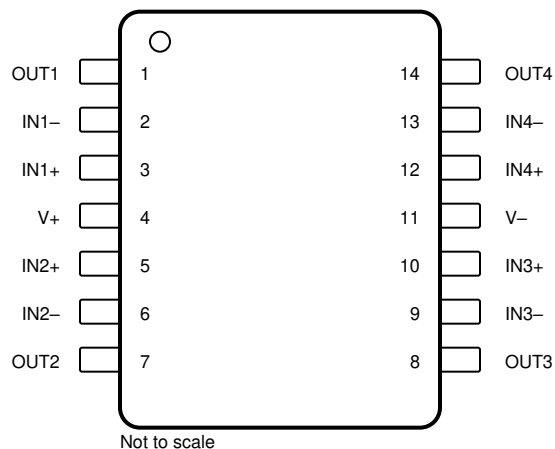
引脚		I/O	说明
名称	编号		
IN -	3	I	反相输入
IN+	1	I	同相输入
OUT	4	O	输出
V -	2	I 或 —	负 (低) 电源或接地 (对于单电源供电)
V+	5	I	正 (高) 电源



**图 5-2. LM358LV D、DGK、PW 和 DDF 封装
8 引脚 SOIC、VSSOP、TSSOP 和 SOT-23
(顶视图)**

表 5-2. 引脚功能 : LM358LV

引脚		I/O	说明
名称	编号		
IN1 -	2	I	反相输入，通道 1
IN1+	3	I	同相输入，通道 1
IN2 -	6	I	反相输入，通道 2
IN2+	5	I	同相输入，通道 2
OUT1	1	O	输出，通道 1
OUT2	7	O	输出，通道 2
V -	4	I 或 —	负 (低) 电源或接地 (对于单电源供电)
V+	8	I	正 (高) 电源



**图 5-3. LM324LV D、PW 和 DYY 封装
14 引脚 SOIC、TSSOP 和 SOT-23
(顶视图)**

表 5-3. 引脚功能 : LM324LV

引脚		I/O	说明
名称	编号		
IN1 -	2	I	反相输入, 通道 1
IN1+	3	I	同相输入, 通道 1
IN2 -	6	I	反相输入, 通道 2
IN2+	5	I	同相输入, 通道 2
IN3 -	9	I	反相输入, 通道 3
IN3+	10	I	同相输入, 通道 3
IN4 -	13	I	反相输入, 通道 4
IN4+	12	I	同相输入, 通道 4
OUT1	1	O	输出, 通道 1
OUT2	7	O	输出, 通道 2
OUT3	8	O	输出, 通道 3
OUT4	14	O	输出, 通道 4
V -	11	I 或 —	负 (低) 电源或接地 (对于单电源供电)
V+	4	I	正 (高) 电源

6 规格

6.1 绝对最大额定值

在工作结温范围内测得（除非另有说明）⁽¹⁾

			最小值	最大值	单位
电源电压, ([V+] - [V-])			0	6	V
信号输入引脚	电压 ⁽²⁾	共模	(V-) - 0.5	(V+) + 0.5	V
		差分	(V+) - (V-) + 0.2		V
	电流 ⁽²⁾		-10	10	mA
输出短路 ⁽³⁾			持续		
温度, T _A			-55	150	°C
运行结温, T _J				150	°C
贮存温度, T _{stg}			-65	150	°C

- (1) 超出绝对最大额定值下列出的值的应力可能会对器件造成永久损坏。这些仅仅是压力额定值，并不表示器件在这些条件下以及在建议运行条件以外的任何其他条件下能够正常运行。长时间处于绝对最大额定条件下可能会影响器件的可靠性。
- (2) 输入引脚被二极管钳制至电源轨。摆幅超过电源轨 0.5V 的输入信号的电流必须限制在 10mA 或者更少。
- (3) 对地短路，每个封装对应一个放大器。

6.2 ESD 额定值

		值	单位
$V_{(ESD)}$ 静电放电	人体放电模型 (HBM), 符合 ANSI/ESDA/JEDEC JS-001 标准 ⁽¹⁾	±2000	V
	充电器件模型 (CDM), 符合 JEDEC 规范 JESD22-C101 ⁽²⁾	±1000	

- (1) JEDEC 文档 JEP155 指出：500V HBM 时能够在标准 ESD 控制流程下安全生产。
- (2) JEDEC 文件 JEP157 指出：250V CDM 可实现在标准 ESD 控制流程下安全生产。

6.3 建议运行条件

在工作结温范围内测得（除非另有说明）

		最小值	最大值	单位
V_S	电源电压 $[(V+) - (V-)]$	2.7	5.5	V
V_{IN}	输入引脚电压范围	$(V-) - 0.1$	$(V+) - 1$	V
T_A	额定温度	-40	125	°C

6.4 热性能信息：LM321LV

热指标 ⁽¹⁾	LM321LV		单位
	DBV (SOT-23)	DCK (SC70)	
	5 引脚	5 引脚	
$R_{\theta JA}$ 结至环境热阻	232.9	239.6	°C/W
$R_{\theta JC(top)}$ 结至外壳 (顶部) 热阻	153.8	148.5	°C/W
$R_{\theta JB}$ 结至电路板热阻	100.9	82.3	°C/W
ψ_{JT} 结至顶部特征参数	77.2	54.5	°C/W
ψ_{JB} 结至电路板特征参数	100.4	81.8	°C/W

(1) 有关新旧热指标的更多信息，请参阅 [半导体和 IC 封装热指标](#)。

6.5 热性能信息：LM358LV

热指标 ⁽¹⁾	LM358LV				单位
	D (SOIC)	DGK (VSSOP)	PW (TSSOP)	DDF (SOT-23)	
	8 引脚	8 引脚	8 引脚	8 引脚	
$R_{\theta JA}$ 结至环境热阻	207.9	201.2	200.7	183.7	°C/W
$R_{\theta JC(top)}$ 结至外壳 (顶部) 热阻	92.8	85.7	95.4	112.5	°C/W
$R_{\theta JB}$ 结至电路板热阻	129.7	122.9	128.6	98.2	°C/W
ψ_{JT} 结至顶部特征参数	26	21.2	27.2	18.8	°C/W
ψ_{JB} 结至电路板特征参数	127.9	121.4	127.2	97.6	°C/W

(1) 有关新旧热指标的更多信息，请参阅 [半导体和 IC 封装热指标](#)。

6.6 热性能信息：LM324LV

热指标 ⁽¹⁾	LM324LV			单位
	D (SOIC)	PW (TSSOP)	DYY (SOT-23)	
	14 引脚	14 引脚	14 引脚	
$R_{\theta JA}$ 结至环境热阻	102.1	148.3	154.6	°C/W
$R_{\theta JC(top)}$ 结至外壳 (顶部) 热阻	56.8	68.1	86.3	°C/W
$R_{\theta JB}$ 结至电路板热阻	58.5	92.7	67.3	°C/W
ψ_{JT} 结至顶部特征参数	20.5	16.9	9.8	°C/W
ψ_{JB} 结至电路板特征参数	58.1	91.8	67.1	°C/W

(1) 有关新旧热指标的更多信息，请参阅 [半导体和 IC 封装热指标](#)。

6.7 电气特性

在 $V_S = (V+) - (V-) = 2.7V$ 至 $5.5V$ ($\pm 1.35V$ 至 $\pm 2.75V$)、 $T_A = 25^\circ C$ 、 $R_L = 10k\Omega$ (连接至 $V_S/2$) 并且 $V_{CM} = V_{OUT} = V_S/2$ 条件下测得 (除非另有说明)

参数	测试条件	最小值	典型值	最大值	单位
失调电压					
V _{OS} 输入失调电压	V _S = 5V	±1		±3	mV
	V _S = 5V , T _A = - 40°C 至 125°C			±5	
dV _{OS} /dT V _{OS} 温漂	T _A = - 40°C 至 125°C	±4			μV/°C
PSRR 电源抑制比	V _S = 2.7 V 至 5.5V , V _{CM} = (V -)	80	100		dB
输入电压范围					
V _{CM} 共模电压范围	无相位反转	(V -) - 0.1		(V+) - 1	V
CMRR 共模抑制比	V _S = 2.7V , (V -) - 0.1V < V _{CM} < (V+) - 1V , T _A = - 40°C 至 125°C	84			dB
	V _S = 5.5V , (V -) - 0.1V < V _{CM} < (V+) - 1V , T _A = - 40°C 至 125°C	63	92		
输入偏置电流					
I _B 输入偏置电流	V _S = 5V	±15			pA
I _{OS} 输入失调电流		±5			pA
噪声					
E _n 输入电压噪声 (峰峰值)	f = 0.1Hz 至 10Hz , V _S = 5V	5.1			μV _{PP}
e _n 输入电压噪声密度	f = 1kHz , V _S = 5V	40			nV/ √ Hz
输入电容					
C _{ID} 差分		2			pF
C _{IC} 共模		5.5			pF
开环增益					
A _{OL} 开环电压增益	V _S = 2.7V , (V -) + 0.15V < V _O < (V+) - 0.15V , R _L = 2k Ω	110			dB
	V _S = 5.5V , (V -) + 0.15V < V _O < (V+) - 0.15V , R _L = 2k Ω	125			
频率响应					
GBW 增益带宽积	V _S = 5V	1			MHz
φ _m 相位裕度	V _S = 5.5V , G = 1	75			°
SR 压摆率	V _S = 5V	1.5			V/μs
t _S 趋稳时间	精度达到 0.1% , V _S = 5V , 2V 阶跃 , G = 1 , C _L = 100pF	4			μs
	精度达到 0.01% , V _S = 5V , 2V 阶跃 , G = 1 , C _L = 100pF	5			
t _{OR} 过载恢复时间	V _S = 5V , V _{IN} × 增益 > V _S	1			μs
THD+N 总谐波失真 + 噪声	V _S = 5.5V , V _{CM} = 2.5V , V _O = 1V _{RMS} , G = 1 , f = 1kHz , 80kHz 测量 BW	0.005%			
输出					
V _{OH} 相对于正电源的电压输出摆幅	R _L ≥ 2k Ω , T _A = - 40°C 至 125°C	1			V
V _{OL} 相对于负电源的电压输出摆幅	R _L ≤ 10k Ω , T _A = - 40°C 至 125°C	40		75	mV
I _{SC} 短路电流	V _S = 5.5V	±40			mA
Z _O 开环输出阻抗	V _S = 5V , f = 1 MHz	1200			Ω
电源					
V _S 额定电压范围		2.7 (±1.35)		5.5 (±2.75)	V
I _Q 每个放大器的静态电流	I _O = 0mA , V _S = 5.5 V	90		150	μA
	I _O = 0mA , V _S = 5.5V , T _A = - 40°C 至 125°C			160	

6.8 典型特性

在 $T_A = 25^\circ\text{C}$ 、 $V_+ = 2.75\text{V}$ 、 $V_- = -2.75\text{V}$ 、 $R_L = 10\text{k}\Omega$ (连接到 $V_S/2$ 、 $V_{CM} = V_S/2$ 并且 $V_{OUT} = V_S/2$ 条件下测得 (除非另有说明)

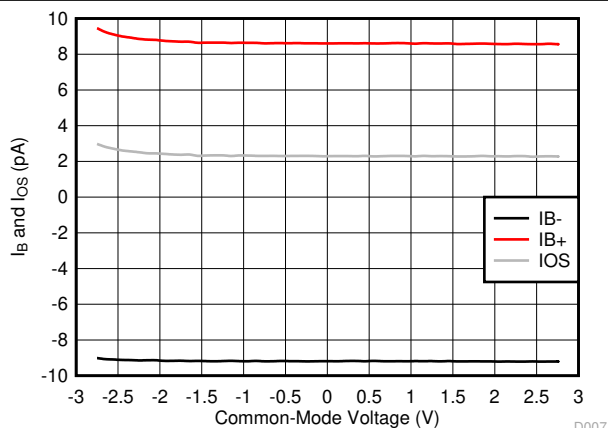


图 6-1. I_B 和 I_{OS} 与共模电压间的关系

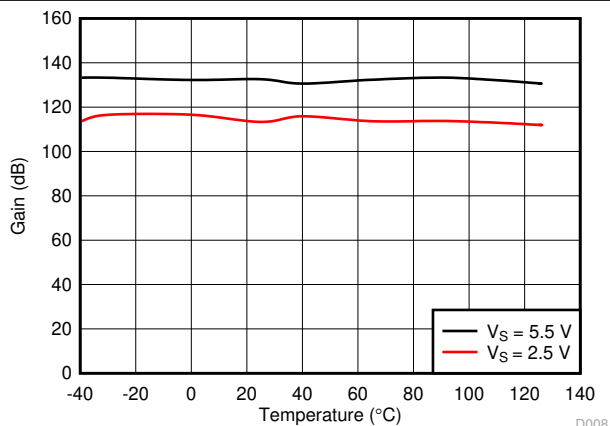


图 6-2. 开环增益与温度间的关系

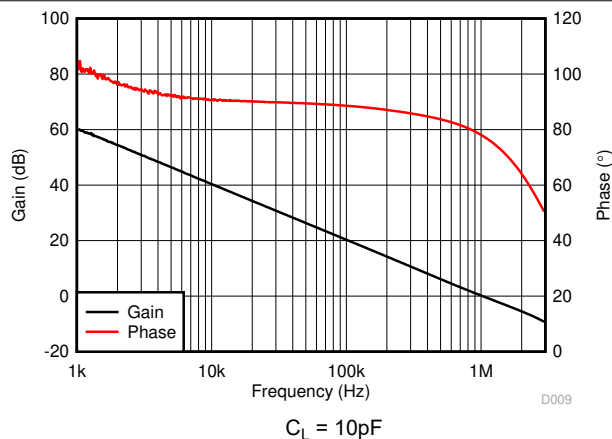


图 6-3. 开环增益和相位与频率间的关系

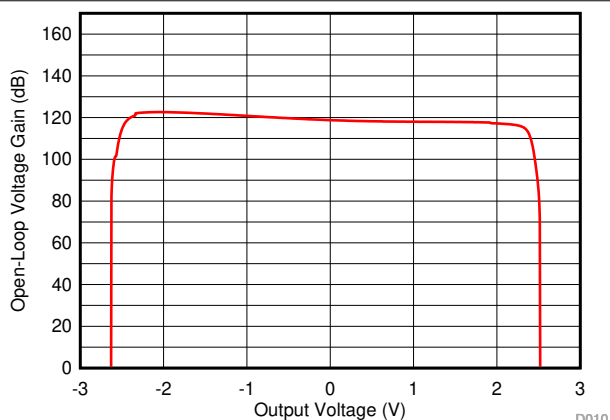


图 6-4. 开环电压增益与输出电压间的关系

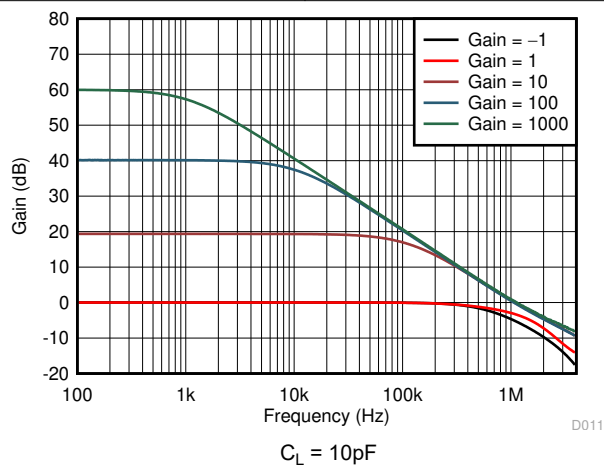


图 6-5. 闭环增益与频率间的关系

6.8 典型特性

在 $T_A = 25^\circ\text{C}$ 、 $V_+ = 2.75\text{V}$ 、 $V_- = -2.75\text{V}$ 、 $R_L = 10\text{k}\Omega$ (连接到 $V_S/2$ 、 $V_{CM} = V_S/2$ 并且 $V_{OUT} = V_S/2$ 条件下测得 (除非另有说明)

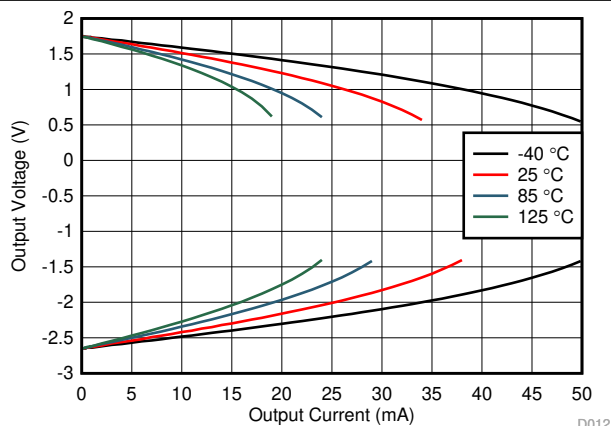


图 6-6. 输出电压与输出电流间的关系 (爪形)

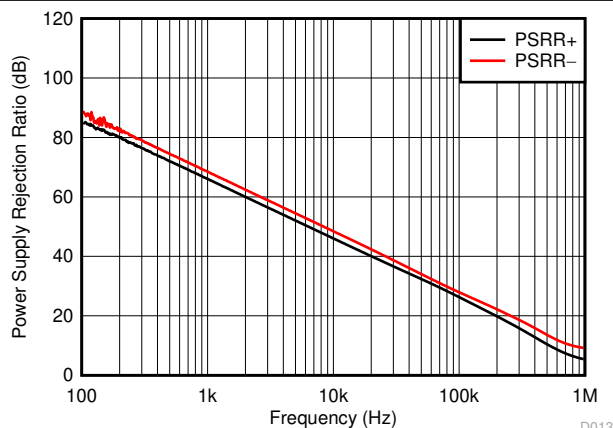
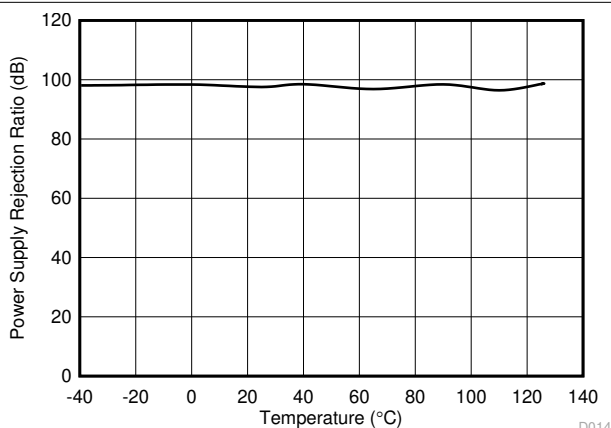


图 6-7. PSRR 与频率间的关系



$V_S = 2.7\text{V}$ 至 5.5V

图 6-8. 直流 PSRR 与温度间的关系

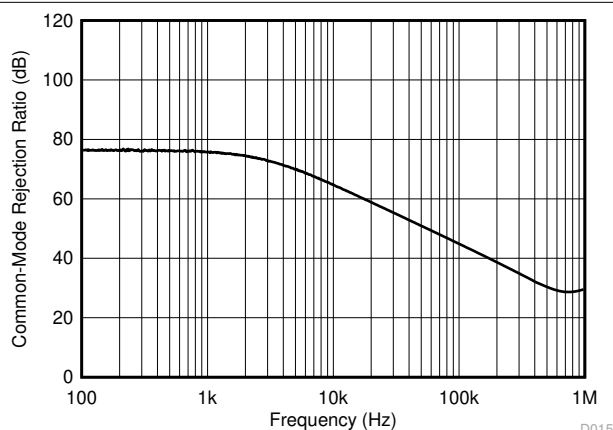
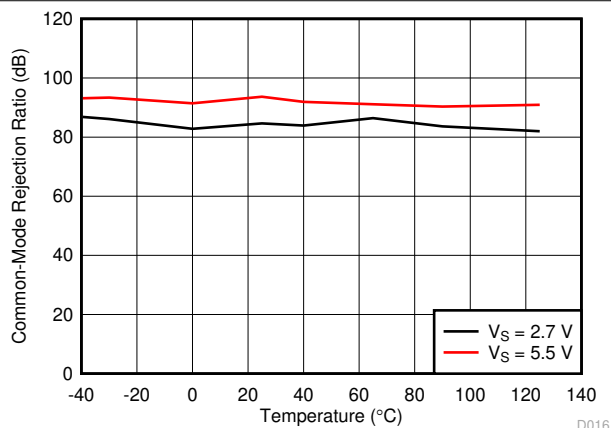


图 6-9. CMRR 与频率间的关系



$V_{CM} = (V_-) - 0.1\text{V}$ 至 $(V_+) - 1.5\text{V}$

图 6-10. 直流 CMRR 与温度间的关系

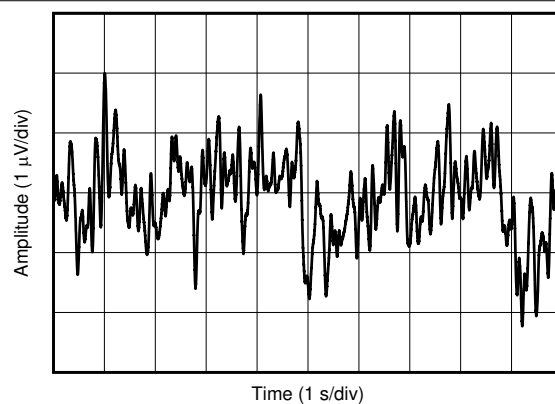


图 6-11. 0.1Hz 至 10Hz 集成电压噪声

6.8 典型特性

在 $T_A = 25^\circ\text{C}$ 、 $V_+ = 2.75\text{V}$ 、 $V_- = -2.75\text{V}$ 、 $R_L = 10\text{k}\Omega$ (连接到 $V_S/2$ 、 $V_{CM} = V_S/2$ 并且 $V_{OUT} = V_S/2$ 条件下测得 (除非另有说明)

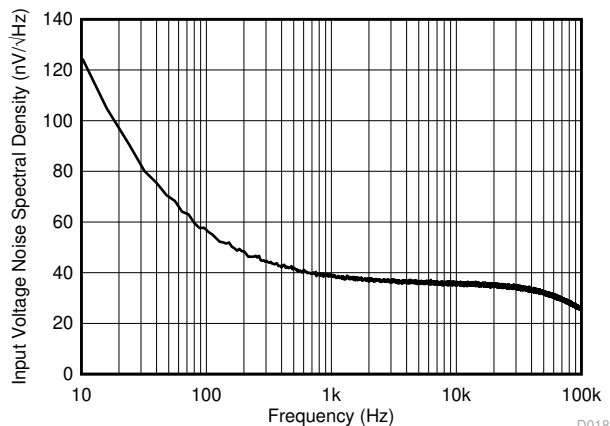


图 6-12. 输入电压噪声频谱密度

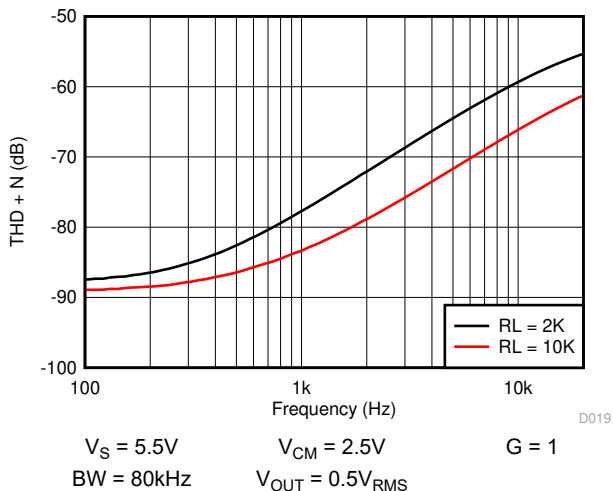


图 6-13. THD+N 与频率间的关系

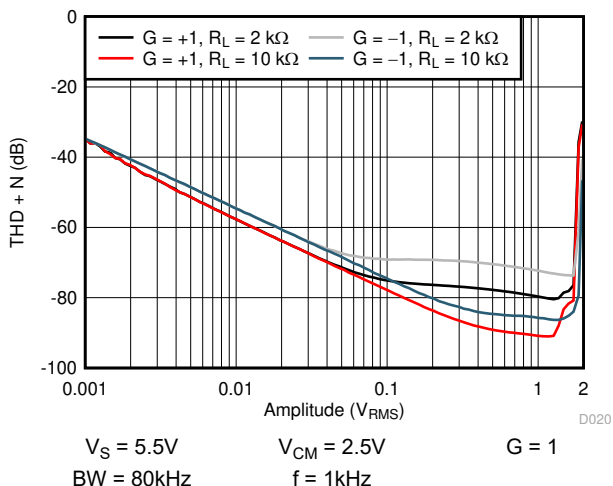


图 6-14. THD + N 与幅度间的关系

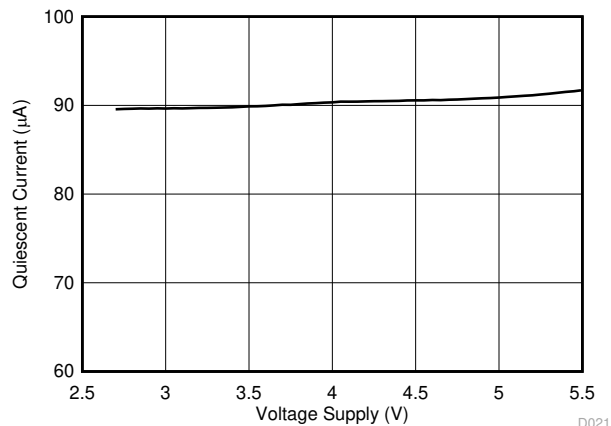


图 6-15. 静态电流与电源电压间的关系

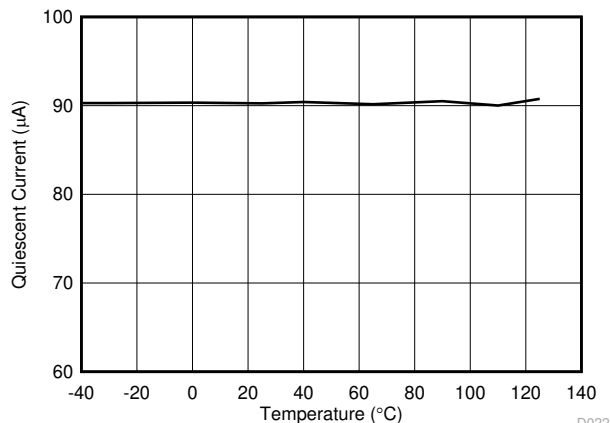


图 6-16. 静态电流与温度间的关系

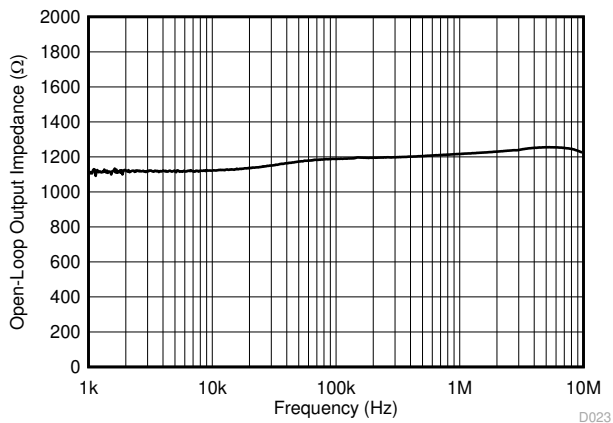
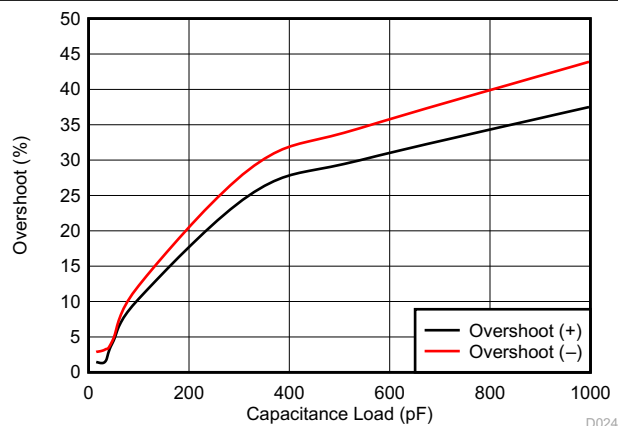


图 6-17. 开环输出阻抗与频率间的关系

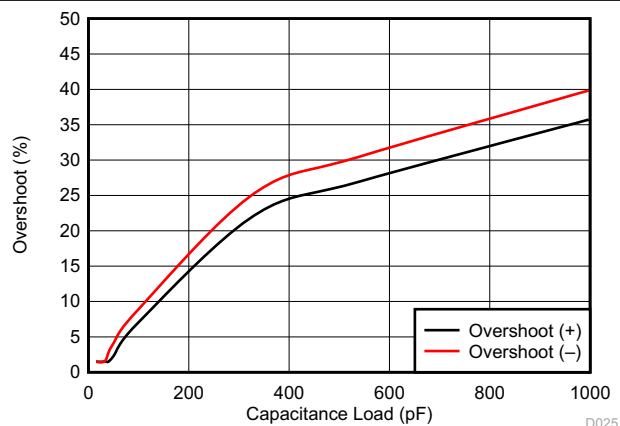
6.8 典型特性

在 $T_A = 25^\circ\text{C}$ 、 $V_+ = 2.75\text{V}$ 、 $V_- = -2.75\text{V}$ 、 $R_L = 10\text{k}\Omega$ (连接到 $V_S/2$ 、 $V_{CM} = V_S/2$ 并且 $V_{OUT} = V_S/2$ 条件下测得 (除非另有说明)



$G = 1$ $V_{IN} = 100\text{mVpp}$

图 6-18. 小信号过冲与容性负载间的关系



$G = -1$ $V_{IN} = 100\text{mVpp}$

图 6-19. 小信号过冲与容性负载间的关系

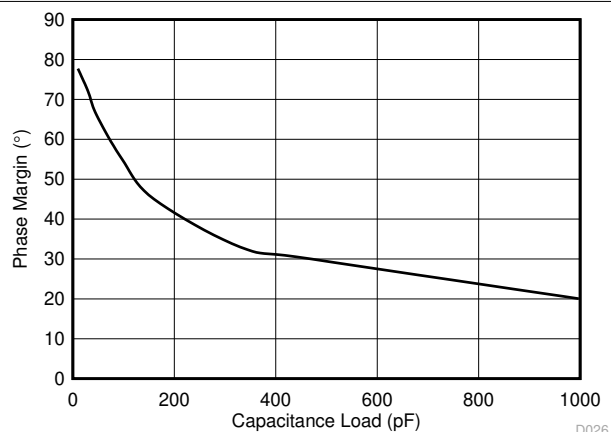
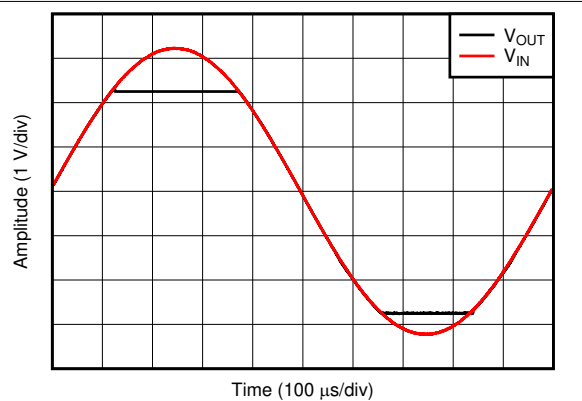
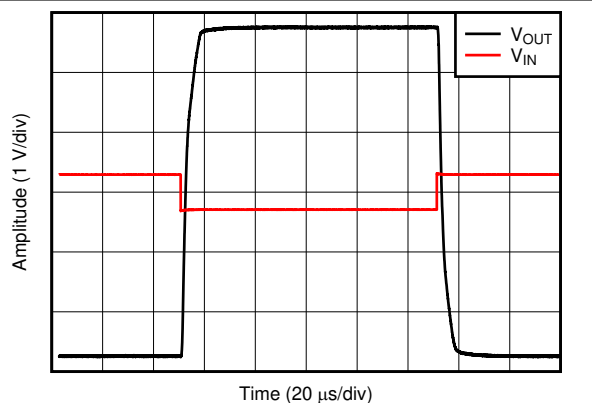


图 6-20. 相位裕度与容性负载间的关系



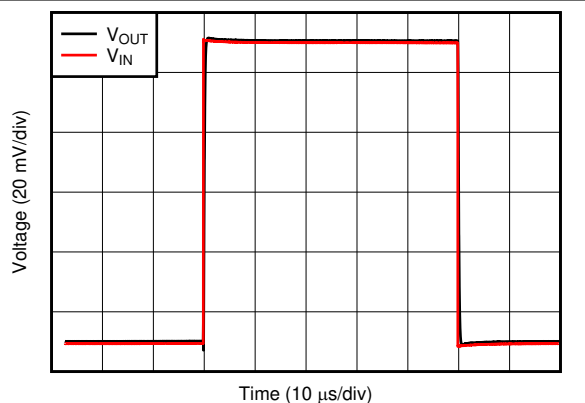
$G = 1$ $V_{IN} = 6.5\text{Vpp}$

图 6-21. 无相位反转



$G = -10$ $V_{IN} = 600\text{mVpp}$

图 6-22. 过载恢复



$G = 1$ $V_{IN} = 100\text{mVpp}$ $C_L = 10\text{pF}$

图 6-23. 小信号阶跃响应

6.8 典型特性 (continued)

在 $T_A = 25^\circ\text{C}$ 、 $V_+ = 2.75\text{V}$ 、 $V_- = -2.75\text{V}$ 、 $R_L = 10\text{k}\Omega$ (连接到 $V_S/2$ 、 $V_{CM} = V_S/2$ 并且 $V_{OUT} = V_S/2$ 条件下测得 (除非另有说明)

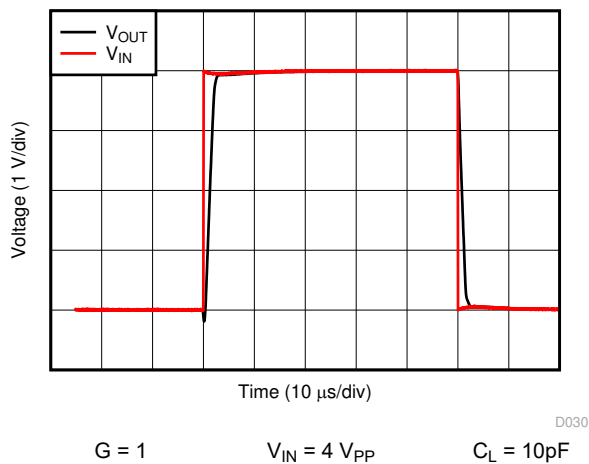


图 6-24. 大信号阶跃响应

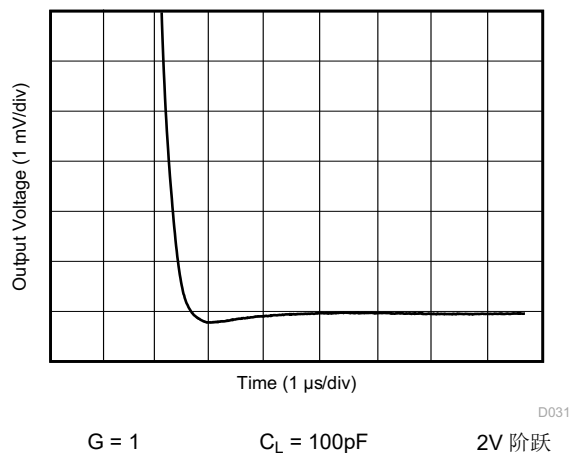


图 6-25. 大信号稳定时间 (负)

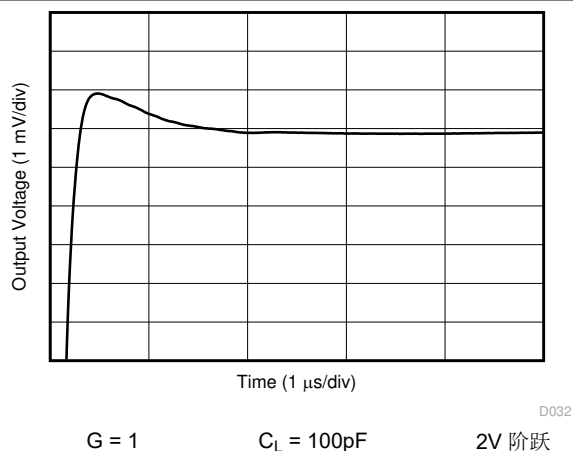


图 6-26. 大信号稳定时间 (正)

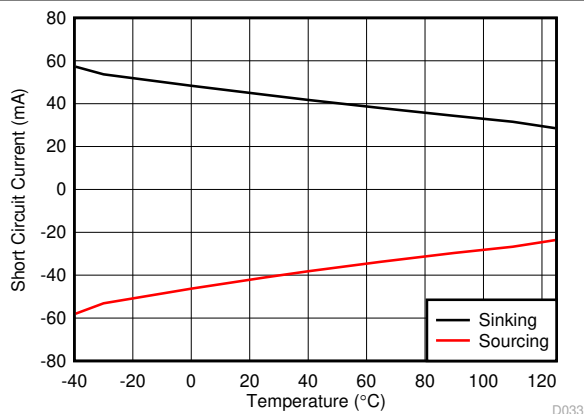


图 6-27. 短路电流与温度间的关系

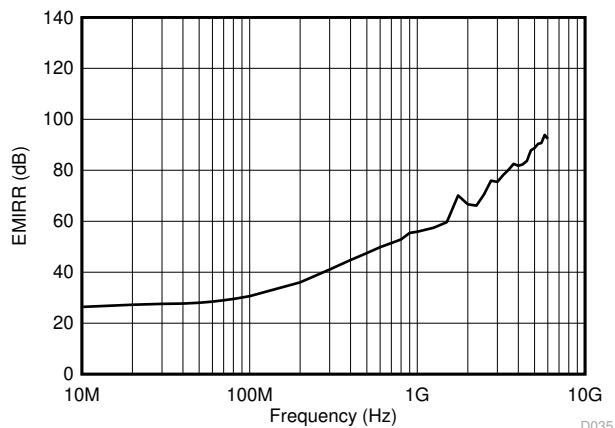


图 6-28. 以同相输入为基准的电磁干扰抑制比 (EMIRR+) 与频率间的关系

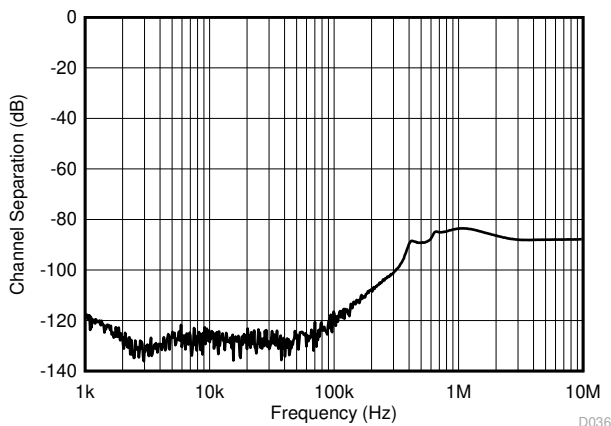


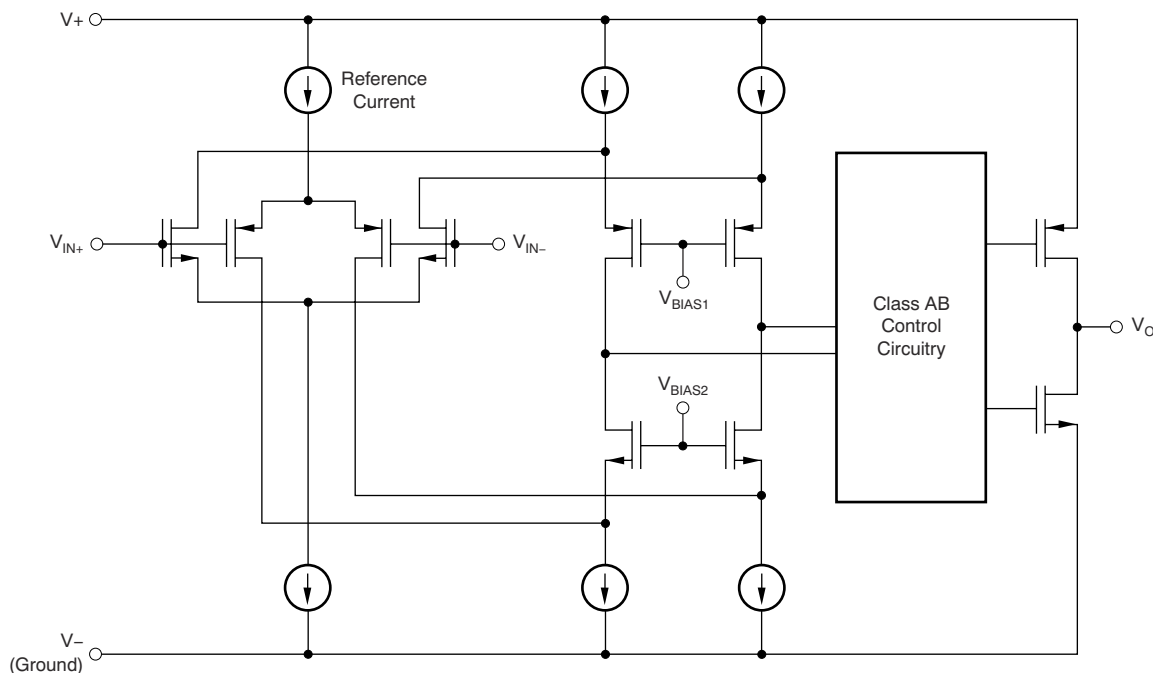
图 6-29. 通道分离

7 详细说明

7.1 概述

LM3xxLV 系列低功耗运算放大器适用于成本优化型系统。这些器件的工作电压范围为 2.7V 至 5.5V，具有单位增益稳定特性，并且适用于各种通用应用。输入共模电压范围包括负电源轨，并支持将 LM3xxLV 系列用于许多单电源应用。

7.2 功能方框图



7.3 特性说明

7.3.1 工作电压

LM3xxLV 系列的运算放大器的额定工作电压范围是 2.7V 至 5.5V。此外，许多规格在 -40°C 至 125°C 的温度范围内都适用。电气特性部分展示了随着工作电压或温度而显著变化的参数。

7.3.2 共模输入范围包括接地

LM3xxLV 系列的输入共模电压范围扩展到负电源轨，低于正电源轨不到 1V，整个供电电压范围为 2.7V 至 5.5V。该性能通过 P 沟道差分对实现，如功能方框图所示。此外，还并联了一个互补的 N 沟道差分对，以消除前几代运算放大器常见的相位反转问题。不过，N 沟道对并未针对运行进行优化，并且在其运行期间性能会显著下降。TI 建议将在输入端施加的任何电压限制为至少比正电源轨 (V+) 低 1V，以确保运算放大器符合电气特性部分中详述的规格。

7.3.3 过载恢复

过载恢复定义为运算放大器输出从饱和状态恢复到线性状态所需的时间。当输出电压由于高输入电压或高增益而超过额定输出电压摆幅时，运算放大器的输出器件进入饱和区。器件进入饱和区后，输出器件中的电荷载体需要时间回到线性状态。当电荷载体回到线性状态时，器件开始以指定的压摆率进行转换。因此，传播延迟（过载情况下）等于过载恢复时间与转换时间之和。LM3xxLV 系列的过载恢复时间通常为 $1\mu\text{s}$ 。

7.3.4 电气过应力

设计人员经常会问到关于运算放大器耐受电气过应力的问题。这些问题往往侧重于器件输入，但是也可能涉及到电源电压引脚。这些不同的引脚功能均具有由特定半导体制造工艺和连接到引脚的特定电路的电压击穿特性所决

定的电应力限制。此外，这些电路均内置内部静电放电 (ESD) 保护功能，可在产品组装之前和组装过程中保护电路不受意外 ESD 事件的影响。

能够充分了解该基本 ESD 电路及其与电气过应力事件的关联性会有所帮助。图 7-1 展示了 LM3xxLV 中包含的 ESD 电路。ESD 保护电路中涉及多个导流二极管，这些二极管从输入引脚和输出引脚连接回内部供电线路，并且它们均连接到运算放大器内部的吸收器件。该保护电路在电路正常工作时处于未激活状态。

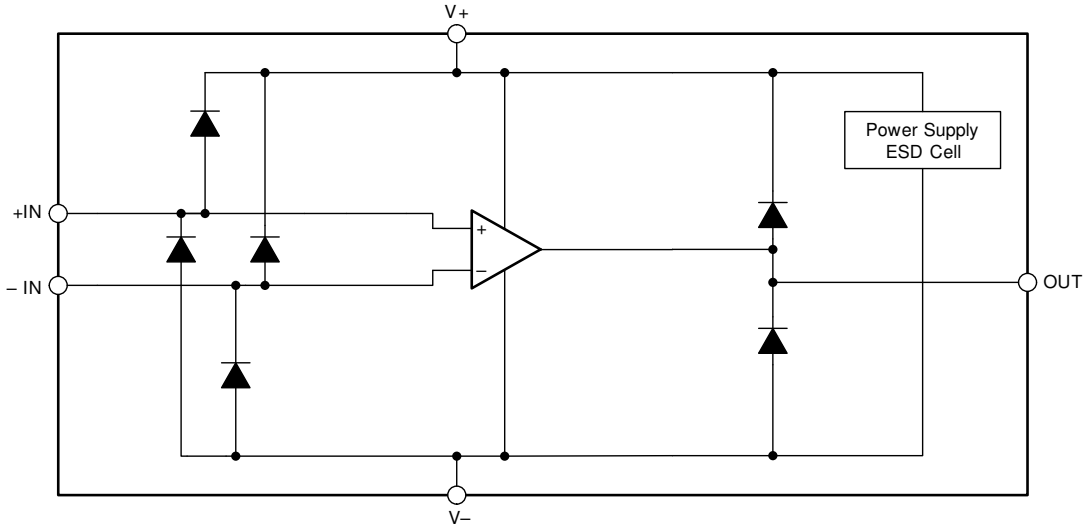


图 7-1. 等效内部 ESD 电路

7.3.5 EMI 易感性和输入滤波

德州仪器 (TI) 已经开发出在 10MHz 至 6GHz 扩展宽频谱范围内准确测量和量化运算放大器抗扰度的功能。图 6-28 图说明了 LM3xxLV 系列的 EMI 滤波器在很宽的频率范围内的性能。更多详细信息请参阅可从 www.ti.com 下载的 [运算放大器的 EMI 抑制比](#)。

7.4 器件功能模式

LM3xxLV 系列具有单功能模式。只要电源电压在 2.7 V (± 1.35 V) 与 5.5V (± 2.75 V) 之间，这些器件就会启动。

8 应用和实现

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 应用信息

LM3xxLV 器件是一系列低功耗、成本优化型运算放大器。这些器件的工作电压为 2.7V 至 5.5V，单位增益稳定，适合广泛的通用应用。输入共模电压范围包括负电源轨，并支持将 LM3xxLV 用于任何单电源应用。

8.2 典型应用

图 8-1 展示了低侧电流感测应用中配置的 LM3xxLV 器件。

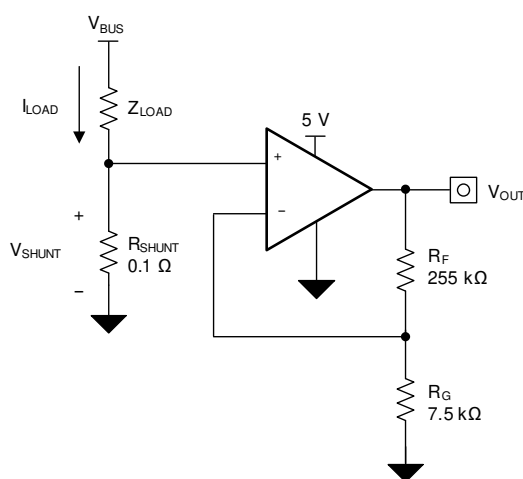


图 8-1. 低侧电流感测应用中的 LM3xxLV 器件

8.2.1 设计要求

此设计的设计要求如下：

- 负载电流：0A 至 1A
- 输出电压：3.5V
- 最大分流电压：100mV

8.2.2 详细设计过程

方程式 1 提供了图 8-1 中的电路传递函数：

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times \text{Gain} \quad (1)$$

负载电流 (I_{LOAD}) 在分流电阻器 (R_{SHUNT}) 上产生压降。负载电流设置为 0A 至 1A。为了在最大负载电流下保持分流电压低于 100mV，使用方程式 2 展示了允许的最大分流电阻器。

$$R_{SHUNT} = \frac{V_{SHUNT_MAX}}{I_{LOAD_MAX}} = \frac{100\text{mV}}{1\text{A}} = 100\text{m}\Omega \quad (2)$$

根据方程式 2 计算出的 R_{SHUNT} 为 100mΩ。 I_{LOAD} 和 R_{SHUNT} 产生的电压降由 LM3xxLV 器件放大，从而产生大约 0V 至 3.5V 的输出电压。LM3xxLV 产生必要输出电压时所需的增益根据方程式 3 算出：

$$\text{Gain} = \frac{(V_{\text{OUT_MAX}} - V_{\text{OUT_MIN}})}{(V_{\text{IN_MAX}} - V_{\text{IN_MIN}})} \quad (3)$$

使用方程式 3 计算出的所需增益为 35 V/V，该值由电阻器 R_F 和 R_G 设置。方程式 4 调整电阻器 R_F 和 R_G 的阻值大小，从而将 LM3xxLV 器件的增益设置为 35V/V。

$$\text{Gain} = 1 + \frac{(R_F)}{(R_G)} \quad (4)$$

8.2.3 应用曲线

将 R_F 选为 255k Ω 以及将 R_G 选为 7.5k Ω ，可提供等同于 35V/V 的组合。图 8-2 展示了图 8-1 中所示电路测得的传递函数。请注意，增益只是反馈和增益电阻器的函数。通过改变电阻器的比率来调整该增益，实际电阻器阻值由设计人员希望建立的阻抗水平决定。阻抗水平决定了电流消耗、杂散电容的影响以及其他一些行为。并不存在适用于每个系统的最佳阻抗选择，您必须选择适合您的系统参数的阻抗。

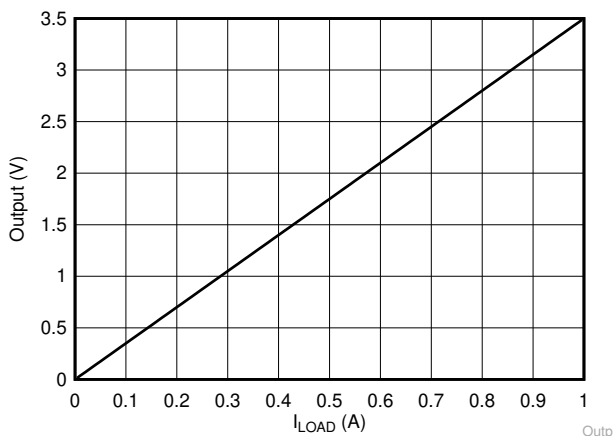


图 8-2. 低侧电流感测传递函数

9 电源相关建议

LM3xxLV 系列的额定工作电压范围为 2.7V 至 5.5V ($\pm 1.35\text{V}$ 至 $\pm 2.75\text{V}$)；多种规格适用于 -40°C 至 125°C 的温度范围。[电气特性](#) 部分介绍了可能会随工作电压或温度而显著变化的参数。

CAUTION

电源电压大于 6V 可能对器件造成永久损坏；请参阅[绝对最大额定值表](#)。

将 $0.1\mu\text{F}$ 旁路电容器置于电源引脚附近，以减少来自高噪声电源或高阻抗电源的耦合误差。有关旁路电容器放置位置的详细信息，请参阅[布局指南](#)部分。

9.1 输入和 ESD 保护

LM3xxLV 系列在所有引脚上均整合了内部 ESD 保护电路。对于输入和输出引脚，这种保护主要包括输入和电源引脚之间连接的导流二极管。只要电流如[表 6.1](#) 中所述不超过 10mA，这些 ESD 保护二极管就能提供电路内输入过驱保护。[图 9-1](#) 展示了如何通过将串联输入电阻器添加到被驱动的输入端来限制输入电流。添加的电阻器会增加放大器输入端的热噪声，在对噪声敏感的应用中，该值必须非常小。

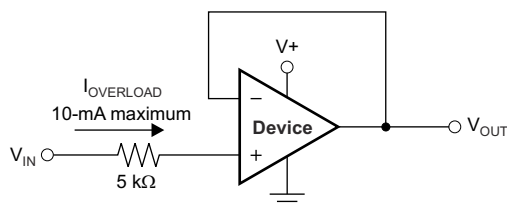


图 9-1. 输入电流保护

10 布局

10.1 布局指南

为了使器件具有最佳运行性能，请使用良好的印刷电路板 (PCB) 布局实践，包括：

- 噪声可以通过整个电路的电源引脚和运算放大器本身的电源引脚传入模拟电路。旁路电容用于通过为局部模拟电路提供低阻抗电源，以降低耦合噪声。
 - 在每个电源引脚和接地端之间接入低等效串联电阻 (ESR) 0.1 μ F 陶瓷旁路电容，并尽量靠近器件放置。针对单电源应用，V+ 与接地端之间可以接入单个旁路电容器。
- 将电路中模拟和数字部分单独接地是最简单和最有效的噪声抑制方法之一。多层 PCB 上的一层或多层通常专门用于作为接地平面。接地层有助于散热和降低电磁干扰 (EMI) 噪声拾取。注意在物理上分离数字接地和模拟接地。使用热特征或 EMI 测量技术来确定大部分接地电流流向何处，并确保将该路径从敏感的模拟电路引开。更多详细信息，请参阅 [电路板布局技巧](#) 应用手册。
- 为了减少寄生耦合，请让输入走线尽可能远离电源或输出走线。如果这些走线不能保持分开，则以 90 度角穿过敏感走线比平行于噪声走线来排布走线要好得多。
- 应尽可能靠近器件放置外部元件，如图 10-2 所示。使 R_F 和 R_G 接近反相输入可最大限度地减小寄生电容。
- 尽可能缩短输入走线。切记，输入走线是电路中最敏感的部分。
- 考虑在关键走线周围设定驱动型低阻抗保护环。这样可显著减少附近不同电势下的走线所产生的泄漏电流。
- 为获得最佳性能，建议在组装 PCB 板后进行清洗。
- 任何精密集成电路都可能因湿气渗入塑料封装中而出现性能变化。请遵循所有的 PCB 水清洁流程，建议将 PCB 组装烘干，以去除清洗时渗入器件封装中的湿气。大多数情形下，清洗后在 85°C 下低温烘干 30 分钟即可。

10.2 布局示例

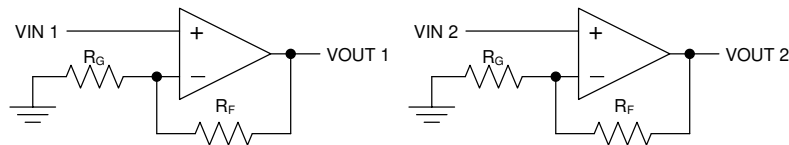


图 10-1. 原理图表示：

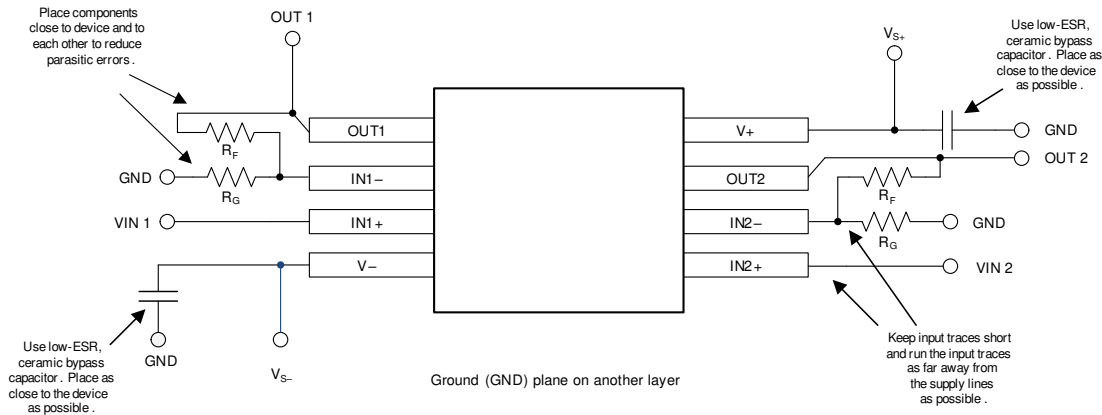


图 10-2. 布局示例

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI), [运算放大器的 EMI 抑制比应用报告](#)
- 德州仪器 (TI), [电路板布局技巧应用手册](#)

11.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 支持资源

TI E2E™ 支持论坛 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

11.4 商标

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 术语表

TI 术语表

本术语表列出并解释了术语、首字母缩略词和定义。

12 机械、封装和可订购信息

下述页面包含机械、封装和订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查看左侧的导航面板。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM321LVIDBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	1SPF
LM321LVIDCKR	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1DH
LM324LVIDR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LM324LV
LM324LVIDYYR	Active	Production	SOT-23-THIN (DYY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM324L
LM324LVIPWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 125	LM324LV
LM358LVIDDFR	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L58L
LM358LVIDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU SN NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1PKX
LM358LVIDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 125	L358LV
LM358LVIPWR	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 125	358LV

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

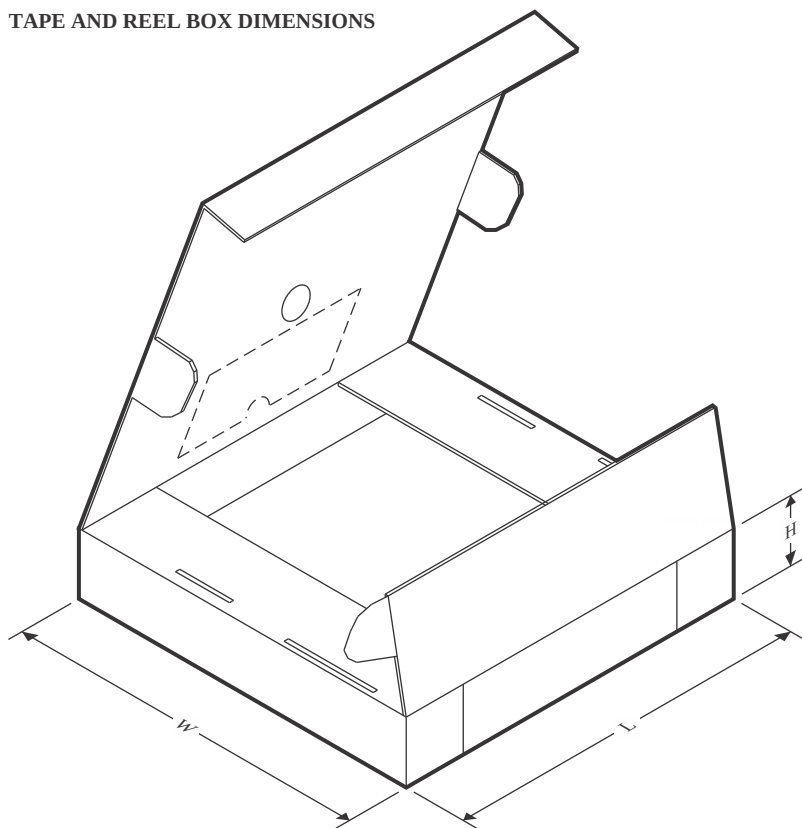
TAPE AND REEL INFORMATION



*All dimensions are nominal

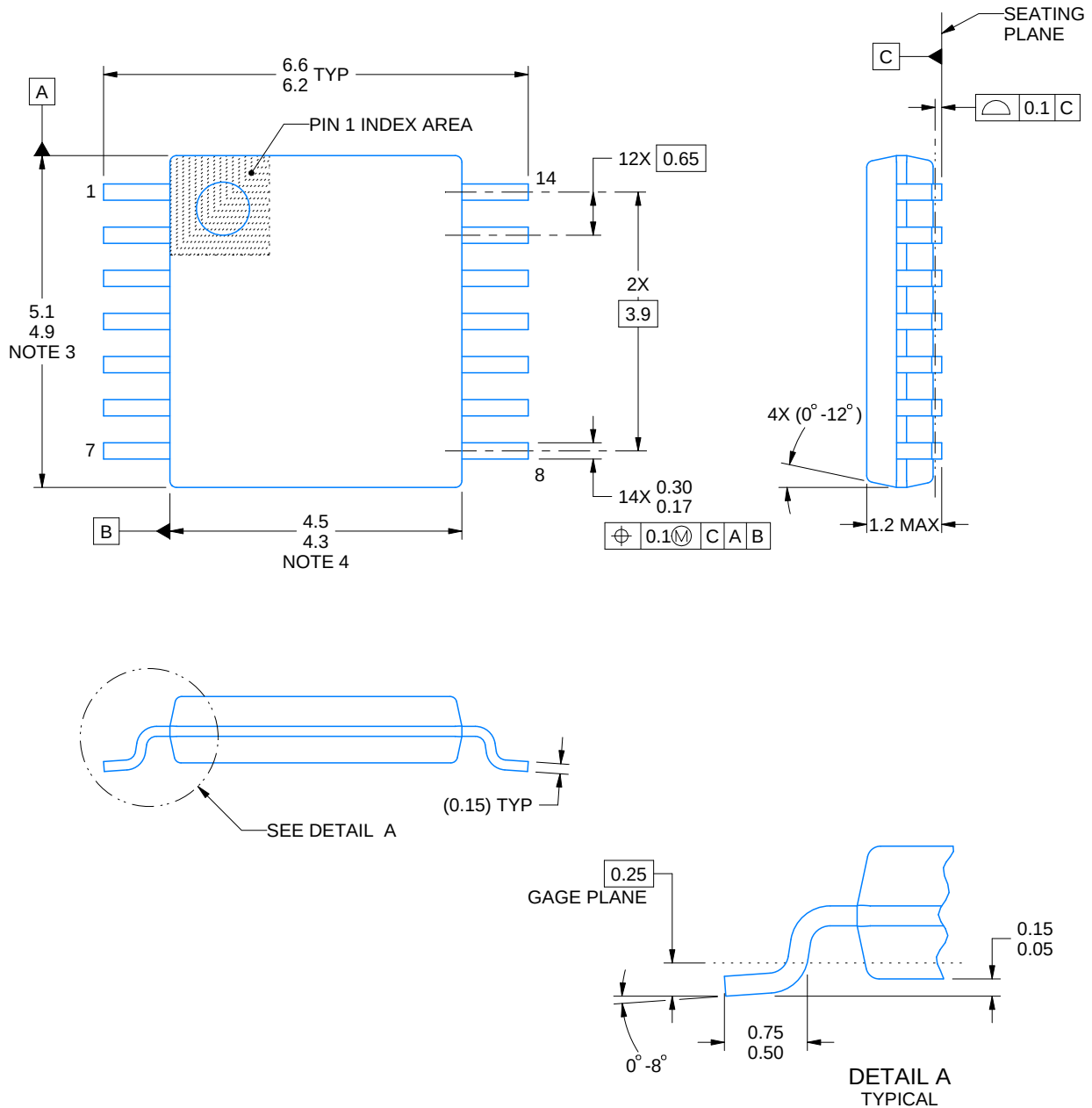
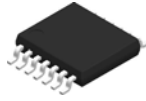
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM321LVDBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM321LVIDCKR	SC70	DCR	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
LM324LVIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM324LVIDYYR	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
LM324LVIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM358LVIDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM358LVIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM358LVIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358LVIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM321LVDBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
LM321LVIDCKR	SC70	DCK	5	3000	210.0	185.0	35.0
LM324LVDR	SOIC	D	14	2500	356.0	356.0	35.0
LM324LVIDYYR	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8
LM324LVIPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
LM358LVIDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
LM358LVIDGKR	VSSOP	DGK	8	2500	356.0	356.0	35.0
LM358LVDR	SOIC	D	8	2500	356.0	356.0	35.0
LM358LVIPWR	TSSOP	PW	8	2000	356.0	356.0	35.0



4220202/B 12/2023

NOTES:

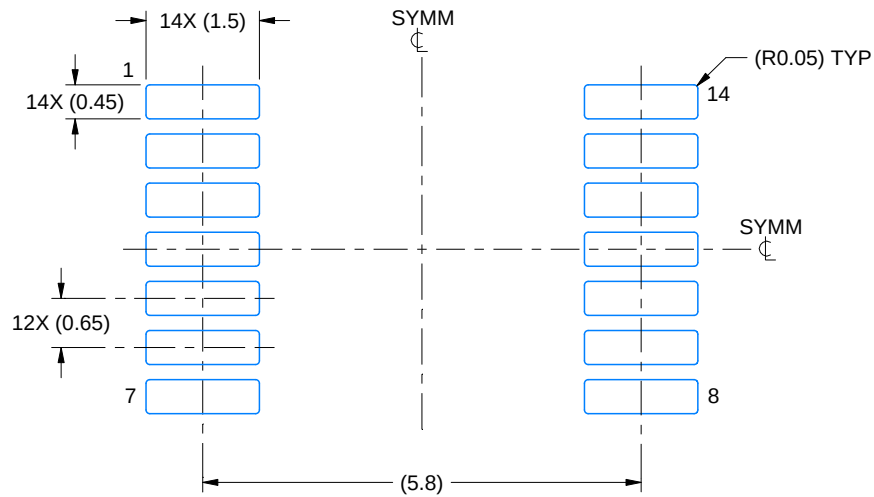
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

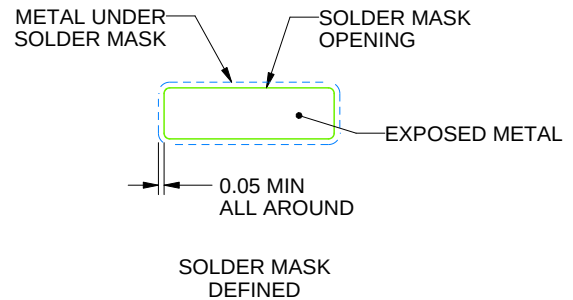
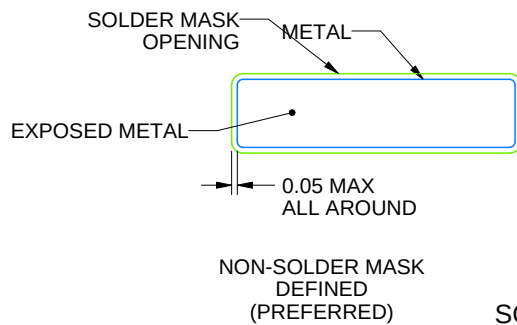
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

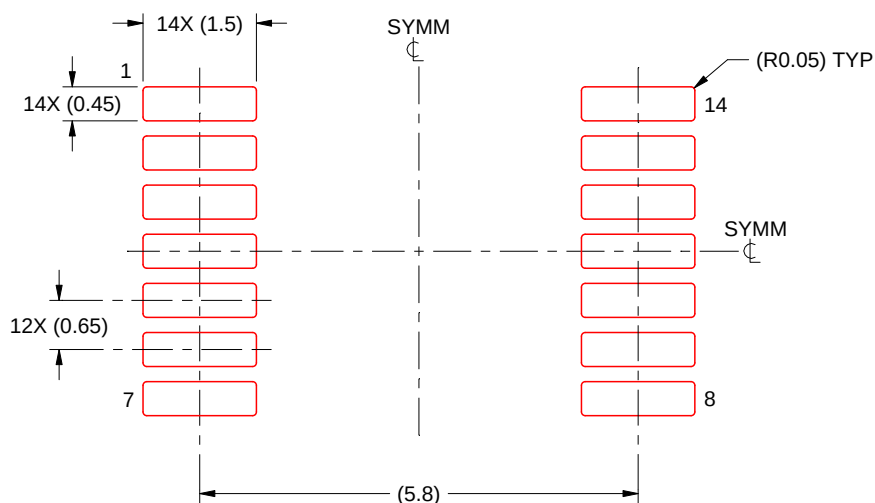
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

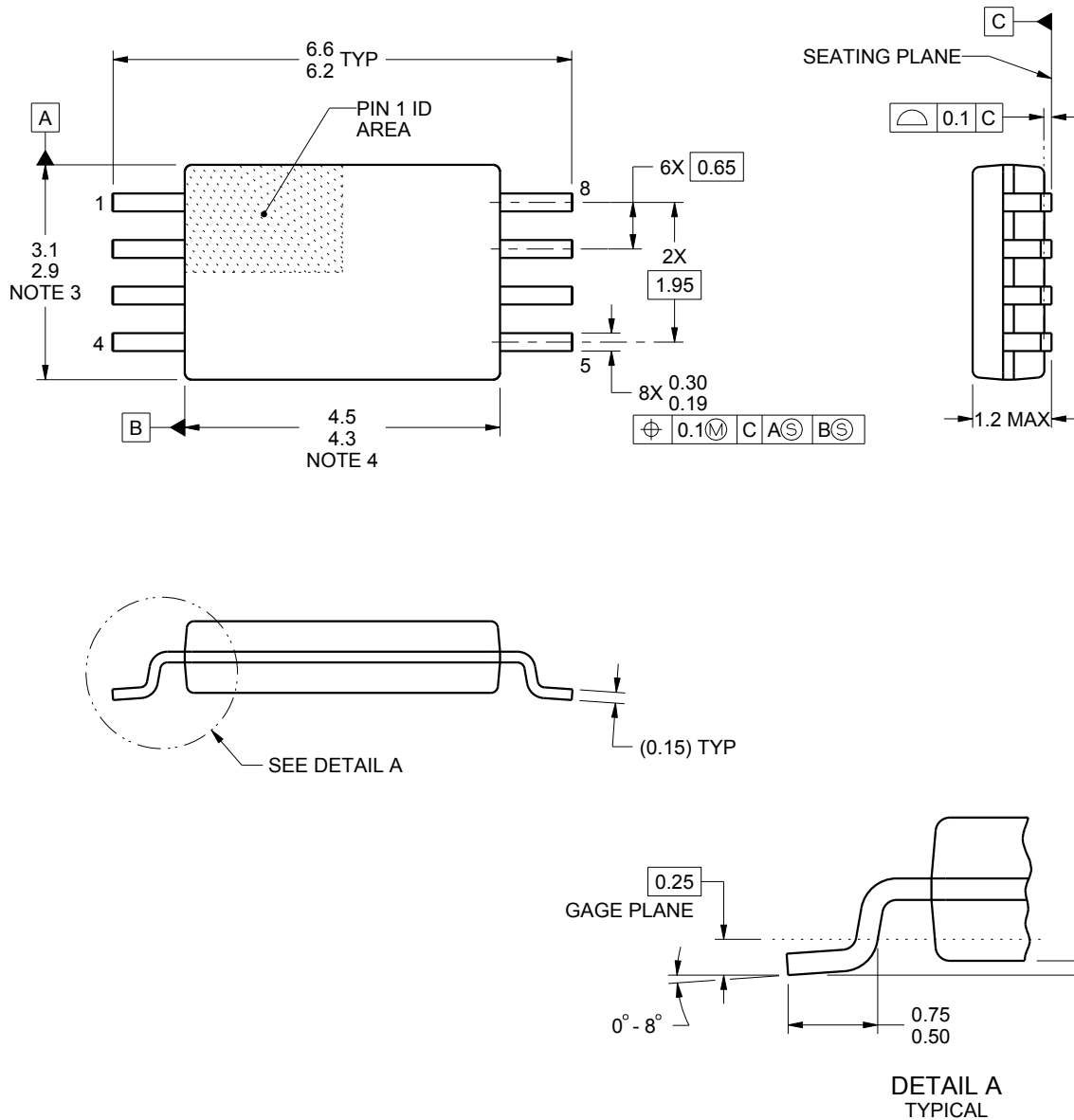
PW0008A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

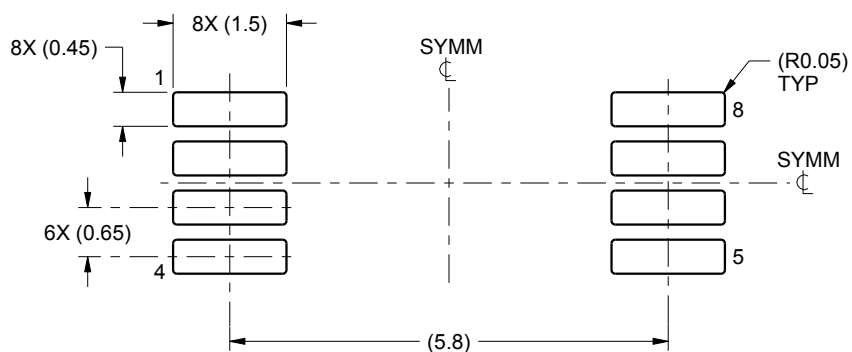
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

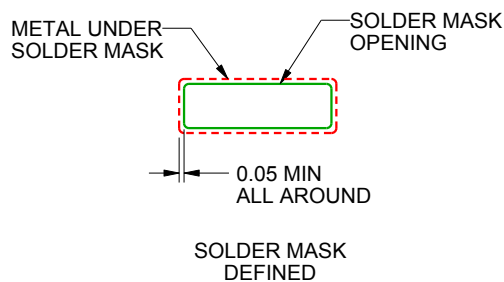
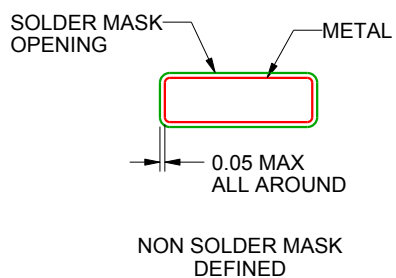
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

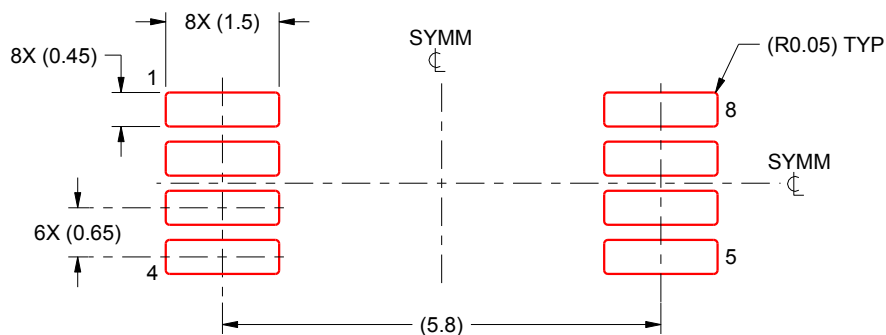
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

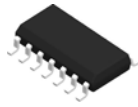


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

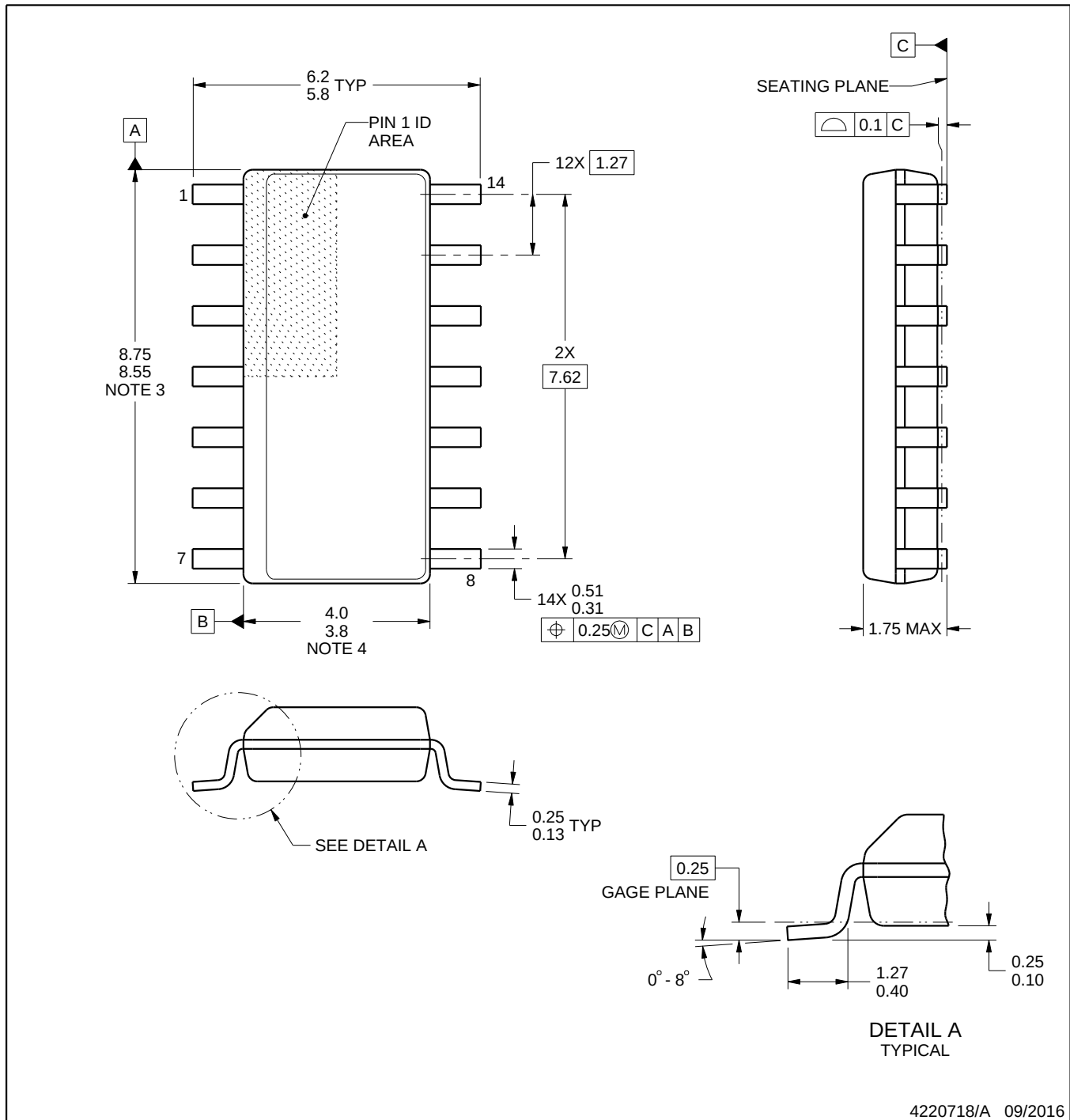
4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

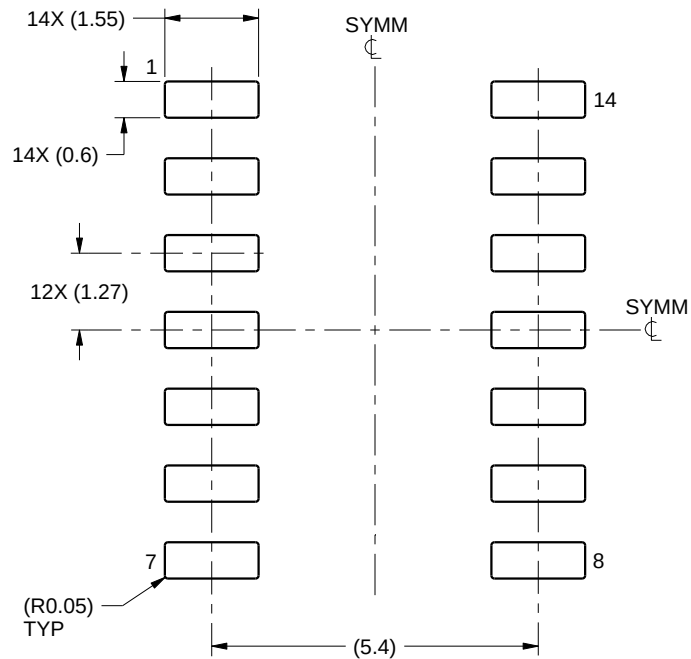
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

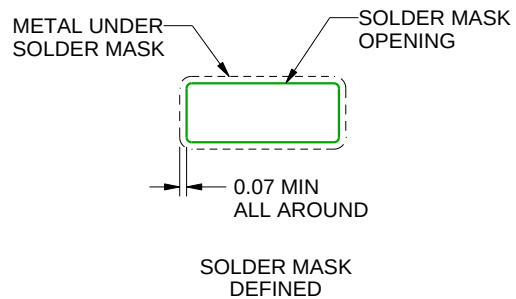
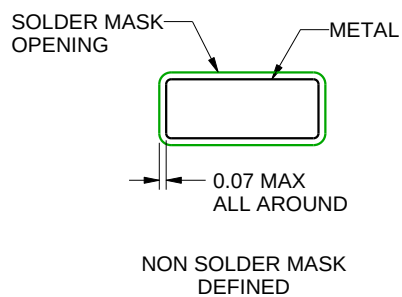
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

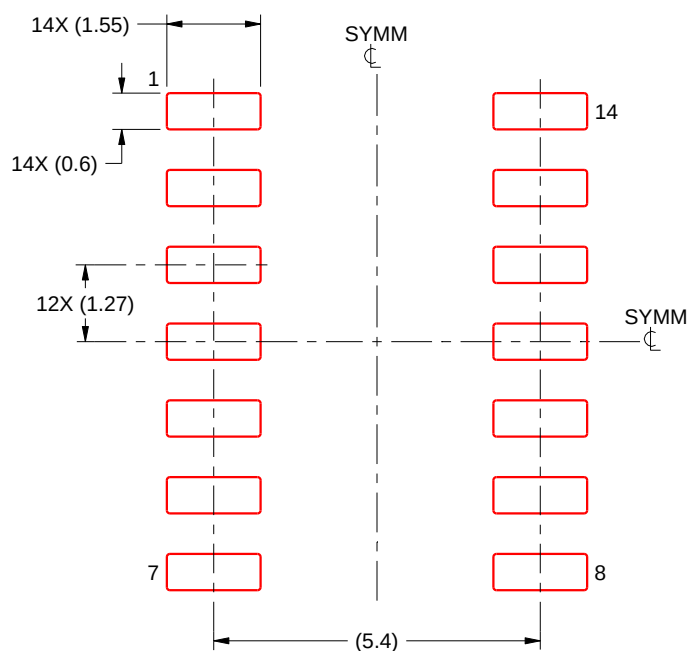
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

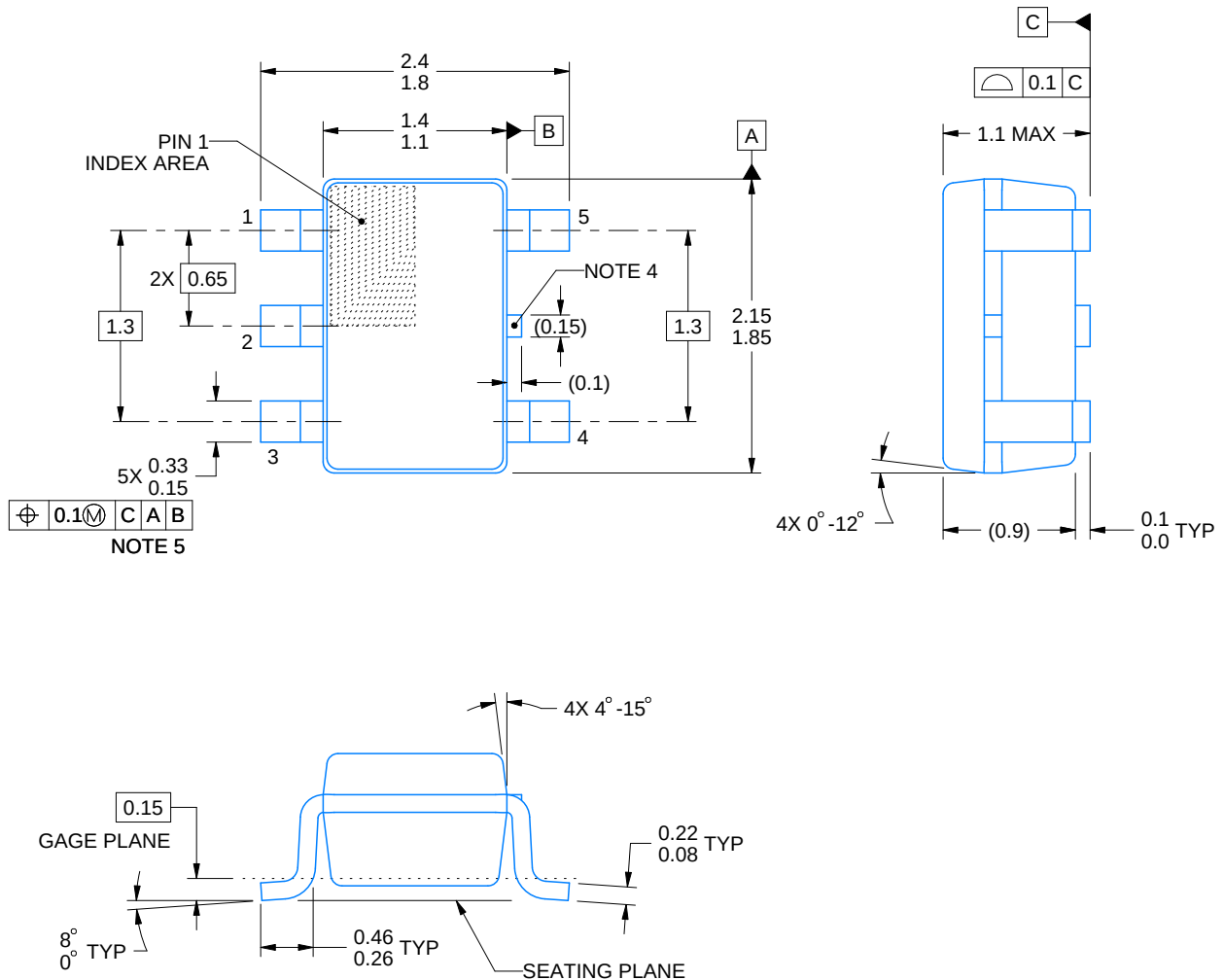


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4214834/G 11/2024

NOTES:

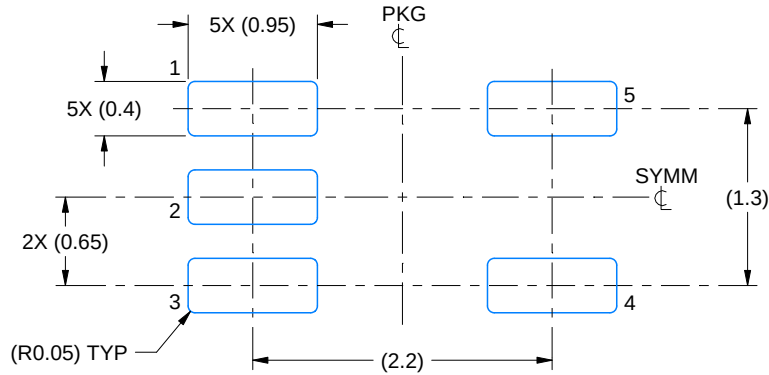
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

EXAMPLE BOARD LAYOUT

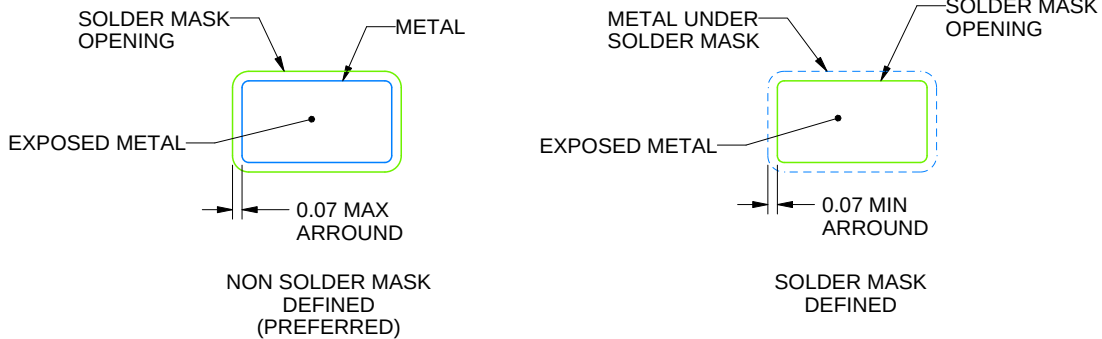
DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214834/G 11/2024

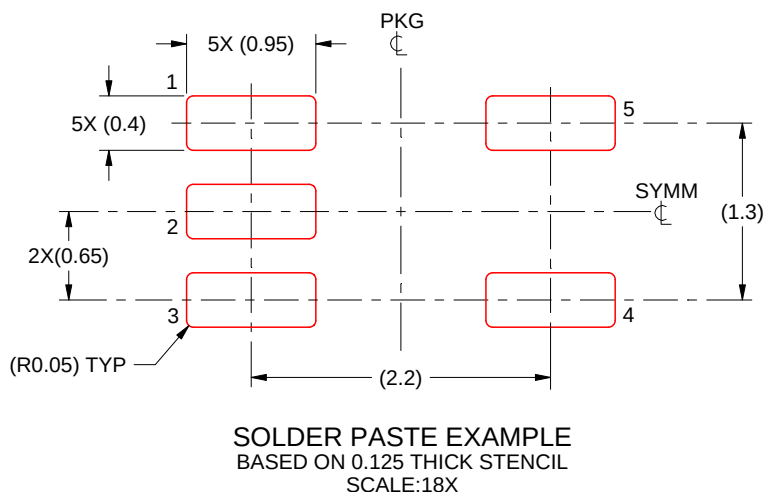
NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214834/G 11/2024

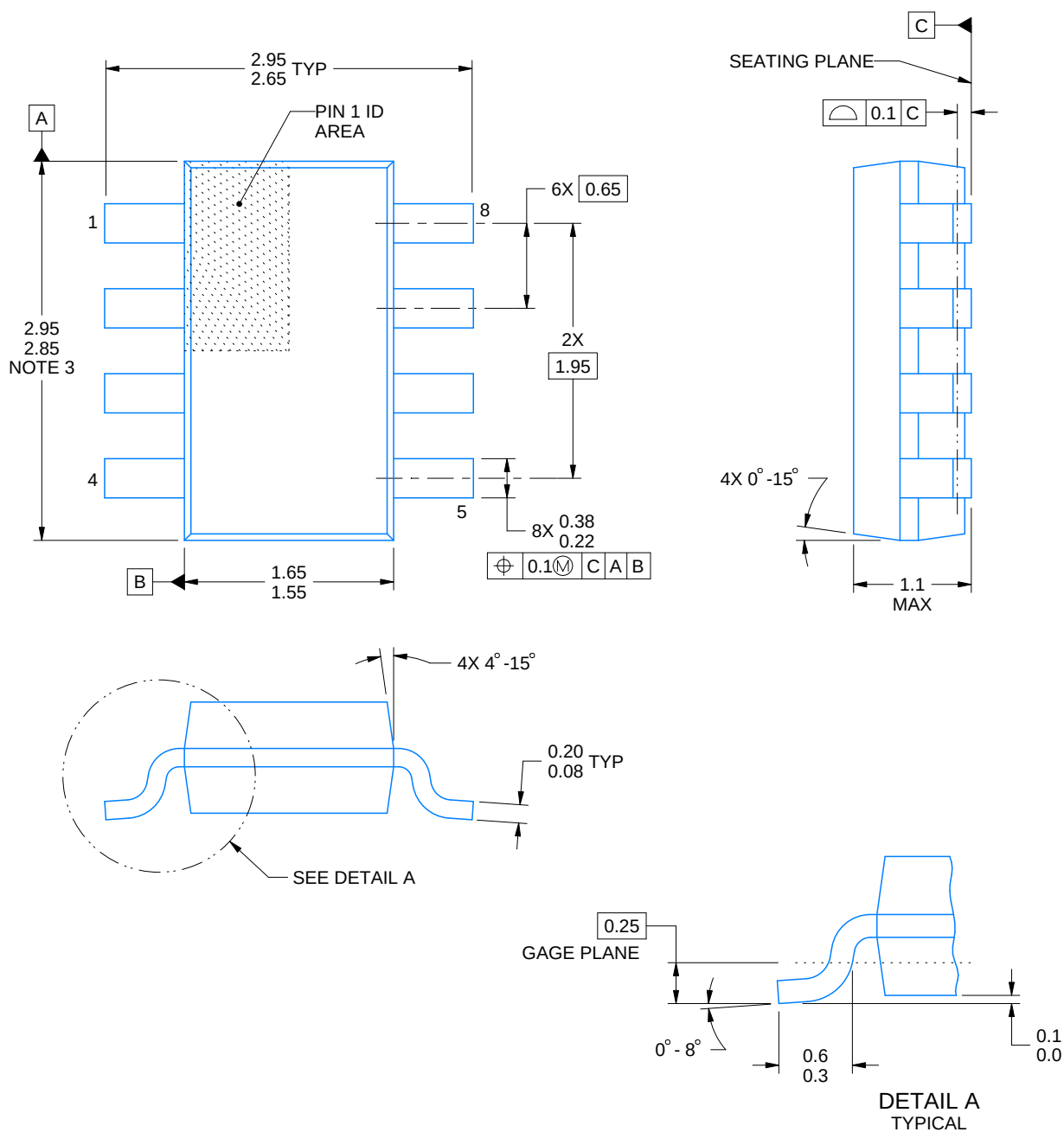
NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.



SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



4222047/E 07/2024

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

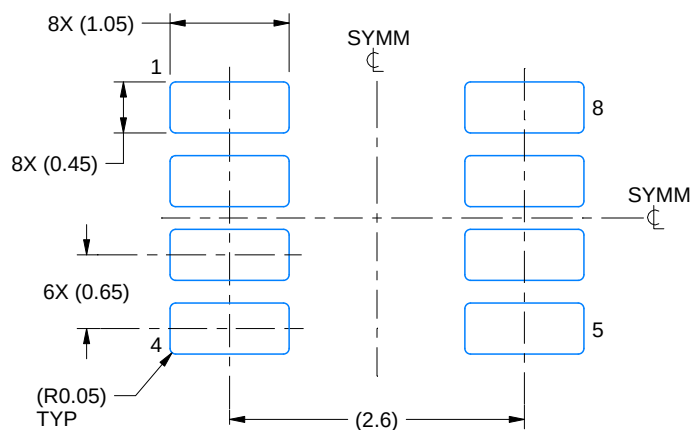
2. This drawing is subject to change without notice.

3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

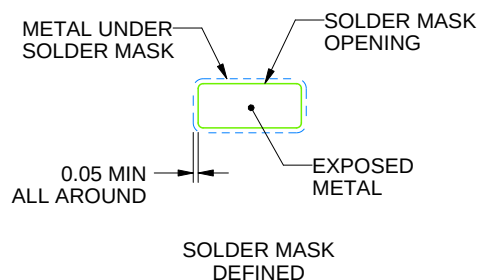
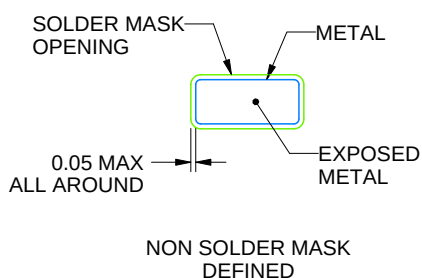
DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

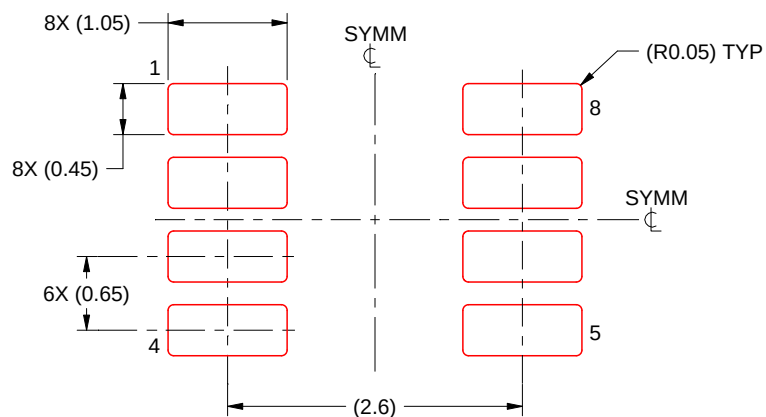
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

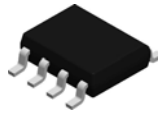


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

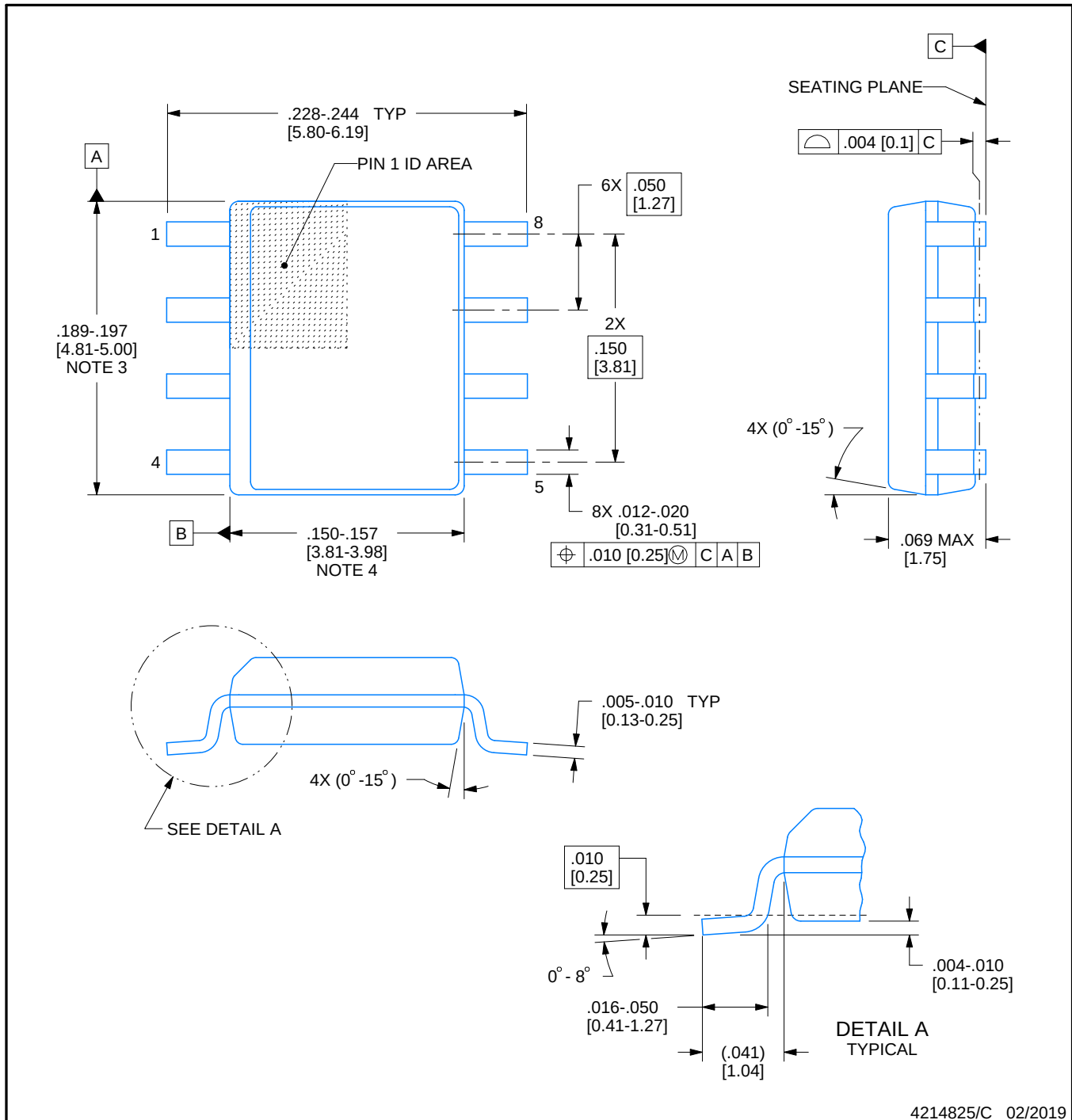
4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

D0008A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

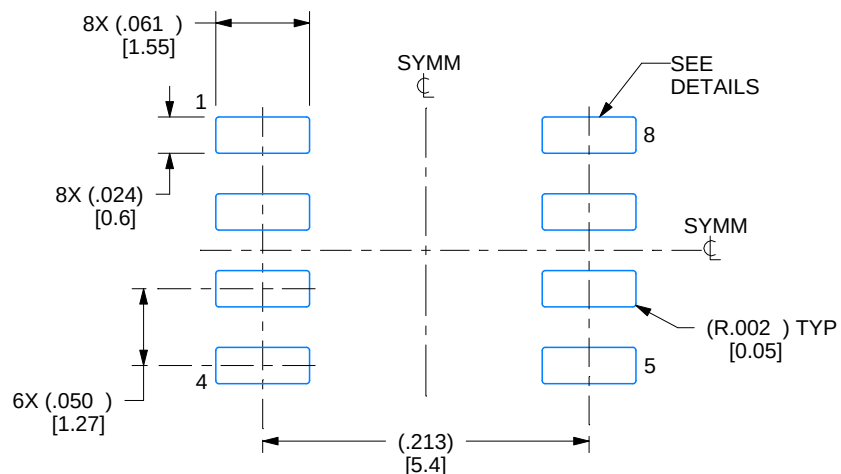
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

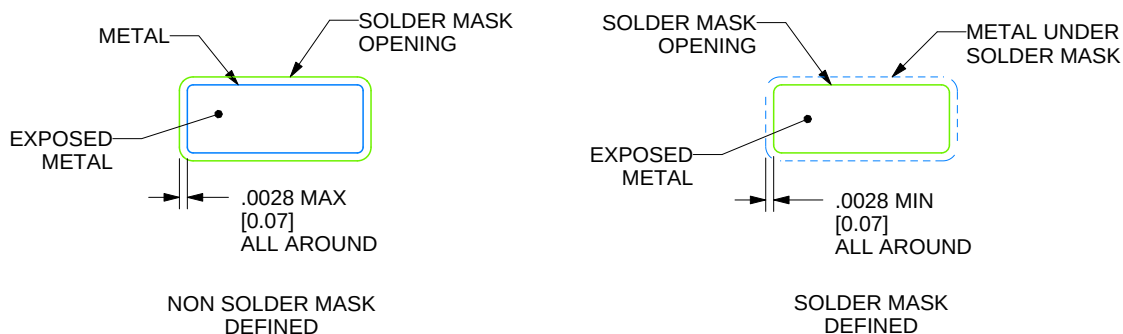
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

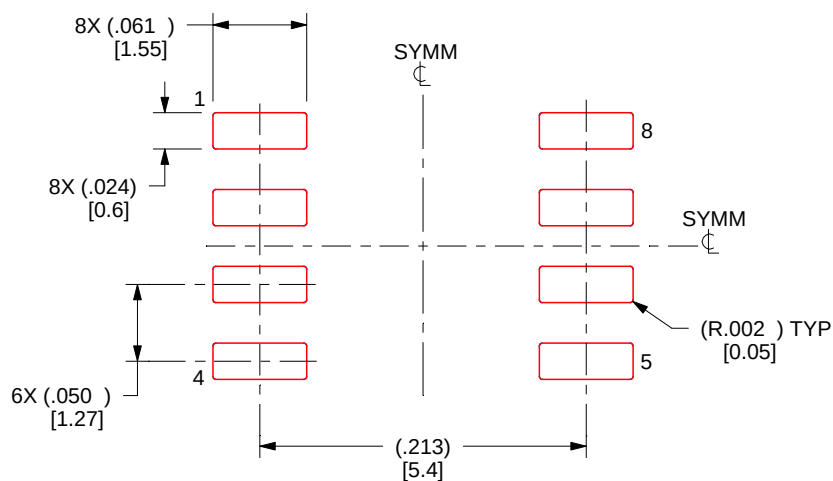
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

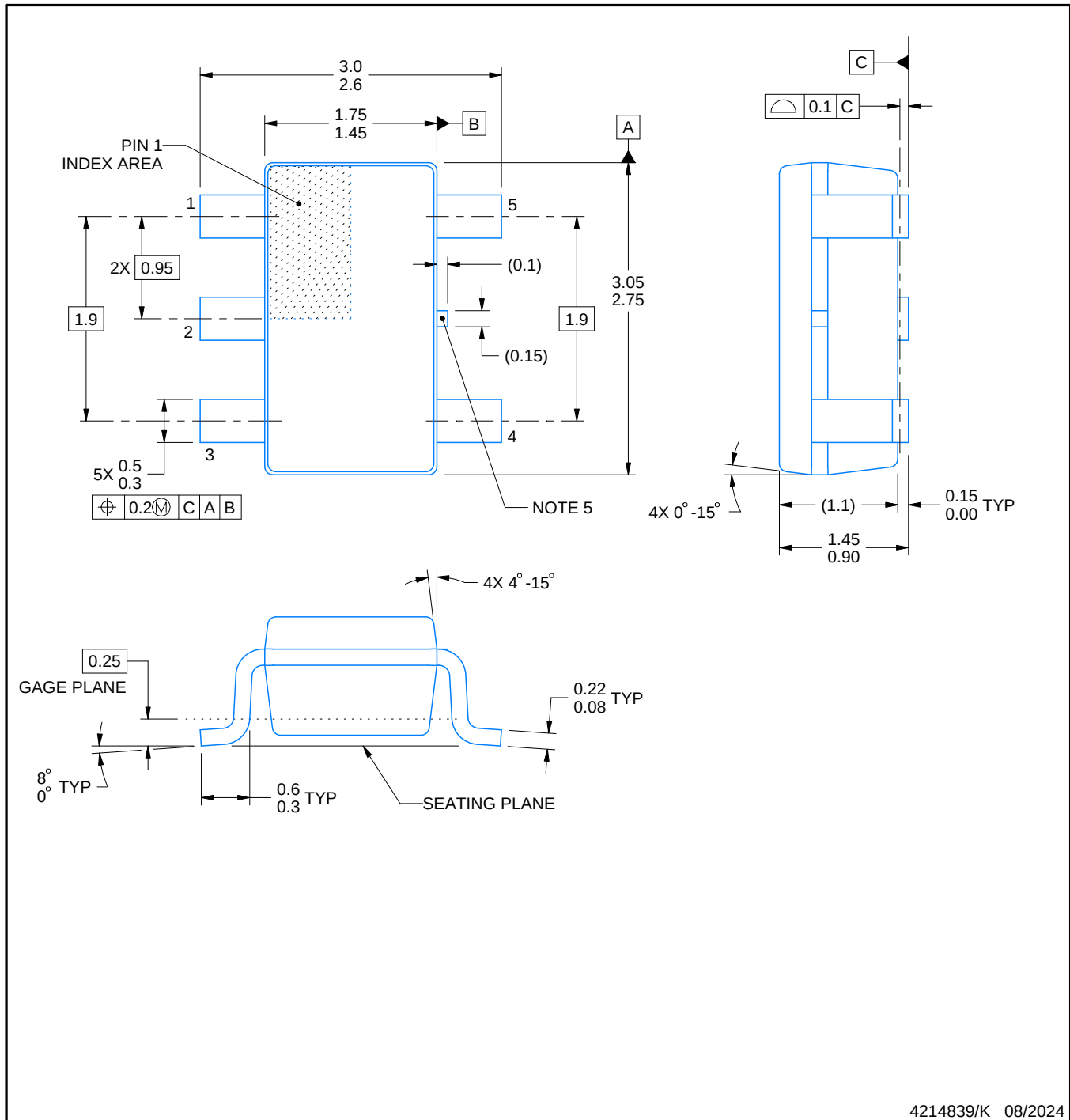
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DBV0005A**PACKAGE OUTLINE****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR

**NOTES:**

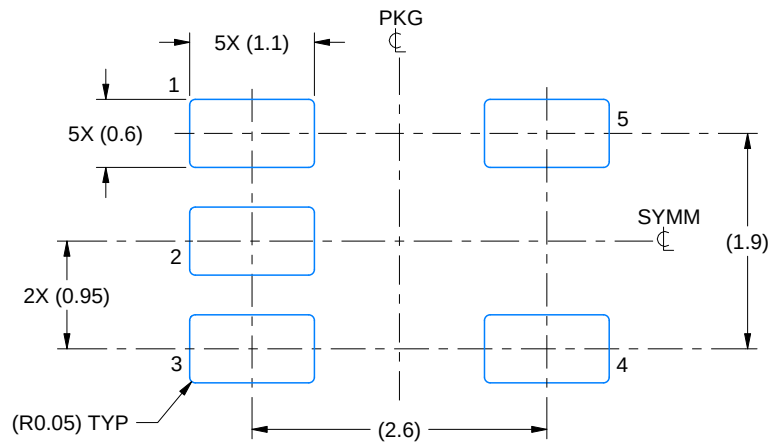
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

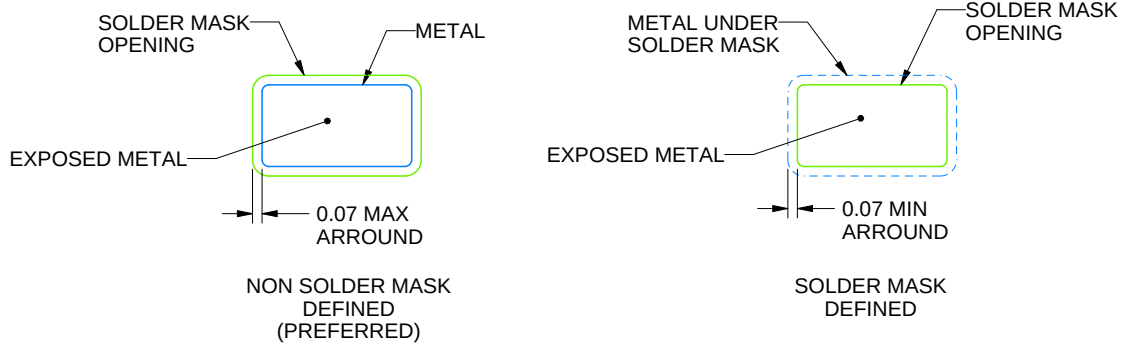
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

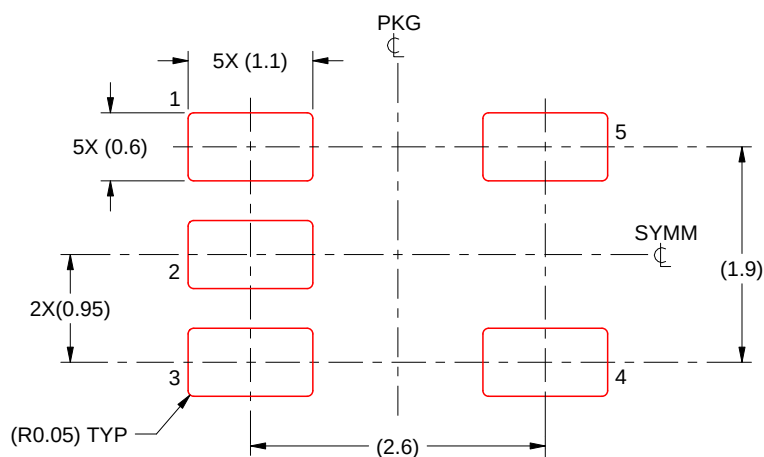
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



VSSOP - 1.1 mm max height

Technical drawing of a connector assembly, showing top, side, and detail views with dimensions and callouts.

Top View:

- Overall width: 5.05 TYP, 4.75
- Overall height: 3.1, 2.9, NOTE 3
- Pin 1 Index Area: Indicated by a dashed circle.
- Pin 1: Dimension 1
- Pin 2: Dimension 2
- Pin 3: Dimension 3
- Pin 4: Dimension 4
- Pin 5: Dimension 5
- Pin 6: Dimension 6
- Pin 7: Dimension 7
- Pin 8: Dimension 8
- Pin 9: Dimension 9
- Pin 10: Dimension 10
- Pin 11: Dimension 11
- Pin 12: Dimension 12
- Pin 13: Dimension 13
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- Pin 246: Dimension 246
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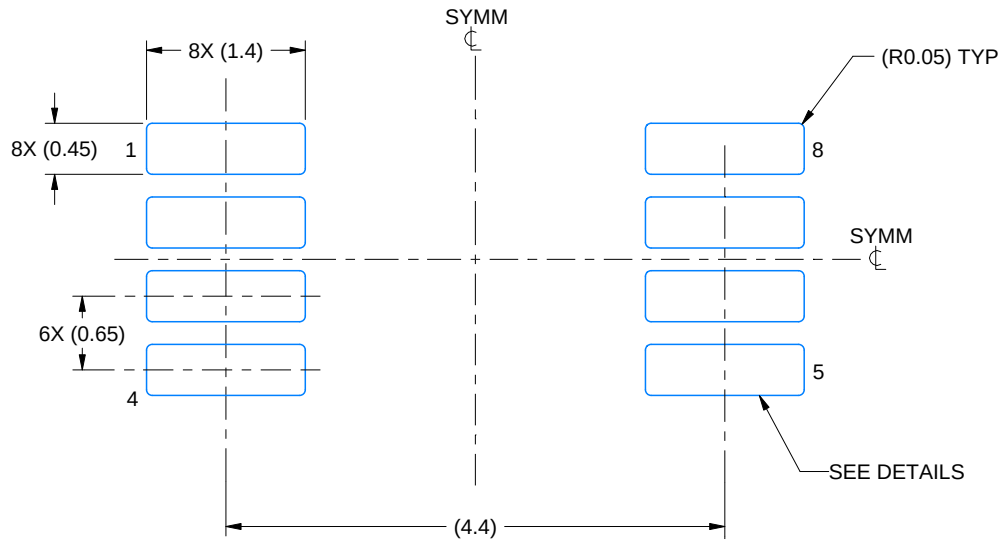
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EXAMPLE BOARD LAYOUT

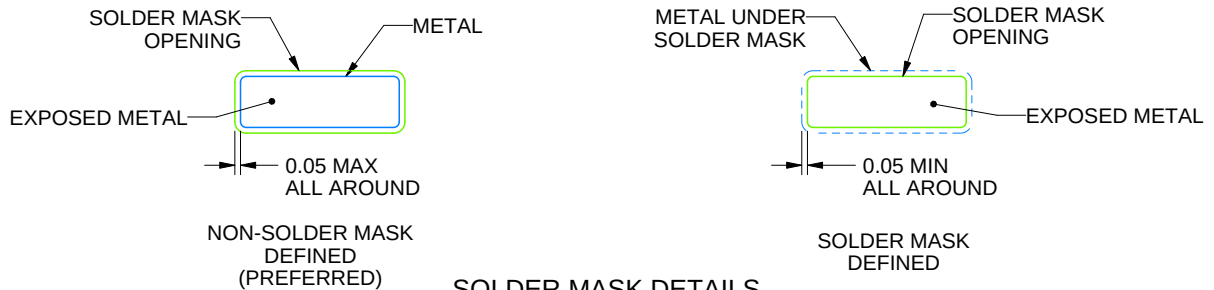
DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

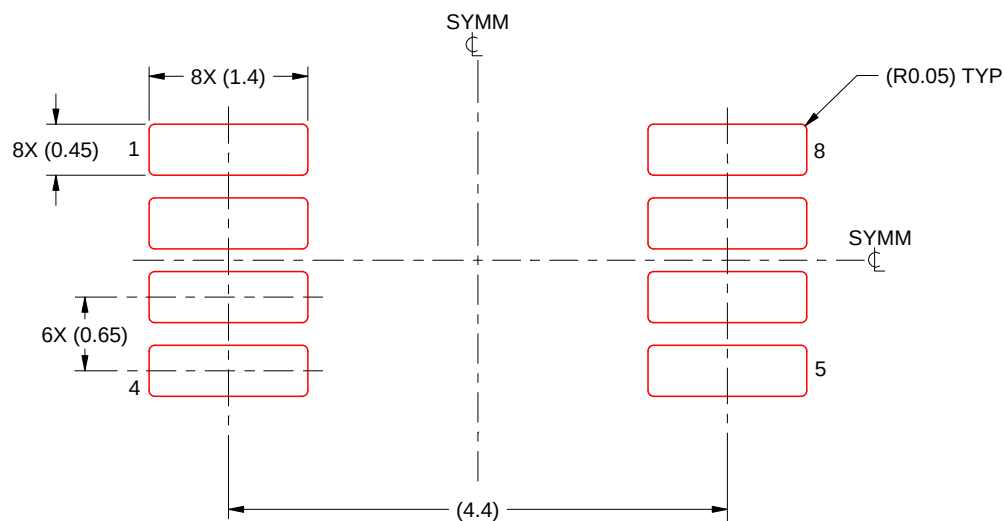
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

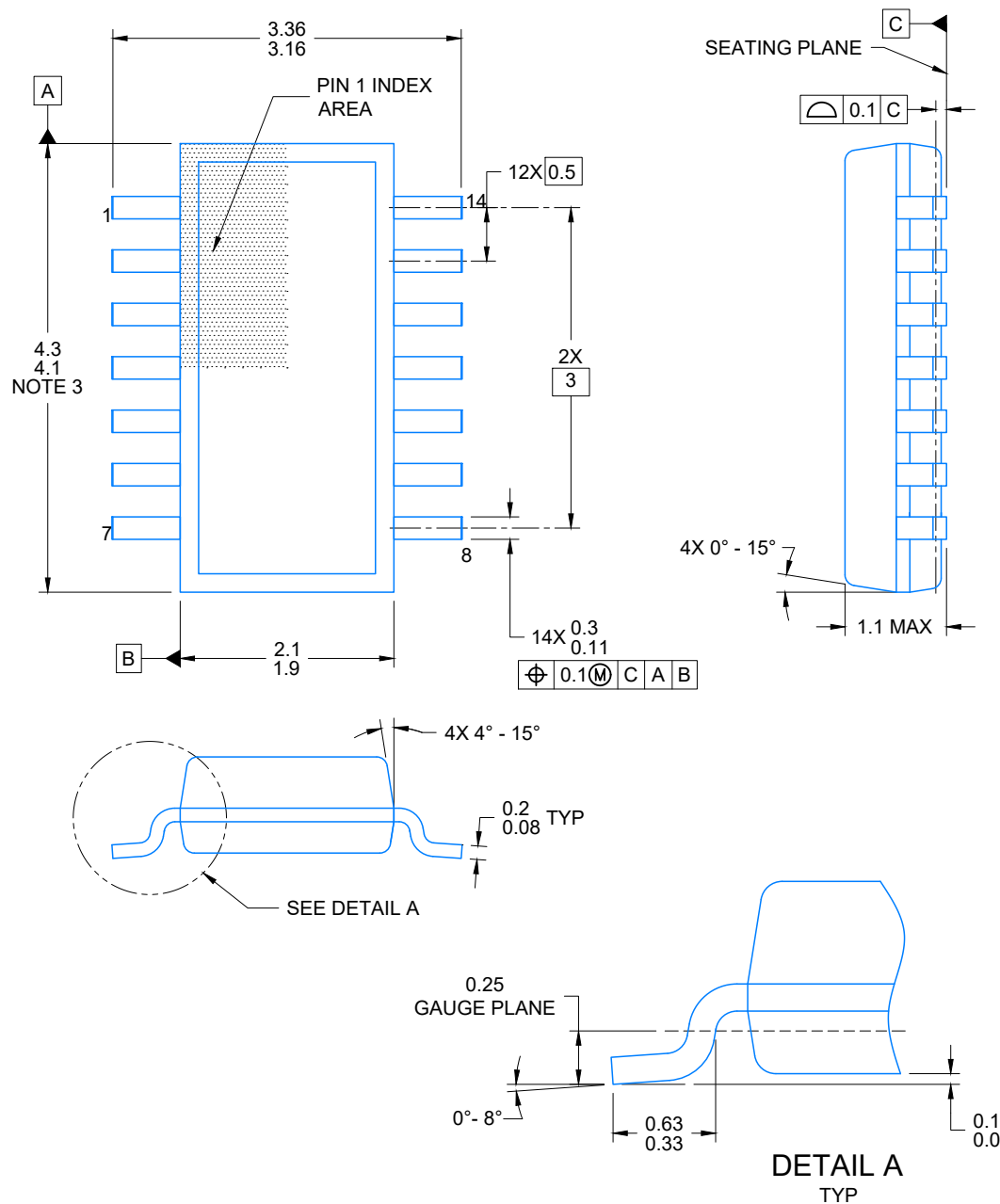


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

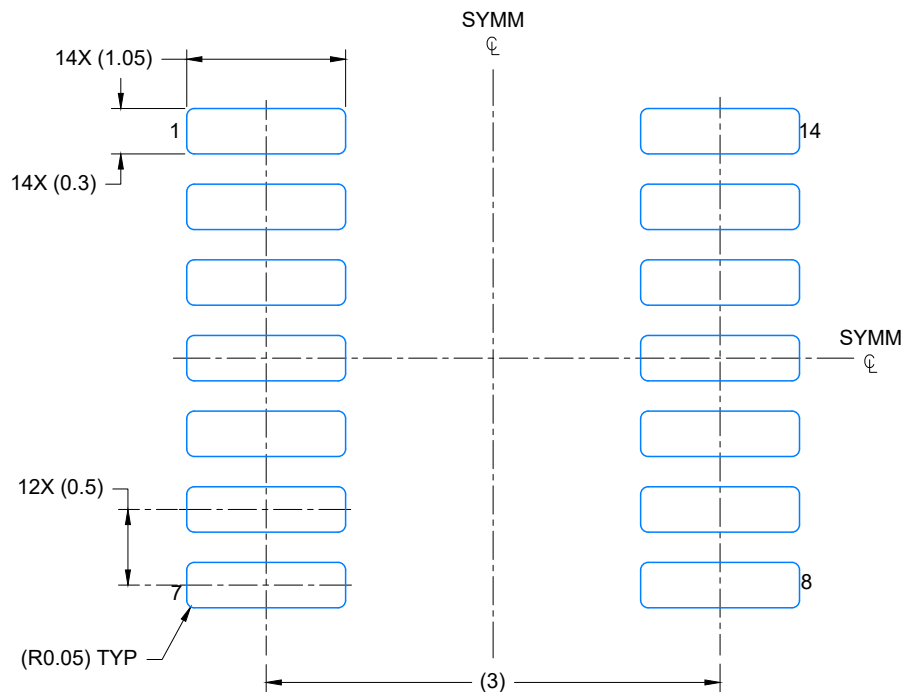
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



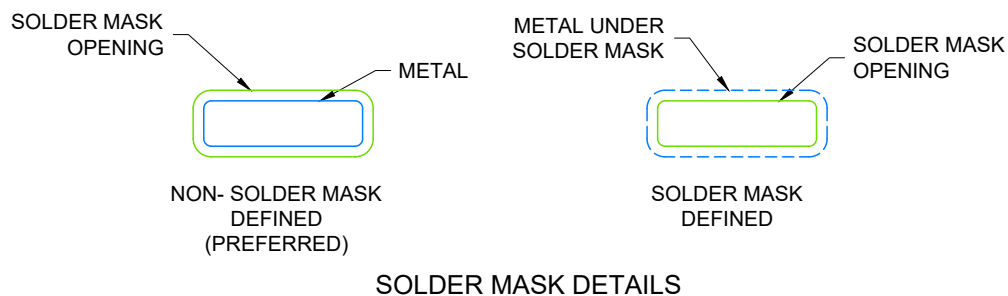
4224643/D 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



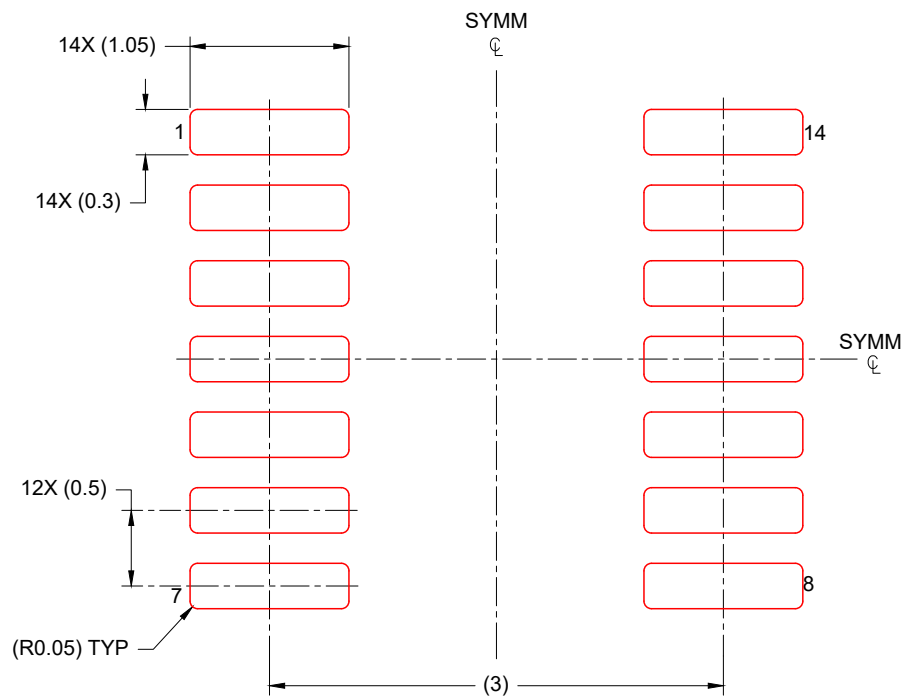
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224643/D 07/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224643/D 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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