TPS6123x 具有 5A 开关的高效同步升压转换器

1 特性

- 输入电压范围：2.3V 至 5.5V
- 输出电压范围：2.5V 至 5.5V
- 同步升压转换器效率高达 96%
- 输出电流 2.1A 的 3.3V 至 5V 电源转换
- 带有可调阀值/滞后的输入电源电压监控器
- 用于在轻载时实现高效率的省电模式
- 关断期间负载断开
- 输出过压保护
- 可编程软启动
- 电源正常输出
- 2MHz 开关频率
- 输出电容器放电 (TPS61231)
- 3mm x 3mm x 0.9mm 超薄小外形尺寸无引线 (VSON) 封装

2 应用范围

- 低压锂离子电池供电类产品
- USB 电源
- 平板电脑
- 移动电源、备用电池
- 工业仪表计量设备

3 说明

TPS6123x 器件系列是一款采用紧凑解决方案尺寸的高效同步升压转换器。 它针对由单节锂离子电池或 3.3V 稳压电源轨供电的产品进行了优化。集成电路 (IC) 中集成了一个 5A 开关，并且能够在由 3.3V 输入电源供电，输出电压为 5V 时传送高达 2.1A 的输出电流。 此器件基于准恒定接通时间谷值电流模式控制机制。 典型运行频率为 2MHZ，这样可使用小型电感器和电容器来实现小解决方案尺寸。 TPS61230 和 TPS61231 通过一个外部电阻分压器提供可调输出电压，而 TPS61232 提供 5V 的固定输出电压。

轻负载期间，TPS6123x 自动进入省电模式，以最低静态电流实现最大效率。 在关断期间，负载完全从输入上断开，并且输入流耗减少至 1.5μA（典型值）。 此器件集成一个精密低功率 EN 比较器。 EN 阀值以及使能比较器的滞后可由外部电阻器调节，并且支持应用专用系统加电和断电要求。 还内置了其他诸如输出过压保护、热关断保护和电源正常输出等特性。

此器件采用 3mm x 3mm x 0.9mm VSON 封装。

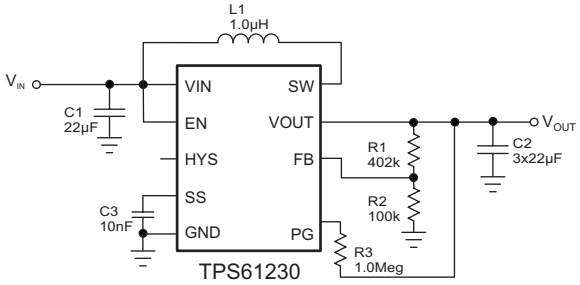
器件信息(1)

部件号	封装	封装尺寸（标称值）
TPS61230	超薄小外形尺寸无引线 (VSON) (10)	3.00mm x 3.00mm
TPS61231(2)		
TPS61232		

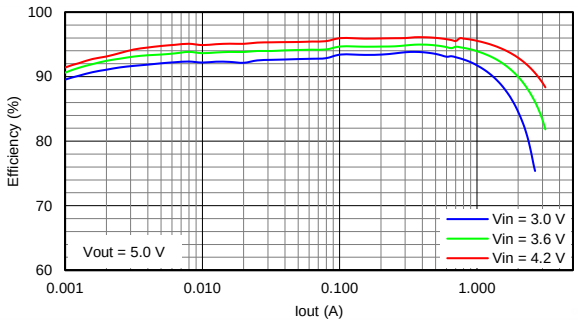
(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

(2) 产品预览。 有关更多信息，请联系 TI 厂家

TPS61230 典型应用



TPS61230 典型应用效率



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4 修订历史记录

Changes from Revision B (June 2014) to Revision C — **Page**

- 已更改 Electrical Characteristics in the I_Q row; V_{OUT} = 3.5 V to V_{OUT} = No Supply ... 5

Changes from Revision A (March 2014) to Revision B — **Page**

- 已将 TPS61232 添加到数据表 ... 1
- 已更改器件信息 ... 1
- Changed the Device Comparison Table ... 3
- Changed the Handling Ratings table ... 4

Changes from Original (September 2013) to Revision A — **Page**

- 已从数据表中删除 TPS61232 ... 1
- 已将数据表更改为全新的 TI 格式 ... 1
- 已将说明从：输入流耗减少至 0.5μA（典型值）更改为：输入流耗减少至 1.5μA（典型值） ... 1
- Changed the Functional Block Diagram. Removed Note 2 ... 8
- Deleted the Programming The Output Voltage section ... 13
- Changed 图 14 label From: Startup (A) To: Startup (Ω) ... 15

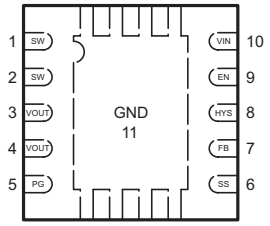
5 Device Comparison Table

PART NUMBER	OUTPUT VOLTAGE	OUTPUT DISCHARGE
TPS61230DRC	Adjustable	No
TPS61231DRC(1)	Adjustable	Yes
TPS61232DRC	5-V fixed output	No

(1) Preview product. Contact TI factory for more information

6 Pin Configuration and Functions

11-PIN VSON
DRC PACKAGE
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
SW	1,2	PWR	The switch pin of the converter. It is connected to the drain of the internal Power MOSFETs.
VOUT	3,4	PWR	Boost converter output pin.
PG	5	OUT	Power Good open drain output. Can be left floating if not used.
SS	6	IN	Soft startup pin. A soft startup capacitor connects to this pin to set the soft start time.
FB	7	IN	Voltage feedback of adjustable versions. Must be connected to VOUT on fixed output voltage version.
HYS	8	OUT	EN hysteresis program pin. See the application section for details. Can be left floating if not used.
EN	9	IN	Enable logic input. Logic HIGH enables the device. Logic LOW disables the device and turns it into shutdown mode. This pin must be terminated.
VIN	10	IN	Supply voltage pin.
GND	11	PWR	Ground pin.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range at pins(2)	EN, FB, PG, SS, HYS, VIN, VOUT, SW	–0.3	7	V
Operating junction temperature range, T_J		–40	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground pin.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		-65	150	°C
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–2	2	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–500	500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
V_{IN}	Supply voltage at VIN pin	2.3		5.5	V
I_{SINK_PG}	Sink current at PG pin			500	µA
V_{PG}	Pull-up resistor voltage			5.5	V
T_J	Operating junction temperature	-40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS6123x	UNIT
		DRC (11 PINS)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	57.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	26.6	
ψ_{JT}	Junction-to-top characterization parameter	0.8	
ψ_{JB}	Junction-to-board characterization parameter	23.8	
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	4.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

T_J = –40°C to 125°C and V_{IN} = 3.6 V. Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{UVLO}	Input under voltage lockout	V_{IN} falling		2.0	2.1	V
		V_{IN} rising		2.1	2.2	
I_Q	Quiescent current into VIN	IC enabled, No load, No switching V_{OUT} = 5 V, T_J = –40 °C to 85°C		35	60	µA
		IC enabled, No load V_{IN} = 4.2 V, V_{OUT} = No supply, T_J = –40 °C to 85°C		200	230	
I_{SD}	Shutdown current into VIN	0 V ≤ V_{EN} ≤ 0.4 V, V_{IN} = 2.3 V to 5.5 V, T_J = -40 °C to 85°C		1.5	6	µA
	Leakage current from SW to VOUT	V_{EN} = 0 V, V_{OUT} = 0 V; V_{SW} = V_{IN} = 3.6 V			2.5	µA
OUTPUT						
V_{OUT}	Output voltage range		2.5		5.5	V
V_{OUT}	Output voltage accuracy, TPS61232	PWM mode	4.9	5.0	5.1	V
V_{OUT}	Output voltage accuracy, TPS61232	PFM mode(1)		5.035		V
V_{FB}	Feedback voltage, TPS61230 and TPS61231	PWM mode	0.985	1	1.015	V
		PFM mode(1)		1.007		
	FB pin leakage current	V_{FB} = 1 V			100	nA
R_{DIS}	Output discharge resistor TPS61231	V_{OUT} = 5 V		200		Ω
V_{OVP}	Over voltage protection DC threshold	V_{OUT} rising	5.7	6	6.2	V
	Over voltage protection hysteresis	V_{OUT} falling below V_{OVP}		0.15		
I_{SS}	Bias current in soft start phase	After pre-charge phase		5		µA
	Line regulation	I_{OUT} = 1 A, V_{IN} = 2.3 V to 4.5 V		0.06		%/V
	Load regulation	I_{OUT} = 0.5 A to 2 A		0.15		%/A
LOGIC INTERFACE						
$V_{TH\_EN\_ON}$	EN pin threshold rising	V_{IN} = 2.3 V to 5.5 V	1.15	1.19	1.23	V
$V_{TH\_EN\_OFF}$	EN pin threshold falling	V_{IN} = 2.3 V to 5.5 V	1.11	1.14	1.18	V
V_{OL_HYS}	HYS pin low level voltage	I_{SINK_HYS} = 1 mA, V_{EN} = 1.1 V			0.7	V
V_{TH_PG}	Power good DC threshold	V_{OUT} rising, referenced to $V_{OUT\_NOMINAL}$	93%	95%	99%	
		V_{OUT} falling referenced to $V_{OUT\_NOMINAL}$	87%	90%	93%	
V_{OL_PG}	PG pin low level voltage	I_{SINK_PG} = 500 µA			0.4	V
POWER STAGE						
I_{LIM_SW}	Switch valley current limit		4.0	5.0	6.0	A
I_{LIM_Pre}	Precharge current limit	V_{OUT} = 5 V	2.0	2.8	3.5	A
		V_{OUT} = 3.5 V	1.8	2.6	3.3	
		V_{OUT} = 0 V	0.4	0.55	0.7	
$R_{DS(on)}$	High side MOSFET on resistance	V_{OUT} = 5 V		50	75	mΩ
	Low side MOSFET on resistance	V_{OUT} = 5 V		50	75	
T_{JSD}	Thermal shutdown threshold	T_J rising		150		°C
	Thermal shutdown hysteresis	T_J falling below T_{JSD}		20		

(1) L = 1 µH, C_{OUT} = 20 µF (effective capacitance value)

7.6 Typical Characteristics

V_{IN} = 3.6 V, V_{OUT} = 5.0 V, T_J = -40°C to 125 °C, unless otherwise noted.

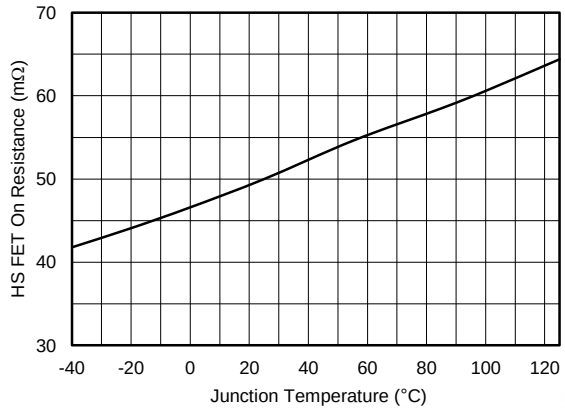


图 1. High-Side MOSFET On Resistance vs Junction Temperature

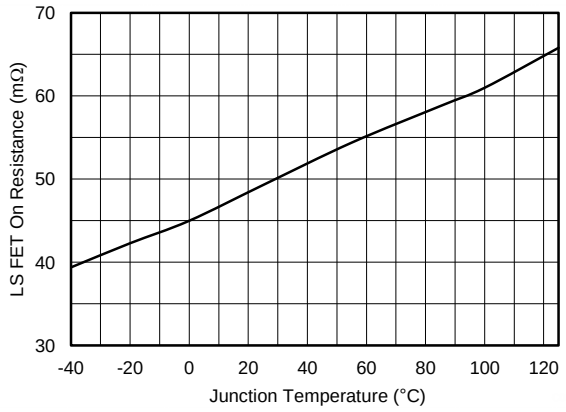


图 2. Low-Side MOSFET On Resistance vs Junction Temperature

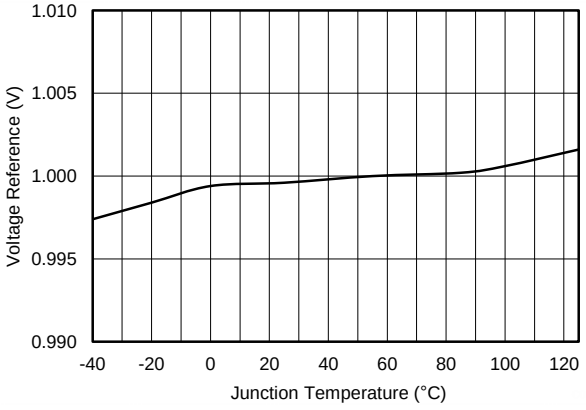


图 3. Voltage Reference vs Junction Temperature

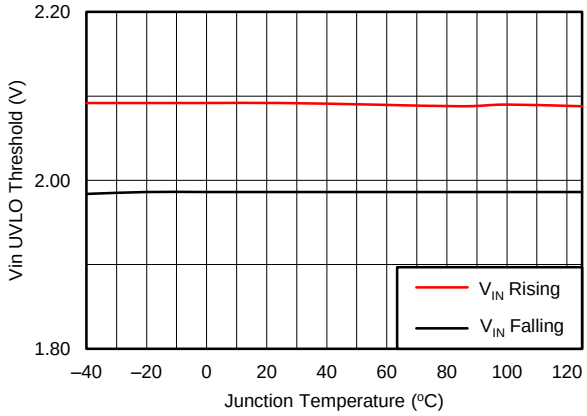


图 4. Vin UVLO Threshold vs Junction Temperature

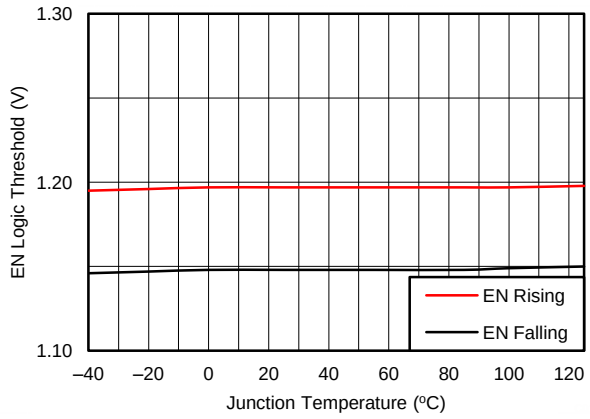


图 5. EN Logic Threshold vs Junction Temperature

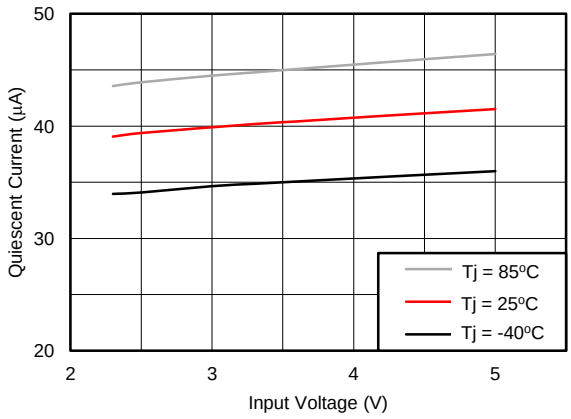


图 6. Quiescent Current vs Input Voltage (Boost Mode)

Typical Characteristics (接下页)

V_{IN} = 3.6 V, V_{OUT} = 5.0 V, T_J = -40°C to 125 °C, unless otherwise noted.

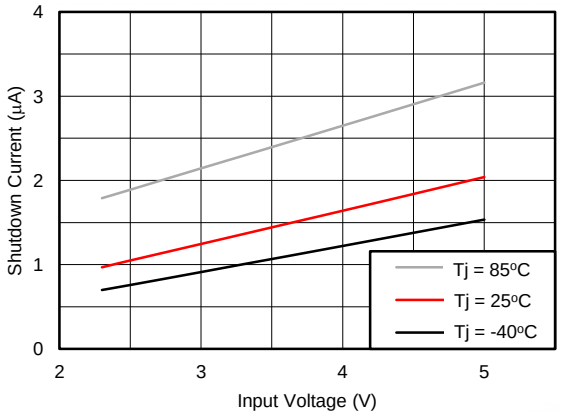


图 7. Shutdown Current vs Input Voltage (Boost Mode)

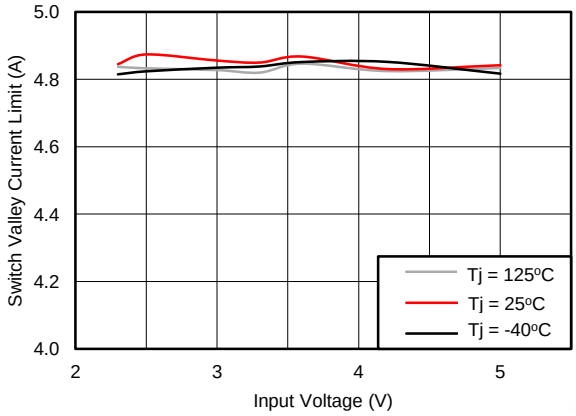


图 8. Switch Valley Current Limit vs Input Voltage (Boost Mode)

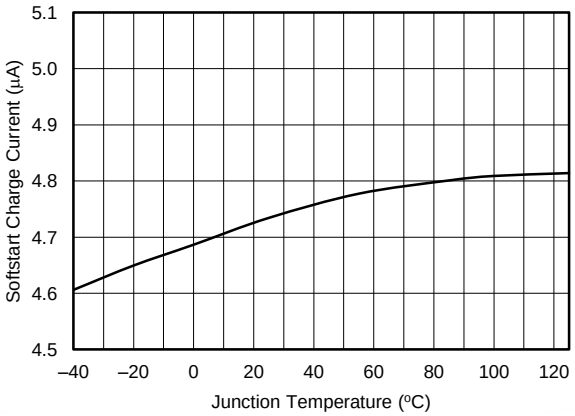


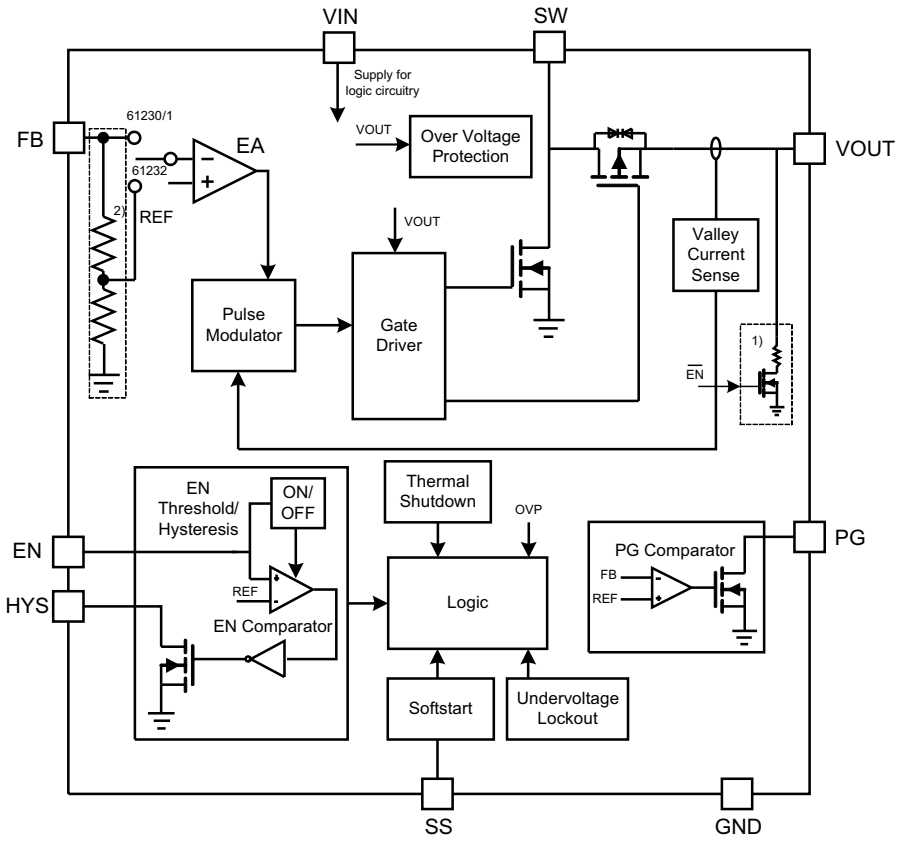
图 9. Soft Start Charge Current vs Junction Temperature

8 Detailed Description

8.1 Overview

The TPS6123x synchronous step-up converter typically operates at a quasi-constant 2-MHz frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents, the TPS6123x converter operates in power-save mode with pulse frequency modulation (PFM). The converter uses a novel quasi-constant on-time valley current mode control scheme which provides excellent transient line / load response with minimal output capacitance. Internal loop compensation simplifies the design process while minimizing the number of external components. The TPS6123x device can smoothly transit in and out of zero duty cycle mode (high side FET full on). Therefore the output can be kept as close as possible to its regulation limits even though the converter is subject to an input voltage that tends to be excessive.

8.2 Functional Block Diagram



(1) Output discharge block is implemented in TPS61231 only.

(2) Internal resistor divider is implemented in TPS61232 only. For adjustable output versions, the FB pin is directly connected to the negative pin of the EA.

8.3 Feature Description

8.3.1 Startup

In boost mode (PWM or PFM), the rectifying switch is turned on first until the output capacitor is charged to 0.5 V with the current limit of 550 mA after the device is enabled. Then, the output capacitor is continuously charged to a value close to the input voltage. This is called the pre-charge phase. During the pre-charge phase, the output current is limited by the pre-charge current limit of the high side rectifying switch and the SS pin voltage follows the FB voltage (in the TPS61232, the SS pin follows the internal FB voltage). Once the output capacitor has been biased to the input voltage, the device starts switching. This is called the soft start phase. During the soft

Feature Description (接下页)

start phase, the SS pin voltage limits the FB pin voltage, and the output voltage rising slope follows the SS pin voltage slope. The capacitor connected to the SS pin is charged by the internal bias current of I_{SS}, giving the time of the soft start phase shown in 公式 1. The larger the soft start capacitor, the longer the soft start phase time. Leaving the SS pin floating sets the minimum soft startup phase time. The device finishes the soft start phase and operates normally when the nominal output voltage is reached.

$$t_{SS} = \frac{C_{SS}}{5\,\mu A} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \times V_{REF} \quad (1)$$

The SS pin voltage is discharged in the cases when the device gets disabled by the EN pin, thermal shutdown and undervoltage lockout. The SS pin may be left floating to disable the soft start phase and start up with the fastest time. In zero duty cycle mode, only the pre-charge phase works during startup.

8.3.2 Current Limit Operation

The device employs a valley current sensing scheme. Switch valley current limit detection occurs during the off time through sensing of the voltage drop across the synchronous rectifier. If the current is above the valley current limit level when it is time to turn off the synchronous rectifier, the device instead keeps the synchronous rectifier on until its current decreases below the valley current limit level. The maximum continuous output current $I_{OUT(MAX)}$, before entering switch valley current limit operation, is defined by 公式 2.

$$I_{OUT(MAX)} = (1-D) \times \left(I_{LIM\_SW} + \frac{1}{2}\Delta I_L\right)$$

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

$$\Delta I_L = \frac{V_{IN}}{L} \times \frac{D}{f_{SW}} \quad (2)$$

Where

I_{LIM_SW} = Switch valley current limit
L = Inductor value
f_{SW} = Switching frequency

When the switch current limit is reached, the output voltage decreases from further load increase. The switch valley current limit works in PWM, PFM and Zero Duty Cycle Mode operations.

Another current limit scheme, pre-charge current limit, I_{LIM_Pre} is implemented. Pre-charge current limit detection works when $V_{OUT} < V_{OUT\_NOM}$ and $V_{OUT} < V_{IN}$. It can happen when the device is in the pre-charge phase or an over load condition. It impacts the minimum load resistance at startup as shown in 图 14 and 图 27.

8.3.3 Enable/Disable

The EN pin is connected to an ON/OFF detector (ON/OFF) and an input of the Enable Comparator, shown in the functional block diagram. With a voltage level of 0.4 V or less at the EN pin, the ON/OFF detector turns the device into Shutdown mode and the quiescent current is reduced to typically 1.5 uA. In this mode, the EN comparator and the entire internal control circuitry are switched off. A voltage level of typically 0.9 V at the EN pin triggers the ON/OFF detector and activates the internal reference, the EN comparator and the UVLO comparator. Once the ON/OFF detector has tripped, the quiescent current into the VIN pin is typically 1.5 µA.

The TPS6123x starts regulation once the voltage at the EN pin trips the threshold $V_{EN\_TH\_ON}$ and the VIN pin voltage is above the UVLO threshold. The device enters startup and ramps up the output voltage. The TPS6123x stops regulation once the voltage on the EN pin falls blow the threshold $V_{EN\_TH\_OFF}$ or the VIN pin voltage falls below the UVLO threshold. For proper operation, The EN pin must be terminated and must not be left floating. An external logic signal applied directly to the EN pin can enable/disable the device. The device can be driven into shutdown mode by pulling the EN pin to GND. In this mode, true load disconnect between the battery and load prevents current flow from V_{IN} to V_{OUT}, as well as reverse flow from V_{OUT} to V_{IN}.

Feature Description (接下页)

8.3.4 Undervoltage Lockout

An under voltage lockout is implemented to avoid mis-operation of the device at low input voltages. It shuts down the device with voltages lower than V_{UVLO}.

Use the HYS pin to configure a new undervoltage lockout threshold and hysteresis shown in 图 10 and 公式 3. The new thresholds must be higher than V_{UVLO}; otherwise it does not work. The devices holds the HYS pin low until the EN voltage rises above $V_{EN\_TH\_ON}$. Then, the HYS pin goes high impedance.

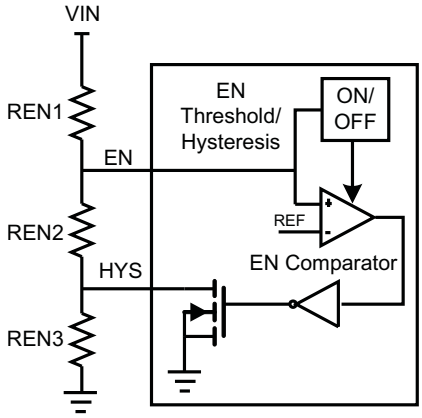


图 10. EN Comparator threshold and hysteresis setting

$$V_{IN\_OFF} = V_{TH\_EN\_OFF} \times \left(1 + \frac{REN1}{REN2 + REN3}\right) = 1.14V \times \left(1 + \frac{REN1}{REN2 + REN3}\right)$$
$$V_{IN\_ON} = V_{TH\_EN\_ON} \times \left(1 + \frac{REN1}{REN2}\right) = 1.19V \times \left(1 + \frac{REN1}{REN2}\right) \quad (3)$$

8.3.5 Output Capacitor Discharge, TPS61231

To make sure the device starts up under defined conditions, the output capacitor of the TPS61231 gets discharged by the VOUT pin with a typical discharge resistor of R_{DIS} in the cases when the device gets disabled by the EN pin, thermal shutdown, and undervoltage lockout.

8.3.6 Power Good Output

The PG output is low when the output voltage is below 90% of its nominal value. The PG pin becomes high impedance once the output is higher than 95% of its nominal voltage. The PG pin is an open drain output and is specified to sink up to 500 µA. This PG output requires a pull-up resistor that cannot be connected to any voltage higher than 5.5 V. PG is held low when the device is disabled by the EN pin and thermal shutdown.

8.3.7 Over Voltage Protection

The device stops switching as soon as the output voltage exceeds V_{OVP}. When the output voltage falls 0.15V below the OVP threshold, the device resumes normal operation until the output voltage exceeds the OVP threshold again.

8.3.8 Thermal Shutdown

The device goes into thermal shutdown and stops switching once the junction temperature exceeds T_{JSD}. Once the junction temperature falls below the threshold, it returns to normal operation automatically.

8.4 Device Functional Modes

The TPS6123x boost converter family has three operation modes, as shown in 表 1.

表 1. Operation Mode Description

MODE	DESCRIPTION	CONDITION
PWM	Boost in normal switching operation	$V_{IN} < V_{OUT}$ + 0.2 V, heavy load
PFM	Boost in power save operation	$V_{IN} < V_{OUT}$ + 0.2 V, light load
Zero Duty Cycle	Zero duty cycle operation	$V_{OUT} < V_{IN} \le V_{OUT}$ + 0.24 V and $V_{OUT} \ge V_{OUT\_NOM}$

8.4.1 Boost Normal Mode

The TPS6123x boost converter family typically operates at a quasi-constant 2-MHz frequency pulse width modulation (PWM) at moderate to heavy load currents. Based on the V_{IN}/V_{OUT} ratio, a simple circuit predicts the required on-time. At the beginning of the switching cycle, the low-side N-MOS switch, shown in the functional block diagram, is turned on and the inductor current ramps up to a peak current that is defined by the on-time and the inductance. In the second phase, once this peak current is reached, the current comparator trips, the on-timer is reset turning off the low-side N-MOS switch and turning on the high-side rectifying switch. The current through the inductor then decays to an internally set valley current. Once this occurs, the on-timer is set to turn the boost switch back on again and the cycle is repeated.

8.4.2 Boost Power Save Mode

The device integrates a power save mode with pulse frequency modulation (PFM) to improve efficiency at light load. In power save mode, the device only switches when the output voltage trips below a set threshold voltage. It ramps up the output with several pulses and enters the power save mode when the output voltage exceeds the set threshold voltage. PFM is left and PWM mode entered when the inductor current becomes discontinuous. The DC output voltage in PFM mode rises above the nominal output voltage in PWM mode by 0.7%.

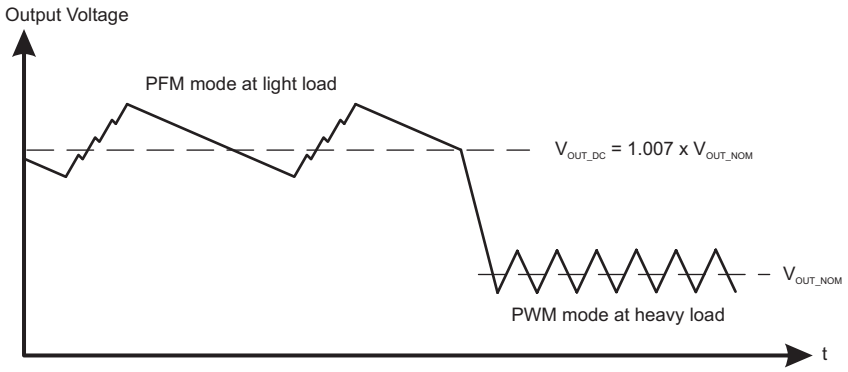


图 11. Output Voltage in PFM/PWM Mode

8.4.3 Zero Duty Cycle Mode

When the input voltage is lower than V_{OUT} + 0.24 V and V_{OUT} is higher than the nominal output voltage, the device automatically changes to a Zero Duty Cycle Mode. In Zero Duty Cycle Mode, the rectifying switch is constantly turned on and the low side switch is turned off. The output voltage in this mode depends on the resistance between the input and the output, calculated as:

$$V_{OUT} = V_{IN} - I_{OUT} \times (R_{DS(on)} + R_L) \quad (4)$$

9 Applications and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The devices are designed to operate from an input voltage supply range between 2.3 V and 5.5 V with a maximum output current of 2.1 A. The devices operate in PWM mode for medium to heavy load conditions and in power save mode at light load currents. In PWM mode the TPS6123x converter operates with the nominal switching frequency of 2 MHz which provides a controlled frequency variation over the input voltage range. As the load current decreases, the converter enters power save mode, reducing the switching frequency and minimizing the IC quiescent current to achieve high efficiency over the entire load current range. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. See the *相关文档* section for additional documentation.

9.2 Typical Applications

9.2.1 TPS61230 2.3-V to 5.5-V Input, 5-V Output Converter

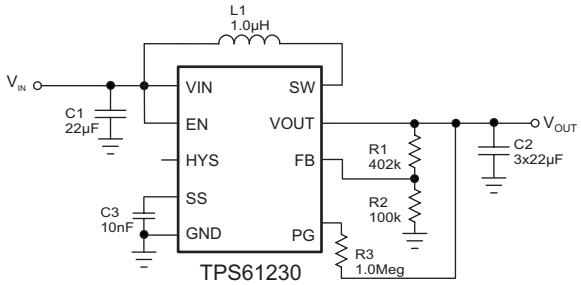


图 12. TPS61230 5-V Output Typical Application

9.2.1.1 TPS61230 5-V Output Design Requirements

Use the following typical application design procedure to select external components values for the TPS61230 device.

表 2. TPS61230 5-V Output Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input Voltage Range	2.3 V to 5.5 V
Output Voltage	5.0 V
Output Voltage Ripple	±3% V_{OUT}
Transient Response	±10% V_{OUT}
Input Voltage Ripple	±200 mV
Output Current Rating	2.1 A
Operating Frequency	2 MHz

9.2.1.2 TPS61230 5-V Detailed Design Procedure

表 3. TPS61230 5-V Output List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
L1	1.0 µH, power inductor, XFL4020-102MEB	Coilcraft
C1	2 µF 6.3 V, 0805, X5R ceramic, GRM21BR60J226ME39	Murata
C2	3 × 22 µF 10 V, 0805, X5R ceramic, LMK212BBJ226MG	YUDEN
C3	10 nF, X7R ceramic	Murata
R1	402 k, resistor, chip, 1/10W, 1%	Rohm
R2	100 k, resistor, chip, 1/10W, 1%	Rohm

9.2.1.2.1 Programming the Output Voltage

The TPS6123x device family's output voltage need to be programmed via an external voltage divider to set the desired output voltage.

An external resistor divider is used, as shown in 公式 5. By selecting R1 and R2, the output voltage is programmed to the desired value. When the output voltage is regulated, the typical voltage at the FB pin is V_{FB}. The following equation can be used to calculate R1 and R2.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 1V \times \left(1 + \frac{R1}{R2}\right) \quad (5)$$

For best accuracy, R2 should be kept smaller than 100 kΩ to ensure that the current following through R2 is at least 100 times larger than FB pin leakage current. Changing R2 towards a lower value increases the robustness against noise injection. Changing the R2 towards higher values reduces the quiescent current for achieving highest efficiency at low load currents.

For the fixed output voltage version, TPS61232, the FB pin must be tied to the output directly.

9.2.1.2.2 Inductor and Capacitor Selection

The second step is the selection of the inductor and capacitor components. To simplify this process, 表 4 outlines possible inductor and output capacitor value combinations.

表 4. Inductor and Output Capacitor Combinations

L (µH)(1)	C_{OUT} (µF)(2)			
	10	20	47	100
0.47		√	√	√
1.0		√(3)	√	√
1.5				

(1) This is the nominal inductance of inductor. Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by -30%.
(2) This is the effective capacitance of output capacitors. A higher nominal value is required.
(3) Typical application configuration. Other check mark indicates alternative filter combinations.

9.2.1.2.2.1 Inductor Selection

A boost converter requires two main passive components for storing energy during the conversion, an inductor and an output capacitor. It is advisable to select an inductor with a saturation current rating higher than the possible peak current flowing through the power switches. The inductor peak current varies as a function of the load, the input and output voltages and is estimated using 公式 6.

$$I_{L(PEAK)} = \frac{I_{OUT}}{(1-D) \times \eta} + \frac{1}{2} \times \frac{V_{IN} \times D}{L \times f_{SW}} \quad (6)$$

Where

η = Power conversion estimated efficiency

Selecting an inductor with insufficient saturation performance can lead to excessive peak current in the converter. This could eventually harm the device and reduce reliability. It's recommended to choose the saturation current for the inductor 20%~30% higher than the $I_{L(PEAK)}$, from 公式 6. The following inductors are recommended to be used in designs.

表 5. List of Inductors

INDUCTANCE [µH]	CURRENT RATING [A]	DC RESISTANCE [mΩ]	PART NUMBER	MANUFACTURER
1.0	5.4	10.8	XFL4020-102ME	Coilcraft
1.0	7.5	9	LQH6PPN1R0	muRata
0.47	6.6	7.6	XFL4015-471ME	Coilcraft

9.2.1.2.2.2 Output Capacitor Selection

For the output capacitor, it is recommended to use small X5R or X7R ceramic capacitors placed as close as possible to the VOUT and GND pins of the IC. If, for any reason, the application requires the use of large capacitors which cannot be placed close to the IC, using a smaller ceramic capacitor of 1 µF in parallel to the large one is highly recommended. This small capacitor should be placed as close as possible to the VOUT and GND pins of the IC.

Care must be taken when evaluating a capacitor's derating under bias. The bias can significantly reduce capacitance. Ceramic capacitors can loss as much as 50% of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance.

The ESR impact on the output ripple must be considered as well, if tantalum or electrolytic capacitors are used. Assuming there is enough capacitance such that the ripple due to the capacitance can be ignored, the ESR needed to limit the V_{Ripple} is:

$$V_{Ripple(ESR)} = I_{L(PEAK)} \times ESR \tag{7}$$

9.2.1.2.2.3 Input Capacitor Selection

Multilayer X5R or X7R ceramic capacitors are an excellent choice for input decoupling of the step-up converter as they have extremely low ESR and are available in small footprints. Input capacitors should be located as close as possible to the device. While a 22-µF input capacitor is sufficient for most applications, larger values may be used to reduce input current ripple without limitations. Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part. Additional "bulk" capacitance (electrolytic or tantalum) should in this circumstance be placed between C_{IN} and the power source to reduce ringing than can occur between the inductance of the power source leads and C_{IN}.

9.2.1.2.3 Loop Stability, Feed Forward Capacitor

The third step is to check the loop stability. The stability evaluation is to look from a steady-state perspective at the following signals:

- Switching node, SW
- Inductor current, I_L
- Output ripple, $V_{Ripple(OUT)}$

When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or L-C combination.

The load transient response is another approach to check the loop stability. During the load transient recovery time, V_{OUT} can be monitored for settling time, overshoot or ringing that helps judge the converter's stability. Without any ringing, the loop has usually more than 45° of phase margin.

As for the heavy load transient applications such as a 2 A load step transient, a feed forward capacitor in parallel with R1 is recommended. The feed forward capacitor increases the loop bandwidth by adding a zero. This results in a lower output voltage drop, as shown in 图 36. Set the feed forward capacitor zero near 20 kHz for most applications. See application report *Optimizing Transient Response of Internally Compensated dc-dc Converters With Feedforward Capacitor* (SLVA289).

9.2.1.3 TPS61230 5-V Output Application Performance Plots

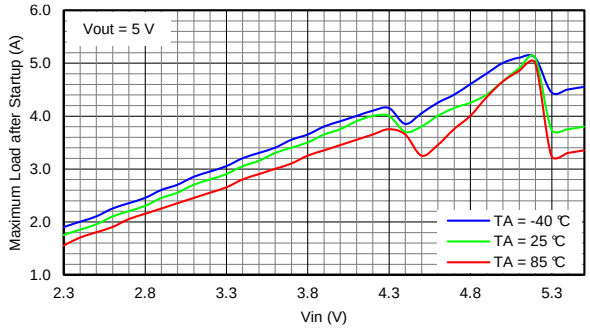


图 13. Maximum Load Current after Startup

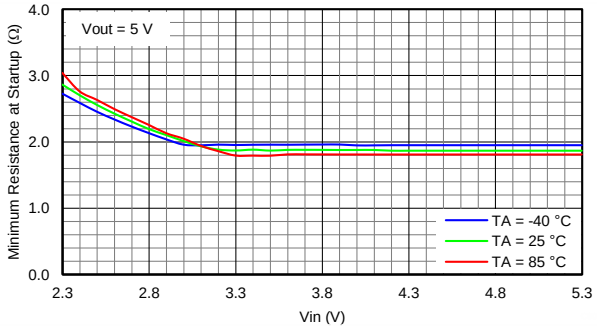


图 14. Minimum Resistance at Startup

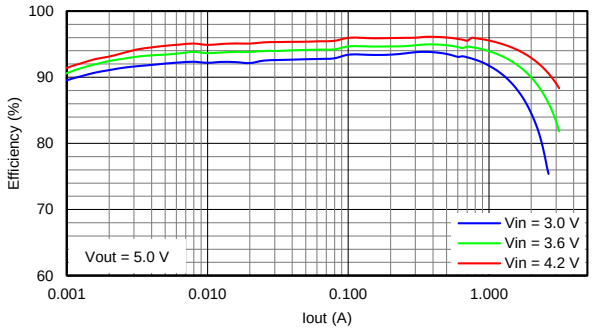


图 15. Efficiency

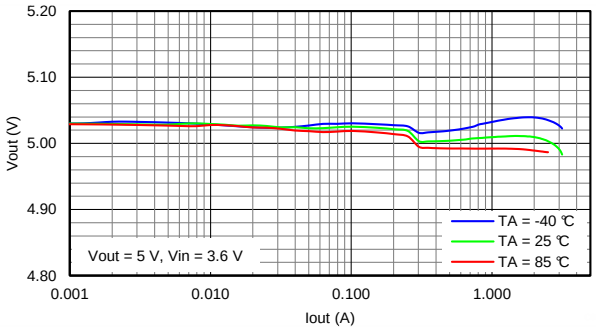


图 16. Load Regulation

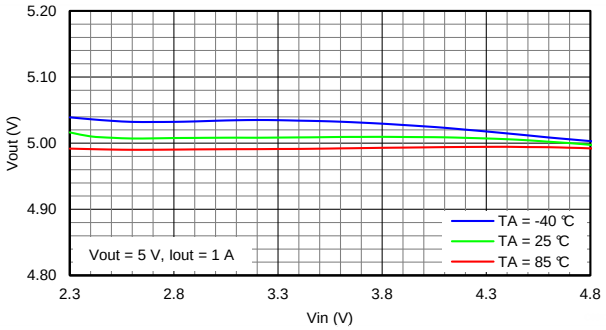


图 17. Line Regulation

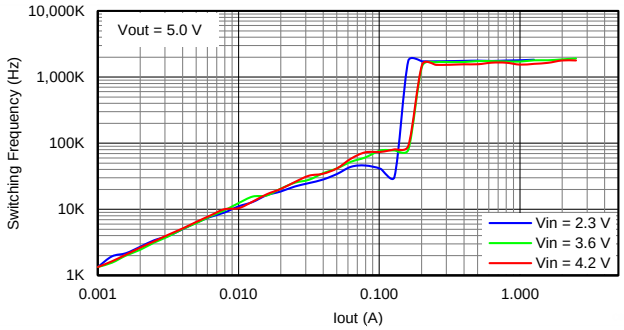


图 18. Switching Frequency

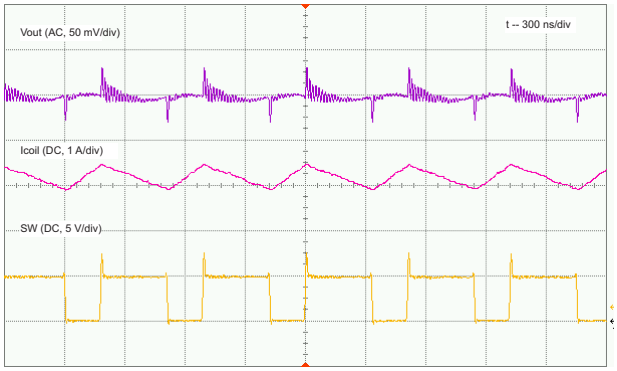


图 19. PWM Operation (V_{OUT} = 5 V, I_{OUT} = 2 A)

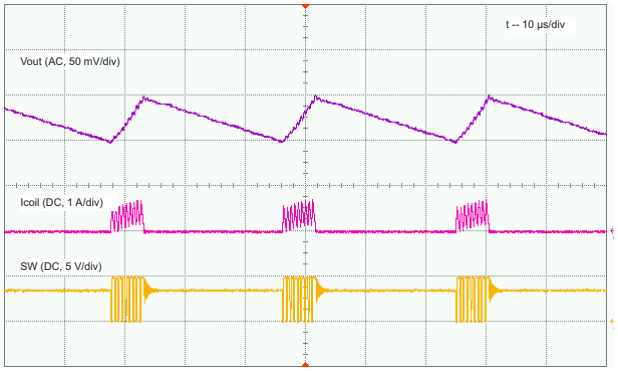


图 20. PFM Operation (V_{OUT} = 5 V, I_{OUT} = 50 mA)

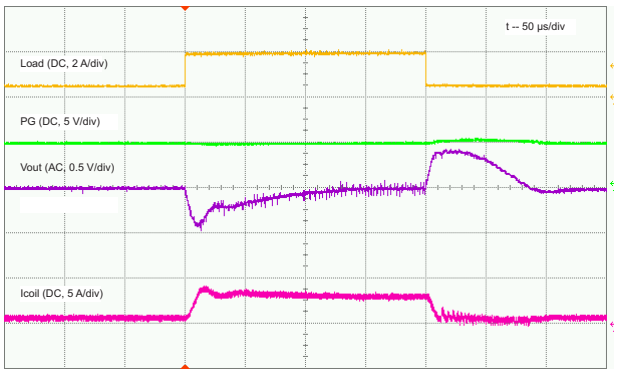


图 21. Load Transient (V_{OUT} = 5 V, I_{OUT} = 0.5 A to 2 A)

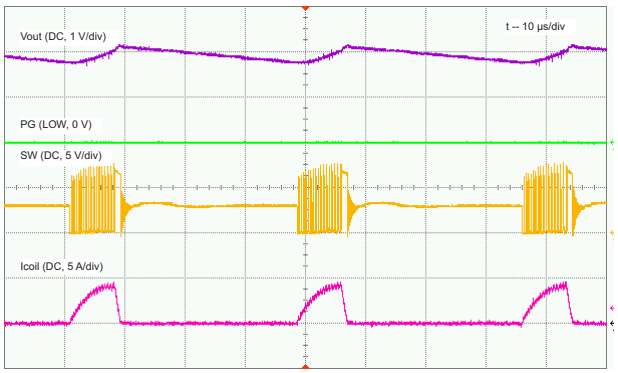


图 22. Output Over Voltage Protection (FB = 0 V, R_{OUT} = 30 Ω)

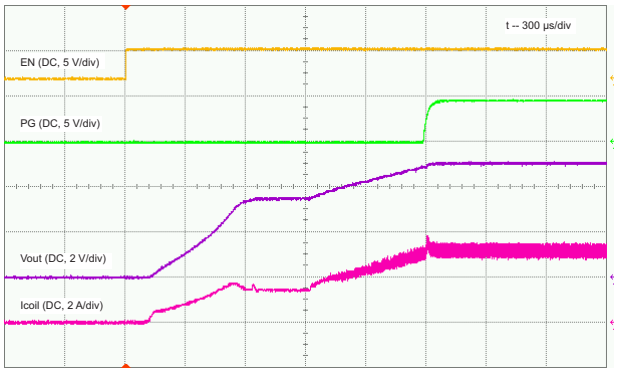


图 23. Startup (V_{OUT} = 5 V, R_{OUT} = 2.5 Ω)

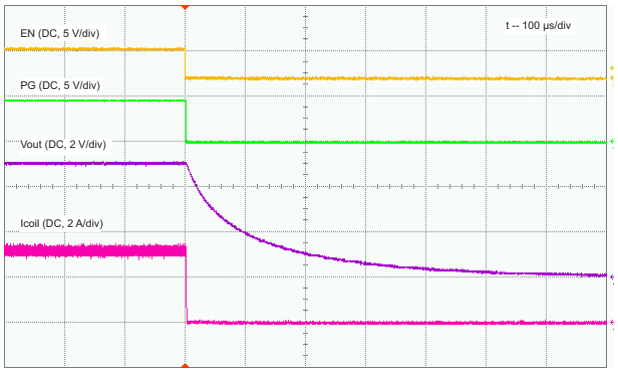


图 24. Shutdown (V_{OUT} = 5 V, R_{OUT} = 2.5 Ω)

9.2.2 TPS61230 2.3-V to 5.5-V Input, 3.5-V Output Converter

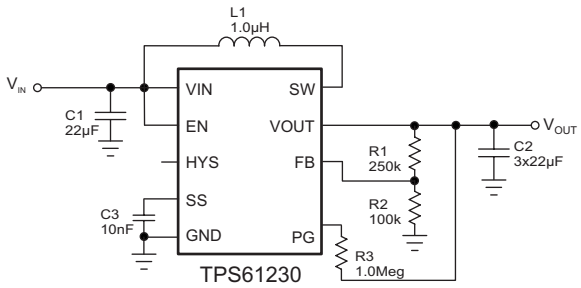


图 25. TPS61230 3.5-V Output Typical Application

9.2.2.1 TPS61230 3.5-V Output Design Requirements

表 6. TPS61230 3.5-V Output Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input Voltage Range	2.3 V to 5.5 V
Output Voltage	3.5 V
Output Voltage Ripple	±3% V_{OUT}
Transient Response	±10% V_{OUT}
Input Voltage Ripple	±200 mV
Output Current Rating	2.1 A
Operating Frequency	2 MHz

9.2.2.2 Detailed Design Procedure

Refer to the *TPS61230 5-V Detailed Design Procedure* section for the 3.5-V detailed design procedures.

9.2.2.3 TPS61230 3.5-V Output Application Performance Plots

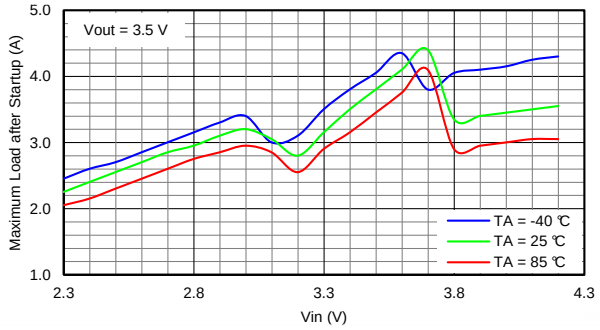


图 26. Maximum Load Current after Startup

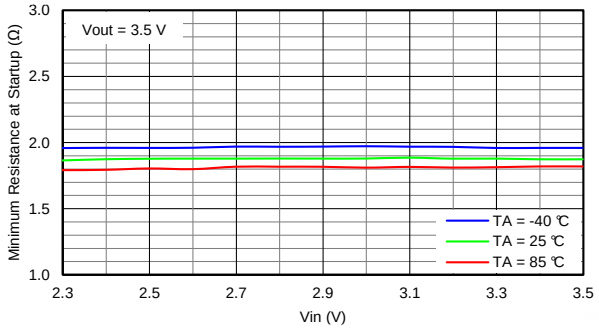


图 27. Minimum Resistance at Startup

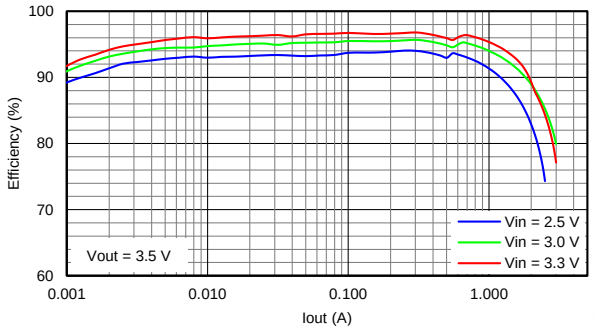


图 28. Efficiency

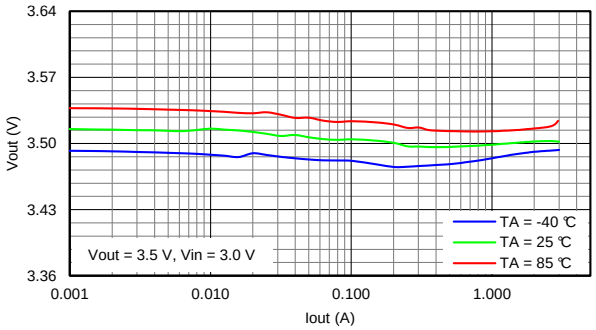


图 29. Load Regulation

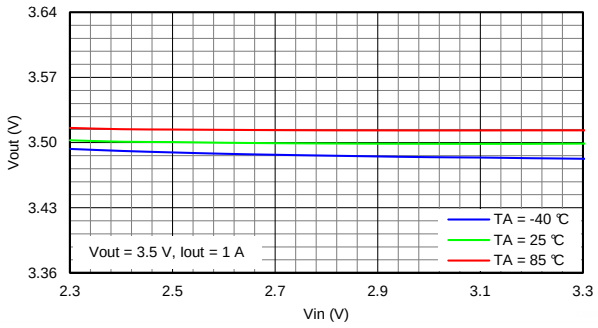


图 30. Line Regulation

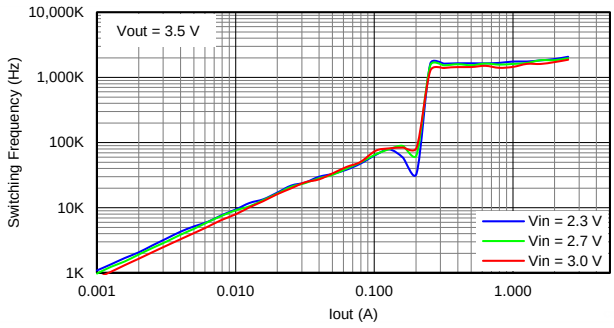


图 31. Switching Frequency

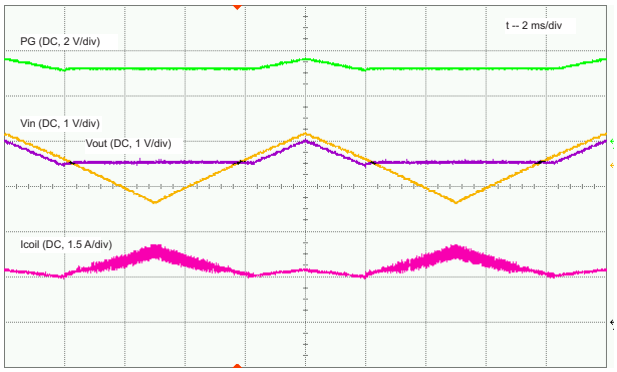


图 32. Input Sweep (V_{OUT} = 3.5 V, V_{IN} = 2.7 V to 4.2 V, I_{OUT} = 1.5 A)

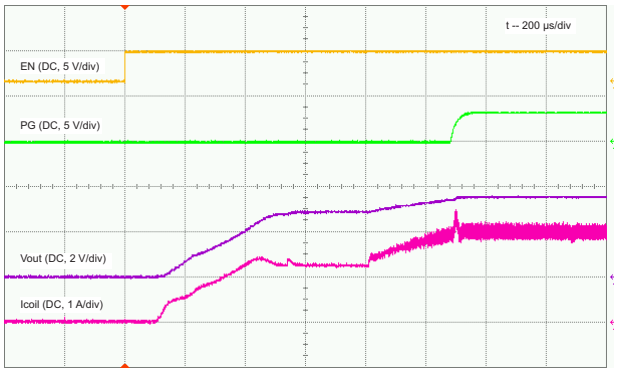


图 33. Startup (V_{OUT} = 3.5 V, V_{IN} = 3.0 V, R_{OUT} = 2.3 Ω)

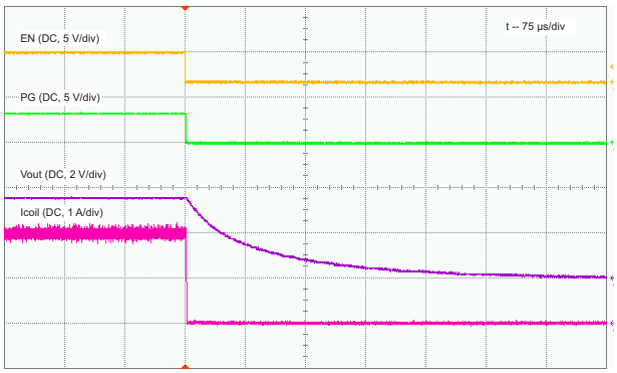


图 34. Shutdown (V_{OUT} = 3.5 V, V_{IN} = 3.0 V, R_{OUT} = 2.3 Ω)

9.2.3 TPS61230 Application with Feed Forward Capacitor for Best Transient Response

As for the heavy load transient applications such as a 2-A load step transient, a feed forward capacitor in parallel with R1 is recommended. The feed forward capacitor increases the loop bandwidth by adding a zero. This results in a lower output voltage drop, as shown in 图 36. Set the feed forward capacitor zero near 20 kHz for most applications. See application report *Optimizing Transient Response of Internally Compensated dc-dc Converters With Feedforward Capacitor* (SLVA289).

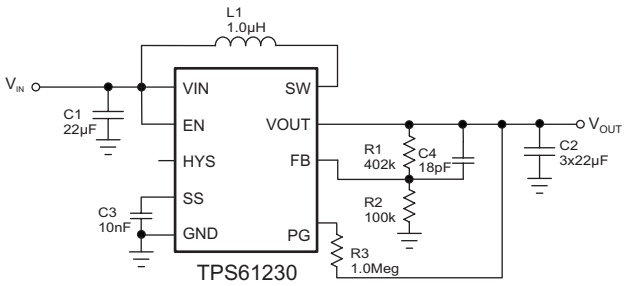


图 35. TPS61230 5-V Output with Cff Typical Application

9.2.3.1 Design Requirements

Refer to the *TPS61230 5-V Output Design Requirements* section for the design requirements.

9.2.3.2 Detailed Design Procedure

Refer to the *TPS61230 5-V Detailed Design Procedure* section for the detailed design procedures.

9.2.3.3 Application Curve

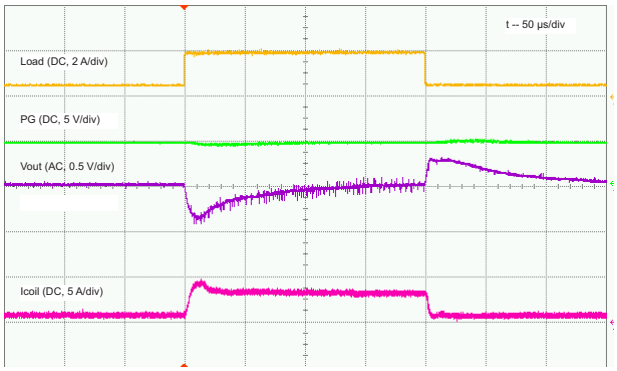


图 36. Load Transient (V_{OUT} = 5 V, I_{OUT} = 0.5 A to 2 A, C_{FF} = 18 pF)

10 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.3 V and 5.5 V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 µF is a typical choice.

11 Layout

11.1 Layout Guidelines

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at the GND pin of the IC. The most critical current path for all boost converters is from the switching FET, through the synchronous FET, then the output capacitors, and back to ground of the switching FET. Therefore, the output capacitors and their traces should be placed on the same board layer as the IC and as close as possible between the IC's VOUT and GND pin.

See 图 37 for the recommended layout.

11.2 Layout Example

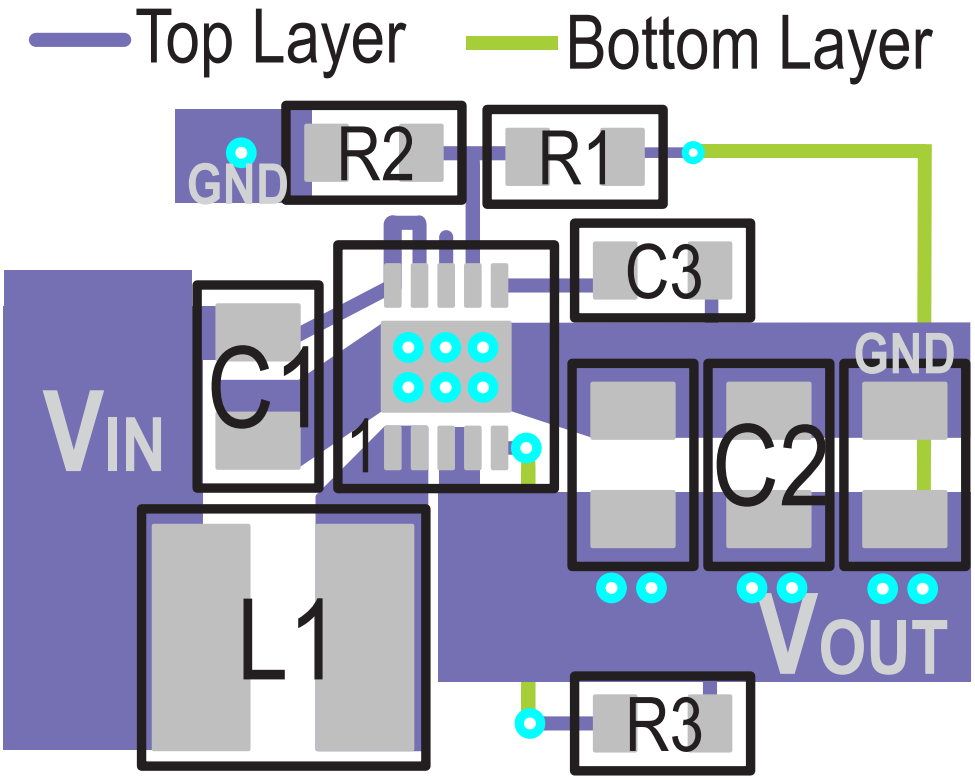


图 37. Layout Recommendation

11.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Two basic approaches for enhancing thermal performance are listed below.

- Improving the power dissipation capability of the PCB design
- Introducing airflow in the system

Thermal Considerations (接下页)

For more details on how to use the thermal parameters in the dissipation ratings table please check the application report *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* (SZZA017) and the application report *Semiconductor and IC Package Thermal Metrics* (SPRA953).

12 器件和文档支持

12.1 器件支持

12.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

12.2 文档支持

12.2.1 相关文档

*《采用前馈电容优化内部补偿 DC-DC 转换器的瞬态响应》*SLVA289

《采用 JEDEC PCB 设计的线性和逻辑封装散热特性》(SZZA017)

《半导体和 IC 封装热指标》(SPRA953)

12.3 相关链接

以下表格列出了快速访问链接。 范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 **7.** 相关链接

部件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
TPS61230	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS61231	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS61232	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.4 商标

All trademarks are the property of their respective owners.

12.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

13 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS61230DRCR	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SBK
TPS61230DRCR.Z	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SBK
TPS61230DRCRG4.Z	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SBK
TPS61230DRCT	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SBK
TPS61230DRCT.Z	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SBK
TPS61232DRCR	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SBL
TPS61232DRCR.Z	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SBL
TPS61232DRCT	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SBL
TPS61232DRCT.Z	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SBL

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

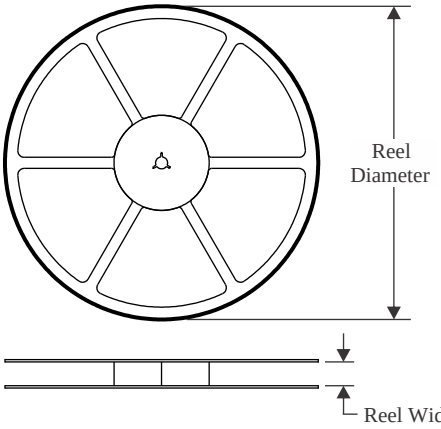
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

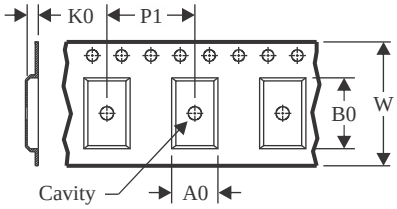
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

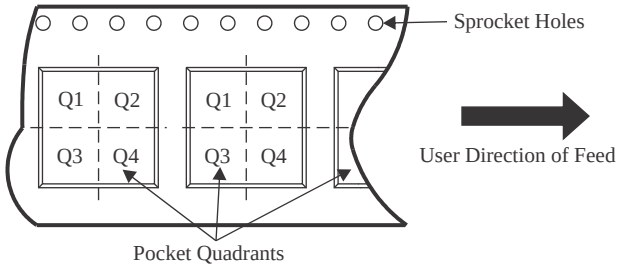


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

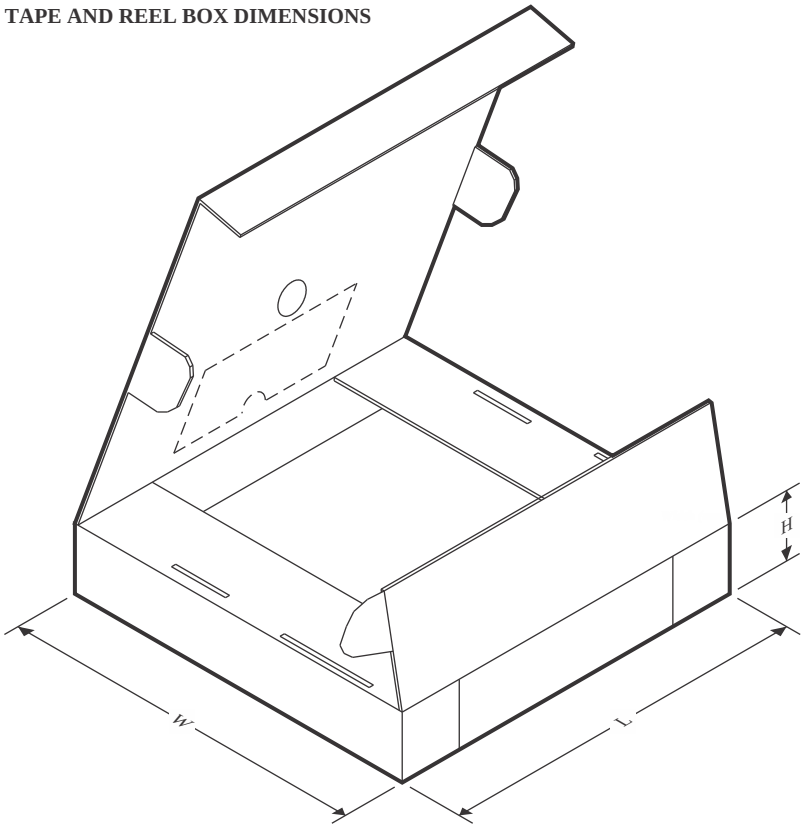
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61230DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61230DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61232DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61232DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61230DRCR	VSON	DRC	10	3000	346.0	346.0	33.0
TPS61230DRCT	VSON	DRC	10	250	182.0	182.0	20.0
TPS61232DRCR	VSON	DRC	10	3000	346.0	346.0	33.0
TPS61232DRCT	VSON	DRC	10	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

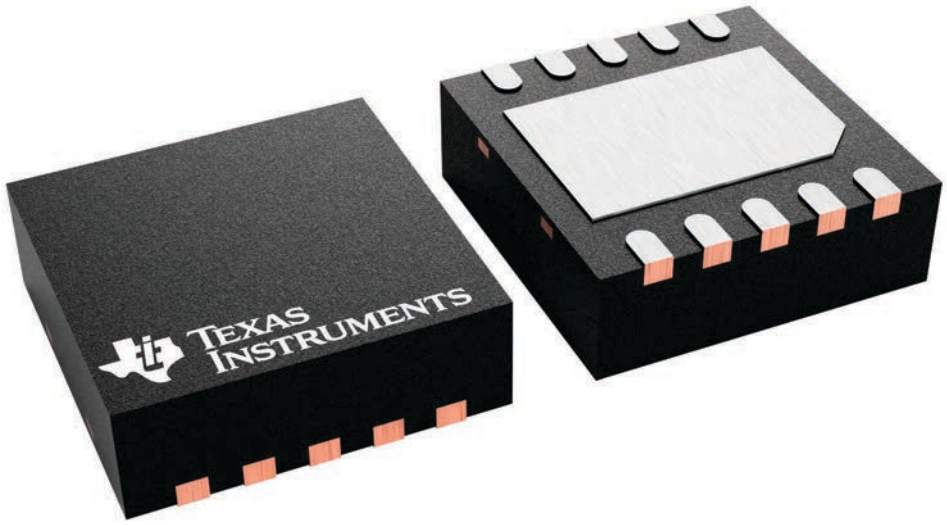
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



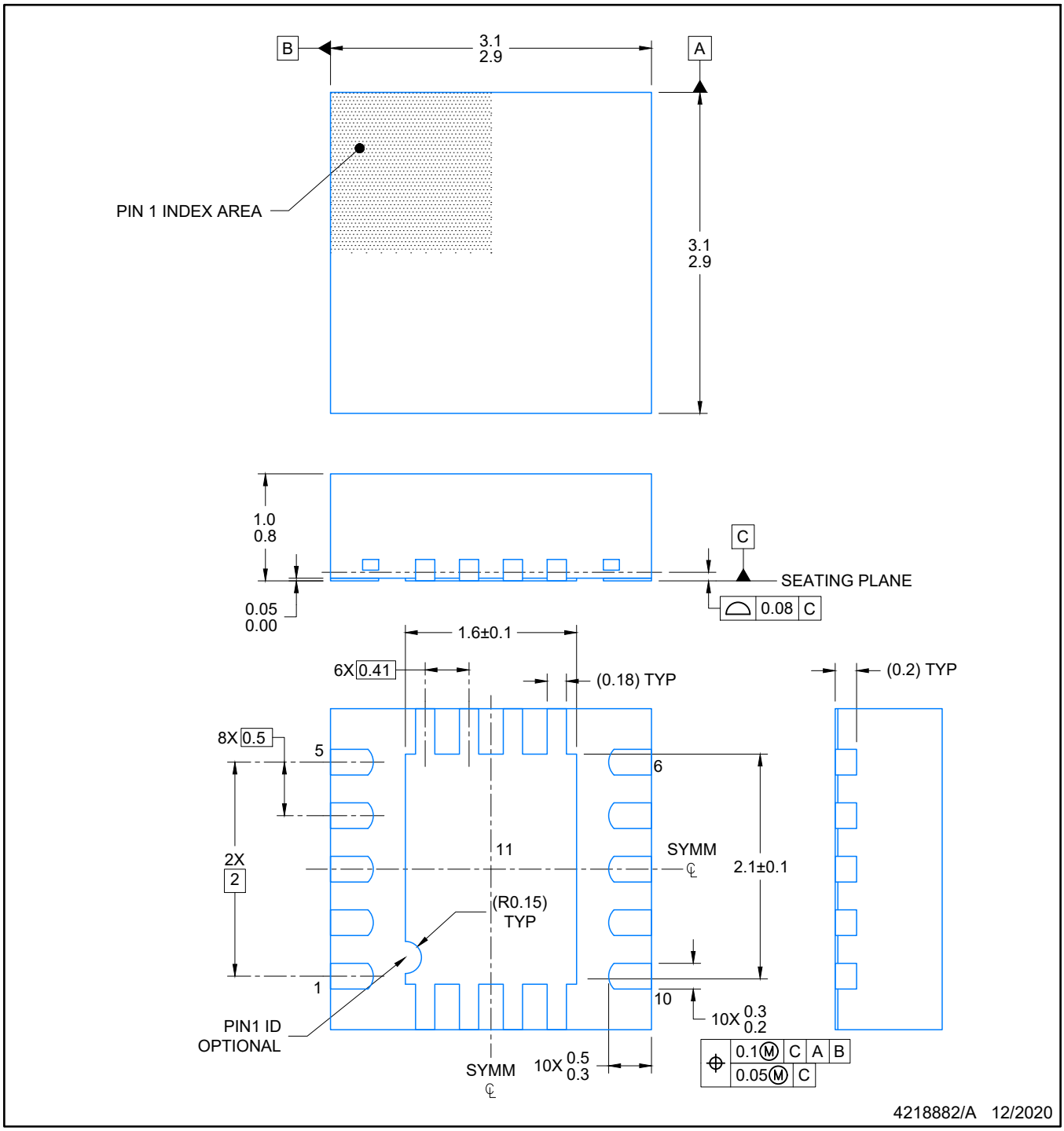
4226193/A

PACKAGE OUTLINE

DRC0010G

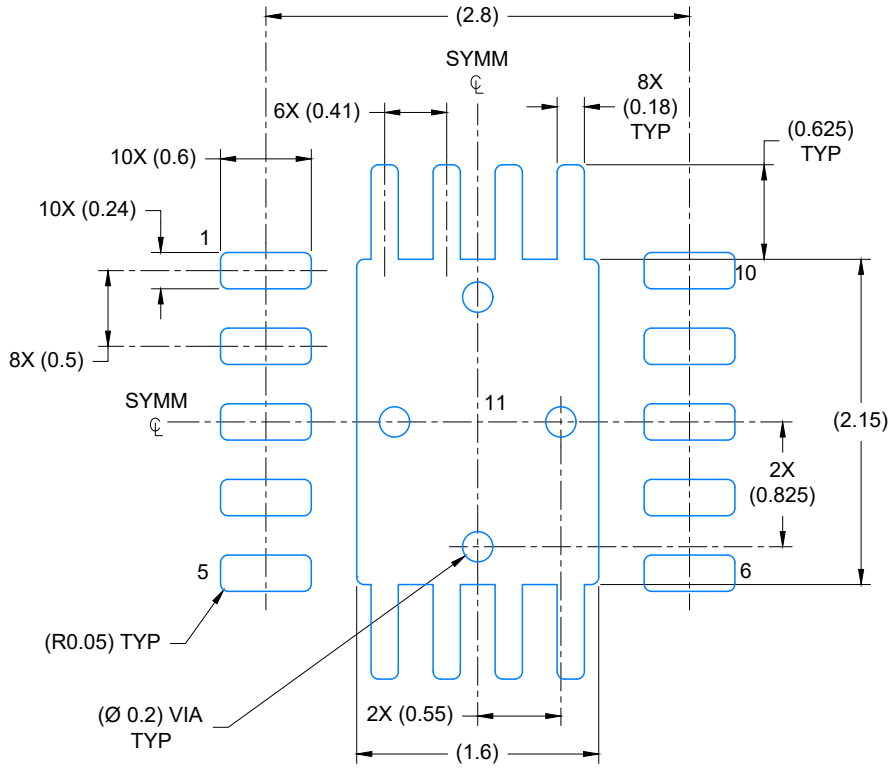
VSON - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD

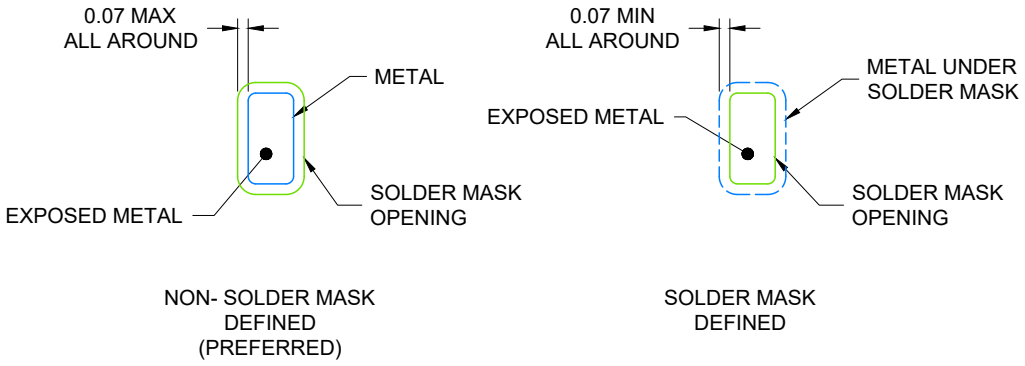


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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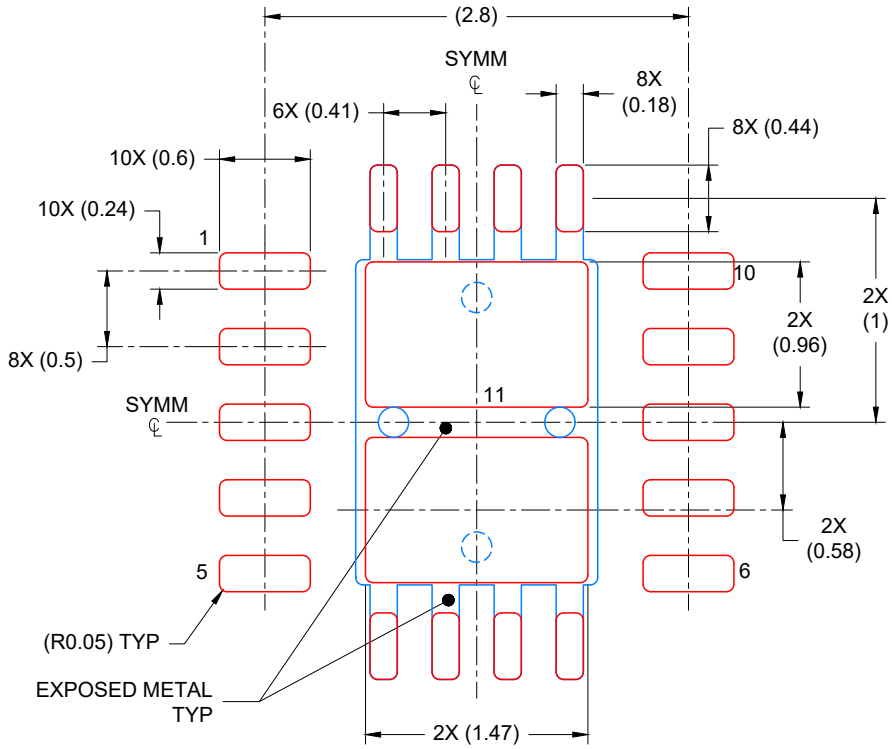
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
79% PRINTED COVERAGE BY AREA
SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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