

## DCP02 系列 2W、1000V<sub>RMS</sub> 隔离式非稳压直流/直流转换器模块

### 1 特性

- 1kV 隔离 (工作) : 1 秒测试
- 在隔离层中施加连续电压 : 60VDC/42.5VAC
- UL1950 认证组件
- EN55022 B 类 EMC 性能
- 7 引脚 PDIP 和 12 引脚 SOP 封装
- 输入电压 : 5V、12V、15V 或 24V
- 输出电压 : 3.3V、±5V、7V、9V、±12V 或 ±15V
- 器件间同步
- 过热保护
- 短路保护
- 高效率

### 2 应用

- 信号路径隔离
- 消除接地环路
- 数据采集
- 工业控制和仪表
- 测试设备

### 3 说明

DCP02 系列器件是一系列 2W 隔离式非稳压直流/直流转换器模块。DCP02 系列器件具有片上器件保护，只需要最少的外部元件即可提供额外的功能，例如输出禁用和开关频率同步。

DCP02 系列器件集这些特性和较小的尺寸于一体，非常适合用于各种应用，并且对需要信号路径隔离的应用来说，它是一个易于使用的解决方案。

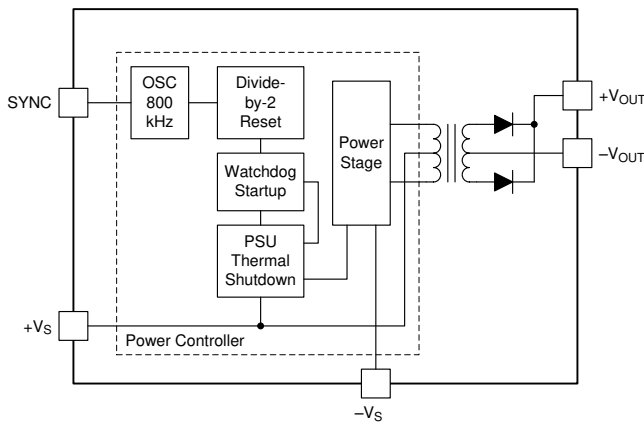
#### WARNING

此产品具有运行隔离功能，仅可用于信号隔离。不可作为需要增强型隔离的安全隔离电路的一部分使用。请参阅 [特性说明](#) 中的定义

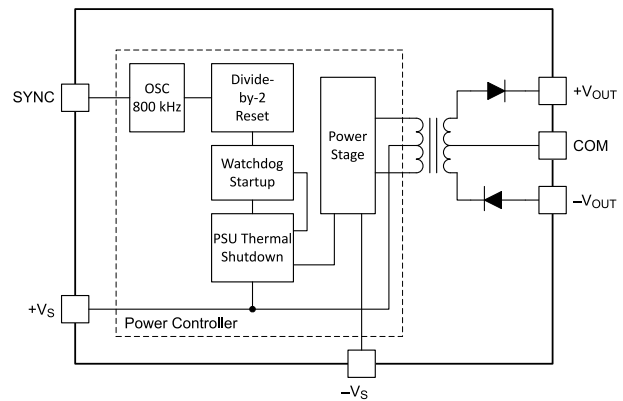
#### 器件信息

| 器件型号      | 封装 <sup>(1)</sup> | 封装尺寸 (标称值)        |
|-----------|-------------------|-------------------|
| DCP02xxxx | PDIP (7)          | 19.18mm × 10.60mm |
|           | SOP (12)          | 17.90mm × 10.33mm |

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。



单路输出方框图



双路输出方框图



## Table of Contents

|                                           |    |                                                          |    |
|-------------------------------------------|----|----------------------------------------------------------|----|
| 1 特性.....                                 | 1  | 7.2 Functional Block Diagrams.....                       | 12 |
| 2 应用.....                                 | 1  | 7.3 Feature Description.....                             | 13 |
| 3 说明.....                                 | 1  | 7.4 Device Functional Modes.....                         | 16 |
| 4 Revision History.....                   | 2  | 8 Layout.....                                            | 24 |
| 5 Pin Configuration and Functions.....    | 4  | 8.1 Layout Guidelines.....                               | 24 |
| Pin Functions.....                        | 4  | 8.2 Layout Example.....                                  | 24 |
| 6 Specifications.....                     | 5  | 9 Device and Documentation Support.....                  | 26 |
| 6.1 Absolute Maximum Ratings.....         | 5  | 9.1 Device Support.....                                  | 26 |
| 6.2 ESD Ratings.....                      | 5  | 9.2 Documentation Support.....                           | 26 |
| 6.3 Recommended Operating Conditions..... | 5  | 9.3 Support Resources.....                               | 26 |
| 6.4 Thermal Information.....              | 5  | 9.4 Related Links.....                                   | 27 |
| 6.5 Electrical Characteristics.....       | 6  | 9.5 Trademarks.....                                      | 27 |
| 6.6 Switching Characteristics.....        | 6  | 9.6 Receiving Notification of Documentation Updates..... | 27 |
| 6.7 Typical Characteristics.....          | 7  | 9.7 Electrostatic Discharge Caution.....                 | 27 |
| 7 Detailed Description.....               | 12 | 9.8 Glossary.....                                        | 27 |
| 7.1 Overview.....                         | 12 |                                                          |    |

## 4 Revision History

### Changes from Revision M (April 2020) to Revision N (July 2020) Page

|                   |   |
|-------------------|---|
| • 更新了 图 3-1 ..... | 1 |
|-------------------|---|

### Changes from Revision L (May 2015) to Revision M (April 2020) Page

|                                                             |    |
|-------------------------------------------------------------|----|
| • 添加了链接至 节 2 .....                                          | 1  |
| • Added Efficiency and Load Regulation plots to 节 6.7 ..... | 7  |
| • Added 节 7.3.6 section.....                                | 14 |
| • Added 节 7.3.7 section.....                                | 14 |
| • Added 节 7.3.10 section.....                               | 15 |

### Changes from Revision K (February 2008) to Revision L (January 2015) Page

|                                                                                                         |    |
|---------------------------------------------------------------------------------------------------------|----|
| • 更新了 节 1 .....                                                                                         | 1  |
| • 添加了 ESD 等级表、特性说明部分、器件功能模式部分、应用和实现部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分.....                       | 1  |
| • 添加了表 3-1 表.....                                                                                       | 1  |
| • 添加了 图 3-1 .....                                                                                       | 1  |
| • Renamed pin "0V" to "COM" (output side common pin) in 节 Pin Functions table.....                      | 4  |
| • Renamed pin "V <sub>S</sub> " to "+V <sub>S</sub> " (input voltage pin) in 节 Pin Functions table..... | 4  |
| • Renamed pin "0V" to " - V <sub>S</sub> " (input side common pin) in 节 Pin Functions table.....        | 4  |
| • Added 节 6.3 table.....                                                                                | 5  |
| • Added 节 6.4 table.....                                                                                | 5  |
| • Added information to the ISOLATION section of the 节 6.5 table .....                                   | 6  |
| • Added 节 7.3.1 section to the 节 7.3 section.....                                                       | 13 |
| • Added a typical application design to the 节 8.1 section.....                                          | 18 |

## Device Comparison Table

| DEVICE<br>NUMBER           | INPUT<br>VOLTAGE<br>V <sub>S</sub> (V) |     |      | OUTPUT<br>VOLTAGE<br>V <sub>NOM</sub> @ V <sub>S</sub> (TYP)(V)<br>75% LOAD |     |        | DEVICE<br>OUTPUT<br>CURRENT<br>(mA) <sup>(3)</sup> | LOAD<br>REGULATION<br>10% TO 100%<br>LOAD <sup>(1)</sup> |     | NO LOAD<br>CURRENT<br>I <sub>Q</sub> (mA)<br>0% LOAD | EFFICIENCY<br>(%)<br>100% LOAD | BARRIER<br>CAPACITANCE<br>C <sub>ISO</sub> (pF)<br>V <sub>ISO</sub> = 750Vrms |
|----------------------------|----------------------------------------|-----|------|-----------------------------------------------------------------------------|-----|--------|----------------------------------------------------|----------------------------------------------------------|-----|------------------------------------------------------|--------------------------------|-------------------------------------------------------------------------------|
|                            | MIN                                    | TYP | MAX  | MIN                                                                         | TYP | MAX    | MAX                                                | TYP                                                      | MAX | TYP                                                  | TYP                            | TYP                                                                           |
| DCP020503P<br>DCP020503U   | 4.5                                    | 5   | 5.5  | 3.13                                                                        | 3.3 | 3.46   | 600                                                | 19                                                       | 30  | 18                                                   | 74                             | 26                                                                            |
| DCP020505P<br>DCP020505U   |                                        |     |      | 4.75                                                                        | 5   | 5.25   | 400                                                | 14                                                       | 20  | 18                                                   | 80                             | 22                                                                            |
| DCP020507P<br>DCP020507U   |                                        |     |      | 6.65                                                                        | 7   | 7.35   | 285                                                | 14                                                       | 25  | 20                                                   | 81                             | 30                                                                            |
| DCP020509P<br>DCP020509U   |                                        |     |      | 8.55                                                                        | 9   | 9.45   | 222                                                | 12                                                       | 20  | 23                                                   | 82                             | 31                                                                            |
| DCP020515DP<br>DCP020515DU |                                        |     |      | ±14.25                                                                      | ±15 | ±15.75 | 133 <sup>(2)</sup>                                 | 11                                                       | 20  | 27                                                   | 85                             | 24                                                                            |
| DCP021205P<br>DCP021205U   | 10.8                                   | 12  | 13.2 | 4.75                                                                        | 5   | 5.25   | 400                                                | 7                                                        | 15  | 14                                                   | 83                             | 33                                                                            |
| DCP021212P<br>DCP021212U   |                                        |     |      | 11.4                                                                        | 12  | 12.6   | 166                                                | 7                                                        | 20  | 15                                                   | 87                             | 47                                                                            |
| DCP021212DP<br>DCP021212DU |                                        |     |      | ±11.4                                                                       | ±12 | ±12.6  | 166 <sup>(2)</sup>                                 | 6                                                        | 20  | 16                                                   | 88                             | 35                                                                            |
| DCP021515P<br>DCP021515U   | 13.5                                   | 15  | 16.5 | 14.25                                                                       | 15  | 15.75  | 133                                                | 6                                                        | 20  | 15                                                   | 88                             | 42                                                                            |
| DCP022405P<br>DCP022405U   | 21.6                                   | 24  | 26.4 | 4.75                                                                        | 5   | 5.25   | 400                                                | 6                                                        | 15  | 13                                                   | 81                             | 33                                                                            |
| DCP022405DP<br>DCP022405DU |                                        |     |      | ±4.75                                                                       | ±5  | ±5.25  | 400 <sup>(2)</sup>                                 | 6                                                        | 15  | 12                                                   | 80                             | 22                                                                            |
| DCP022415DP<br>DCP022415DU |                                        |     |      | ±14.25                                                                      | ±15 | ±15.75 | 133 <sup>(2)</sup>                                 | 6                                                        | 25  | 16                                                   | 79                             | 44                                                                            |

(1) Load regulation = (V<sub>OUT</sub> at 10% load - V<sub>OUT</sub> at 100%)/V<sub>OUT</sub> at 75% load

(2) I<sub>OUT1</sub> + I<sub>OUT2</sub>

(3) P<sub>OUT(max)</sub> = 2 W

## 5 Pin Configuration and Functions

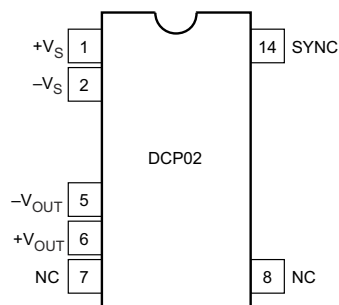


图 5-1. NVA Package 7-Pin PDIP (Single Output) (Top View)

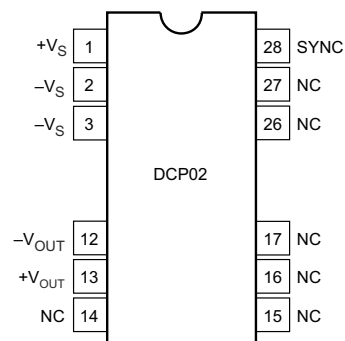


图 5-2. DVB PACKAGE 12-Pin SOP (Single Output) (Top View)

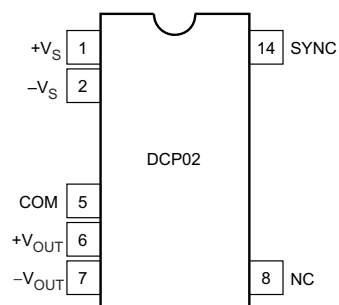


图 5-3. NVA Package 7-Pin PDIP (Dual Output) (Top View)

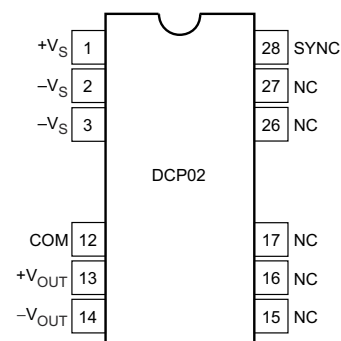


图 5-4. DVB Package 12-Pin SOP (Dual Output) (Top View)

## Pin Functions

| PIN NAME           | NUMBER     |              |            |              | I/O <sup>(1)</sup> | DESCRIPTION                                                                                                                                       |
|--------------------|------------|--------------|------------|--------------|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------|
|                    | DVB (DUAL) | DVB (SINGLE) | NVA (DUAL) | NVA (SINGLE) |                    |                                                                                                                                                   |
| COM                | 12         | —            | 5          | —            | O                  | Output side common                                                                                                                                |
| NC                 | 15         | 14           | 8          | 7            | —                  | No connection                                                                                                                                     |
|                    |            | 15           |            |              |                    |                                                                                                                                                   |
|                    | 16         | 16           |            |              |                    |                                                                                                                                                   |
|                    | 17         | 17           |            |              |                    |                                                                                                                                                   |
|                    | 26         | 26           |            |              |                    |                                                                                                                                                   |
|                    | 27         | 27           |            |              |                    |                                                                                                                                                   |
| SYNC               | 28         | 28           | 14         | 14           | I                  | Synchronization Pin - Synchronize multiple devices by connecting their SYNC pins together. Pulling this pin low disables the internal oscillator. |
| +V <sub>OUT</sub>  | 13         | 13           | 6          | 6            | O                  | Positive output voltage                                                                                                                           |
| – V <sub>OUT</sub> | 14         | 12           | 7          | 5            | O                  | Negative output voltage                                                                                                                           |
| +V <sub>S</sub>    | 1          | 1            | 1          | 1            | I                  | Input voltage                                                                                                                                     |
| – V <sub>S</sub>   | 2          | 2            | 2          | 2            | I                  | Input side common                                                                                                                                 |
|                    | 3          | 3            |            |              |                    |                                                                                                                                                   |

(1) I = Input, O = Output

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

|                                       |                    | MIN  | MAX | UNIT |
|---------------------------------------|--------------------|------|-----|------|
| Input voltage                         | 5-V input devices  |      | 7   | V    |
|                                       | 12-V input devices |      | 15  |      |
|                                       | 15-V input devices |      | 18  |      |
|                                       | 24-V input devices |      | 29  |      |
| Storage temperature, T <sub>stg</sub> |                    | - 60 | 125 | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

|                                            |                                                                                | VALUE | UNIT |
|--------------------------------------------|--------------------------------------------------------------------------------|-------|------|
| V <sub>(ESD)</sub> Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±1000 | V    |
|                                            | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±250  |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                       |                    | MIN  | NOM | MAX  | UNIT |
|-----------------------|--------------------|------|-----|------|------|
| Input Voltage         | 5-V input devices  | 4.5  | 5   | 5.5  | V    |
|                       | 12-V input devices | 10.8 | 12  | 13.2 |      |
|                       | 15-V input devices | 13.5 | 15  | 16.5 |      |
|                       | 24-V input devices | 21.6 | 24  | 26.4 |      |
| Operating temperature |                    | - 40 |     | 85   | °C   |

### 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | DCP020x    | DCP020x   | UNIT |
|-------------------------------|----------------------------------------------|------------|-----------|------|
|                               |                                              | NVA (PDIP) | DVB (SOP) |      |
|                               |                                              | 7 PINS     | 12 PINS   |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 61         | 61        | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 19         | 19        |      |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 24         | 24        |      |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 7          | 7         |      |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 24         | 24        |      |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | N/A        | N/A       |      |

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).



## 6.7 Typical Characteristics

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

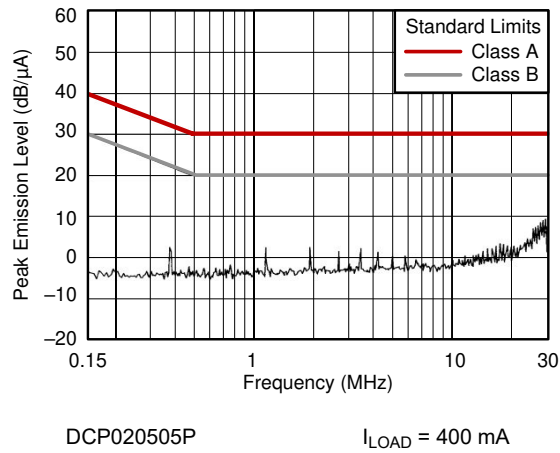


图 6-1. Conducted Emissions versus Frequency

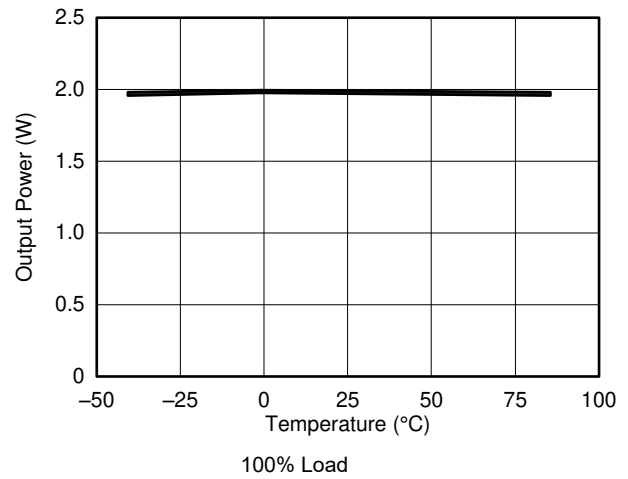


图 6-2. Output Power versus Temperature

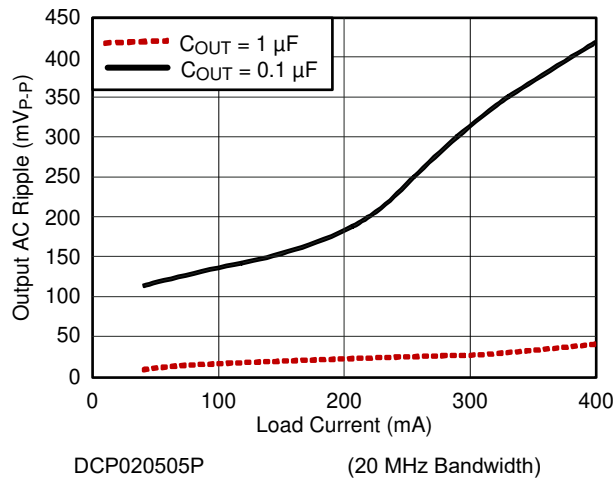


图 6-3. Output AC Ripple versus Load Current

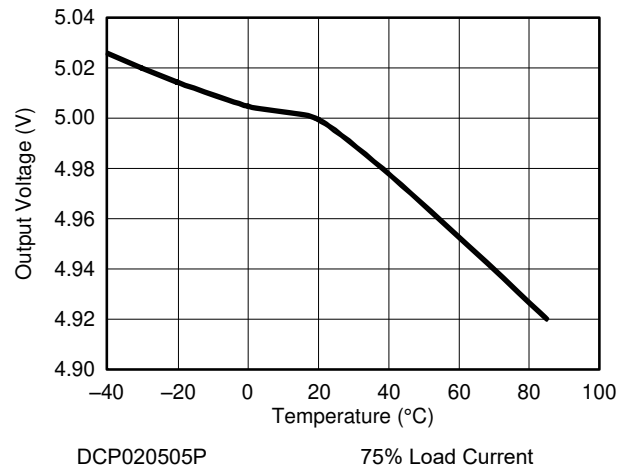


图 6-4. Output Voltage versus Temperature

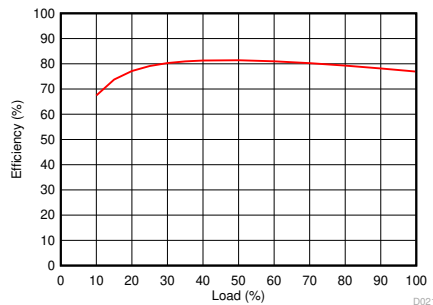
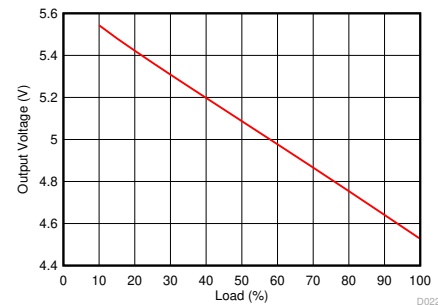
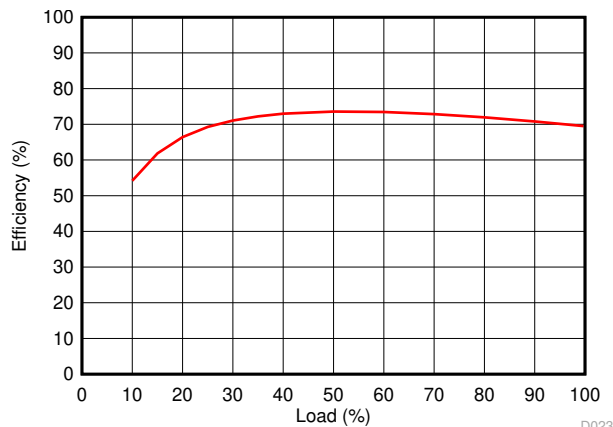


图 6-5. Efficiency versus Load



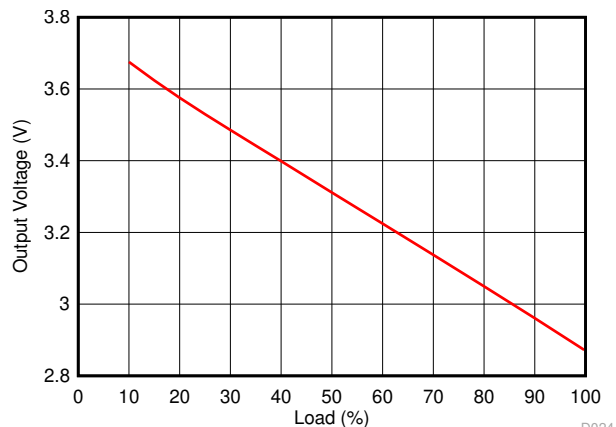
Note: Operations under 10% Load

图 6-6. Load Regulation



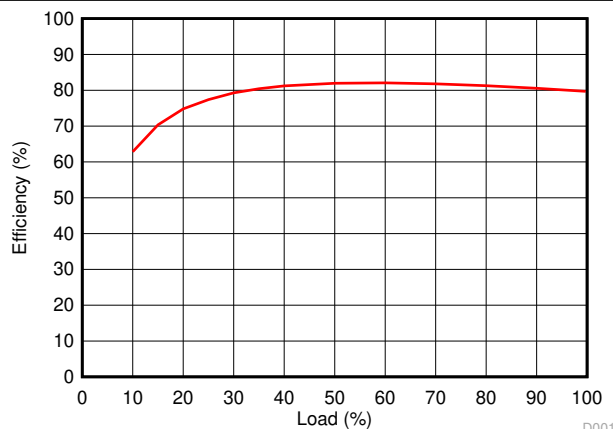
A. DCP020503P

图 6-7. Efficiency versus Load



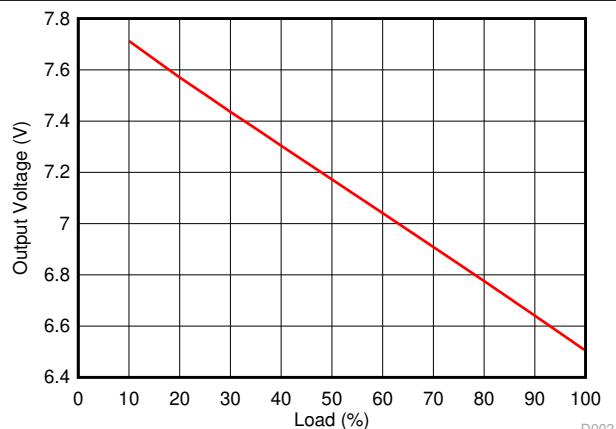
A. DCP020503P **Note:** Operations under 10% Load

图 6-8. Load Regulation



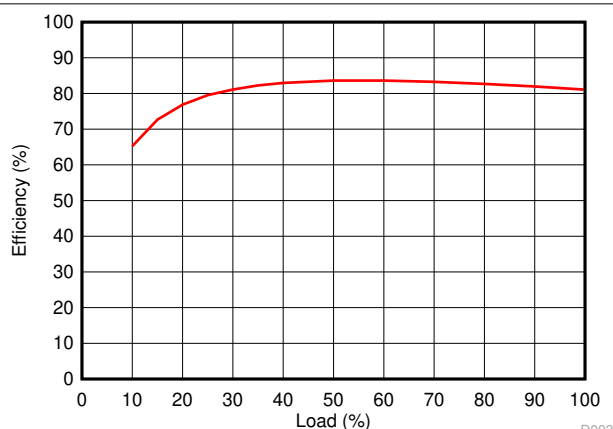
A. DCP020507P

图 6-9. Efficiency versus Load



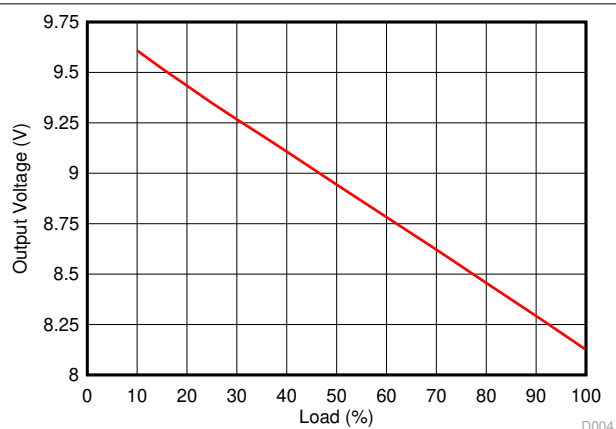
A. DCP020507P **Note:** Operations under 10% Load

图 6-10. Load Regulation



A. DCP020509P

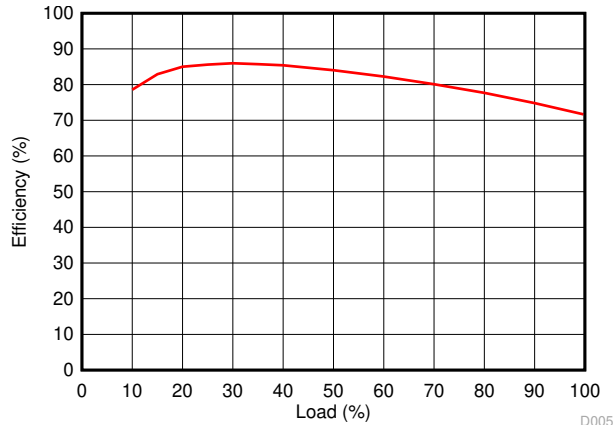
图 6-11. Efficiency versus Load



A. DCP020509P **Note:** Operations under 10% Load

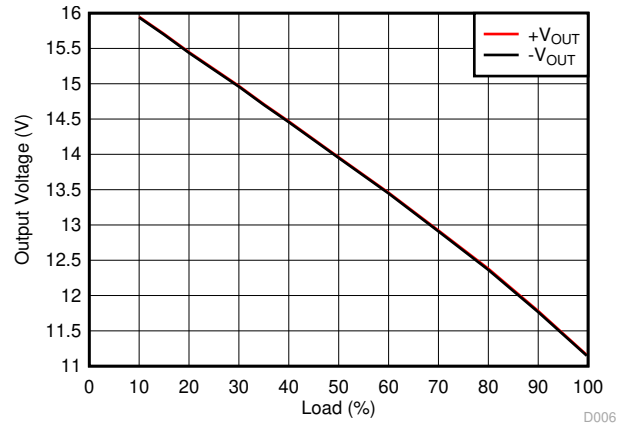
图 6-12. Load Regulation





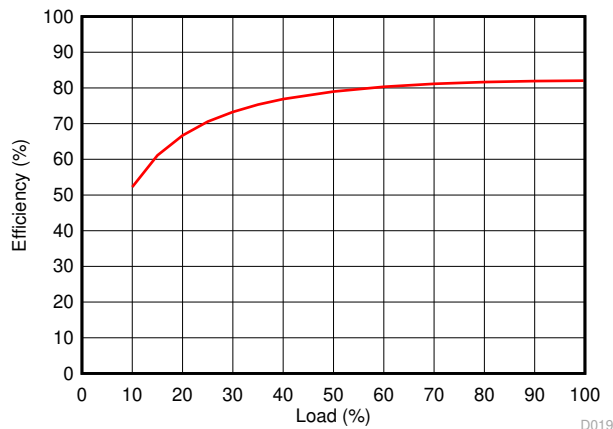
A. DCP020515DP

图 6-13. Efficiency versus Load



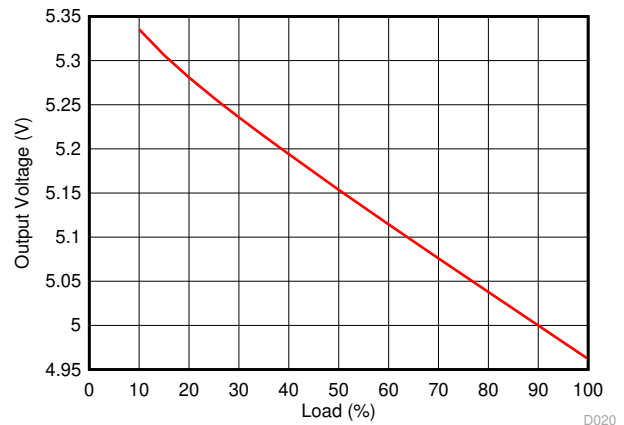
A. DCP020515P **Note:** Operations under 10% Load

图 6-14. Load Regulation



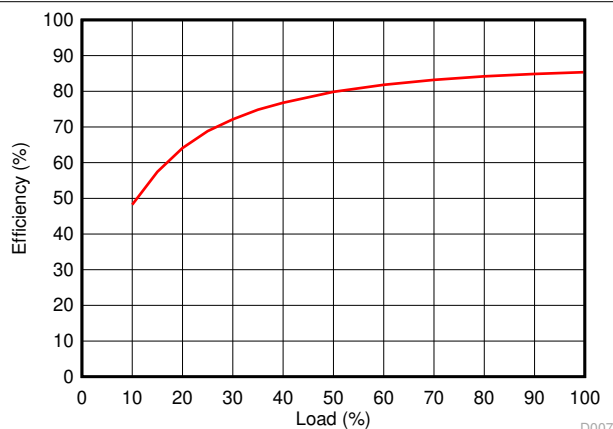
A. DCP021205P

图 6-15. Efficiency versus Load



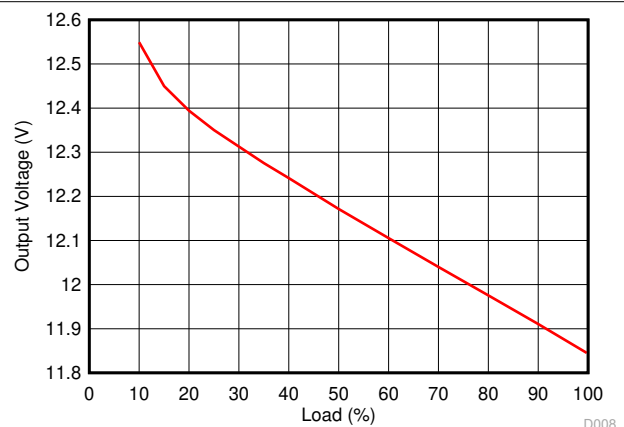
DCP021205P **Note:** Operations under 10% Load

图 6-16. Load Regulation



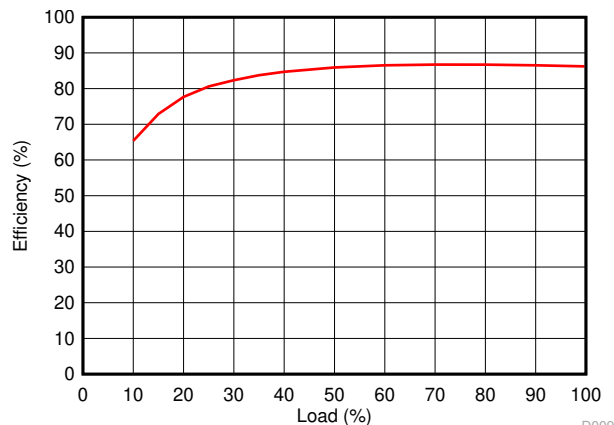
A. DCP021212P

图 6-17. Efficiency versus Load



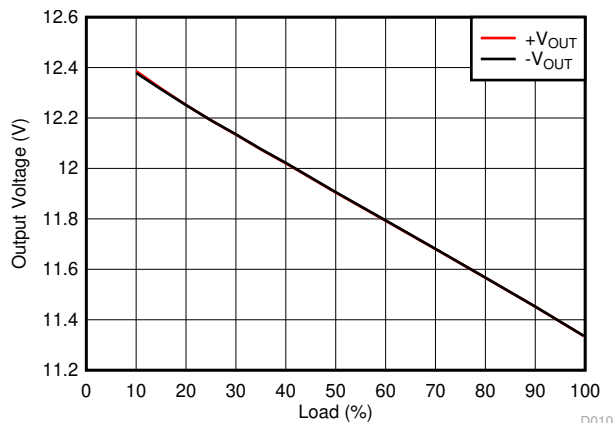
A. DCP021212P **Note:** Operations under 10% Load

图 6-18. Load Regulation



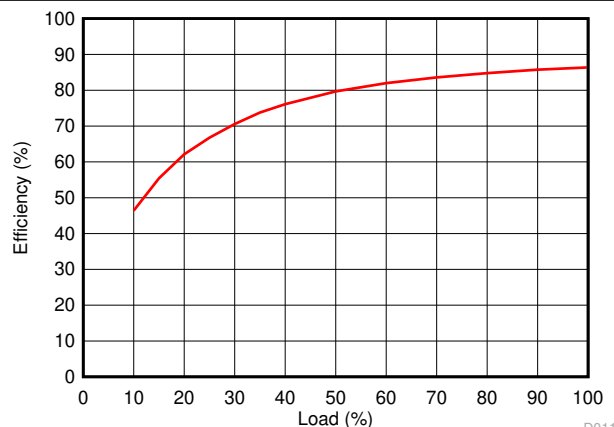
A. DCP021212DP

图 6-19. Efficiency versus Load



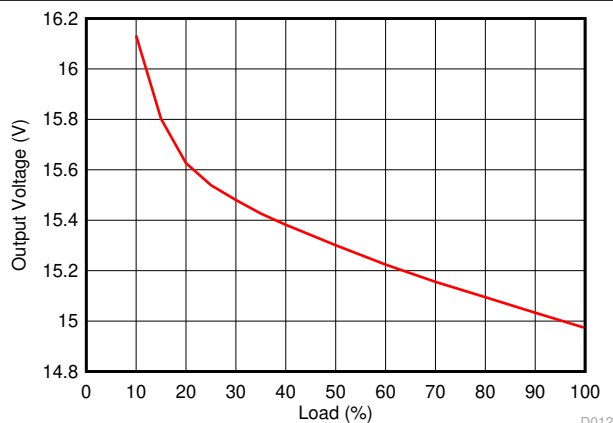
A. DCP021212DP **Note:** Operations under 10% Load

图 6-20. Load Regulation



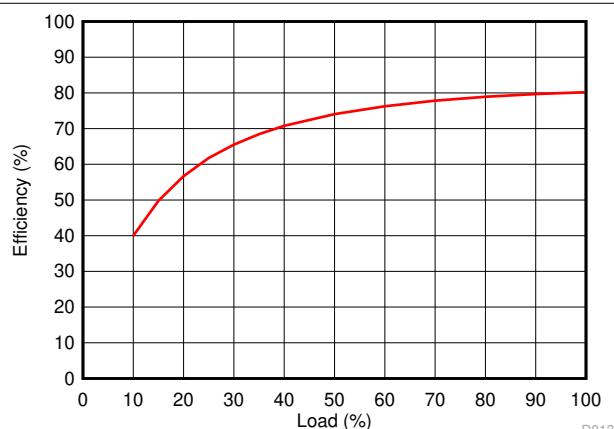
A. DCP021515P

图 6-21. Efficiency versus Load



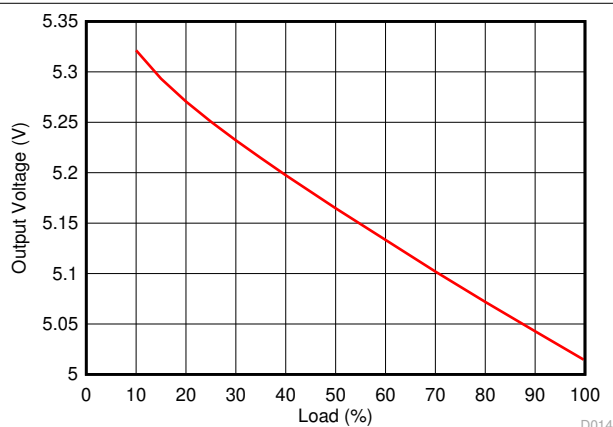
A. DCP021515P **Note:** Operations under 10% Load

图 6-22. Load Regulation



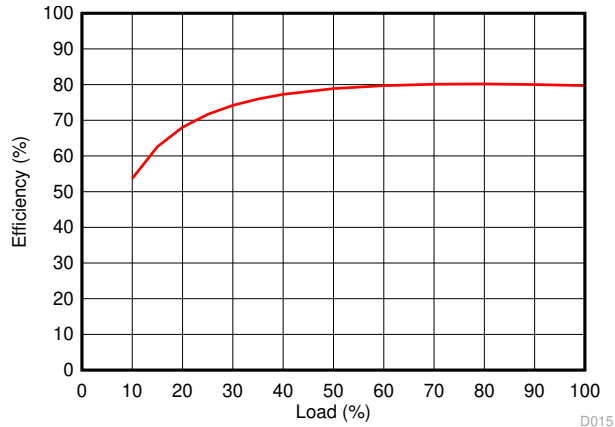
A. DCP022405P

图 6-23. Efficiency versus Load



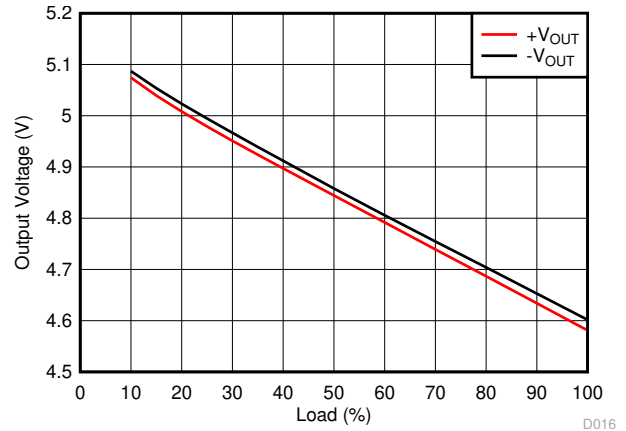
A. DCP022405P **Note:** Operations under 10% Load

图 6-24. Load Regulation



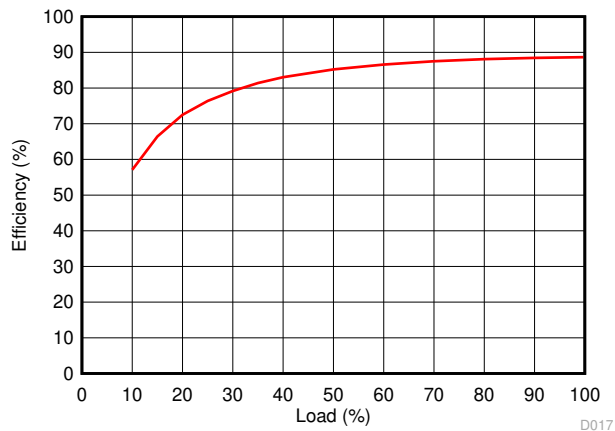
A. DCP022405DP

图 6-25. Efficiency versus Load



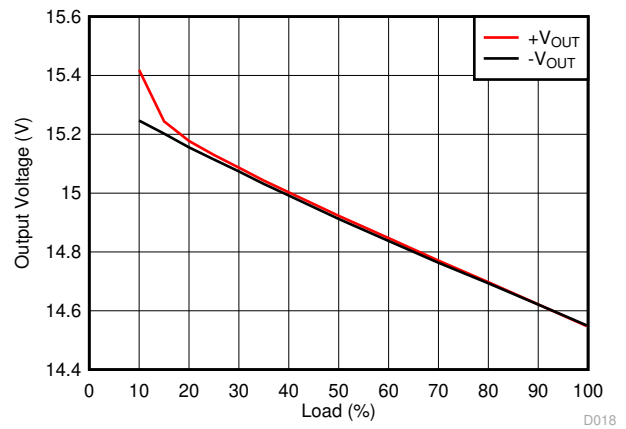
A. DCP022405DP **Note:** Operations under 10% Load

图 6-26. Load Regulation



A. DCP022415DP

图 6-27. Efficiency versus Load



A. DCP022415DP **Note:** Operations under 10% Load

图 6-28. Load Regulation

## 7 Detailed Description

### 7.1 Overview

The DCP02 offers up to 2 W of isolated, unregulated output power from a 5-V, 12-V, 15-V, or 24-V input source with a typical efficiency of up to 89%. This efficiency is achieved through highly integrated packaging technology and the implementation of a custom power stage and control device. The DCP02 devices are specified for operational isolation only. The circuit design uses an advanced BiCMOS and DMOS process.

### 7.2 Functional Block Diagrams

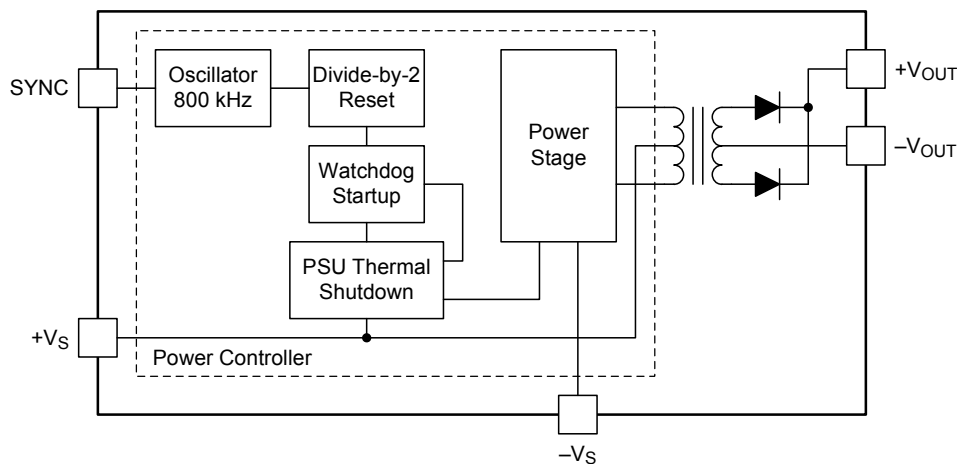


图 7-1. Single Output Device

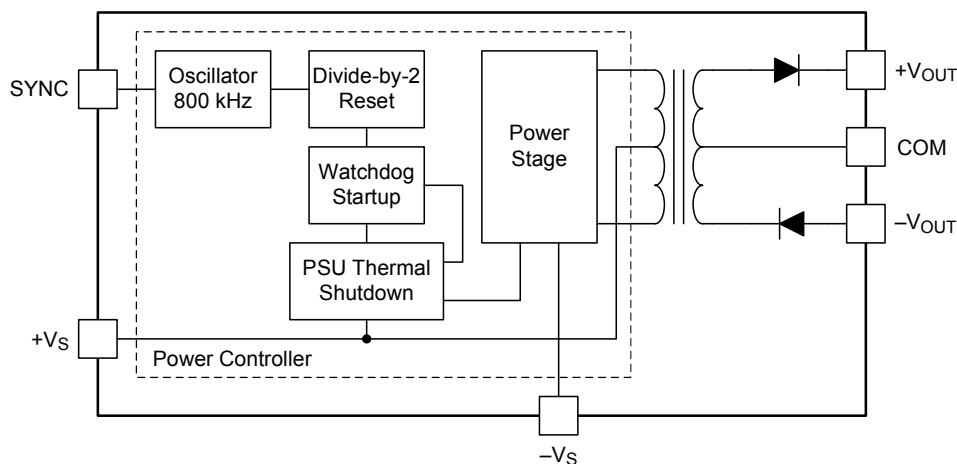


图 7-2. Dual Output Device

## 7.3 Feature Description

### 7.3.1 Isolation

Underwriters Laboratories, UL™ defines several classes of isolation that are used in modern power supplies.

*Safety extra low voltage* (SELV) is defined by UL (UL1950 E199929) as a secondary circuit which is so designated and protected that under normal and single fault conditions the voltage between any two accessible parts, or between an accessible part and the equipment earthing terminal for operational isolation does not exceed steady state 42.5 V peak or 60 V<sub>DC</sub> for more than 1 second.

#### 7.3.1.1 Operation or Functional Isolation

Operational or functional isolation is defined by the use of a high-potential (hipot) test only. Typically, this isolation is defined as the use of insulated wire in the construction of the transformer as the primary isolation barrier. The hipot one-second duration test (dielectric voltage, withstand test) is a production test used to verify that the isolation barrier is functioning. Products with operational isolation should never be used as an element in a safety-isolation system.

#### 7.3.1.2 Basic or Enhanced Isolation

Basic or enhanced isolation is defined by specified creepage and clearance limits between the primary and secondary circuits of the power supply. Basic isolation is the use of an isolation barrier in addition to the insulated wire in the construction of the transformer. Input and output circuits must also be physically separated by specified distances.

#### 7.3.1.3 Continuous Voltage

For a device that has no specific safety agency approvals (operational isolation), the continuous voltage that can be applied across the part in normal operation is less than 42.5 V<sub>RMS</sub> or 60 V<sub>DC</sub>. Ensure that both input and output voltages maintain normal SELV limits. The isolation test voltage represents a measure of immunity to transient voltages.

#### WARNING

Do not use the device as an element of a safety isolation system that exceeds the SELV limit.

If the device is expected to function correctly with more than 42.5 V<sub>RMS</sub> or 60 V<sub>DC</sub> applied continuously across the isolation barrier, then the circuitry on both sides of the barrier must be regarded as operating at an unsafe voltage, and further isolation or insulation systems must form a barrier between these circuits and any user-accessible circuitry according to safety standard requirements.

#### 7.3.1.4 Isolation Voltage

*Hipot test, flash-tested, withstand voltage, proof voltage, dielectric withstand voltage, and isolation test voltage* are all terms that relate to the same thing: a test voltage applied for a specified time across a component designed to provide electrical isolation to verify the integrity of that isolation. TI's DCP02 series of dc-dc converters are all 100% production tested at 1.0 kV<sub>AC</sub> for one second.

#### 7.3.1.5 Repeated High-Voltage Isolation Testing

Repeated high-voltage isolation testing of a barrier component can degrade the isolation capability, depending on materials, construction, and environment. The DCP02 series of dc-dc converters have toroidal, enameled, wire isolation transformers with no additional insulation between the primary and secondary windings. While a device can be expected to withstand several times the stated test voltage, the isolation capability depends on the wire insulation. Any material, including this enamel (typically polyurethane), is susceptible to eventual chemical degradation when subject to very-high applied voltages. Therefore, strictly limit the number of high-voltage tests and repeated high-voltage isolation testing. However, if it is absolutely required, reduce the voltage by 20% from specified test voltage with a duration limit of one second per test.

### 7.3.2 Power Stage

The DCP02 series of devices use a push-pull, center-tapped topology. The DCP02 devices switch at 400 kHz (divide-by-2 from an 800-kHz oscillator).

### 7.3.3 Oscillator And Watchdog Circuit

The onboard, 800-kHz oscillator generates the switching frequency via a divide-by-2 circuit. The oscillator can be synchronized to other DCP02-series device circuits or an external source, and is used to minimize system noise.

A watchdog circuit checks the operation of the oscillator circuit. The oscillator can be disabled by pulling the SYNC pin low. When the SYNC pin goes low, the output pins transition into tri-state mode, which occurs within 2  $\mu$ s.

### 7.3.4 Thermal Shutdown

The DCP02 series of devices are protected by a thermal-shutdown circuit.

If the on-chip temperature rises above 150°C, the device shuts down. Normal operation resumes as soon as the temperature falls below 150°C.

### 7.3.5 Synchronization

In the event that more than one DC/DC converter is needed onboard, beat frequencies and other electrical interference can be generated. This interference occurs because of the small variations in switching frequencies between the DC/DC converters.

The DCP02 series of devices overcome this interference by allowing devices to be synchronized to one another. Up to eight devices can be synchronized by connecting the SYNC pins together, taking care to minimize the capacitance of tracking. Stray capacitance (greater than 3 pF) has the effect of reducing the switching frequency, or even stopping the oscillator circuit. The maximum recommended voltage applied to the SYNC pin is 3.0 V.

For an application that uses more than eight synchronized devices use an external device to drive the SYNC pins. The application report [External Synchronization of the DCP01/02 Series of DC/DC Converters](#) describes this configuration.

#### Note

**During the start-up period, all synchronized devices draw maximum current from the input simultaneously. If the input voltage falls below approximately 4 V, the devices may not start up. A 2.2-  $\mu$ F capacitor should be connected close to each device's input pin.**

### 7.3.6 Light Load Operation (< 10%)

Operation below 10% load can cause the output voltage to increase up to double the typical output voltage. For applications that operate less than 10% of rated output current, it is recommended to add a minimum load to ensure the output voltage of the device is within the load regulation range. For example, connect a 125- $\Omega$  pre-load resistor to meet the 10% minimum load condition for the DCP020505P.

### 7.3.7 Load Regulation (10% to 100%)

The load regulation of the DCP02 series of devices is specified at 10% to 100% load placing a minimum 10% load will ensure the output voltage is within the range specified in the [# 6.5](#) table. For more information regarding operation below 10% load, see the [# 7.3.6](#) section.

### 7.3.8 Construction

The basic construction of the DCP02 series of devices is the same as standard integrated circuits. The molded package contains no substrate. The DCP02 series of devices are constructed using an IC, rectifier diodes, and a wound magnetic toroid on a leadframe. Because the package contains no solder, the devices do not require any special printed circuit board (PCB) assembly processing. This architecture results in an isolated DC/DC converter with inherently high reliability.

### 7.3.9 Thermal Management

Due to the high power density of this device, it is advisable to provide ground planes on the input and output.

### 7.3.10 Power-Up Characteristics

The DCP02 series of devices do not include a soft-start feature. Therefore, a high in-rush current during power up is expected. To ensure a more stable start-up, allow the input voltage to be in regulation before enabling the device. 图 7-6 shows the typical start-up waveform for a DCP020505P when enabled after the input voltage is in regulation. 图 7-3 shows the typical start-up waveform for a DCP020505P, operating from a 5-V input with no load on the output. 图 7-4 shows the start-up waveform for a DCP020505P starting up into a 10% load. 图 7-5 shows the start-up waveform into a full (100%) load.

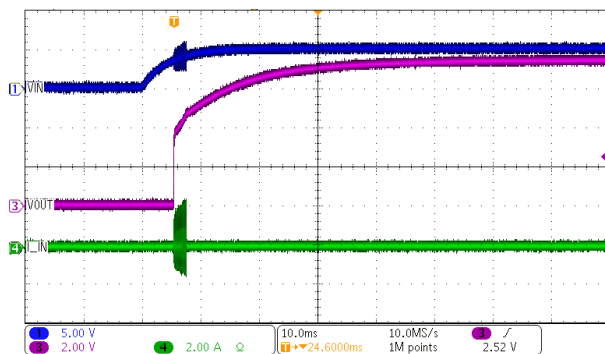


图 7-3. DCP020505P Start-Up at No Load

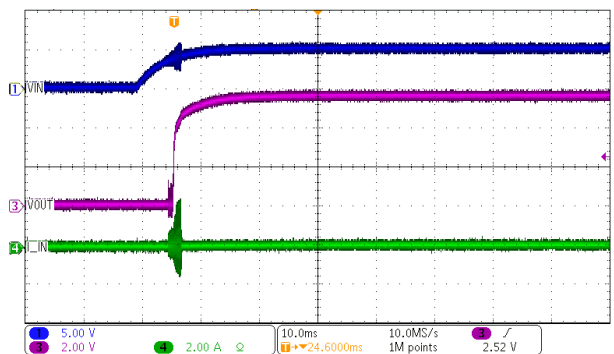


图 7-4. DCP020505P Start-Up at 10% Load

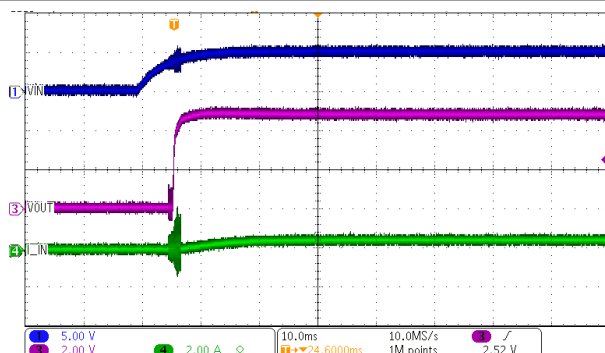


图 7-5. DCP020505P Start-Up at 100% Load

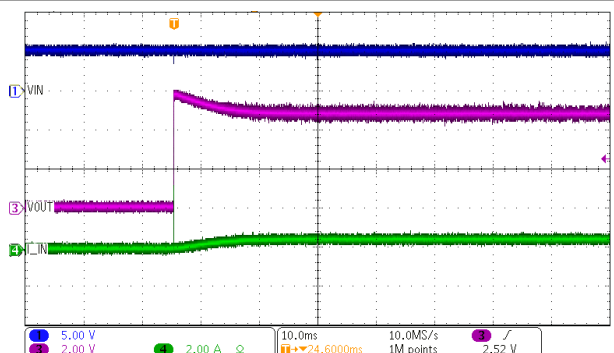


图 7-6. DCP020505P Enable Start-Up at 100% Load

## 7.4 Device Functional Modes

### 7.4.1 Disable/Enable (SYNC pin)

Any of the DCP02 series devices can be disabled or enabled by driving the SYNC pin using an open drain CMOS gate. If the SYNC pin is pulled low, the DCP02 becomes disabled. The disable time depends upon the external loading. The internal disable function is implemented in 2  $\mu$ s. Removal of the pull down causes the DCP02 to be enabled.

Capacitive loading on the SYNC pin should be minimized ( $\leq 3$  pF) in order to prevent a reduction in the oscillator frequency. The application report [External Synchronization of the DCP01/02 Series of DC/DC Converters](#) describes disable/enable control circuitry.

### 7.4.2 Decoupling

#### 7.4.2.1 Ripple Reduction

The high switching frequency of 400 kHz allows simple filtering. To reduce ripple, it is recommended that a minimum of 1- $\mu$ F capacitor be used on the  $V_{OUT}$  pin. For dual output devices, decouple both of the outputs to the COM pin. A 2.2- $\mu$ F capacitor on the input is also recommended.

#### 7.4.2.2 Connecting the DCP02 in Series

Multiple DCP02 isolated 2W DC/DC converters can be connected in series to provide non-standard voltage rails. This configuration is possible by using the floating outputs provided by the galvanic isolation of the DCP02.

Connect the  $+V_{OUT}$  from one DCP02 to the  $-V_{OUT}$  of another (see [Figure 7-7](#)). If the SYNC pins are tied together, the self-synchronization feature of the DCP02 prevents beat frequencies on the voltage rails. The SYNC feature of the DCP02 allows easy series connection without external filtering, thus minimizing cost.

The outputs of a dual-output DCP02 can also be connected in series to provide two times the magnitude of  $V_{OUT}$ , as shown in [Figure 7-8](#). For example, connect a dual-output, 15-V, DCP022415D device to provide a 30-V rail.

All 5-V, 12-V, and 15-V input voltage designs require a 2.2- $\mu$ F, low-ESR ceramic input capacitor, while 24-V input applications require only 0.47  $\mu$ F of input capacitance.

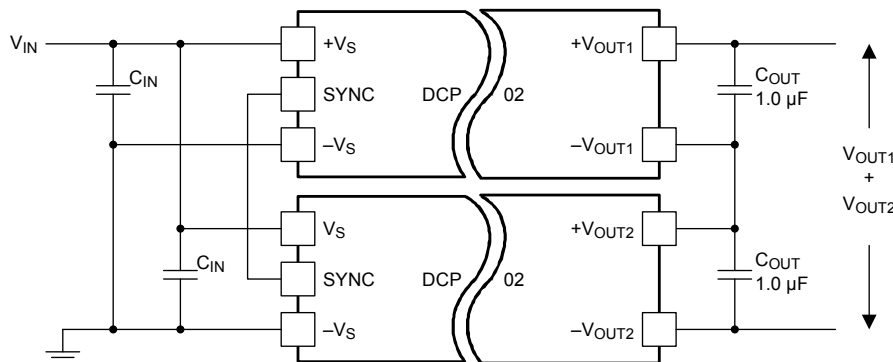


图 7-7. Multiple DCP02 Devices Connected in Series

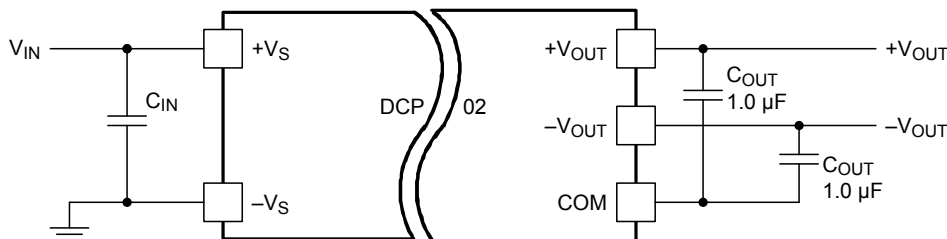


图 7-8. Dual Output Devices Connected in Series



### 7.4.2.3 Connecting the DCP02 in Parallel

If the output power from one DCP02 is not sufficient, it is possible to parallel the outputs of multiple DCP02s, as shown in 图 7-9, (applies to single output devices only). The SYNC feature allows easy synchronization to prevent power-rail beat frequencies at no additional filtering cost.

All 5-V, 12-V, and 15-V input voltage designs require a 2.2-  $\mu$ F, low-ESR, ceramic input capacitor, while 24-V input applications require only 0.47  $\mu$ F of input capacitance.

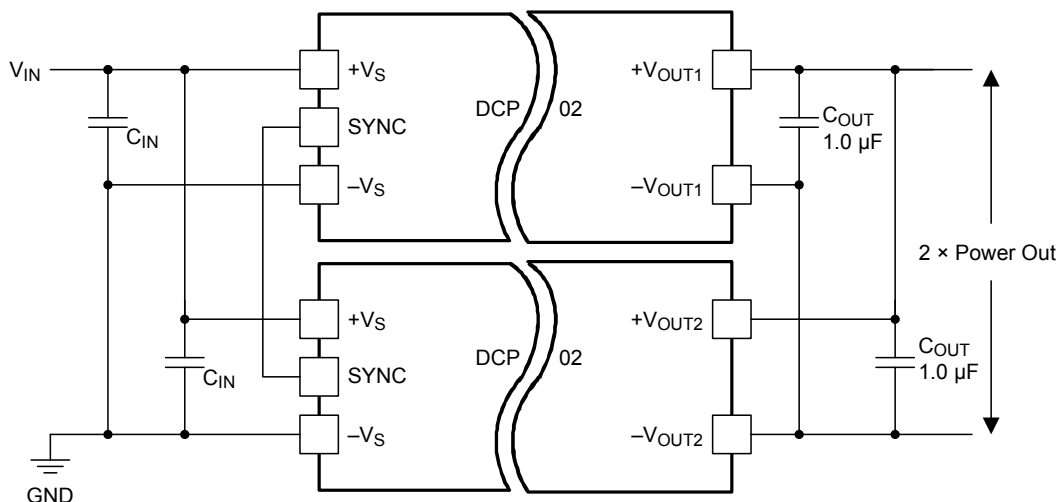
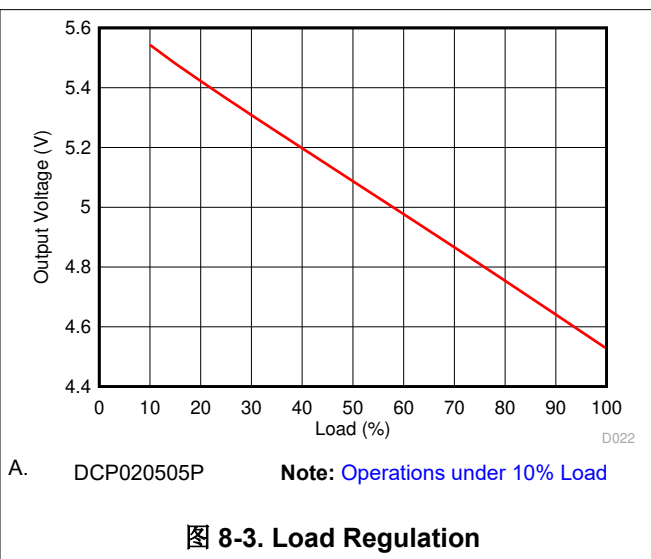
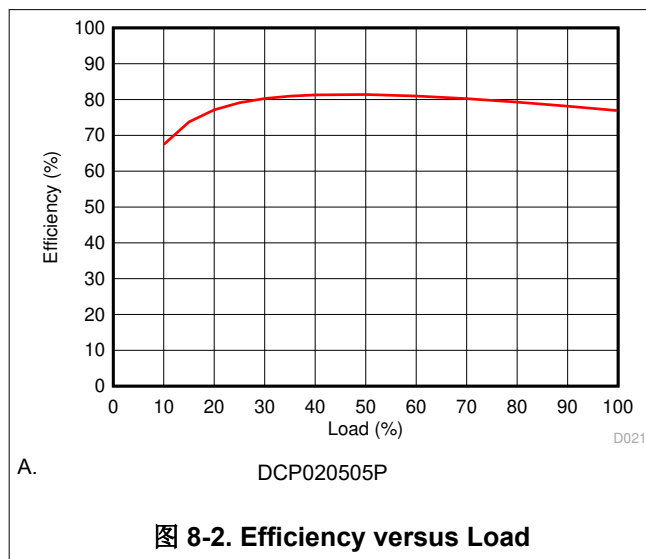


图 7-9. Multiple DCP02 Devices Connected in Parallel



### 8.2.3 DCP020505 Application Curves



### 8.2.4 PCB Design

The copper losses (resistance and inductance) can be minimized by the use of mutual ground and power planes (tracks) where possible. If that is not possible, use wide tracks to reduce the losses. If several devices are being powered from a common power source, a star-connected system for the track must be deployed; devices must not be connected in series, as this will cascade the resistive losses. The position of the decoupling capacitors is important. They must be as close to the devices as possible in order to reduce losses. See the [PCB Layout](#) section for more details.

### 8.2.5 Decoupling Ceramic Capacitors

All capacitors have losses because of internal equivalent series resistance (ESR), and to a lesser degree, equivalent series inductance (ESL). Values for ESL are not always easy to obtain. However, some manufacturers provide graphs of frequency versus capacitor impedance. These graphs typically show the capacitor impedance falling as frequency is increased (as shown in 图 8-4). In 图 8-4,  $X_C$  is the reactance due to the capacitance,  $X_L$  is the reactance due to the ESL, and  $f_0$  is the resonant frequency. As the frequency increases, the impedance stops decreasing and begins to rise. The point of minimum impedance indicates the resonant frequency of the capacitor. This frequency is where the components of capacitance and inductance reactance are of equal magnitude. Beyond this point, the capacitor is not effective as a capacitor.

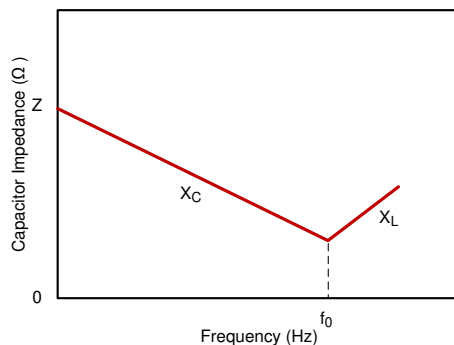


图 8-4. Capacitor Impedance versus Frequency

At  $f_0$ ,  $X_C = X_L$ ; however, there is a  $180^\circ$  phase difference resulting in cancellation of the imaginary component. The resulting effect is that the impedance at the resonant point is the real part of the complex impedance;

namely, the value of the ESR. The resonant frequency must be well above the 800-kHz switching frequency of the DCP and DCVs.

The effect of the ESR is to cause a voltage drop within the capacitor. The value of this voltage drop is simply the product of the ESR and the transient load current, as shown in [方程式 1](#).

$$V_{IN} = V_{PK} - (ESR \times I_{TR}) \quad (1)$$

where

- $V_{IN}$  is the voltage at the device input
- $V_{PK}$  is the maximum value of the voltage on the capacitor during charge
- $I_{TR}$  is the transient load current

The other factor that affects the performance is the value of the capacitance. However, for the input and the full wave outputs (single-output voltage devices), ESR is the dominant factor.

### 8.2.6 Input Capacitor and the Effects of ESR

If the input decoupling capacitor is not ceramic (and has an ESR greater than 20 mΩ), then at the instant the power transistors switch on, the voltage at the input pins falls momentarily. If the voltage falls below approximately 4 V, the DCP detects an undervoltage condition and switches the DCP drive circuits to the off state. This detection is carried out as a precaution against a genuine low input voltage condition that could slow down or even stop the internal circuits from operating correctly. A slow-down or stoppage results in the drive transistors being turned on too long, causing saturation of the transformer and destruction of the device.

Following detection of a low input voltage condition, the device switches off the internal drive circuits until the input voltage returns to a safe value, at which time the device tries to restart. If the input capacitor is still unable to maintain the input voltage, shutdown recurs. This process repeats until the input capacitor charges sufficiently to start the device correctly.

Normal start-up should occur in approximately 1 ms after power is applied to the device. If a considerably longer start-up duration time is encountered, it is likely that either (or both) the input supply or the capacitors are not performing adequately.

For 5-V to 15-V input devices, a 2.2-μF, low-ESR ceramic capacitor ensures a good start-up performance. For 24-V input voltage devices, 0.47 μF ceramic capacitors are recommended. Tantalum capacitors are not recommended, since most do not have low-ESR values and will degrade performance. If tantalum capacitors must be used, close attention must be paid to both the ESR and voltage as derated by the vendor.

#### Note

**During the start-up period, these devices may draw maximum current from the input supply. If the input voltage falls below approximately 4 V, the devices may not start up. Connect a 2.2-μF ceramic capacitor close to the input pins.**

### 8.2.7 Ripple and Noise

A good quality, low-ESR ceramic capacitor placed as close as practical across the input reduces reflected ripple and ensures a smooth startup.

A good quality, low-ESR ceramic capacitor placed as close as practical across the rectifier output terminal and output ground gives the best ripple and noise performance. See application report [DC-to-DC Converter Noise Reduction](#) for more information on noise rejection.

#### 8.2.7.1 Output Ripple Calculation Example

The following example shows that increasing the capacitance has a much smaller effect on the output ripple voltage than does reducing the value of the ESR for the filter capacitor.

To calculate the output ripple for a DCP020505 device:

- $V_{OUT} = 5 \text{ V}$
- $I_{OUT} = 0.4 \text{ A}$

- At full output power, the load resistor is  $12.5\ \Omega$
- Output capacitor of  $1\ \mu\text{F}$ , ESR of  $0.1\ \Omega$
- Capacitor discharge time 1% of 800-kHz (ripple frequency)

$$t_{\text{DIS}} = 0.0125\ \mu\text{s}$$

$$\tau = C \times R_{\text{LOAD}}$$

$$\tau = 1 \times 10^{-6} \times 12.5 = 12.5\ \mu\text{s}$$

$$V_{\text{DIS}} = V_{\text{O}}(1 - \text{EXP}(-t_{\text{DIS}} / \tau))$$

$$V_{\text{DIS}} = 5\ \text{mV}$$

By contrast, the voltage dropped because of ESR:

$$V_{\text{ESR}} = I_{\text{LOAD}} \times \text{ESR}$$

$$V_{\text{ESR}} = 40\ \text{mV}$$

$$\text{Ripple voltage} = 45\ \text{mV}$$

### 8.2.8 Dual DCP02 Output Voltage

The voltage output for dual DCP02 devices is half wave rectified; therefore, the discharge time is  $1.25\ \mu\text{s}$ . Repeating the above calculations using the 100% load resistance of  $25\ \Omega$  (0.2 A per output), the results are:

$$\tau = 25\ \mu\text{s}$$

$$t_{\text{DIS}} = 1.25\ \mu\text{s}$$

$$V_{\text{DIS}} = 244\ \text{mV}$$

$$V_{\text{ESR}} = 20\ \text{mV}$$

$$\text{Ripple Voltage} = 266\ \text{mV}$$

This time, it is the capacitor discharging that contributes to the largest component of ripple. Changing the output filter to  $10\ \mu\text{F}$ , and repeating the calculations, the result is:

$$\text{Ripple Voltage} = 45\ \text{mV}$$

This value is composed of almost equal components.

The previous calculations are offered as a guideline only. Capacitor parameters usually have large tolerances and can be susceptible to environmental conditions.

### 8.2.9 Optimizing Performance

Optimum performance can only be achieved if the device is correctly supported. The very nature of a switching converter requires power to be instantly available when it switches on. If the converter has DMOS switching transistors, the fast edges will create a high current demand on the input supply. This transient load placed on the input is supplied by the external input decoupling capacitor, thus maintaining the input voltage. Therefore, the input supply does not see this transient (this is an analogy to high-speed digital circuits). The positioning of the capacitor is critical and must be placed as close as possible to the input pins and connected by a low-impedance path.

The optimum performance primarily depends on two factors:

- Connection of the input and output circuits for minimal loss.
- The ability of the decoupling capacitors to maintain the input and output voltages at a constant level.

## Power Supply Recommendations

The DCP02 is a switching power supply, and as such can place high peak current demands on the input supply. In order to avoid the supply falling momentarily during the fast switching pulses, ground and power planes must

be used to connect the power to the input of DCP02. If this connection is not possible, then the supplies must be connected in a star formation with the traces made as wide as possible.

## 8 Layout

### 8.1 Layout Guidelines

Due to the high power density of these devices, provide ground planes on the input and output.

图 8-4 和 图 8-2 illustrate a printed circuit board (PCB) layout for the two conventional (DCP01/02, DCP01), and two SOP surface-mount packages (DCP02U). 图 8-1 shows the schematic.

Including input power and ground planes provides a low-impedance path for the input power. For the output, the COM signal connects via a ground plane, while the connections for the positive and negative voltage outputs conduct through wide traces in order to minimize losses.

The output should be taken from the device using ground and power planes, thereby ensuring minimum losses.

The location of the decoupling capacitors in close proximity to their respective pins ensures low losses due to the effects of stray inductance, thus improving the ripple performance. This location is of particular importance to the input decoupling capacitor, because this capacitor supplies the transient current associated with the fast switching waveforms of the power drive circuits.

Allow the unused SYNC pin, to remain configured as a floating pad. It is advisable to place a guard ring (connected to input ground) or annulus connected around this pin to avoid any noise pick up. When connecting a SYNC pin to one or more SYNC design the linking trace to be short and narrow to avoid stray capacitance. Ensure that no other trace is in close proximity to this trace SYNC trace to decrease the stray capacitance on this pin. The stray capacitance affects the performance of the oscillator.

### 8.2 Layout Example

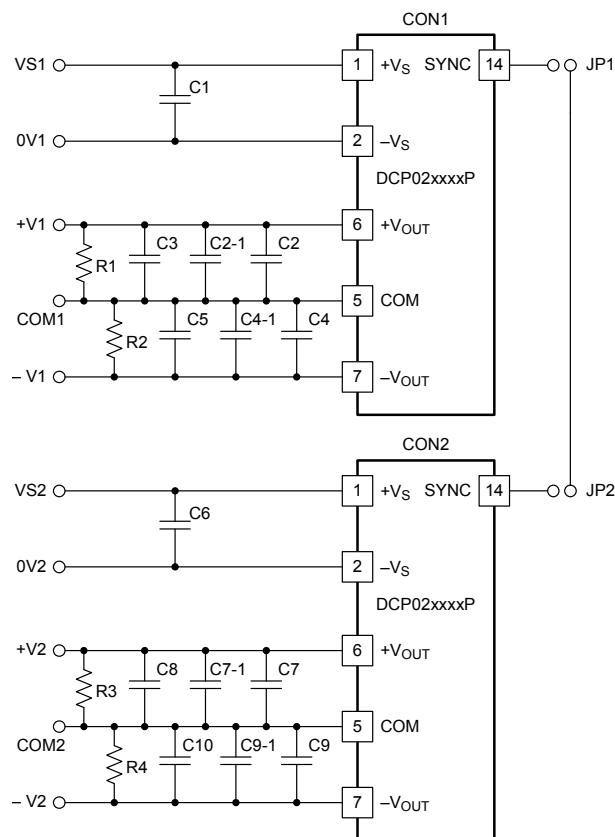


图 8-1. PCB Schematic, P Package

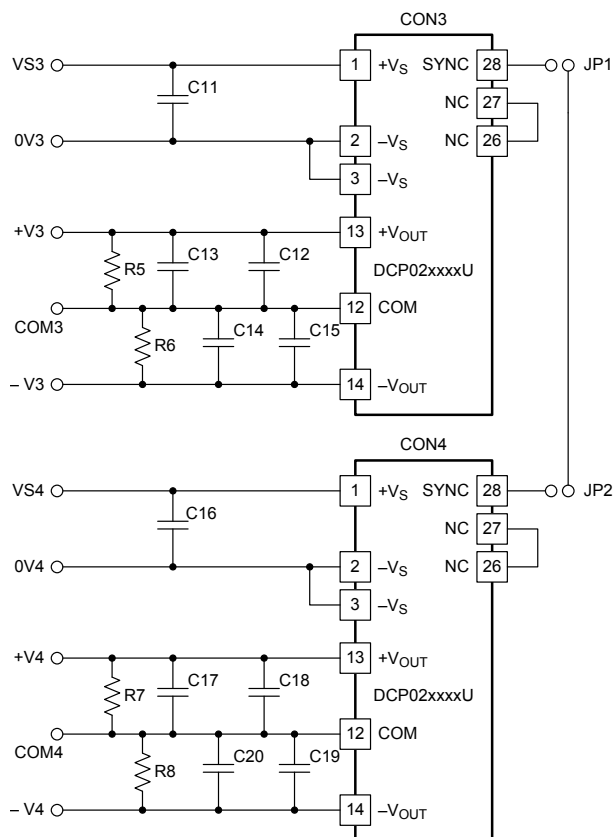


图 8-2. PCB Schematic, U Package



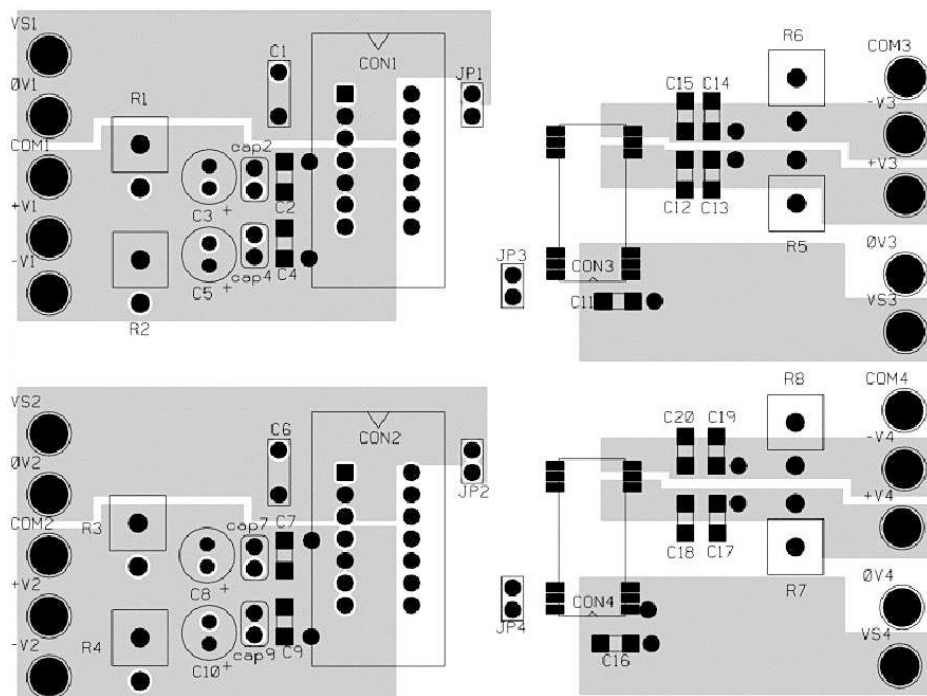


图 8-3. PCB Layout Example, Component-Side View

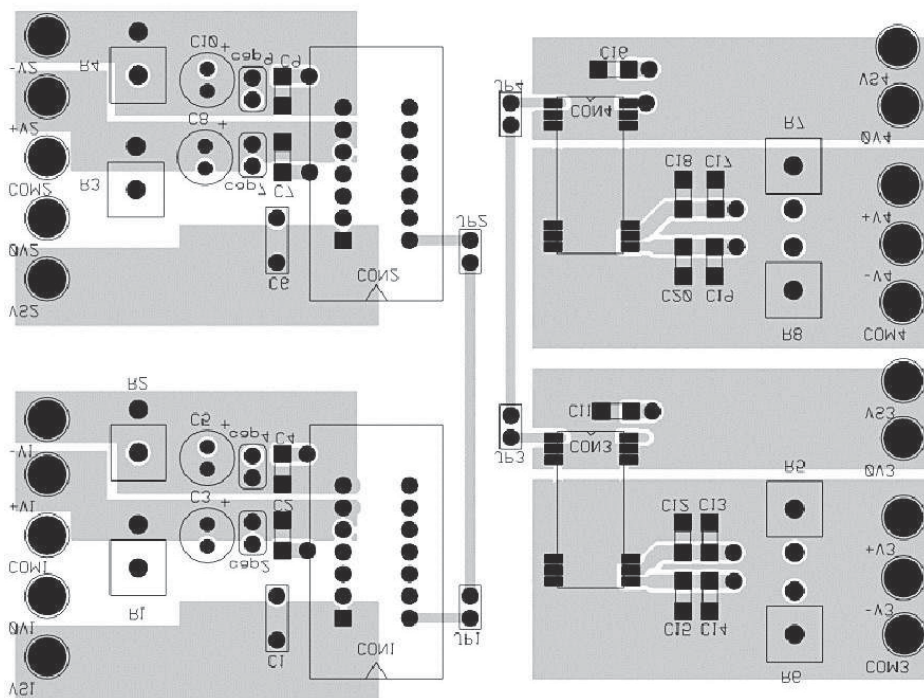


图 8-4. PCB Layout Example, Non-Component-Side View

## 9 Device and Documentation Support

### 9.1 Device Support

#### 9.1.1 Device Nomenclature

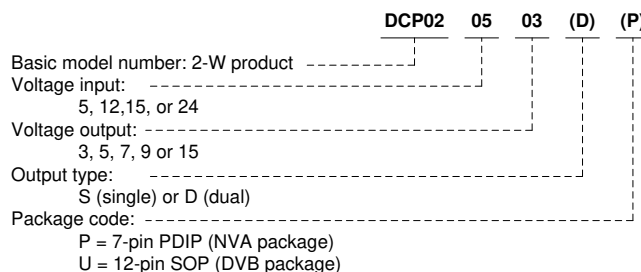


图 9-1. Supplemental Ordering Information

### 9.2 Documentation Support

#### 9.2.1 Related Documentation

- Texas Instruments, [DC-to-DC Converter Noise Reduction](#)
- Texas Instruments, [External Synchronization of the DCP01/02 Series of DC/DC Converters](#)
- Texas Instruments, [Optimizing Performance of the DCP01/02 Series of DC/DC Converters](#)

### 9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

## 9.4 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 9-1. Related Links**

| PARTS      | PRODUCT FOLDER             | SAMPLE & BUY               | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| DCP020503  | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| DCP020505  | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| DCP020507  | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| DCP020509  | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| DCP020515D | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| DCP021205  | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| DCP021212  | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| DCP021212D | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| DCP021515  | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| DCP022405  | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| DCP022405D | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| DCP022415D | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

## 9.5 Trademarks

Underwriters Laboratories, UL™ is a trademark of UL LLC.

TI E2E™ is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

## 9.6 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.7 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.8 Glossary

### TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

## Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable<br>part number       | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|--------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">DCP020503P</a>     | Active        | Production           | PDIP (NVA)   7 | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | DCP020503P          |
| <a href="#">DCP020503U</a>     | Active        | Production           | SOP (DVB)   12 | 28   TUBE             | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | DCP020503U          |
| <a href="#">DCP020505P</a>     | Active        | Production           | PDIP (NVA)   7 | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | DCP020505P          |
| <a href="#">DCP020505U</a>     | Active        | Production           | SOP (DVB)   12 | 28   TUBE             | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | DCP020505U          |
| <a href="#">DCP020505U/1K</a>  | Active        | Production           | SOP (DVB)   12 | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | DCP020505U          |
| <a href="#">DCP020505UE4</a>   | Active        | Production           | SOP (DVB)   12 | 28   TUBE             | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | DCP020505U          |
| <a href="#">DCP020507P</a>     | Active        | Production           | PDIP (NVA)   7 | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | DCP020507P          |
| <a href="#">DCP020507U</a>     | Active        | Production           | SOP (DVB)   12 | 28   TUBE             | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | DCP020507U          |
| <a href="#">DCP020507U/1K</a>  | Active        | Production           | SOP (DVB)   12 | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | DCP020507U          |
| <a href="#">DCP020509P</a>     | Active        | Production           | PDIP (NVA)   7 | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | DCP020509P          |
| <a href="#">DCP020509U</a>     | Active        | Production           | SOP (DVB)   12 | 28   TUBE             | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | DCP020509U          |
| <a href="#">DCP020515DP</a>    | Active        | Production           | PDIP (NVA)   7 | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | DCP020515DP         |
| <a href="#">DCP020515DU</a>    | Active        | Production           | SOP (DVB)   12 | 28   TUBE             | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | DCP020515DU         |
| <a href="#">DCP020515DU/1K</a> | Active        | Production           | SOP (DVB)   12 | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | DCP020515DU         |
| <a href="#">DCP021205P</a>     | Active        | Production           | PDIP (NVA)   7 | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | DCP021205P          |
| <a href="#">DCP021205U</a>     | Active        | Production           | SOP (DVB)   12 | 28   TUBE             | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | DCP021205U          |
| <a href="#">DCP021205U/1K</a>  | Active        | Production           | SOP (DVB)   12 | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | DCP021205U          |
| <a href="#">DCP021212DP</a>    | Active        | Production           | PDIP (NVA)   7 | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | DCP021212DP         |
| <a href="#">DCP021212DU</a>    | Active        | Production           | SOP (DVB)   12 | 28   TUBE             | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | DCP021212DU         |
| <a href="#">DCP021212DU/1K</a> | Active        | Production           | SOP (DVB)   12 | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | DCP021212DU         |
| <a href="#">DCP021212P</a>     | Active        | Production           | PDIP (NVA)   7 | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | DCP021212P          |
| <a href="#">DCP021212U</a>     | Active        | Production           | SOP (DVB)   12 | 28   TUBE             | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | DCP021212U          |
| <a href="#">DCP021212U/1K</a>  | Active        | Production           | SOP (DVB)   12 | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | DCP021212U          |
| <a href="#">DCP021515P</a>     | Active        | Production           | PDIP (NVA)   7 | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | DCP021515P          |
| <a href="#">DCP021515U</a>     | Active        | Production           | SOP (DVB)   12 | 28   TUBE             | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | DCP021515U          |
| <a href="#">DCP021515U/1K</a>  | Active        | Production           | SOP (DVB)   12 | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | DCP021515U          |
| <a href="#">DCP022405DP</a>    | Active        | Production           | PDIP (NVA)   7 | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | DCP022405DP         |
| <a href="#">DCP022405DU</a>    | Active        | Production           | SOP (DVB)   12 | 28   TUBE             | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | DCP022405DU         |
| <a href="#">DCP022405P</a>     | Active        | Production           | PDIP (NVA)   7 | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | DCP022405P          |

| Orderable part number          | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|--------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">DCP022405U</a>     | Active        | Production           | SOP (DVB)   12 | 28   TUBE             | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | DCP022405U          |
| <a href="#">DCP022415DP</a>    | Active        | Production           | PDIP (NVA)   7 | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | DCP022415DP         |
| <a href="#">DCP022415DU</a>    | Active        | Production           | SOP (DVB)   12 | 28   TUBE             | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | DCP022415DU         |
| <a href="#">DCP022415DU/1K</a> | Active        | Production           | SOP (DVB)   12 | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | DCP022415DU         |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

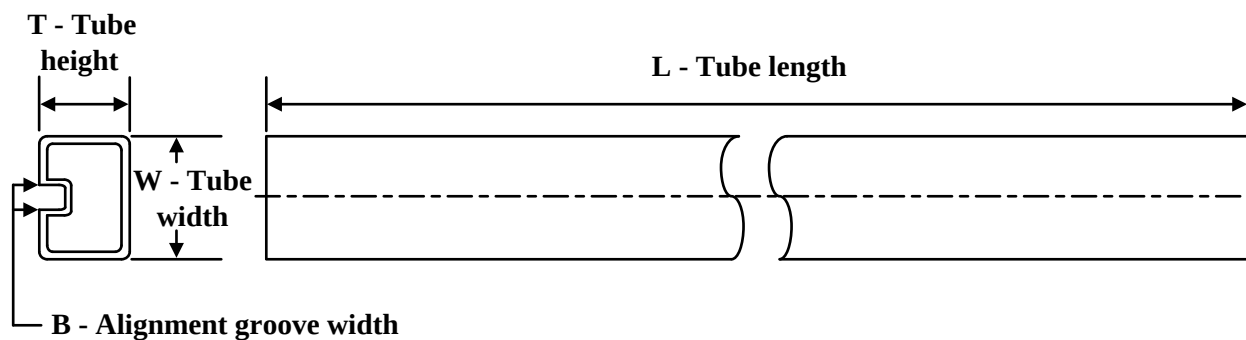
<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TUBE**


\*All dimensions are nominal

| Device       | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|--------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| DCP020503P   | NVA          | PDIP         | 7    | 25  | 533.4  | 14.33  | 13.03  | 8.07   |
| DCP020503U   | DVB          | SOP          | 12   | 28  | 532.13 | 14.73  | 5.13   | 6.6    |
| DCP020505P   | NVA          | PDIP         | 7    | 25  | 533.4  | 14.33  | 13.03  | 8.07   |
| DCP020505U   | DVB          | SOP          | 12   | 28  | 532.13 | 14.73  | 5.13   | 6.6    |
| DCP020505UE4 | DVB          | SOP          | 12   | 28  | 532.13 | 14.73  | 5.13   | 6.6    |
| DCP020507P   | NVA          | PDIP         | 7    | 25  | 533.4  | 14.33  | 13.03  | 8.07   |
| DCP020507U   | DVB          | SOP          | 12   | 28  | 532.13 | 14.73  | 5.13   | 6.6    |
| DCP020509P   | NVA          | PDIP         | 7    | 25  | 533.4  | 14.33  | 13.03  | 8.07   |
| DCP020509U   | DVB          | SOP          | 12   | 28  | 532.13 | 14.73  | 5.13   | 6.6    |
| DCP020515DP  | NVA          | PDIP         | 7    | 25  | 533.4  | 14.33  | 13.03  | 8.07   |
| DCP020515DU  | DVB          | SOP          | 12   | 28  | 532.13 | 14.73  | 5.13   | 6.6    |
| DCP021205P   | NVA          | PDIP         | 7    | 25  | 533.4  | 14.33  | 13.03  | 8.07   |
| DCP021205U   | DVB          | SOP          | 12   | 28  | 532.13 | 14.73  | 5.13   | 6.6    |
| DCP021212DP  | NVA          | PDIP         | 7    | 25  | 533.4  | 14.33  | 13.03  | 8.07   |
| DCP021212DU  | DVB          | SOP          | 12   | 28  | 532.13 | 14.73  | 5.13   | 6.6    |
| DCP021212P   | NVA          | PDIP         | 7    | 25  | 533.4  | 14.33  | 13.03  | 8.07   |
| DCP021212U   | DVB          | SOP          | 12   | 28  | 532.13 | 14.73  | 5.13   | 6.6    |
| DCP021515P   | NVA          | PDIP         | 7    | 25  | 533.4  | 14.33  | 13.03  | 8.07   |
| DCP021515U   | DVB          | SOP          | 12   | 28  | 532.13 | 14.73  | 5.13   | 6.6    |
| DCP022405DP  | NVA          | PDIP         | 7    | 25  | 533.4  | 14.33  | 13.03  | 8.07   |
| DCP022405DU  | DVB          | SOP          | 12   | 28  | 532.13 | 14.73  | 5.13   | 6.6    |
| DCP022405P   | NVA          | PDIP         | 7    | 25  | 533.4  | 14.33  | 13.03  | 8.07   |
| DCP022405U   | DVB          | SOP          | 12   | 28  | 532.13 | 14.73  | 5.13   | 6.6    |
| DCP022415DP  | NVA          | PDIP         | 7    | 25  | 533.4  | 14.33  | 13.03  | 8.07   |
| DCP022415DU  | DVB          | SOP          | 12   | 28  | 532.13 | 14.73  | 5.13   | 6.6    |



## PACKAGE OUTLINE

**SOP - 2.65 mm max height**

PLASTIC SMALL OUTLINE



1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-013.



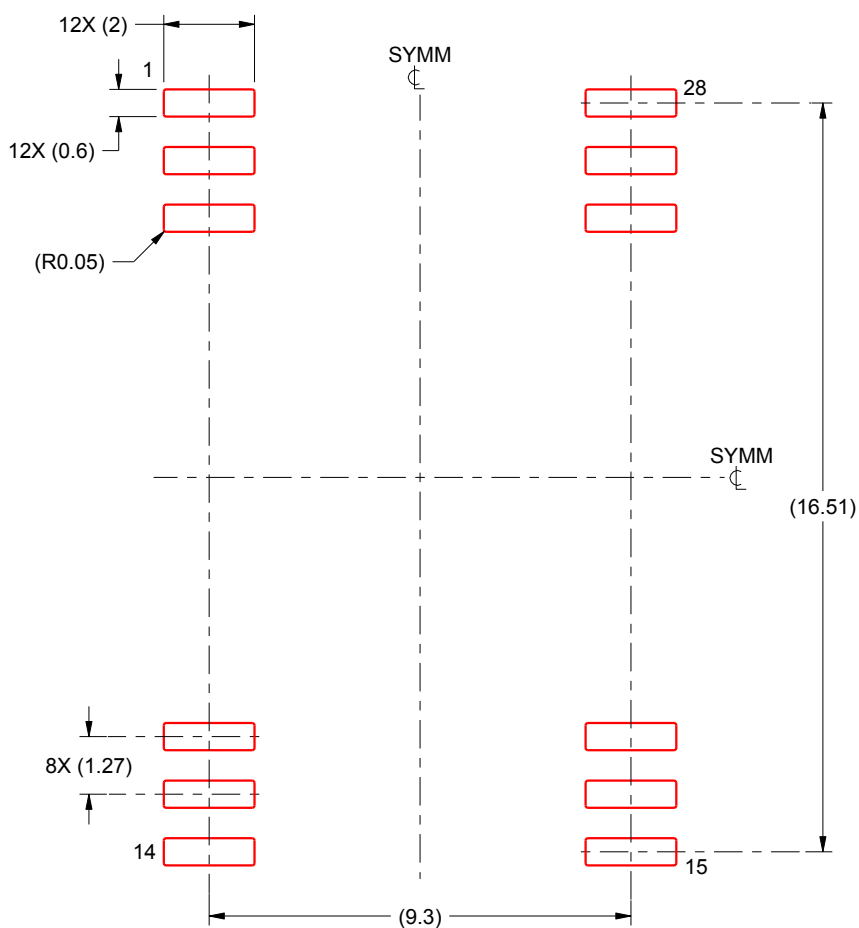


# EXAMPLE STENCIL DESIGN

DVB0012A

SOP - 2.65 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

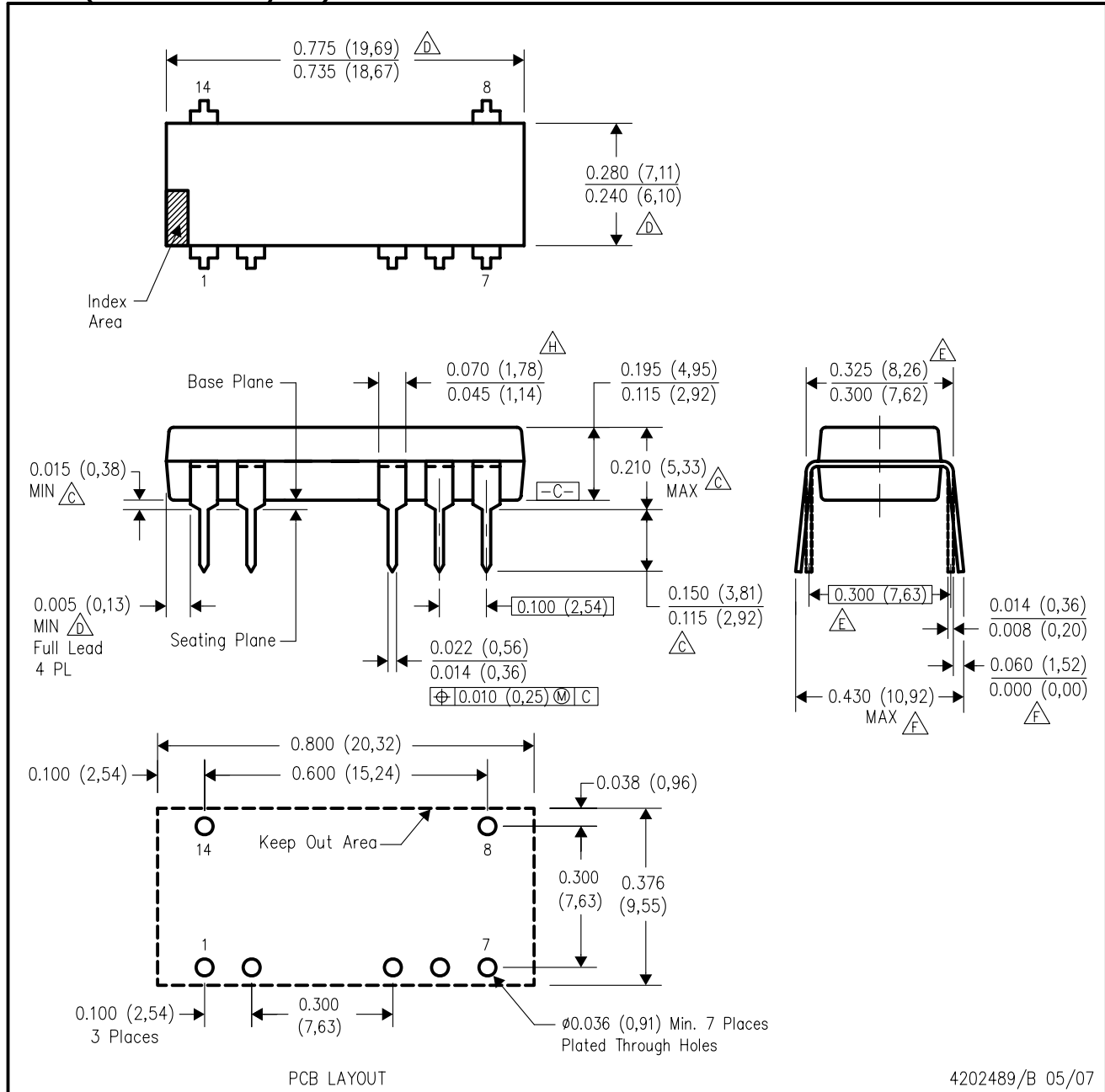
4222497/A 10/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## NVA (R-PDIP-T7/14)

## PLASTIC DUAL-IN-LINE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Dimensions are measured with the package seated in JEDEC seating plane gauge GS-3.
  - Dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 (0,25).
  - Dimensions measured with the leads constrained to be perpendicular to Datum C.
  - Dimensions are measured at the lead tips with the leads unconstrained.
  - Pointed or rounded lead tips are preferred to ease insertion.

- Lead shoulder maximum dimension does not include dambar protrusions. Dambar protrusions shall not exceed 0.010 (0,25).
- Distance between leads including dambar protrusions to be 0.005 (0,13) minimum.
- A visual index feature must be located within the cross-hatched area.
- For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.
- Falls within JEDEC MS-001-AA.

## 重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
版权所有 © 2025，德州仪器 (TI) 公司