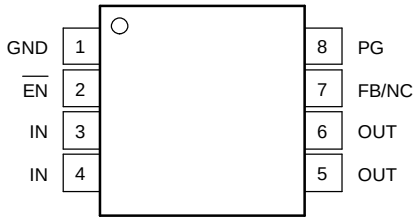
FAST TRANSIENT RESPONSE, 1-A LOW-DROPOUT VOLTAGE REGULATORS

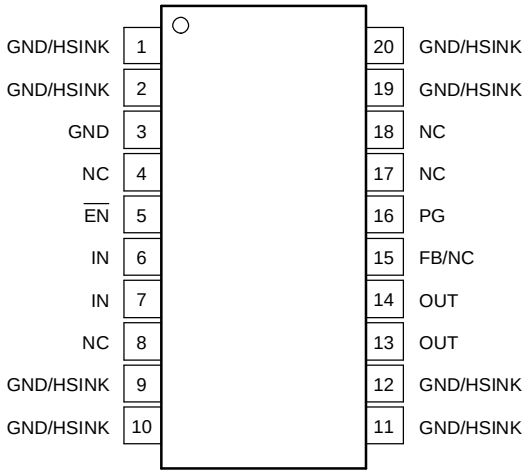
FEATURES

- **Input Voltage Range: 2.7 V to 10 V**
- **Low-Dropout Voltage: 230 mV typical at 1 A (TPS76850)**
- **2% Tolerance Over Specified Conditions for Fixed-Output Versions**
- **Open Drain Power Good (See TPS767xx for Power-On Reset With 200-ms Delay Option)**
- **Ultralow 85 μA Typical Quiescent Current**
- **Available in 1.5-V, 1.8-V, 2.5-V, 2.7-V, 2.8-V, 3.0-V, 3.3-V, 5.0-V Fixed Output and Adjustable (1.2 V to 5.5 V) Versions**
- **Fast Transient Response**
- **Thermal Shutdown Protection**
- **SOIC-8 (D) and TSSOP-20 (PWP) Package**

D PACKAGE
(Top View)



PWP PACKAGE
(Top View)



NC = No Internal Connection

DESCRIPTION

This device is designed to have a fast transient response and be stable with 10 μF capacitors. This combination provides high performance at a reasonable cost.

Since the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 230 mV at an output current of 1 A for the TPS76850) and is directly proportional to the output current. Additionally, because the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (typically 85 μA over the full range of output current, 0 mA to 1 A). These two key specifications yield a significant improvement in operating life for battery-powered systems. This LDO family also features a shutdown mode; applying a TTL high signal to $\overline{EN}$ (enable) shuts down the regulator, reducing the quiescent current to less than 1 μA at T_J = 25°C.

Power good (PG) is an active high output, which can be used to implement a power-on reset or a low-battery indicator.

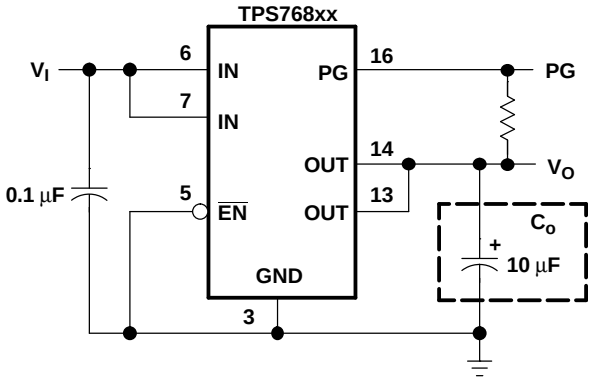


Figure 1. Typical Application Configuration (For Fixed Output Options)

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	V_{OUT}(2)
TPS768**xxQyyyz**	**XX** is nominal output voltage (for example, 28 = 2.8 V, 285 = 2.85 V, 01 = Adjustable). **YYY** is package designator. **Z** is package quantity.

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Custom output voltages are available; minimum order quantities may apply. Contact factory for details and availability.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

	VALUE
Input voltage range, V_I(2)	–0.3 V to 13.5 V
Voltage range at $\overline{EN}$	–0.3 V to V_I + 0.3 V
Maximum PG voltage	16.5 V
Peak output current	Internally limited
Continuous total power dissipation	See Dissipation Rating Table
Output voltage, V_O (OUT, FB)	7 V
Operating junction temperature range, T_J	–40°C to +125°C
Storage temperature range, T_{stg}	–65°C to +150°C
ESD rating, HBM	2 kV

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network terminal ground.

DISSIPATION RATING TABLE—FREE-AIR TEMPERATURES

PACKAGE	AIR FLOW (CFM)	T_A < +25°C POWER RATING	DERATING FACTOR ABOVE T_A = +25°C	T_A = +70°C POWER RATING	T_A = +85°C POWER RATING
D	0	568.18 mW	5.6818 mW/°C	312.5 mW	227.27 mW
	250	904.15 mW	9.0415 mW/°C	497.28 mW	361.66 mW
PWP(1)	0	3.1 W	30.7 mW/°C	1.7 W	1.2 W
	250	4.1 W	41.2 mW/°C	2.3 W	1.6 W

(1) This parameter is measured with the recommended copper heat sink pattern on a 4-layer, 5-in × 5-in PCB, 1 oz. copper, 4-in × 4-in coverage (4 in^2).

RECOMMENDED OPERATING CONDITIONS

	MIN	MAX	UNIT
Input voltage, V_I(1)	2.7	10	V
Output voltage range, V_O	1.2	5.5	V
Output current, I_O(2)	0	1.0	A
Operating junction temperature, T_J(2)	–40	+125	°C

(1) Minimum $V_{IN} = V_{OUT} + V_{DO}$ or 2.7 V, whichever is greater.
(2) Continuous current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, $V_I = V_{O(typ)} + 1$ V, $I_O = 1$ mA, $\overline{EN} = 0$ V, $C_O = 10$ µF (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT} Accuracy		–40°C ≤ T_J ≤ +125°C, V_O + 1 V ≤ V_{IN} ≤ 10V(1), 10 µA ≤ I_O ≤ 1A	(0.98)V_O	V_O	(1.02)V_O	V
Quiescent current (GND current) $\overline{EN}$ = 0V (1)		10 µA < I_O < 1 A, T_J = +25°C		85		µA
		I_O = 1 A, T_J = –40°C to +125°C			125	
Output voltage line regulation ($\Delta V_O/V_O$) (1)(2)		V_O + 1 V < V_I ≤ 10 V, T_J = +25°C		0.01		%/V
Load regulation				3		mV
Output noise voltage (TPS76818)		BW = 200 Hz to 100 kHz, C_O = 10 µF, I_C = 1 A, T_J = +25°C		55		µVrms
Output current limit		V_O = 0 V	1.2	1.7	2	A
Thermal shutdown junction temperature				150		°C
Standby current		$V_{\overline{EN}} = V_I$, T_J = +25°C, 2.7 V < V_I < 10 V		1		µA
		$V_{\overline{EN}} = V_I$, T_J = –40°C to +125°C, 2.7 V < V_I < 10 V			10	µA
FB pin current, I_{FB}	TPS76801	V_{FB} = 1.5 V		2		nA
High-level enable input voltage			1.7			V
Low-level enable input voltage					0.9	V
Power-supply ripple rejection (1)		f = 1 kHz, C_O = 10 µF, T_J = +25°C		60		dB
Power Good (PG)	Minimum input voltage for valid PG	$I_{O(PG)}$ = 300 µA		1.1		V
	Trip threshold voltage	V_O decreasing	92		98	%V_O
	Hysteresis voltage	Measured at V_O		0.5		%V_O
	Output low voltage	V_I = 2.7 V, $I_{O(PG)}$ = 1 mA		0.15	0.4	V
	Leakage current	$V_{(PG)}$ = 5 V			1	µA
Enable pin current ($I_{\overline{EN}}$)		$V_{\overline{EN}}$ = 0 V	1	0	1	µA
		$V_{\overline{EN}} = V_I$	1		1	
Dropout voltage (3)	TPS76828	I_O = 1 A, T_J = +25°C		500		mV
		I_O = 1 A, T_J = –40°C to +125°C			825	
	TPS76830	I_O = 1 A, T_J = +25°C		450		
		I_O = 1 A, T_J = –40°C to +125°C			675	
	TPS76833	I_O = 1 A, T_J = +25°C		350		
		I_O = 1 A, T_J = –40°C to +125°C			575	
	TPS76850	I_O = 1 A, T_J = +25°C		230		
		I_O = 1 A, T_J = –40°C to +125°C		380		

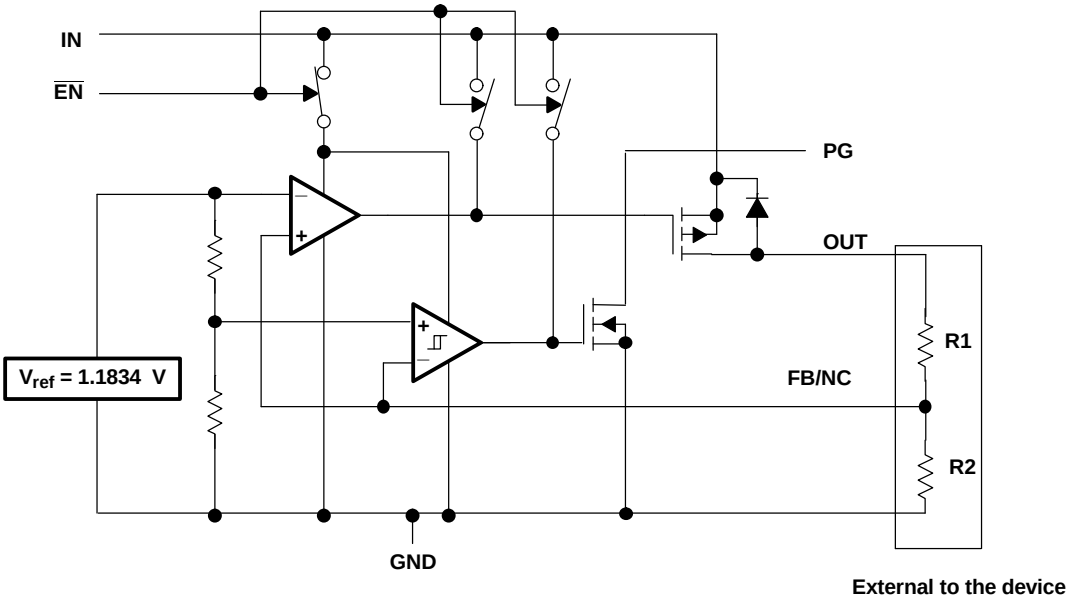
(1) Minimum IN operating voltage is 2.7 V or $V_{O(typ)}$ + 1 V, whichever is greater. Maximum IN voltage 10 V.

(2) If $V_O \leq 1.8$ V then $V_{Imax} = 10$ V, $V_{Imin} = 2.7$ V: $\text{Line Reg. (mV)} = (\%/V) \times V_O \frac{(V_{Imax} - 2.7V)}{100} \times 1000$

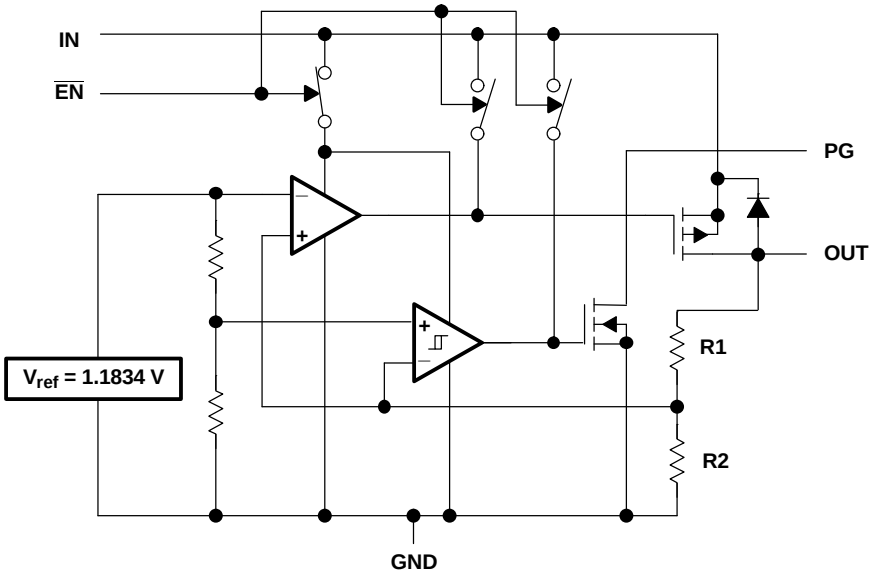
If $V_O \geq 2.5$ V then $V_{Imax} = 10$ V, $V_{Imin} = V_O + 1$ V: $\text{Line Reg. (mV)} = (\%/V) \times V_O \frac{(V_{Imax} - (V_O + 1V))}{100} \times 1000$

(3) IN voltage equals V_O(typ) – 100 mV; TPS76801 output voltage set to 3.3 V nominal with external resistor divider. TPS76815, TPS76818, TPS76825, and TPS76827 dropout voltage limited by input voltage range limitations (that is, TPS76830 input voltage must drop to 2.9 V for the purpose of this test).

FUNCTIONAL BLOCK DIAGRAM—Adjustable Version



FUNCTIONAL BLOCK DIAGRAM—Fixed-Voltage Version



Terminal Functions

NAME	SOIC-8 (D) PIN NO.	TSSOP-20 (PWP) PIN NO.	DESCRIPTION
GND	1	3	Regulator ground
GND/HSINK	—	1, 2, 9-12, 19, 20	Regulator ground and heatsink
NC	—	4, 8, 17, 18	No connect
$\overline{EN}$	2	5	Enable input
IN	3, 4	6, 7	Input voltage
OUT	5, 6	13, 14	Regulated output voltage
FB/NC	7	15	Feedback input voltage for adjustable device (no connect for fixed options)
PG	8	16	PG output

TYPICAL CHARACTERISTICS

TPS76833
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

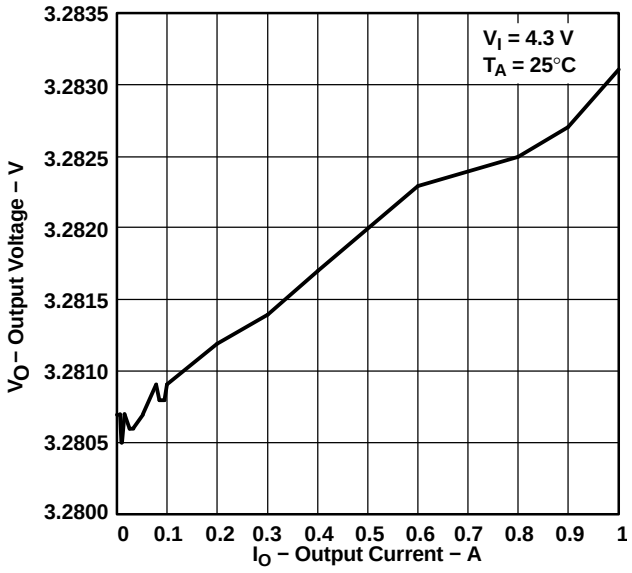


Figure 2.

TPS76815
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

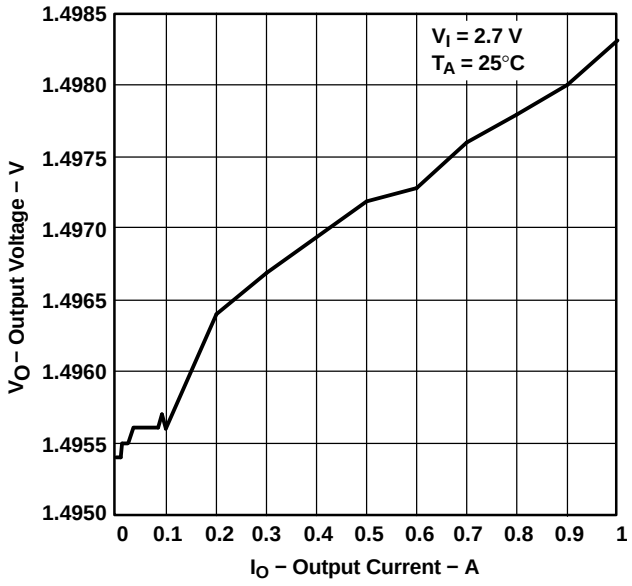


Figure 3.

TPS76825
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

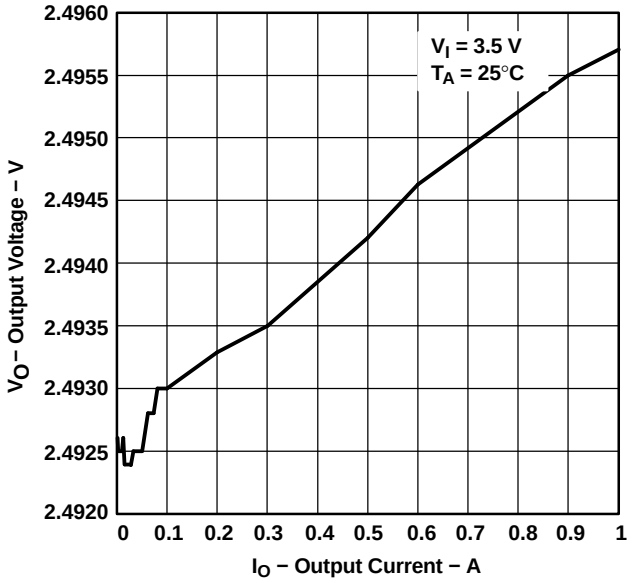


Figure 4.

TPS76833
OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

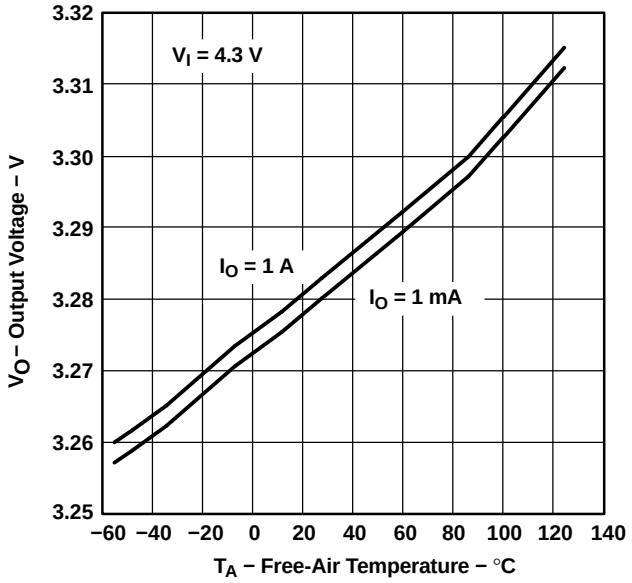


Figure 5.

TYPICAL CHARACTERISTICS (continued)

TPS76815
OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

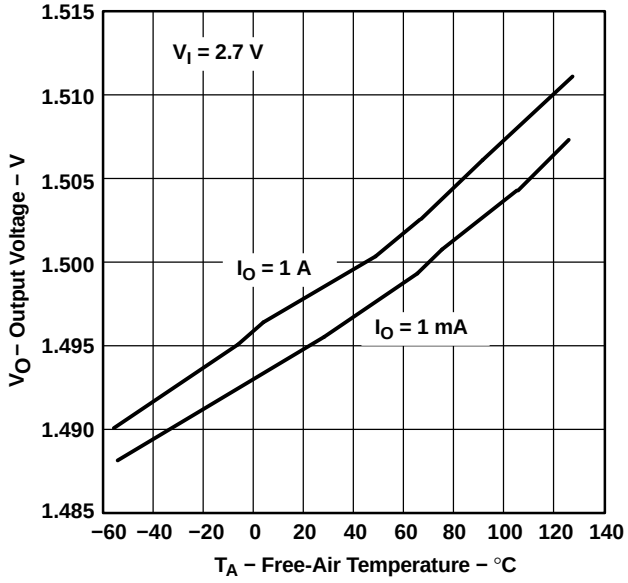


Figure 6.

TPS76825
OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

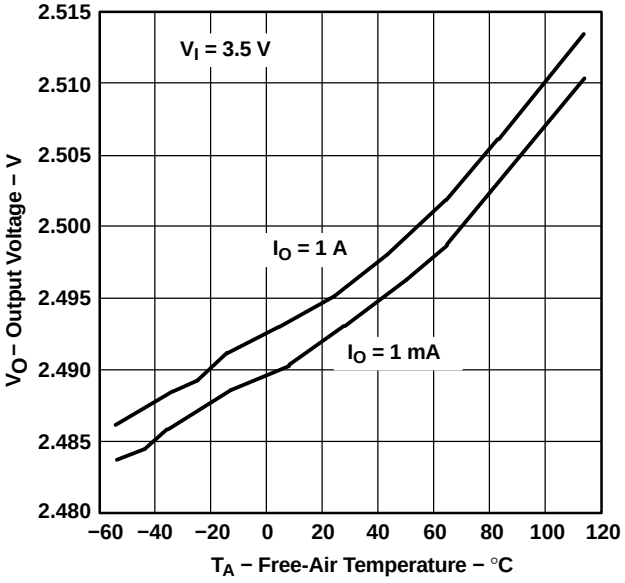


Figure 7.

TPS76833
GROUND CURRENT
vs
FREE-AIR TEMPERATURE

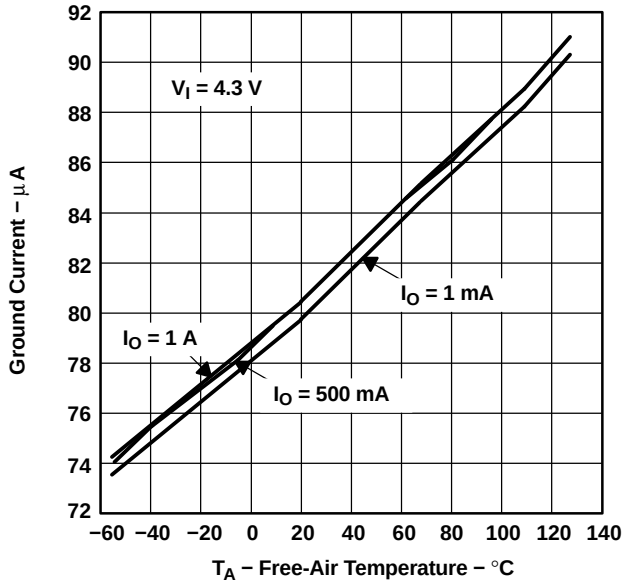


Figure 8.

TPS76815
GROUND CURRENT
vs
FREE-AIR TEMPERATURE

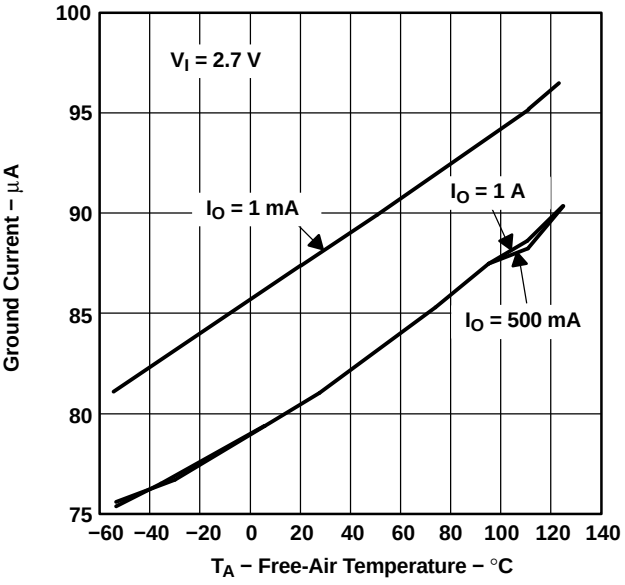


Figure 9.

TYPICAL CHARACTERISTICS (continued)

TPS76833
POWER-SUPPLY RIPPLE REJECTION
vs
FREQUENCY

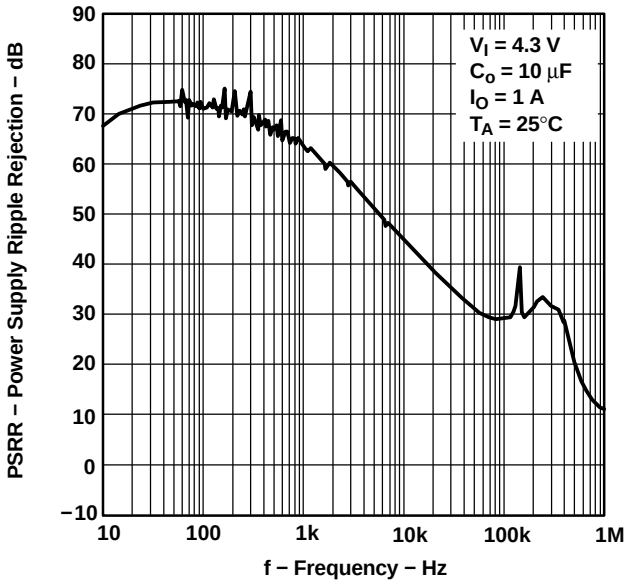


Figure 10.

TPS76833
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

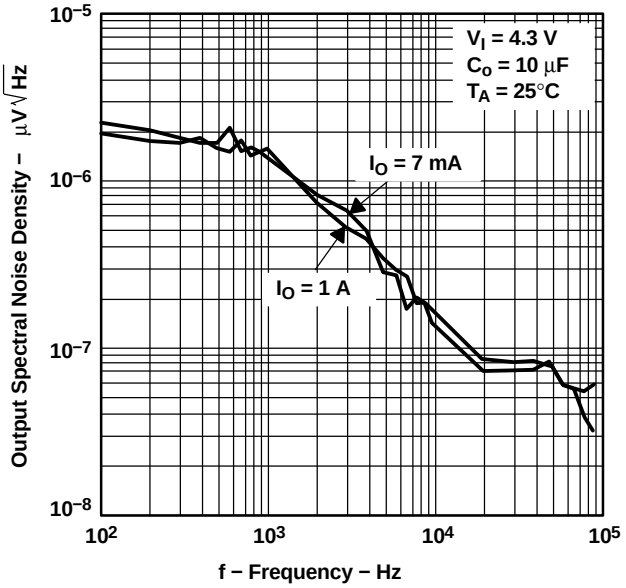


Figure 11.

INPUT VOLTAGE (MIN)
vs
OUTPUT VOLTAGE

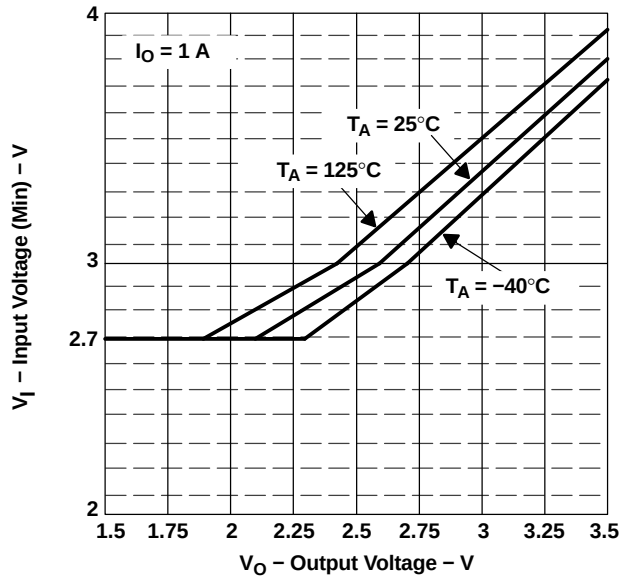


Figure 12.

TPS76833
OUTPUT IMPEDANCE
vs
FREQUENCY

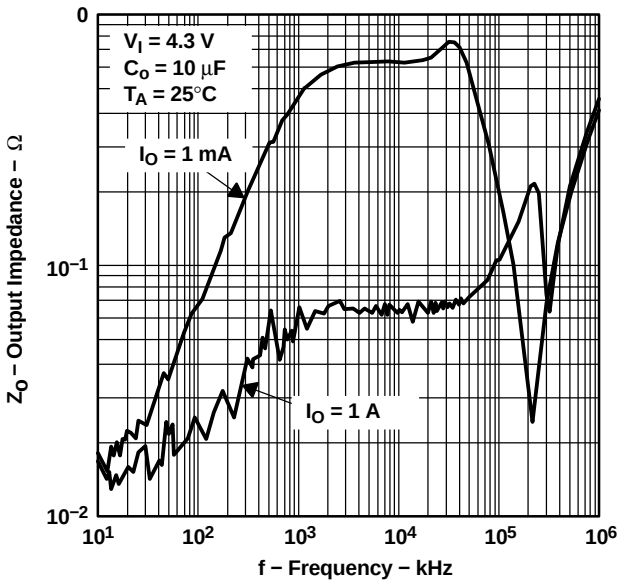


Figure 13.

TYPICAL CHARACTERISTICS (continued)

TPS76833
DROPOUT VOLTAGE
vs
FREE-AIR TEMPERATURE

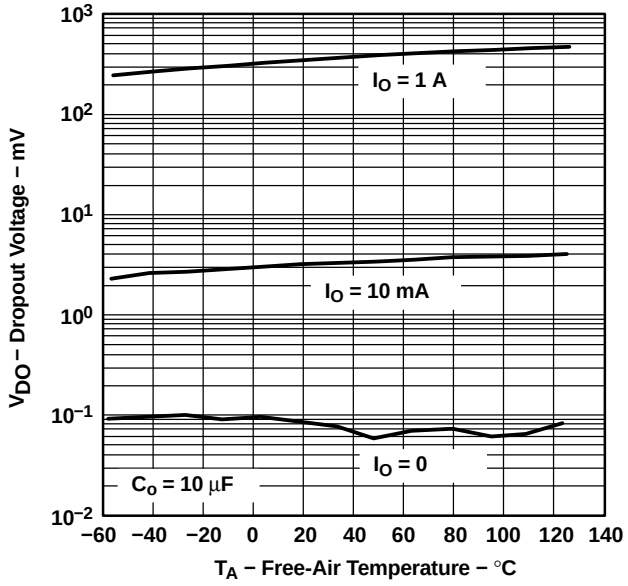


Figure 14.

TPS76815
LINE TRANSIENT RESPONSE

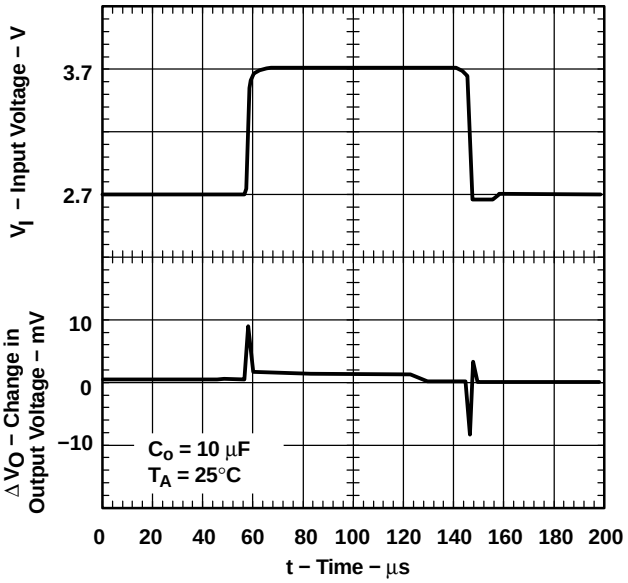


Figure 15.

TPS76815
LOAD TRANSIENT RESPONSE

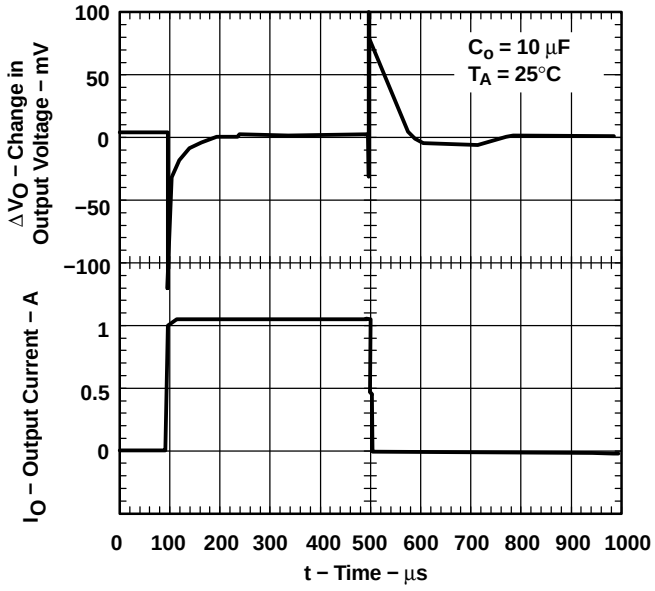


Figure 16.

TPS76833
LINE TRANSIENT RESPONSE

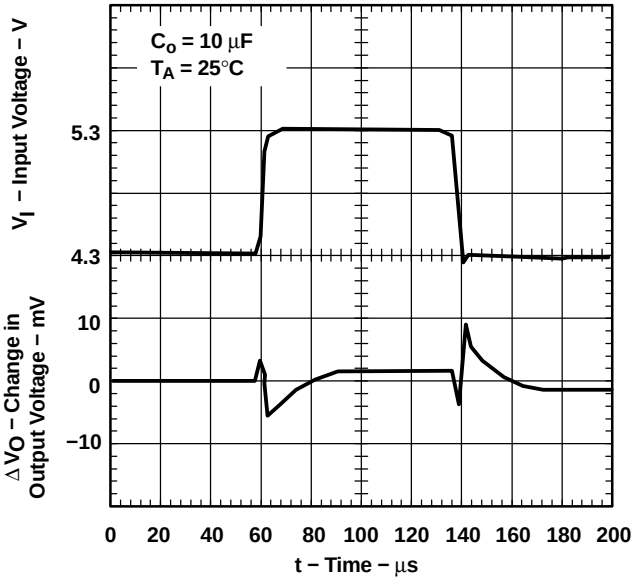


Figure 17.

TYPICAL CHARACTERISTICS (continued)

TPS76833
LOAD TRANSIENT RESPONSE

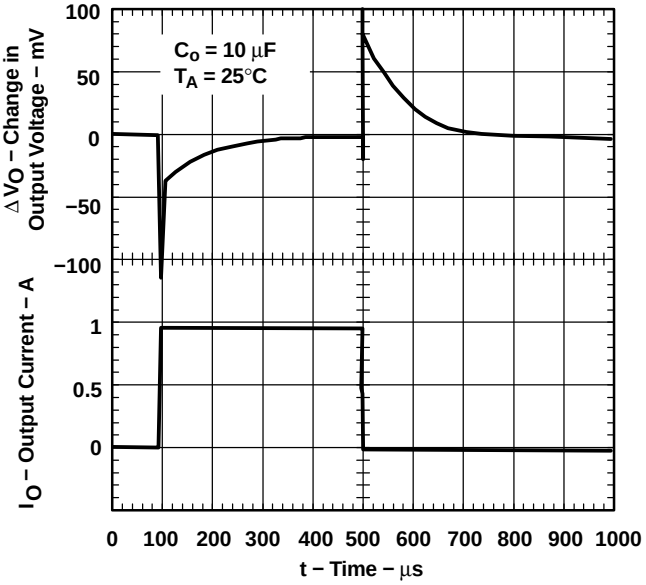


Figure 18.

TPS76833
OUTPUT VOLTAGE
vs
TIME (AT START-UP)

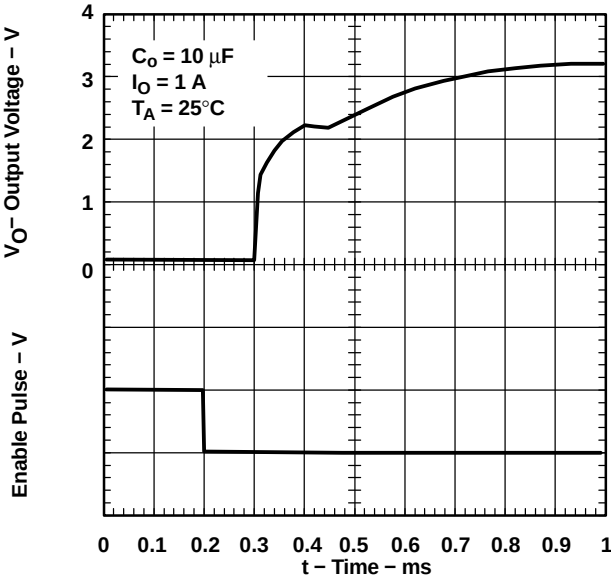


Figure 19.

TPS76801
DROPOUT VOLTAGE
vs
INPUT VOLTAGE

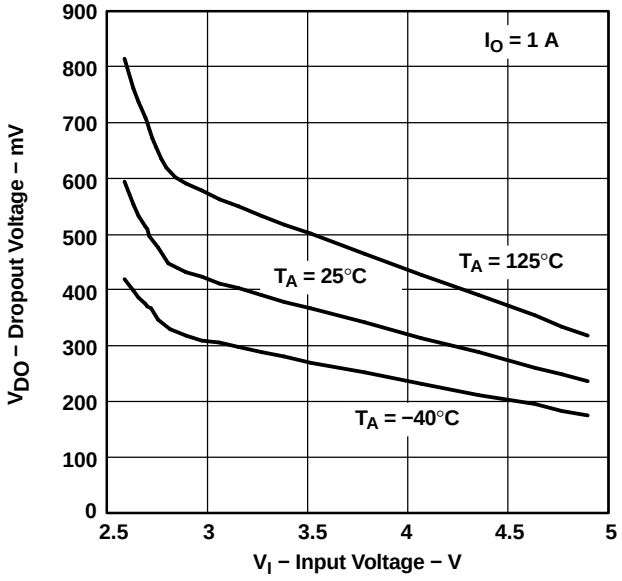


Figure 20.

TEST CIRCUIT FOR TYPICAL REGIONS OF STABILITY
(Figure 22 through Figure 25)
(Fixed Output Options)

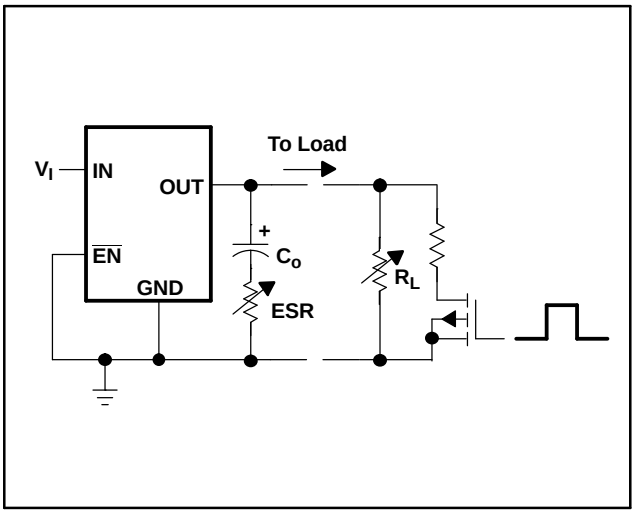


Figure 21.

TYPICAL CHARACTERISTICS (continued)

Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE
vs
OUTPUT CURRENT

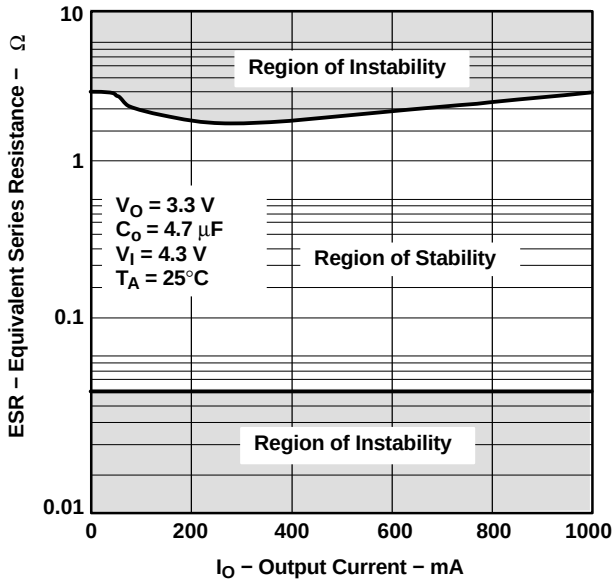


Figure 22.

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE
vs
OUTPUT CURRENT

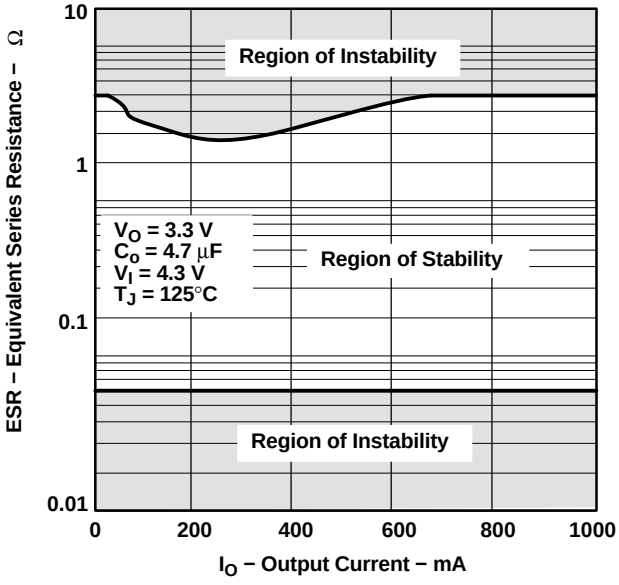


Figure 23.

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE
vs
OUTPUT CURRENT

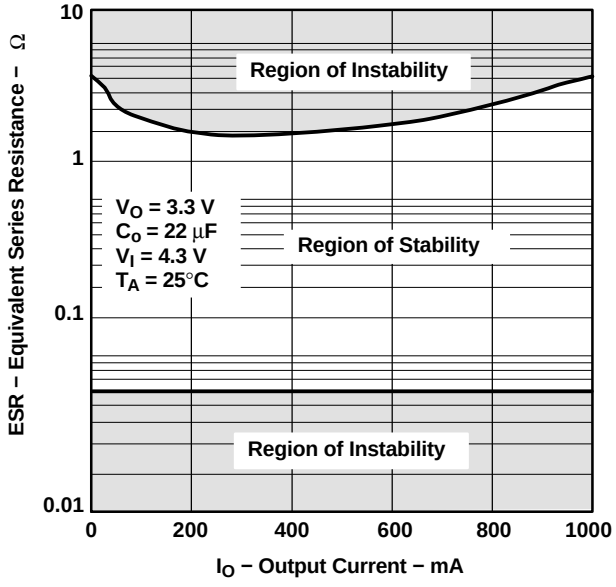


Figure 24.

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE
vs
OUTPUT CURRENT

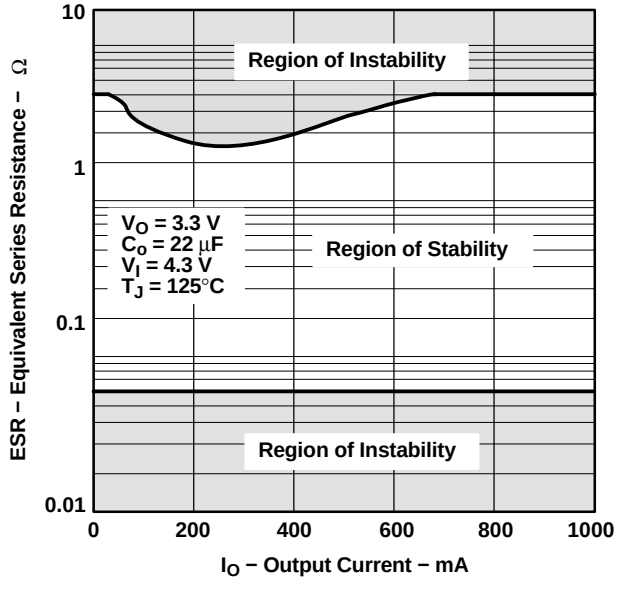


Figure 25.

APPLICATION INFORMATION

The TPS768xxQ family includes eight fixed-output voltage regulators (1.5 V, 1.8 V, 2.5 V, 2.7 V, 2.8 V, 3.0 V, 3.3 V, and 5.0 V), and offers an adjustable device, the TPS76801 (adjustable from 1.2 V to 5.5 V).

DEVICE OPERATION

The TPS768xxQ features very low quiescent current, which remains virtually constant even with varying loads. Conventional LDO regulators use a PNP pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). The TPS768xxQ uses a PMOS transistor to pass current; because the gate of the PMOS is voltage driven, operating current is low and invariable over the full load range.

Another pitfall associated with the PNP-pass element is its tendency to saturate when the device goes into dropout. The resulting drop in β forces an increase in I_B to maintain the load. During power up, this translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation. The TPS768xxQ quiescent current remains low even when the regulator drops out, eliminating both problems.

The TPS768xxQ family also features a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to 2 μA. If the shutdown feature is not used, $\overline{EN}$ should be tied to ground.

MINIMUM LOAD REQUIREMENTS

The TPS768xxQ family is stable even at zero load; no minimum load is required for operation.

FB - PIN CONNECTION (ADJUSTABLE VERSION ONLY)

The FB pin is an input pin to sense the output voltage and close the loop for the adjustable option. The output voltage is sensed through a resistor divider network to close the loop as shown in Figure 27. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit to improve performance at that point. Internally, FB connects to a high-impedance wide-bandwidth amplifier and noise pickup feeds through to the regulator output. Routing the FB connection to minimize/avoid noise pickup is essential.

EXTERNAL CAPACITOR REQUIREMENTS

An input capacitor is not usually required; however, a ceramic bypass capacitor (0.047 μF or larger) improves load transient response and noise rejection if the TPS768xxQ is located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

Like all low dropout regulators, the TPS768xxQ requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 10 μF and the ESR (equivalent series resistance) must be between 60 mΩ and 1.5 Ω. Capacitor values 10 μF or larger are acceptable, provided the ESR is less than 1.5Ω . Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described above.

APPLICATION INFORMATION (continued)

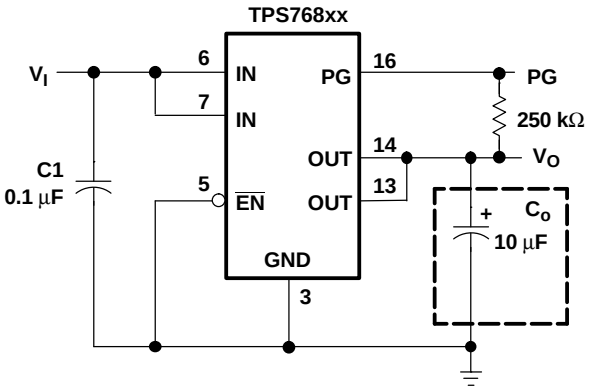


Figure 26. Typical Application Circuit (Fixed Versions)

The output voltage of the TPS76801 adjustable regulator is programmed using an external resistor divider as shown in Figure 27. The output voltage is calculated using:

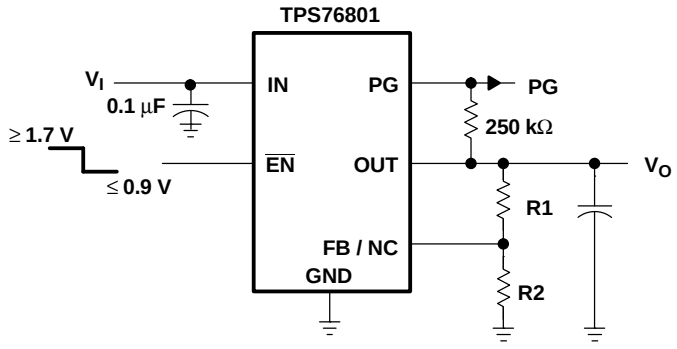
$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

where:

V_{ref} = 1.1834 V typ (the internal reference voltage)

Resistors R1 and R2 should be chosen for approximately 50-µA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 30.1 kΩto set the divider current at 50 µA and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \quad (2)$$



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	UNIT
2.5 V	33.2	30.1	kΩ
3.3 V	53.6	30.1	kΩ
3.6 V	61.9	30.1	kΩ
4.75 V	90.8	30.1	kΩ

Figure 27. TPS76801 Adjustable LDO Regulator Programming

POWER-GOOD INDICATOR

The TPS768xxQ features a power-good (PG) output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the PG output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. PG can be used to drive power-on reset circuitry or used as a low-battery indicator. PG does not assert itself when the regulated output voltage falls out of the specified 2% tolerance, but instead reports an output voltage low, relative to its nominal regulated value.

APPLICATION INFORMATION (continued)

REGULATOR PROTECTION

The TPS768xxQ PMOS-pass transistor has a built-in back diode that conducts reverse currents when the input voltage drops below the output voltage (for example, during power-down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS768xxQ also features internal current limiting and thermal protection. During normal operation, the TPS768xxQ limits output current to approximately 1.7 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds +150°C (typ), thermal-protection circuitry shuts it down. Once the device has cooled below +130°C (typ), regulator operation resumes.

POWER DISSIPATION AND JUNCTION TEMPERATURE

Specified regulator operation is assured to a junction temperature of +125°C; the maximum junction temperature should be restricted to +125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_D$max, and the actual dissipation, P_D, which must be less than or equal to $P_D$max.

The maximum-power-dissipation limit is determined using the following equation:

$$P_D\text{max} = \frac{T_J\text{max} - T_A}{R_{\theta JA}} \quad (3)$$

Where:

- $T_J$max is the maximum allowable junction temperature.
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package; that is, 172°C/W for the 8-pin SOIC (D) and 32.6°C/W for the 20-pin TSSOP (PWP) with no airflow.
- T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = \left(V_I - V_O\right) \times I_O \quad (4)$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS76801QD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU | NIPDAU	Level-1-260C-UNLIM	-40 to 125	76801
TPS76801QDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-1-260C-UNLIM	-40 to 125	76801
TPS76801QPWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76801
TPS76801QPWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76801
TPS76801QPWPRG4	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76801
TPS76815QD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76815
TPS76815QDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76815
TPS76815QPWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76815
TPS76815QPWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76815
TPS76818QD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76818
TPS76818QDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76818
TPS76818QPWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76818
TPS76818QPWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76818
TPS76825QD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76825
TPS76825QDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76825
TPS76825QPWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76825
TPS76825QPWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76825
TPS76827QD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76827
TPS76828QD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76828
TPS76830QD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76830
TPS76830QPWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76830
TPS76833QD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76833
TPS76833QDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76833
TPS76833QPWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76833
TPS76833QPWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76833
TPS76850QD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76850
TPS76850QDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76850
TPS76850QPWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76850
TPS76850QPWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76850

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TPS768 :

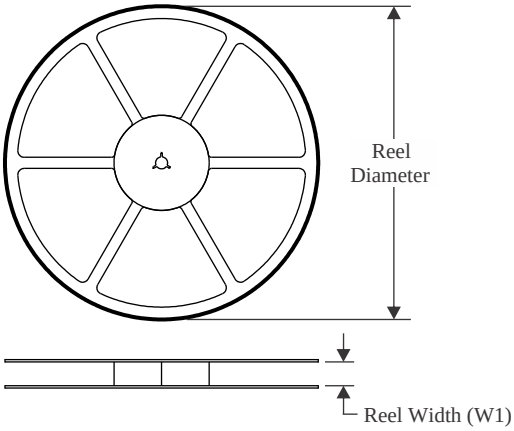
- Automotive : TPS768-Q1

NOTE: Qualified Version Definitions:

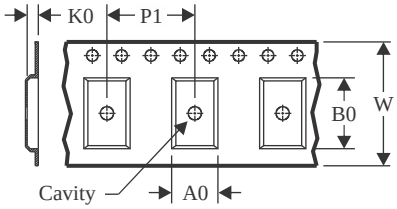
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

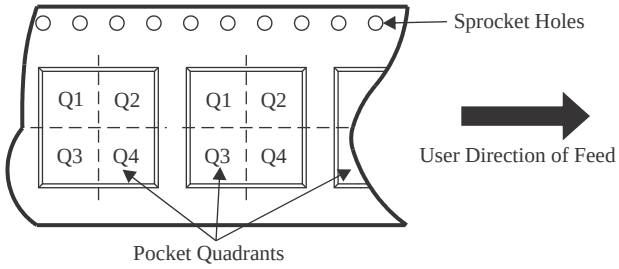


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

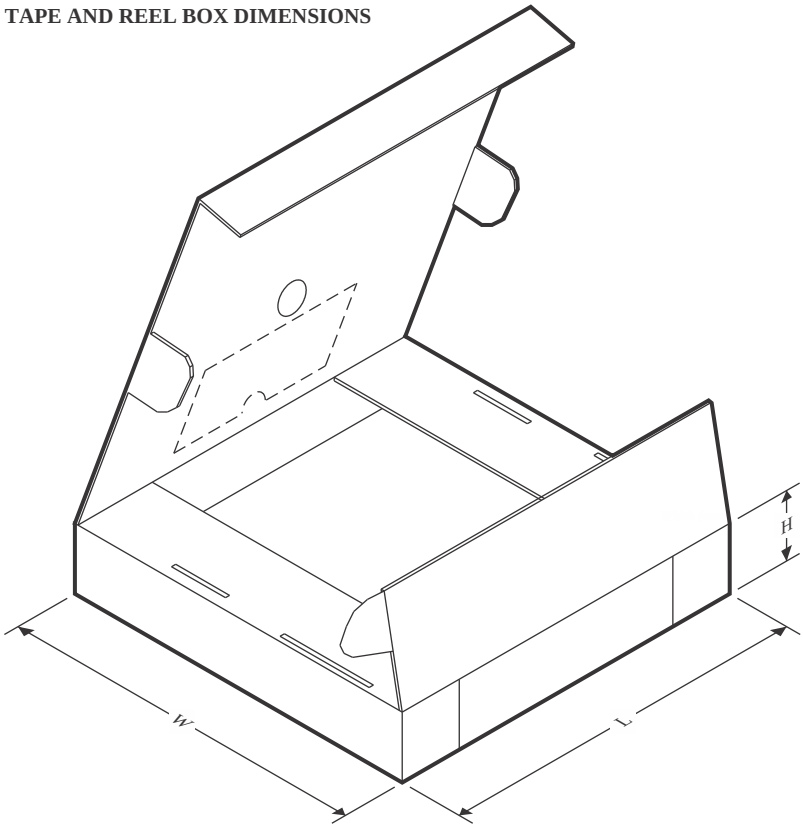
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS76801QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS76801QPWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS76815QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS76815QPWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS76818QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS76818QPWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS76825QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS76825QPWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS76833QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS76833QPWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS76850QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS76850QPWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

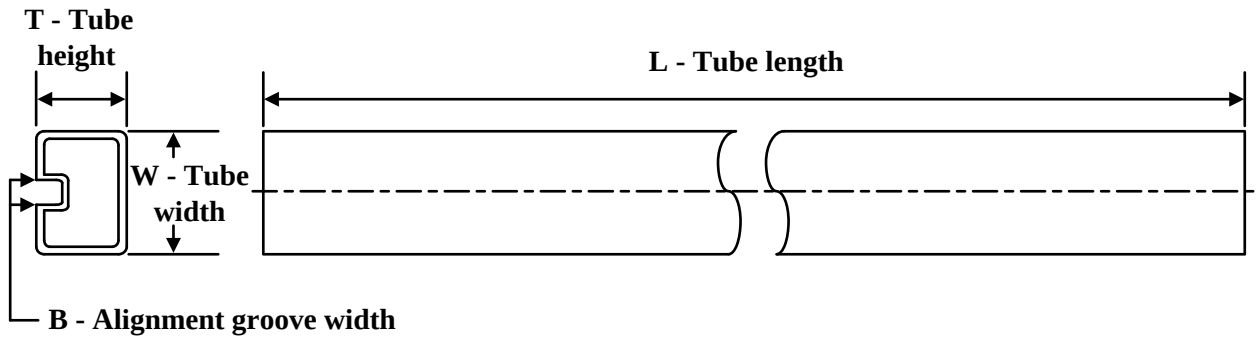
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS76801QDR	SOIC	D	8	2500	356.0	356.0	35.0
TPS76801QPWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS76815QDR	SOIC	D	8	2500	350.0	350.0	43.0
TPS76815QPWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS76818QDR	SOIC	D	8	2500	350.0	350.0	43.0
TPS76818QPWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS76825QDR	SOIC	D	8	2500	350.0	350.0	43.0
TPS76825QPWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS76833QDR	SOIC	D	8	2500	350.0	350.0	43.0
TPS76833QPWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS76850QDR	SOIC	D	8	2500	350.0	350.0	43.0
TPS76850QPWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS76801QD	D	SOIC	8	75	505.46	6.76	3810	4
TPS76801QD	D	SOIC	8	75	506.6	8	3940	4.32
TPS76801QPWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS76801QPWPG4	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS76815QD	D	SOIC	8	75	505.46	6.76	3810	4
TPS76815QPWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS76818QD	D	SOIC	8	75	505.46	6.76	3810	4
TPS76818QPWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS76825QD	D	SOIC	8	75	505.46	6.76	3810	4
TPS76825QPWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS76827QD	D	SOIC	8	75	505.46	6.76	3810	4
TPS76828QD	D	SOIC	8	75	505.46	6.76	3810	4
TPS76830QD	D	SOIC	8	75	505.46	6.76	3810	4
TPS76830QPWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS76833QD	D	SOIC	8	75	505.46	6.76	3810	4
TPS76833QPWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS76833QPWPG4	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS76850QD	D	SOIC	8	75	505.46	6.76	3810	4
TPS76850QDG4	D	SOIC	8	75	505.46	6.76	3810	4
TPS76850QPWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

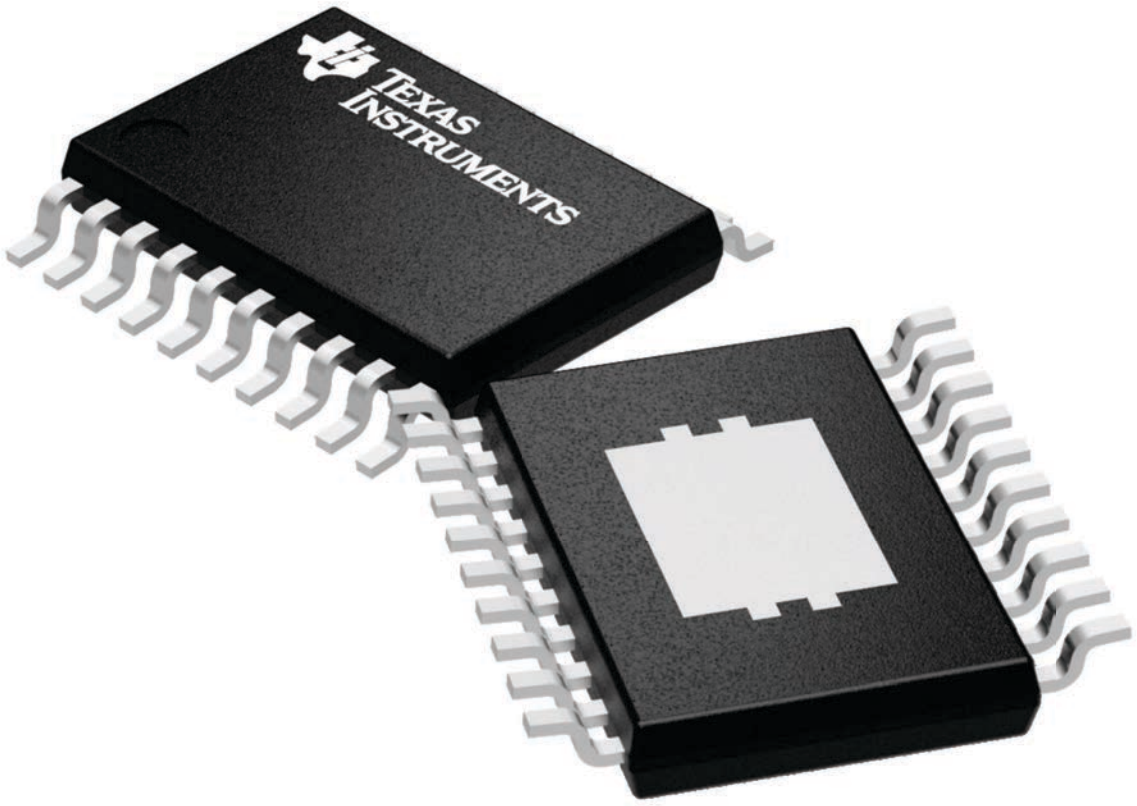
PWP 20

HTSSOP - 1.2 mm max height

6.5 x 4.4, 0.65 mm pitch

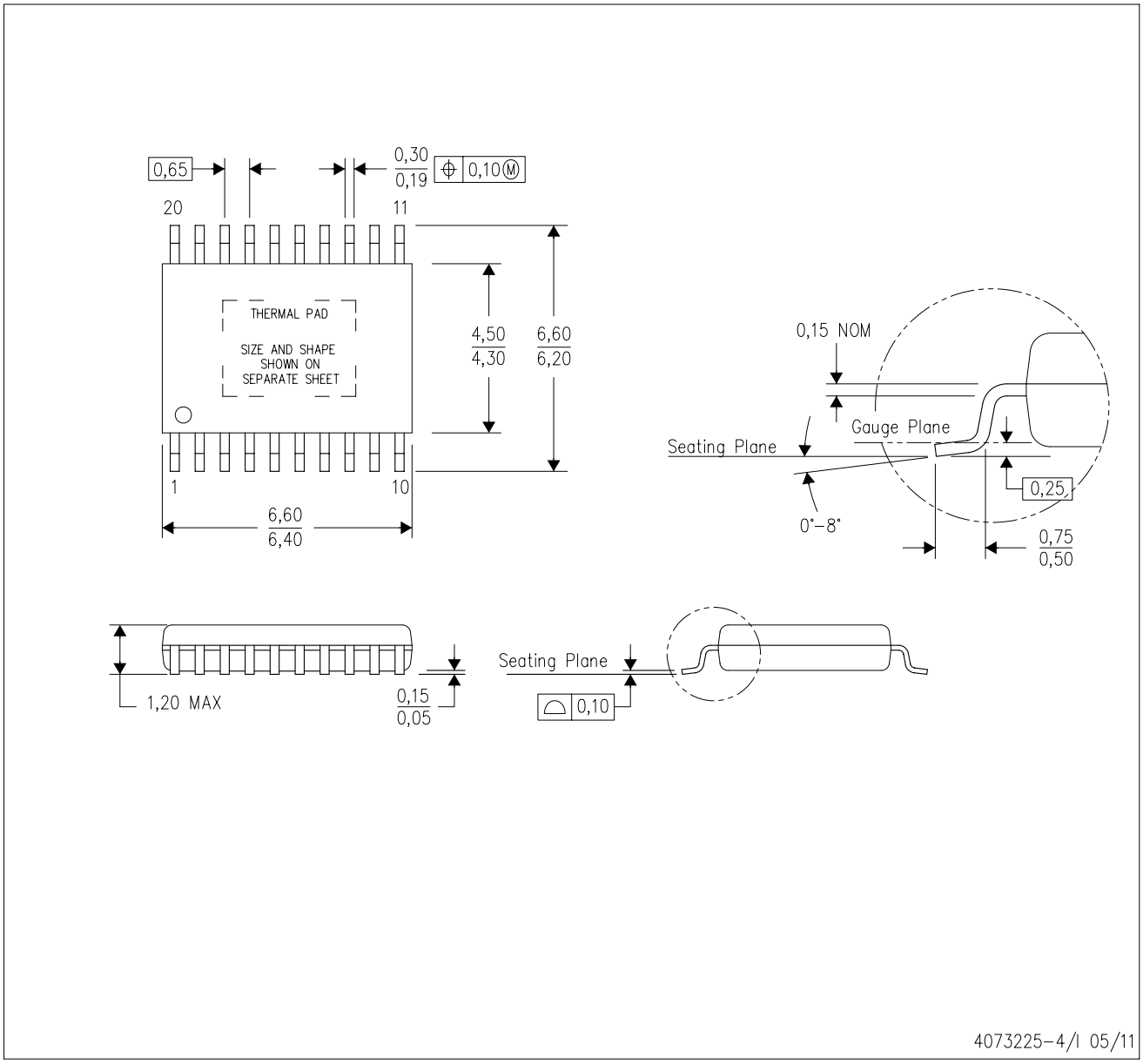
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224669/A

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

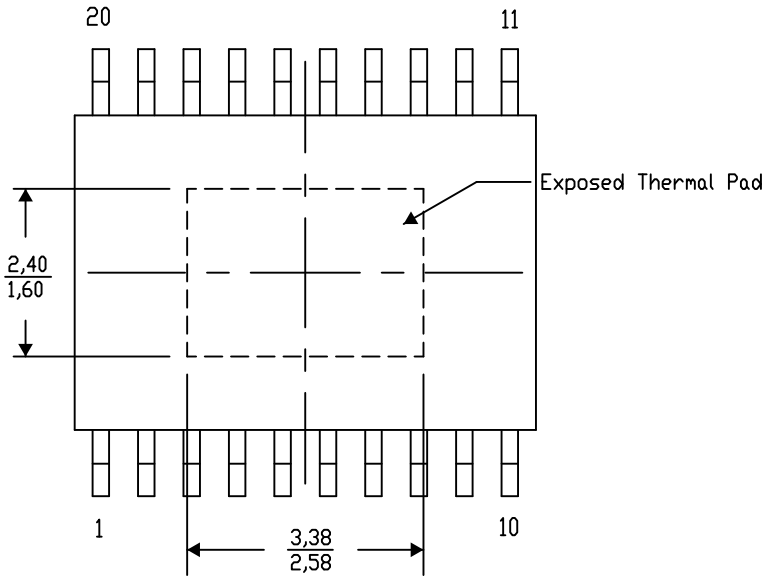
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

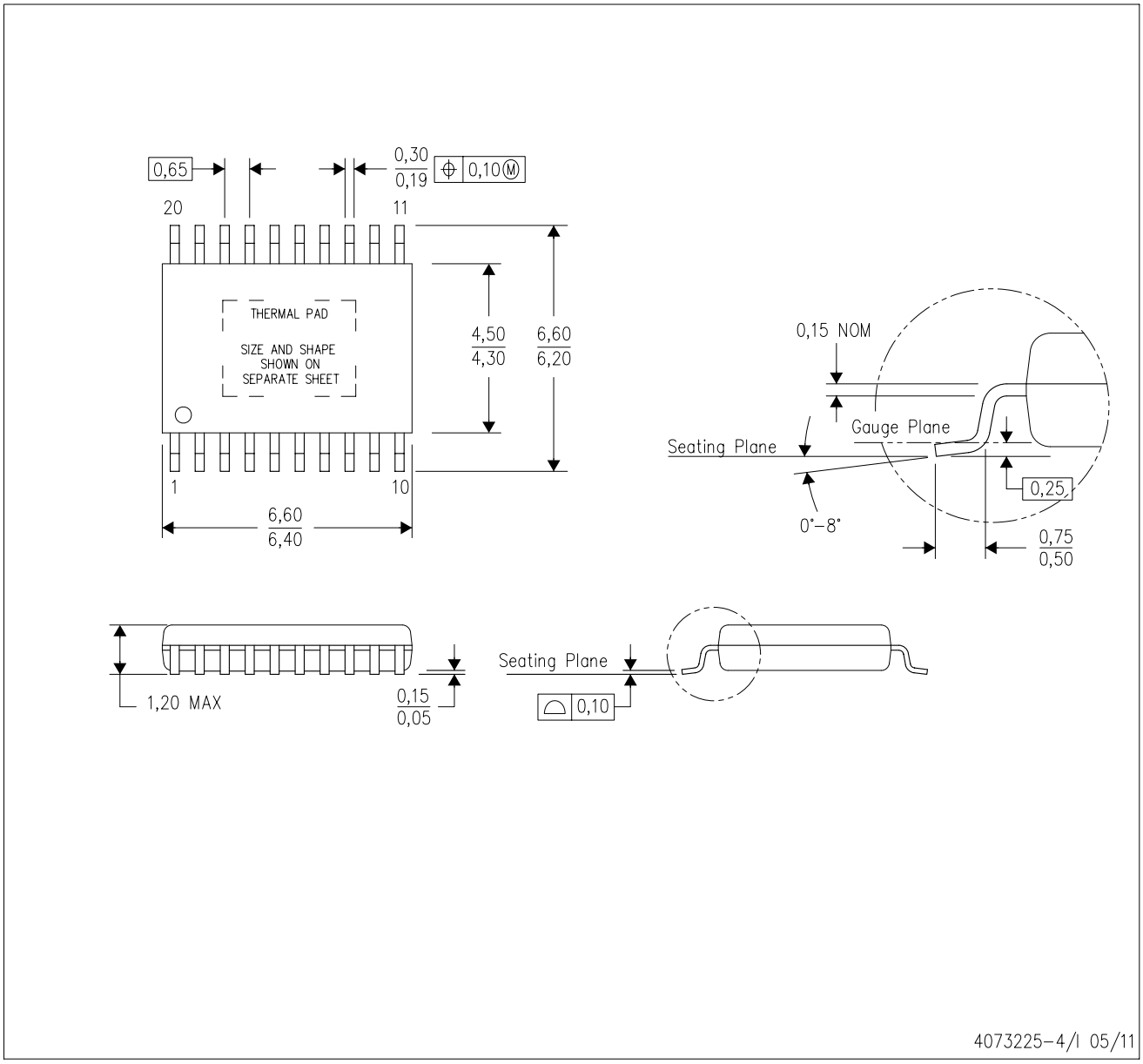
Exposed Thermal Pad Dimensions

4206332–21/AO 01/16

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

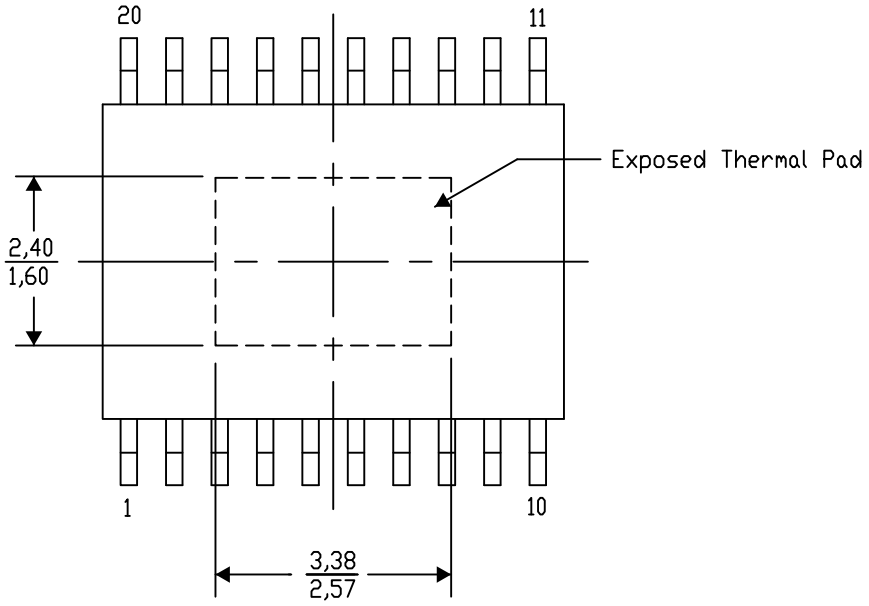
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

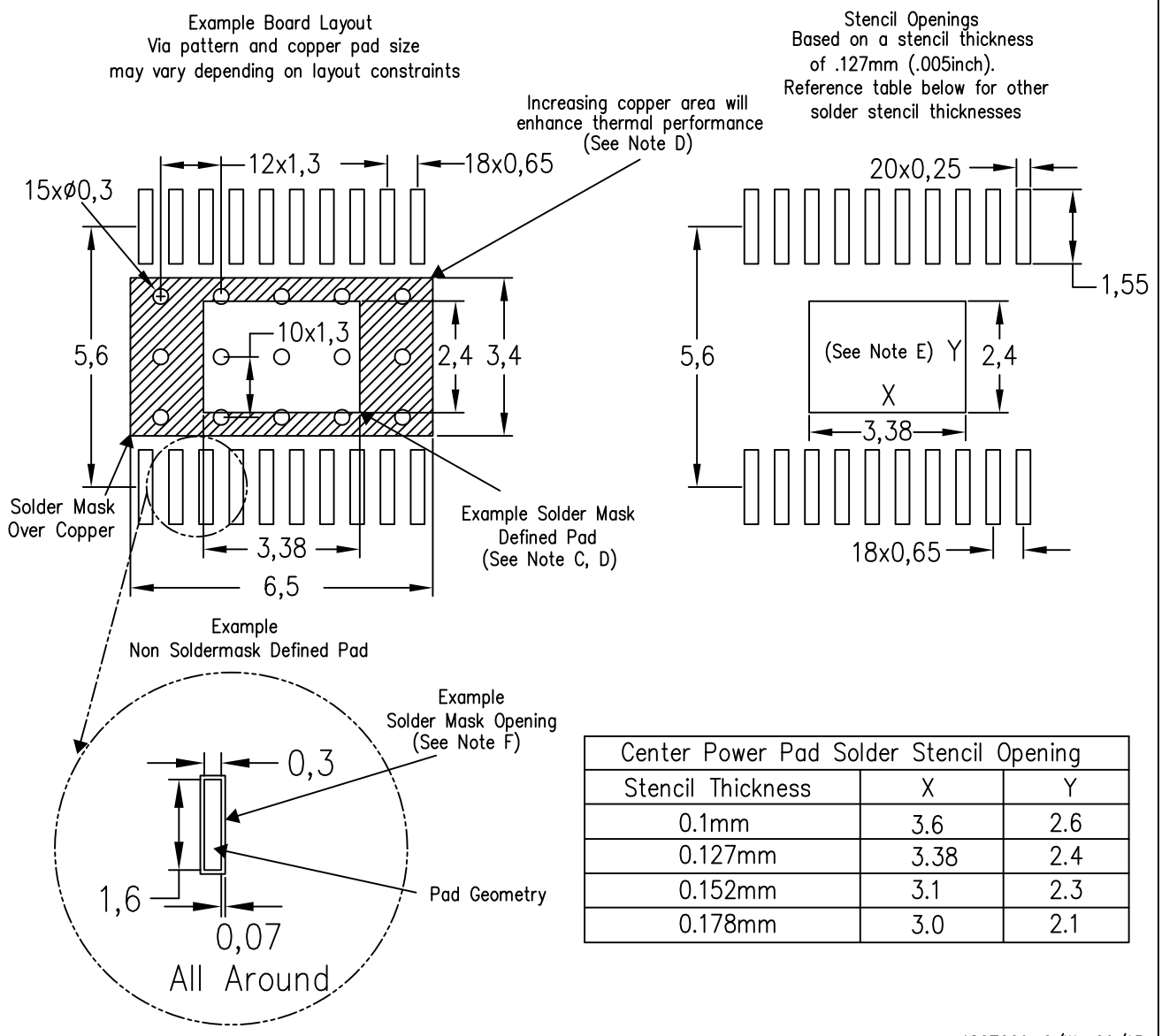
Exposed Thermal Pad Dimensions

4206332–13/AO 01/16

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

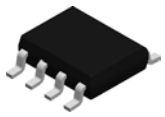
PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.6	2.6
0.127mm	3.38	2.4
0.152mm	3.1	2.3
0.178mm	3.0	2.1

4207609–6/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

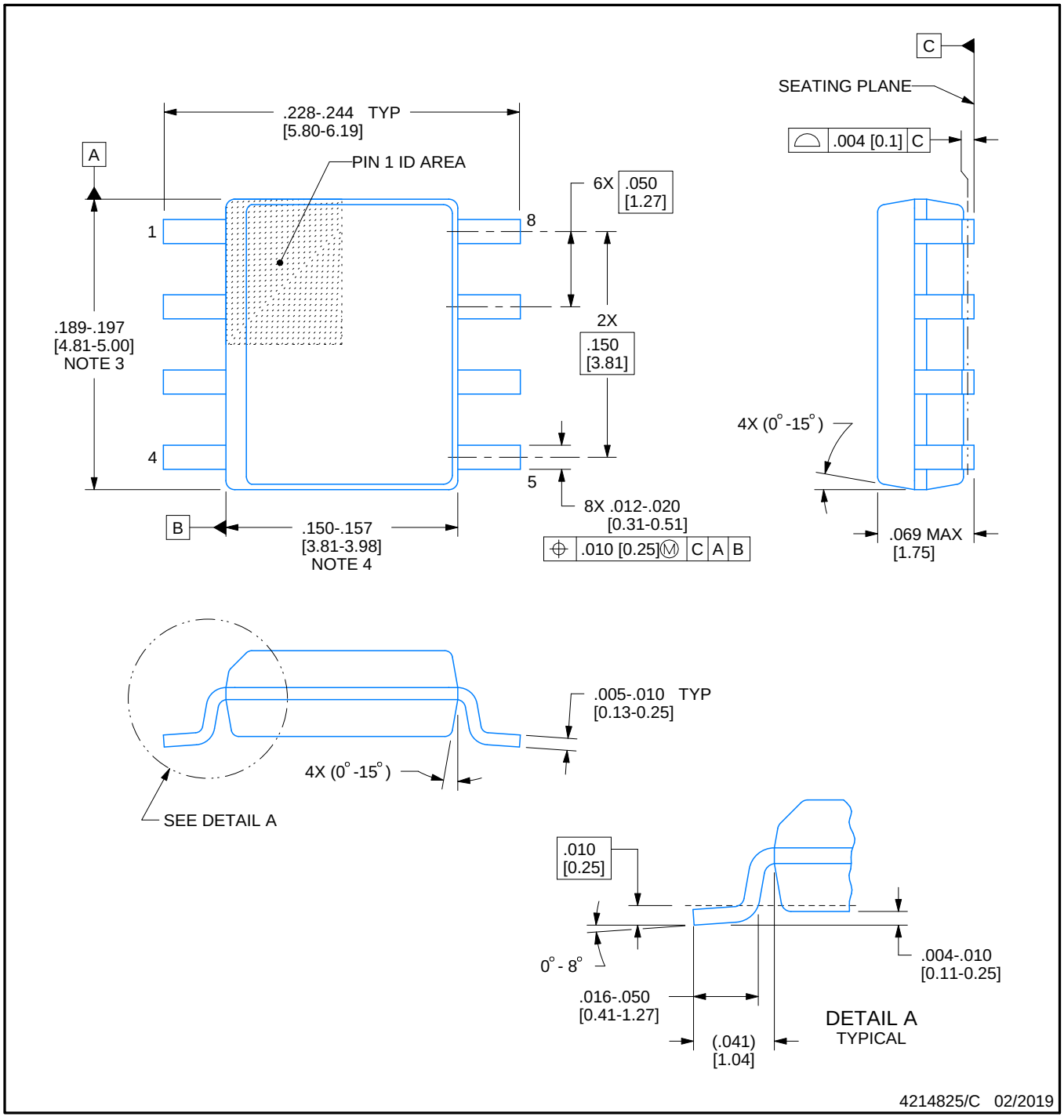


PACKAGE OUTLINE

D0008A

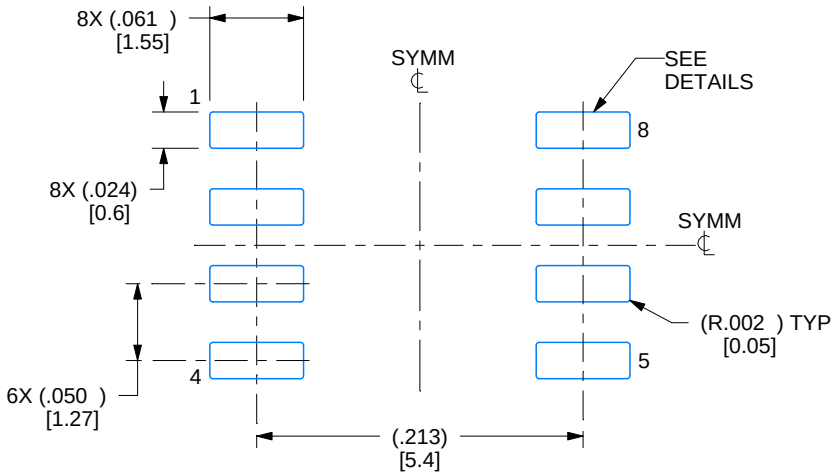
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

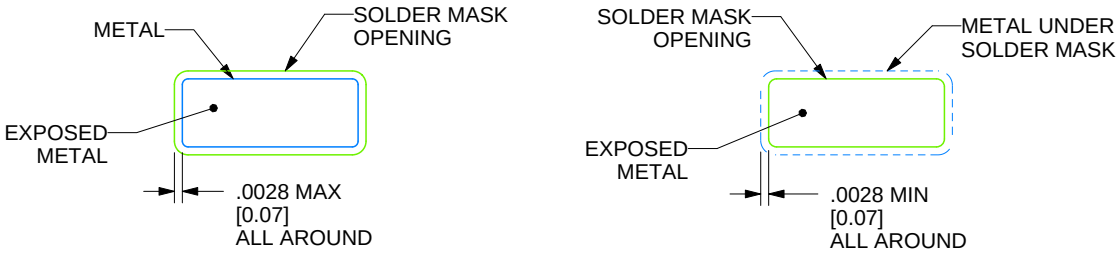


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

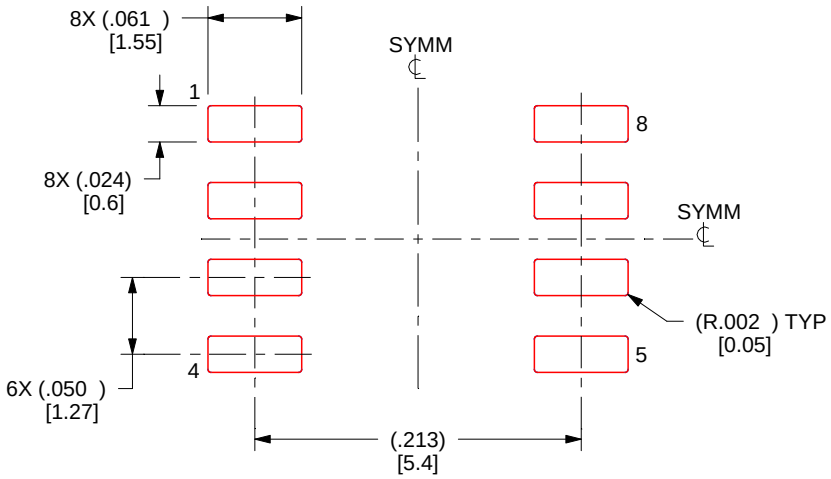
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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