

## TLV3801、TLV3802、TLV3811(C) 具有 LVDS 输出的 225ps 高速比较器

### 1 特性

- 低传播延迟：225 ps
- 低过驱动分散：5 ps
- 静态电流：17mA
- 高切换频率：3GHz/6Gbps
- 窄脉宽检测功能：240ps
- LVDS 输出
- 分离输入和输出接地基准
- 单电源电压：2.7V 至 5.25V
- 低输入失调电压：±0.5mV
- 内部 2mV 迟滞：TLV380x
- 内部 1.1mV 迟滞：TLV3811
- 内部 0mV 迟滞：TLV3811C
- 封装：TLV3801 ( 8 引脚 WSON )、TLV3811(C) ( 6 引脚 DSBGA )、TLV3802 ( 12 引脚 WSON )

### 2 应用

- 激光雷达中的距离感测
- 飞行时间传感器
- 示波器和逻辑分析仪中的高速触发器功能
- 高速差分线路接收器
- 无人机视觉

### 3 说明

TLV380x/TLV3811(C) 是具有宽电源电压范围和 3GHz 超高切换频率的 225ps 高速比较器。这些器件具有 2.7V 至 5.25V 的单电源工作电压范围和 2.7V 至 5.25V

的双电源工作电压范围，采用业界通用的小型封装承载所有特性，是激光雷达、差分线路接收器应用以及测试和测量系统的理想选择。

TLV380x/TLV3811(C) 具有 5ps 的强大输入过驱性能，并且能够检测仅 240ps 的窄脉冲宽度。这些器件具有输入过驱可实现较小传播延迟变化，并且能够检测窄脉冲，是飞行时间 (ToF) 应用 ( 例如工厂自动化和无人机视觉 ) 的理想选择。

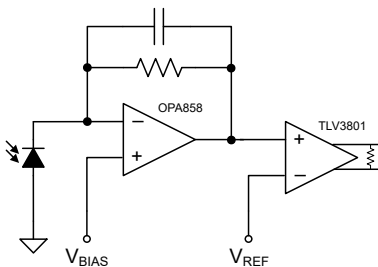
TLV380x/TLV3811(C) 的低压差分信号 (LVDS) 输出有助于提高数据吞吐量并优化功耗。同样，互补输出有助于通过抑制每个输出上的共模噪声来降低 EMI。LVDS 输出旨在驱动和直接连接可接受标准 LVDS 输入 ( 例如大多数 FPGA 和 CPU ) 的其他应用下游器件。

TLV3801 和 TLV3802 分别采用 8 引脚 WSON 和 12 引脚 WSON 封装，而 TLV3811(C) 采用微型 6 引脚 DSBGA 封装，均非常适合空间敏感型应用，例如光学传感器模块。

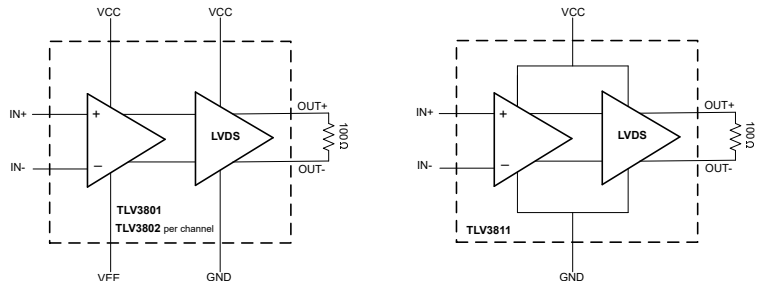
#### 器件信息

| 器件型号       | 封装 <sup>(1)</sup> | 封装尺寸 ( 标称值 )      |
|------------|-------------------|-------------------|
| TLV3801    | WSON (8)          | 2.00mm × 2.00mm   |
| TLV3811(C) | DSBGA (6)         | 1.218mm × 0.818mm |
| TLV3802    | WSON (12)         | 3.00mm × 2.00mm   |

1.如需了解所有可订购封装，请参阅数据表末尾的可订购产品附录。



TLV3801 光学接收器电路



功能方框图



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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision B (March 2023) to Revision C (November 2023) | Page     |
|--------------------------------------------------------------------|----------|
| • 将 TLV3802 的预发布更改为 RTM 版本.....                                    | <b>1</b> |

| Changes from Revision A (October 2022) to Revision B (March 2023) | Page     |
|-------------------------------------------------------------------|----------|
| • 在整个数据表中添加了 TLV3811(C) 和 TLV3802 ( 初始 ) .....                    | <b>1</b> |

| Changes from Revision * (December 2021) to Revision A (October 2022) | Page |
|----------------------------------------------------------------------|------|
|----------------------------------------------------------------------|------|

## 5 Pin Configuration and Functions

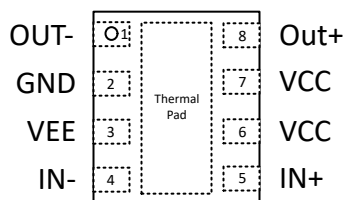


图 5-1. WSON Package  
8-Pin DSG  
Top View

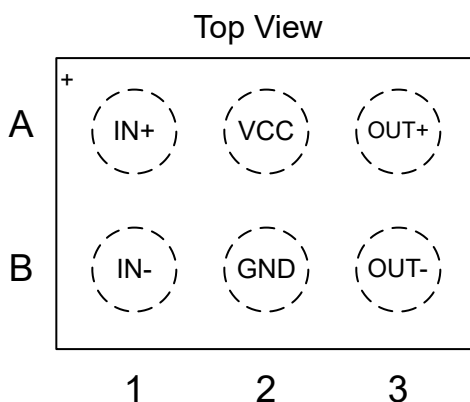
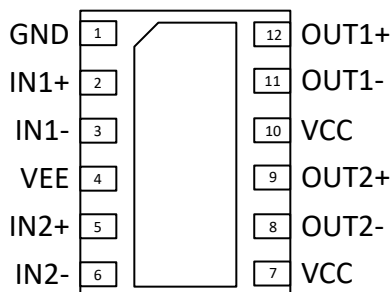


图 5-2. DSBGA Package  
6-Pin YBG  
Top View

表 5-1. Pin Functions

| PIN             |         |            | I/O | DESCRIPTION                                                       |
|-----------------|---------|------------|-----|-------------------------------------------------------------------|
| NAME            | TLV3801 | TLV3811(C) |     |                                                                   |
| IN+             | 5       | A1         | I   | Non-inverting input                                               |
| IN -            | 4       | B1         | I   | Inverting input                                                   |
| OUT+            | 8       | A3         | O   | Non-inverting output                                              |
| OUT -           | 1       | B3         | O   | Inverting output                                                  |
| V <sub>EE</sub> | 3       | -          | I   | Negative power supply<br>(If using single supply, connect to GND) |
| V <sub>CC</sub> | 6, 7    | A2         | I   | Positive power supply                                             |
| GND             | 2       | B2         | I   | Ground                                                            |



**图 5-3. WSON Package  
12-Pin DSS  
Top View**

**表 5-2. Pin Functions**

| PIN         |         | I/O | DESCRIPTION                                                       |
|-------------|---------|-----|-------------------------------------------------------------------|
| NAME        | TLV3802 |     |                                                                   |
| GND         | 1       | I   | Ground                                                            |
| IN1+        | 2       | I   | Channel 1 Non-inverting input                                     |
| IN1 -       | 3       | I   | Channel 1 Inverting input                                         |
| VEE         | 4       | I   | Negative power supply<br>(If using single supply, connect to GND) |
| IN2+        | 5       | I   | Channel 2 Non-inverting input                                     |
| IN2 -       | 6       | I   | Channel 2 Inverting input                                         |
| VCC         | 7       | I   | Positive power supply                                             |
| OUT2 -      | 8       | O   | Channel 2 Inverting output                                        |
| OUT2+       | 9       | O   | Channel 2 Non-inverting output                                    |
| VCC         | 10      | I   | Positive power supply                                             |
| OUT1 -      | 11      | O   | Channel 1 Inverting output                                        |
| OUT1+       | 12      | O   | Channel 1 Non-inverting output                                    |
| Thermal Pad | -       | -   | Connect directly to VEE                                           |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                                                                             | MIN            | MAX            | UNIT |
|-----------------------------------------------------------------------------|----------------|----------------|------|
| Supply voltage: ( $V_{CC} - V_{EE}$ ) and ( $V_{CC} - GND$ ) <sup>(2)</sup> | - 0.3          | 5.5            | V    |
| Input pins (IN+, IN-) from $V_{EE}$ (WSO) <sup>(3)</sup>                    | $V_{EE} - 0.3$ | $V_{CC} + 0.3$ | V    |
| Input pins (IN+, IN-) from GND (DSBGA) <sup>(4)</sup>                       | GND - 0.3      | $V_{CC} + 0.3$ | V    |
| Current into input pins (IN+, IN-)                                          | - 10           | 10             | mA   |
| Output (OUT+, OUT-)                                                         | GND            | $V_{CC}$       | V    |
| Current into output pins (OUT+, OUT-)                                       |                | 10             | mA   |
| Junction temperature, $T_J$                                                 |                | 150            | °C   |
| Storage temperature, $T_{slg}$                                              | - 65           | 150            | °C   |

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2)  $V_{EE}$  less than or equal to GND
- (3) Input terminals are diode-clamped to  $V_{EE}$  and  $V_{CC}$
- (4) Input terminals are diode-clamped to GND and  $V_{CC}$

### 6.2 ESD Ratings

|             |                         | VALUE                                                                 | UNIT  |
|-------------|-------------------------|-----------------------------------------------------------------------|-------|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>     | ±2000 |
|             |                         | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup> | ±1000 |

- (1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | TLV3801   | TLV3811(C)  | TLV3802   | UNIT |
|-------------------------------|----------------------------------------------|-----------|-------------|-----------|------|
|                               |                                              | DSG (WSO) | YBG (DSBGA) | DSS (WSO) |      |
|                               |                                              | 8 PINS    | 6 PINS      | 12 PINS   |      |
| $R_{qJA}$                     | Junction-to-ambient thermal resistance       | 69.4      | 132.1       | 63.2      | °C/W |
| $R_{qJC(top)}$                | Junction-to-case (top) thermal resistance    | 95.7      | 1.4         | 61.9      | °C/W |
| $R_{qJB}$                     | Junction-to-board thermal resistance         | 36.2      | 41          | 30.7      | °C/W |
| $\gamma_{JT}$                 | Junction-to-top characterization parameter   | 3.5       | 0.3         | 2.4       | °C/W |
| $\gamma_{JB}$                 | Junction-to-board characterization parameter | 36.0      | 41          | 30.7      | °C/W |
| $R_{qJC(bot)}$                | Junction-to-case (bottom) thermal resistance | 9.4       | n/a         | 8.7       | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) report.

### 6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                                                                     | MIN            | MAX            | UNIT |
|---------------------------------------------------------------------|----------------|----------------|------|
| Single supply operation: $V_{CC} - V_{EE}$ with $V_{EE} = GND$      | 2.7            | 5.25           | V    |
| Split supply operation: $V_{CC} - V_{EE}$ with $V_{EE} < GND$ (WSO) | 2.7            | 5.25           | V    |
| Split supply operation: $V_{CC} - GND$ with $V_{EE} < GND$ (WSO)    | 2.4            | 5.25           | V    |
| Input voltage range (WSO)                                           | $V_{EE} + 1.5$ | $V_{CC} + 0.1$ | V    |
| Input voltage range (DSBGA)                                         | GND + 1.5      | $V_{CC} + 0.1$ | V    |
| Differential Input voltage range                                    | - 1.5          | +1.5           | V    |

## 6.4 Recommended Operating Conditions (续)

over operating free-air temperature range (unless otherwise noted)

|                            | MIN  | MAX | UNIT |
|----------------------------|------|-----|------|
| Ambient temperature, $T_A$ | - 40 | 125 | °C   |

## 6.5 Electrical Characteristics

For  $V_{CC} = 3.3\text{ V}$ ,  $V_{EE} = \text{GND} = 0$ ,  $V_{CM} = 2.5\text{ V}$  at  $T_A = 25^\circ\text{C}$  (Unless otherwise noted)

| PARAMETER                                 |                                                 | TEST CONDITIONS                                                                                                                                                                                             | MIN                | TYP       | MAX               | UNIT          |
|-------------------------------------------|-------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|-----------|-------------------|---------------|
| <b>DC Input Characteristics</b>           |                                                 |                                                                                                                                                                                                             |                    |           |                   |               |
| $V_{OS}$                                  | Input offset voltage                            | $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$                                                                                                                                                           | - 5 <sup>(1)</sup> | $\pm 0.5$ | +5 <sup>(1)</sup> | mV            |
| $V_{HYS}$                                 | Input hysteresis voltage                        | TLV3801, TLV3802                                                                                                                                                                                            |                    | 2         |                   | mV            |
| $V_{HYS}$ (DSBGA)                         | Input hysteresis voltage                        | TLV3811                                                                                                                                                                                                     |                    | 1.1       |                   | mV            |
|                                           | Input hysteresis voltage                        | TLV3811C                                                                                                                                                                                                    |                    | 0         |                   | mV            |
| $V_{CM\text{-}Range}$                     | Common-mode voltage range                       | Single Supply: $V_{EE} = \text{GND}$<br>$V_{CC} - V_{EE} = 2.7\text{ V}$ to $5.25\text{ V}$<br>$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$                                                            | $V_{EE} + 1.5$     |           | $V_{CC}$          | V             |
| $V_{CM\text{-}Range}$ (WSO <sub>N</sub> ) | Common-mode voltage range                       | Split Supply: $V_{EE} < \text{GND}$<br>$V_{CC} - V_{EE} = 2.7\text{ V}$ to $5.25\text{ V}$ and $V_{CC} - \text{GND} = 2.4\text{ V}$ to $5.25\text{ V}$<br>$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ | $V_{EE} + 1.5$     |           | $V_{CC}$          | V             |
| CMRR (WSO <sub>N</sub> )                  | Common mode rejection ratio                     | $V_{CM} = V_{EE} + 1.5\text{ V}$ to $V_{CC}$                                                                                                                                                                |                    | 80        |                   | dB            |
| CMRR (DSBGA)                              | Common mode rejection ratio                     | $V_{CM} = \text{GND} + 1.5\text{ V}$ to $V_{CC}$                                                                                                                                                            |                    | 80        |                   | dB            |
| PSRR                                      | Power supply rejection ratio                    | Single Supply: $V_{EE} = \text{GND}$<br>$V_{CC} - V_{EE} = 2.7\text{ V}$ to $5.25\text{ V}$                                                                                                                 |                    | 80        |                   | dB            |
| PSRR (WSO <sub>N</sub> )                  | Power supply rejection ratio                    | Split Supply: $V_{EE} < \text{GND}$<br>$V_{CC} - V_{EE} = 2.7\text{ V}$ to $5.25\text{ V}$ and $V_{CC} - \text{GND} = 2.4\text{ V}$ to $5.25\text{ V}$                                                      |                    | 80        |                   | dB            |
| $I_B$                                     | Input bias current                              | $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$                                                                                                                                                           | - 10               | 2         | 10                | $\mu\text{A}$ |
| $I_{OS}$                                  | Input offset current                            | $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$                                                                                                                                                           | - 4                | $\pm 0.1$ | 4                 | $\mu\text{A}$ |
| $C_{IC}$                                  | Input capacitance, common mode                  |                                                                                                                                                                                                             |                    | 1         |                   | pF            |
| <b>DC Output Characteristics</b>          |                                                 |                                                                                                                                                                                                             |                    |           |                   |               |
| $V_{OCM}$                                 | Output common mode voltage                      | $V_{CC} - \text{GND} \geq 2.6\text{ V}$<br>$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$                                                                                                                | 1.125              | 1.25      | 1.375             | V             |
|                                           | Output common mode voltage                      | $V_{CC} - \text{GND} < 2.6\text{ V}$<br>$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$                                                                                                                   | 0.92               | 1.2       | 1.29              | V             |
| $\Delta V_{OCM}$                          | Output common mode voltage mismatch             | $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$                                                                                                                                                           | - 30               |           | 30                | mV            |
| $V_{OCM\_PP}$                             | Peak-to-Peak output common mode voltage         |                                                                                                                                                                                                             |                    | 50        |                   | mVpp          |
| $V_{OD}$                                  | Differential output voltage (WSO <sub>N</sub> ) | $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$                                                                                                                                                           | 250                | 350       | 450               | mV            |
| $V_{OD}$                                  | Differential output voltage (DSBGA)             | $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$                                                                                                                                                           | 240                | 350       | 450               | mV            |
| $\Delta V_{OD}$                           | Differential output voltage mismatch            | $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$                                                                                                                                                           | -30                |           | 30                | mV            |
| <b>Power Supply</b>                       |                                                 |                                                                                                                                                                                                             |                    |           |                   |               |
| $I_Q$ (TLV3801)                           | Quiescent current per comparator                | $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$                                                                                                                                                           |                    | 20        | 26.6              | mA            |

## 6.5 Electrical Characteristics (续)

For  $V_{CC} = 3.3\text{ V}$ ,  $V_{EE} = \text{GND} = 0$ ,  $V_{CM} = 2.5\text{ V}$  at  $T_A = 25^\circ\text{C}$  (Unless otherwise noted)

| PARAMETER                      |                                              | TEST CONDITIONS                                                                      | MIN | TYP       | MAX  | UNIT                 |
|--------------------------------|----------------------------------------------|--------------------------------------------------------------------------------------|-----|-----------|------|----------------------|
| $I_Q$<br>(TLV3811(C))          | Quiescent current per comparator             | $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$                                    |     | 17        | 23   | mA                   |
| $I_Q$<br>(TLV3802)             | Quiescent current per comparator             | $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$                                    |     | 19        | 23.5 | mA                   |
| <b>AC Characteristics</b>      |                                              |                                                                                      |     |           |      |                      |
| $t_{PD}$                       | Propagation delay                            | $V_{OVERDRIVE} = 50\text{ mV}$ , $V_{UNDERDRIVE} = 50\text{ mV}$ , 50 MHz Squarewave |     | 225       |      | ps                   |
| Tempco of $t_{PD}$             | Temperature Coefficient of propagation delay |                                                                                      |     | $\pm 0.2$ |      | ps/ $^\circ\text{C}$ |
| $t_{PD\_SKEW}$                 | Propagation delay skew                       | $V_{OVERDRIVE} = 50\text{ mV}$ , $V_{UNDERDRIVE} = 50\text{ mV}$ , 50 MHz Squarewave |     | $\pm 2.5$ |      | ps                   |
| $\Delta t_{PD}$ (TLV3802 only) | Channel-to-channel propagation delay skew    | $V_{OVERDRIVE} = V_{UNDERDRIVE} = 50\text{ mV}$ , 50 MHz Squarewave                  |     | 6         |      | ps                   |
| $t_{CM\_DISPERSION}$           | Common mode dispersion                       | $V_{CM}$ varied from $V_{CM}(\text{min})$ to $V_{CM}(\text{max})$                    |     | 2         |      | ps                   |
| $t_{OD\_DISPERSION}$           | Overdrive dispersion                         | Overdrive varied from 20 mV to 100 mV                                                |     | 5         |      | ps                   |
| $t_{OD\_DISPERSION}$           | Overdrive dispersion                         | Overdrive varied from 10 mV to 1 V                                                   |     | 15        |      | ps                   |
| $t_{UD\_DISPERSION}$           | Underdrive dispersion                        | Underdrive varied from 20 mV to 100 mV                                               |     | 7         |      | ps                   |
| $t_{UD\_DISPERSION}$           | Underdrive dispersion                        | Underdrive varied from 10 mV to 1 V                                                  |     | 10        |      | ps                   |
| $t_R$                          | Rise time                                    | 20% to 80%                                                                           |     | 135       |      | ps                   |
| $t_F$                          | Fall time                                    | 80% to 20%                                                                           |     | 135       |      | ps                   |
| $f_{TOGGLE}$                   | Input toggle frequency                       | $V_{IN} = 200\text{ mV}_{PP}$ Sine Wave, $V_{OD} = 550\text{ mV}$                    |     | 2.3       |      | GHz                  |
| $f_{TOGGLE}$                   | Input toggle frequency                       | $V_{IN} = 200\text{ mV}_{PP}$ Sine Wave, 50% Output swing                            |     | 3         |      | GHz                  |
| TR                             | Toggle Rate                                  | $V_{IN} = 200\text{ mV}_{PP}$ Sine Wave, $V_{OD} = 550\text{ mV}$                    |     | 4.6       |      | Gbps                 |
| TR                             | Toggle Rate                                  | $V_{IN} = 200\text{ mV}_{PP}$ Sine Wave, 50% Output swing                            |     | 6         |      | Gbps                 |
| PulseWidth                     | Minimum allowed input pulse width            | $V_{OVERDRIVE} = V_{UNDERDRIVE} = 50\text{ mV}$<br>$PW_{OUT} = 90\%$ of $PW_{IN}$    |     | 240       |      | ps                   |

(1) Ensured by characterization

## 6.6 Timing Diagrams

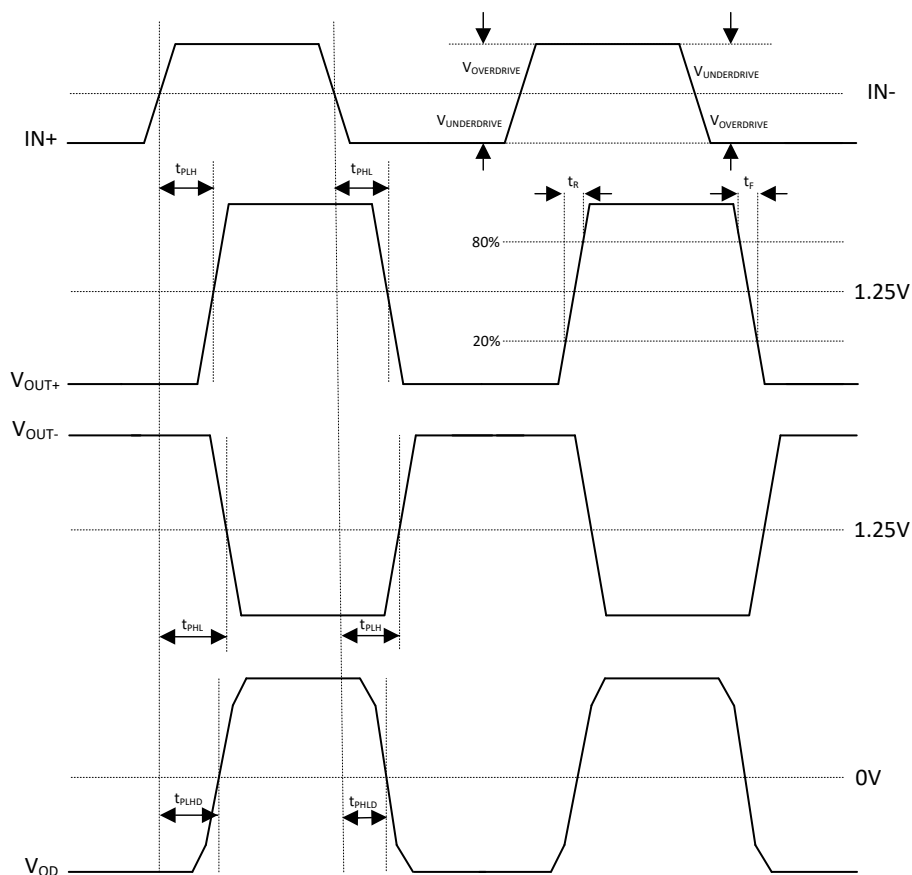


图 6-1. General Timing Diagram

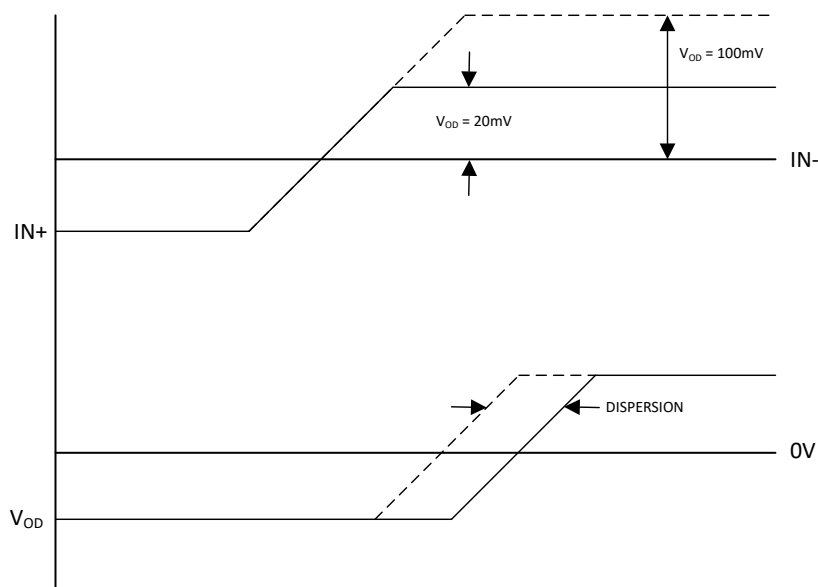


图 6-2. Overdrive Dispersion

## 6.7 Typical Characteristics

At  $T_A = 25^\circ\text{C}$ ,  $V_{CC} - V_{EE} = 3.3\text{ V}$  to  $5\text{ V}$  while  $V_{EE} = \text{GND} = 0$ ,  $V_{CM} = 2.5\text{ V}$ , and input overdrive/underdrive =  $50\text{ mV}$ , unless otherwise noted.

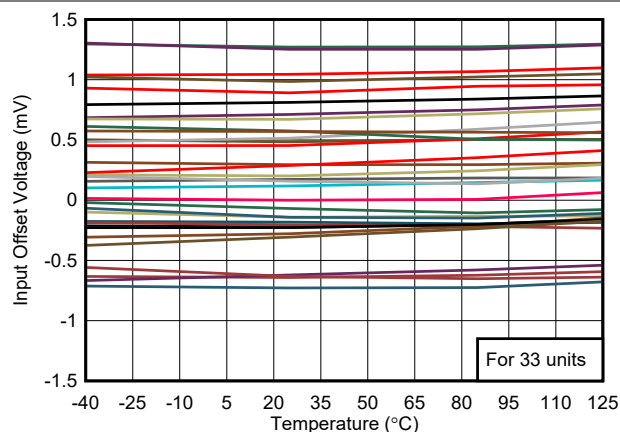


图 6-3. Offset vs. Temperature

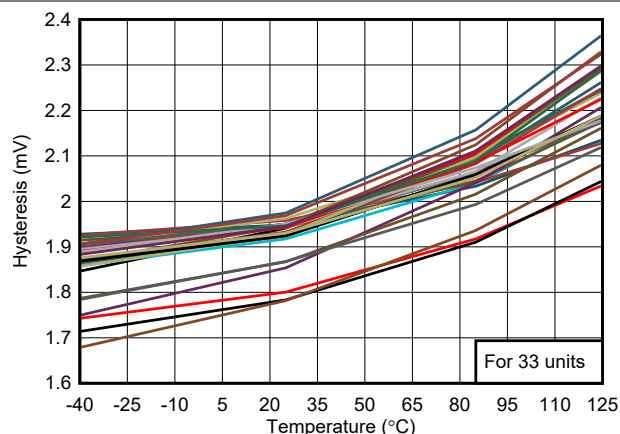


图 6-4. TLV3801 Hysteresis vs. Temperature

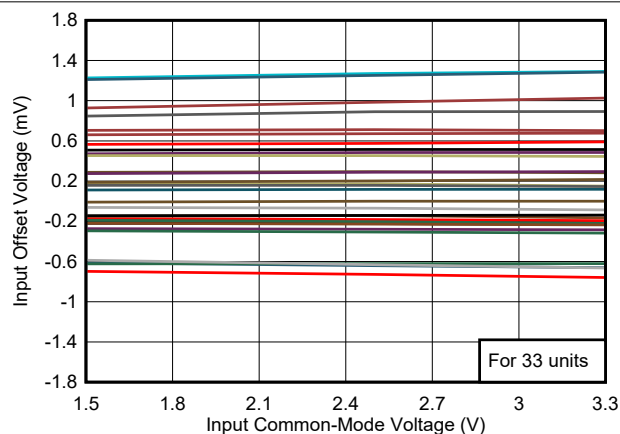


图 6-5. Offset vs. Common-Mode, 3.3 V

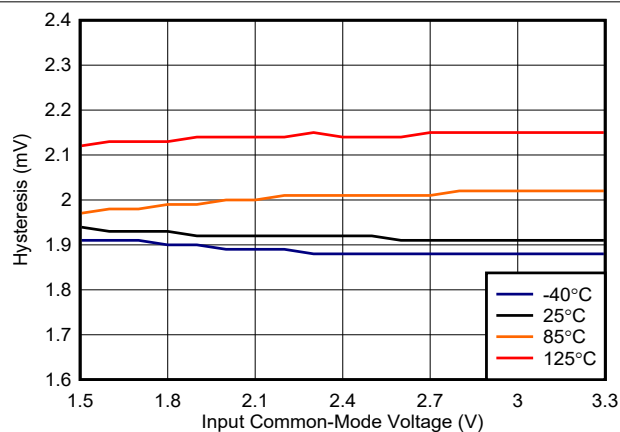


图 6-6. TLV3801 Hysteresis vs. Common-Mode, 3.3 V

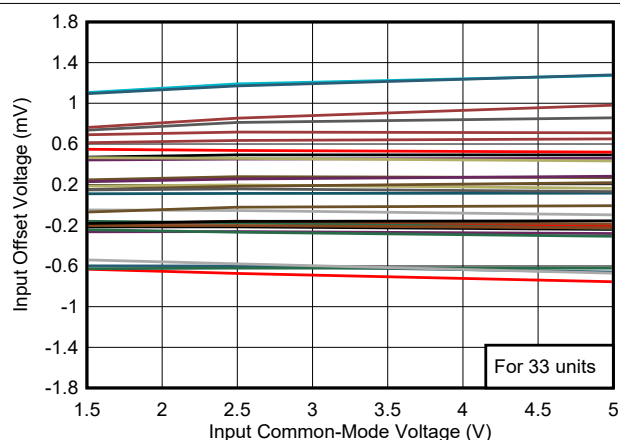


图 6-7. Offset vs. Common-Mode, 5 V

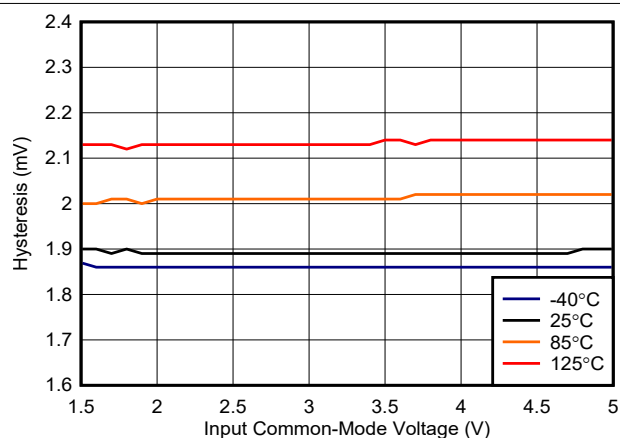


图 6-8. TLV3801 Hysteresis vs. Common-Mode, 5 V

## 6.7 Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $V_{CC} - V_{EE} = 3.3\text{ V}$  to  $5\text{ V}$  while  $V_{EE} = \text{GND} = 0$ ,  $V_{CM} = 2.5\text{ V}$ , and input overdrive/underdrive =  $50\text{ mV}$ , unless otherwise noted.

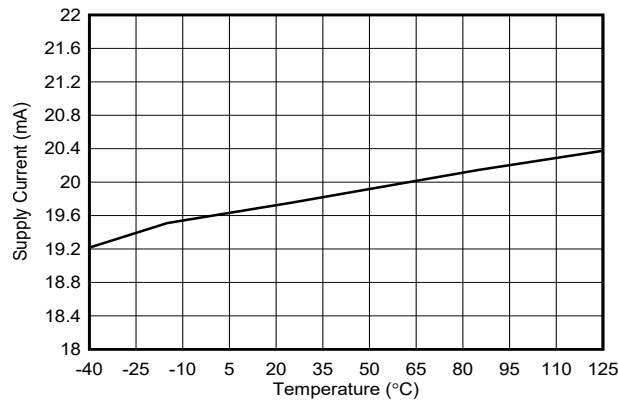


图 6-9. TLV3801 Supply Current vs. Temperature

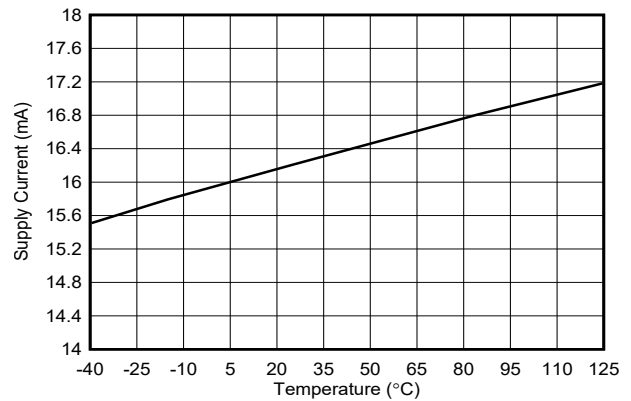


图 6-10. TLV3811(C) Supply Current vs. Temperature

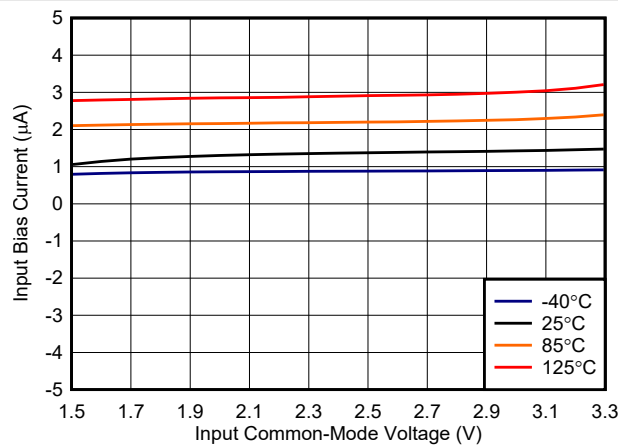


图 6-11. Bias Current vs. Common-Mode, 3.3 V

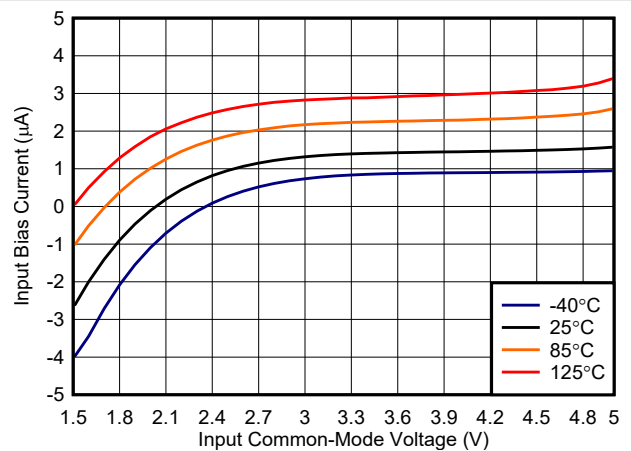


图 6-12. Bias Current vs. Common-Mode, 5 V

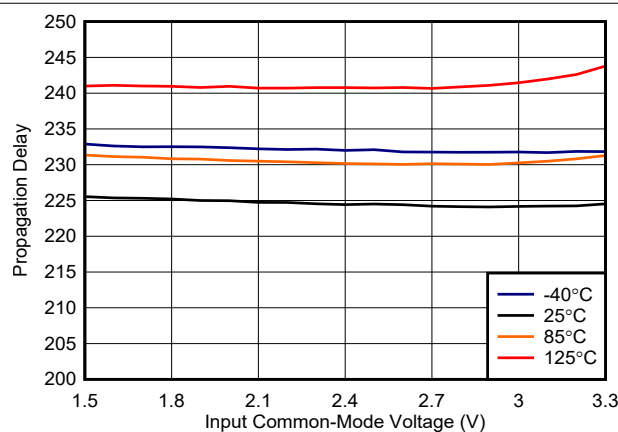


图 6-13. Propagation Delay vs. Common-Mode, 3.3 V

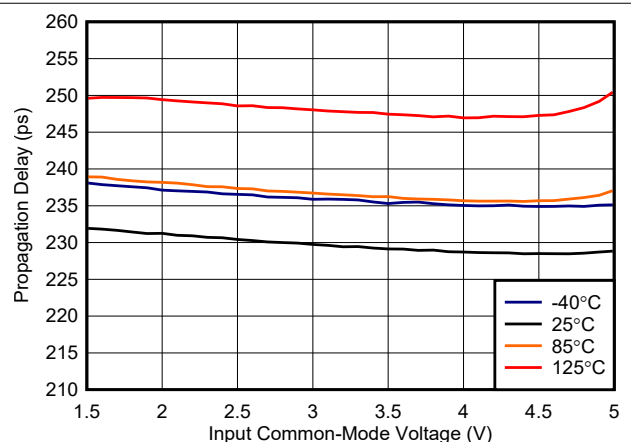


图 6-14. Propagation Delay vs. Common-Mode, 5 V

## 6.7 Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $V_{CC} - V_{EE} = 3.3\text{ V}$  to  $5\text{ V}$  while  $V_{EE} = \text{GND} = 0$ ,  $V_{CM} = 2.5\text{ V}$ , and input overdrive/underdrive =  $50\text{ mV}$ , unless otherwise noted.

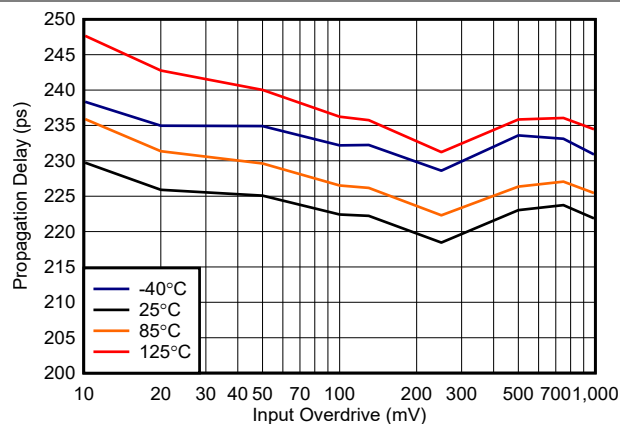


图 6-15. Propagation Delay vs. Overdrive, 3.3 V

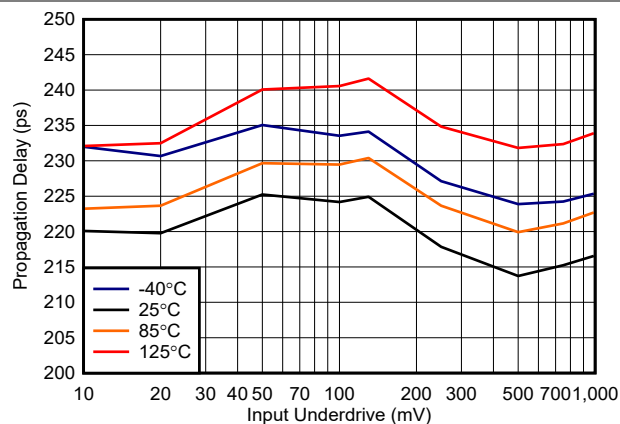


图 6-16. Propagation Delay vs. Underdrive, 3.3 V

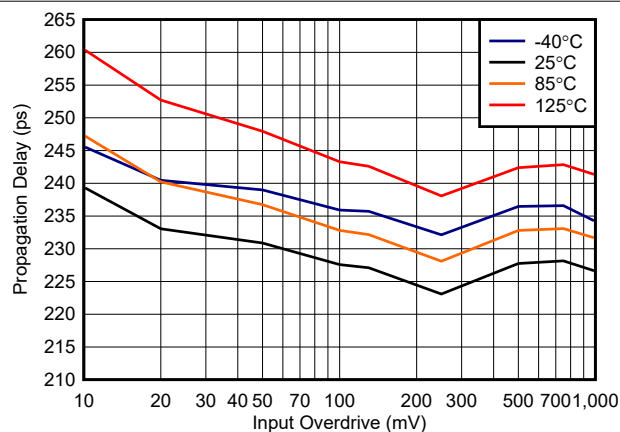


图 6-17. Propagation Delay vs. Overdrive, 5 V

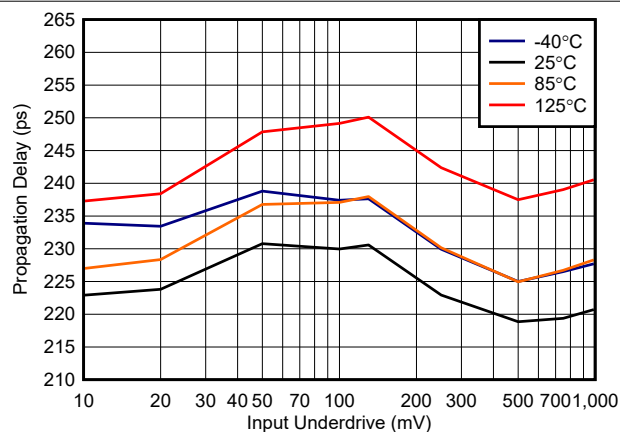


图 6-18. Propagation Delay vs. Underdrive, 5 V

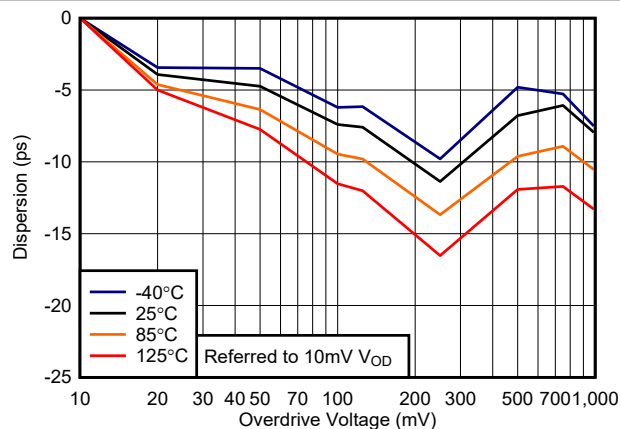


图 6-19. Dispersion vs. Overdrive, 3.3 V

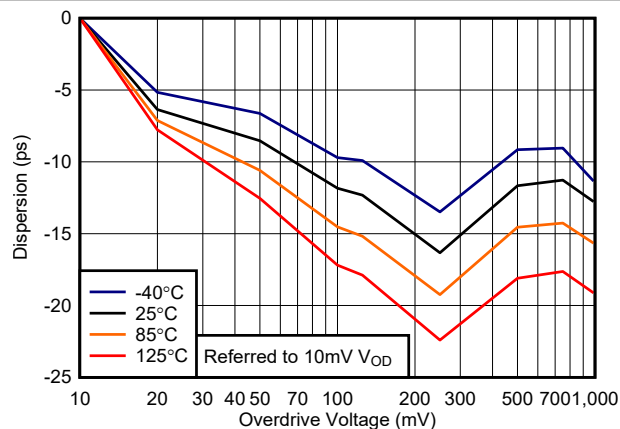


图 6-20. Dispersion vs. Overdrive, 5 V

## 6.7 Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $V_{CC} - V_{EE} = 3.3\text{ V}$  to  $5\text{ V}$  while  $V_{EE} = \text{GND} = 0$ ,  $V_{CM} = 2.5\text{ V}$ , and input overdrive/underdrive =  $50\text{ mV}$ , unless otherwise noted.

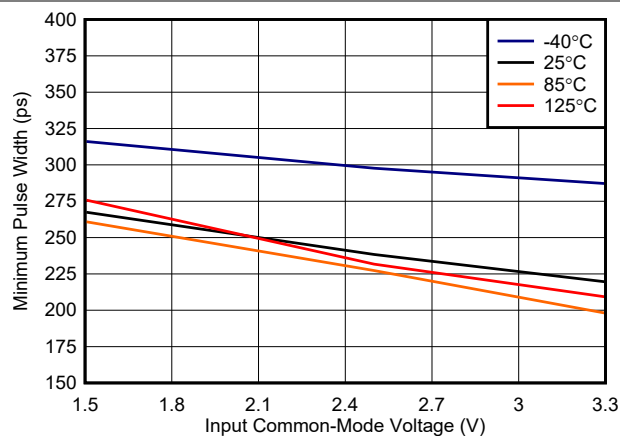


图 6-21. Minimum Pulse Width vs. Common-Mode, 3.3 V

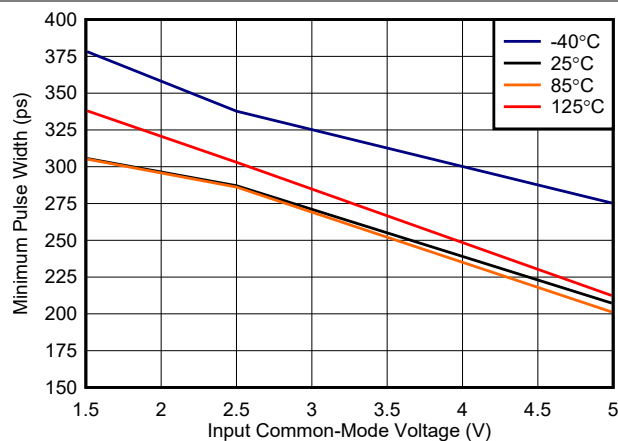


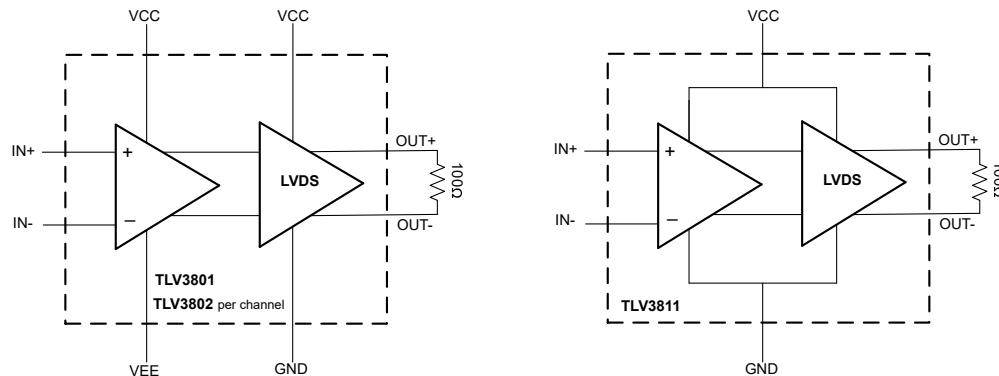
图 6-22. Minimum Pulse Width vs. Common-Mode, 5 V

## 7 Detailed Description

### 7.1 Overview

The TLV380x/TLV3811(C) are high-speed comparators with LVDS output. The fast response time of these comparators make them well suited for applications that require narrow pulse width detection or high toggle frequencies. The TLV3801 is available in the 8-pin WSON package and the TLV3802 is available in the 12-pin WSON package while the TLV3811(C) is available in the 6-pin DSBGA package.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

The TLV380x/TLV3811(C) are high-speed comparators with a typical propagation delay of 225 ps and LVDS output. The minimum pulse width detection capability is 240 ps and the typical toggle frequency is 3 GHz (6 Gbps). These comparators are well suited for distance sensing for LIDAR and time-of-flight applications as well as for high-speed test and measurement systems. The TLV380x has two separate power rails for the input and the output; this allows the input to be referenced from either single or split supply (VCC and VEE) while the output is referenced from ground (VCC and GND). On the other hand, the TLV3811(C) has one power rail for both inputs and outputs and can only be operated at a single supply.

### 7.4 Device Functional Modes

The TLV380x has a single functional mode and is operational on the condition that both the input supply voltage (VCC - VEE) is greater than or equal to 2.7 V and the output supply voltage (VCC - GND) is greater than or equal to 2.4 V.

The TLV3811(C) has a single functional mode and is operational when the power supply voltage (VCC - GND) is greater than or equal to 2.7 V.

#### 7.4.1 Inputs

The TLV380x/TLV3811(C) feature an input stage, capable of operating between 1.5 V above VEE (GND for TLV3811(C)) and 0.1 V above VCC, with an internal ESD protection circuit that includes two pairs of front-to-back diodes between IN+ and IN- as well as two 50 Ω resistors, as shown in 图 7-1. This prevents damage to the input stage by limiting the differential input voltage to be no more than twice the diode's forward-voltage drop  $2 \times V_F$  ( $2 \times 0.7$  V).

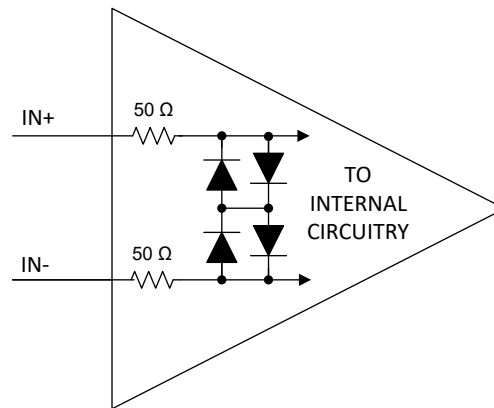


图 7-1. Input Stage Circuitry

When the differential input voltage exceeds  $2 \times V_F$ , the input bias current increases at the input pins IN+ and IN-, as shown in 方程式 1.

$$\text{Input Current} = [(V_{IN+} - V_{IN-}) - 2 \times V_F] / (2 \times 50) \quad (1)$$

To avoid damaging the inputs when exceeding the recommended input voltage range, an external resistor should be used to limit the current. The current should be limited to less than 10 mA.

#### 7.4.2 LVDS Output

The TLV380x/TLV3811(C) outputs are LVDS compliant. When the input of the downstream device is terminated with a 100  $\Omega$  resistor, the comparators provide a  $\pm 350$  mV differential swing at an output common-mode voltage of 1.25 V above GND. Fully differential outputs enable fast digital toggling and reduce EMI compared to single-ended output standards.

## 8 Application and Implementation

### 备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

#### 8.1.1 Capacitive Loads

Under reasonable capacitive loads, the device maintains specified propagation delay. However, excessive capacitive loading under high switching frequencies may increase supply current, propagation delay, or induce decreased slew rate.

#### 8.1.2 Hysteresis

A comparator's high, open-loop gain creates a small band of input differential voltage where the comparator may produce "chatter" which causes the output to toggle back and forth between a "logic high" and a "logic low". This can cause design challenges for inputs with slow rise and fall times or systems with excessive noise. These challenges can be prevented by adding hysteresis to the comparator. However, hysteresis must be added strategically when input signals are small since it can cause signals to go undetected. As a result, TLV3811C is optimized for detecting small, fast-switching inputs and has 0 mV of internal hysteresis. On the other hand, for detecting larger input signals in the presence of noise, the TLV3811 has 1.1 mV of internal hysteresis and TLV3801 and TLV3802 have 2 mV.

Since the TLV380x/TLV3811(C) only have a minimal amount of internal hysteresis, external hysteresis can be applied in the form of a positive feedback loop that adjusts the trip point of the comparator depending on its current output state. See the [Non-Inverting Comparator With Hysteresis](#) section for more details.

### 8.2 Typical Application

#### 8.2.1 Optical Receiver

The TLV380x/TLV3811(C) can be used in conjunction with a high performance amplifier such as the OPA858 to create an optical receiver as shown in the [图 8-1](#). The photodiode operates in photoconductive mode: exposure to light will cause a reverse current through the photodiode. A bias voltage is applied to the op amp's non-inverting input to prevent saturation at the negative power supply. The OPA858 takes the current conducting through the diode and translates it into a voltage for a high speed comparator to detect. The TLV380x/TLV3811(C) will then output the proper LVDS signal according to the threshold set ( $V_{REF}$ ).

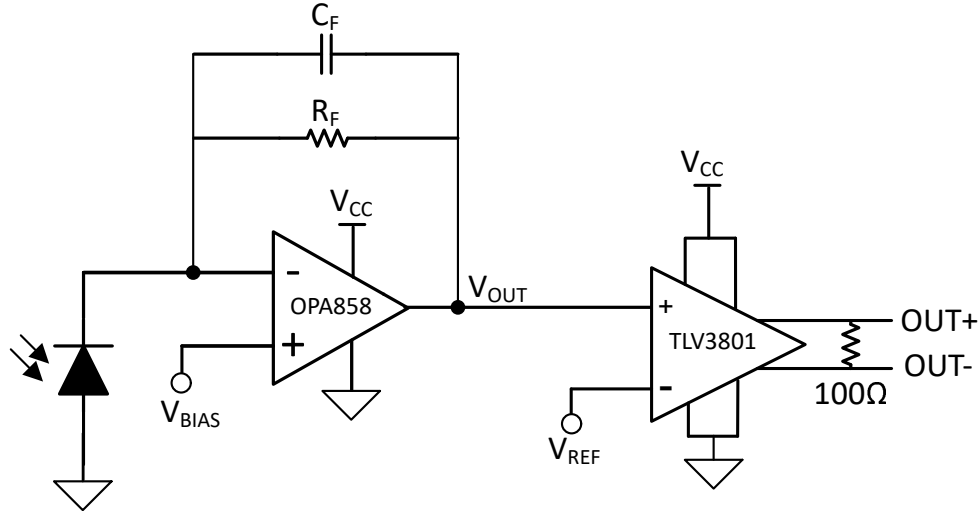


图 8-1. Optical Receiver

### 8.2.1.1 Design Requirements

表 8-1. Design Parameters

| PARAMETER        | VALUE       |
|------------------|-------------|
| $V_{CC}$         | +5 V        |
| $V_{EE}$         | 0 V         |
| $V_{OUT, SWING}$ | 100 mV      |
| $I_{DIODE}$      | 100 $\mu$ A |
| $f_p$            | 159 MHz     |

### 8.2.1.2 Detailed Design Procedure

Set  $V_{BIAS}$  to be in the recommended common-mode voltage range of the OPA858. This is also the minimum output voltage of the op amp  $V_{OUT, MIN}$  as the op amp will attempt to settle at the voltage applied to the non-inverting input.

The maximum output voltage of the op amp  $V_{OUT, MAX}$  can be calculated from the desired output voltage swing  $V_{OUT, SWING}$  and  $V_{OUT, MIN}$ , as shown in 方程式 2.

$$V_{OUT, MAX} = V_{OUT, SWING} + V_{OUT, MIN} \quad (2)$$

The gain resistor  $R_F$  is determined by the desired  $V_{OUT, MAX}$  and  $V_{OUT, MIN}$  and the maximum current  $I_{DIODE}$  through the diode, as shown in 方程式 2.

$$R_F = (V_{OUT, MAX} - V_{OUT, MIN}) / I_{DIODE} \quad (3)$$

The feedback capacitor, in combination with the gain resistor, forms a pole in the frequency response of the amplifier. The feedback capacitor can be determined by the gain resistor and the desired pole frequency  $f_p$ , as shown in 方程式 2.

$$C_F = 1 / (2 \times \pi \times R_F \times f_p) \quad (4)$$

Set  $V_{REF}$  to be the switching threshold voltage between  $V_{OUT, MAX}$  and  $V_{OUT, MIN}$ .

Select values for  $V_{BIAS}$  and  $V_{REF}$ . Plug in given values for  $V_{OUT, MAX}$ ,  $I_{DIODE}$ , and  $f_p$ . For the given example,  $V_{BIAS} = 1.5\text{ V}$ ,  $V_{REF} = 1.55\text{ V}$ , and  $R_F$ ,  $C_F$  is solved as  $1\text{ k}\Omega$  and  $1\text{ pF}$ , respectively.

For more information, please refer to the op amp tutorials for stability analysis on the transimpedance amplifier [Spice Stability Analysis](#) and [Op Amp Stability](#). See application note SBOA268A [Transimpedance Amplifier Circuit](#) for more detailed procedures.

### 8.2.1.3 Application Performance Plots

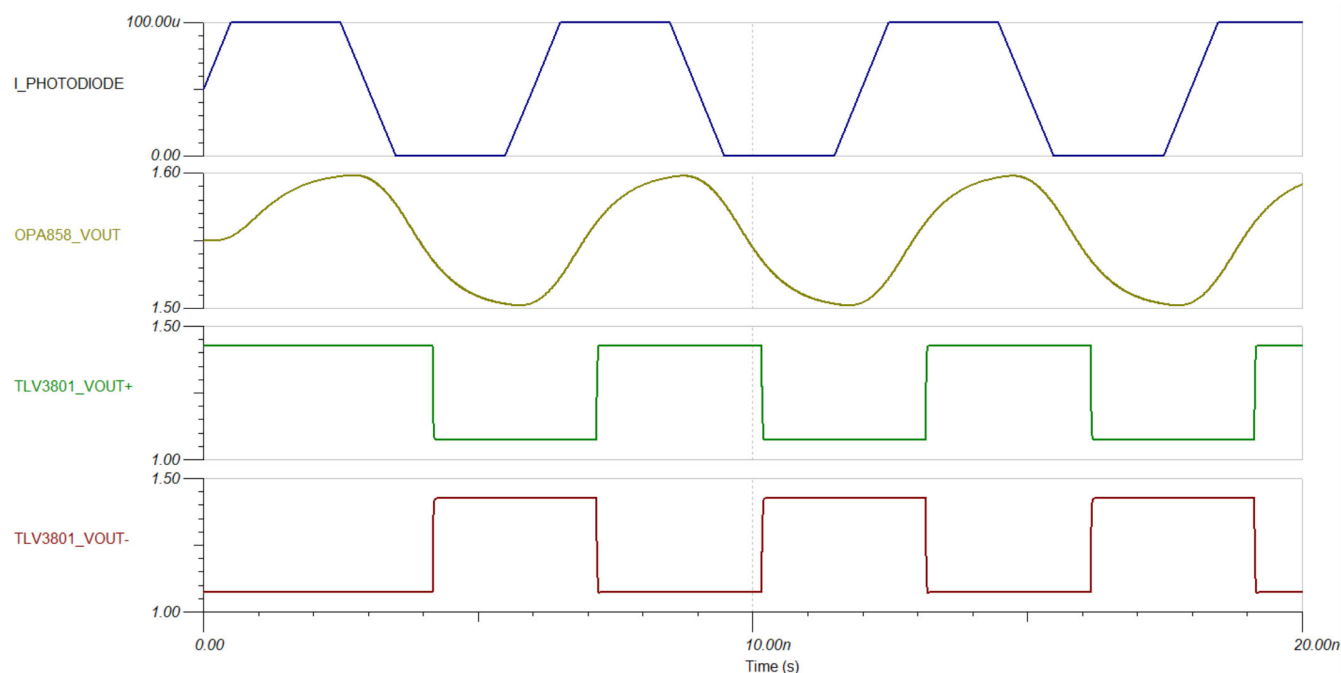


图 8-2. Optical Receiver Output Waveforms

### 8.2.2 Non-Inverting Comparator With Hysteresis

A way to implement external hysteresis is to add two resistors to the circuit: one in series between the reference voltage and the inverting pin, and another from the inverting pin to one of the differential output pins.

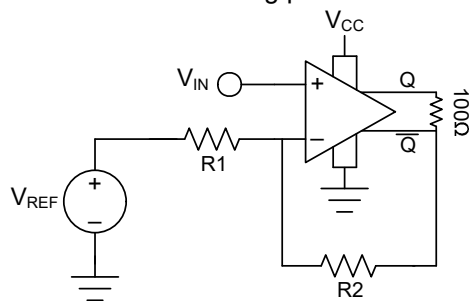


图 8-3. Non-Inverting Comparator with Hysteresis Circuit

#### 8.2.2.1 Design Requirements

表 8-2. Design Parameters

| PARAMETER | VALUE |
|-----------|-------|
| $V_{HYS}$ | 50 mV |
| $V_{REF}$ | 2.5 V |

表 8-2. Design Parameters (续)

| PARAMETER | VALUE   |
|-----------|---------|
| $V_{T1}$  | 2.34 V  |
| $V_{T2}$  | 2.29 V  |
| Q         | 1.375 V |
| $\bar{Q}$ | 1.025 V |

### 8.2.2.2 Detailed Design Procedure

First, create an equation for  $V_T$  that covers both output voltages when the output is high or low.

$$V_{T1} = \frac{V_{REF}R_2 + QR_1}{R_1 + R_2} \quad (5)$$

$$V_{T2} = \frac{V_{REF}R_2 + \bar{Q}R_1}{R_1 + R_2} \quad (6)$$

The hysteresis voltage in this network is equal to the difference in the two threshold voltage equations.

$$V_{HYS} = V_{T1} - V_{T2} \quad (7)$$

$$V_{HYS} = \frac{V_{REF}R_2 + QR_1}{R_1 + R_2} - \frac{V_{REF}R_2 + \bar{Q}R_1}{R_1 + R_2} \quad (8)$$

$$V_{HYS} = \frac{(Q - \bar{Q})R_1}{R_1 + R_2} \quad (9)$$

$$V_{HYS} = \frac{V_{OD}R_1}{R_1 + R_2} \quad (10)$$

Note that these equations do not take into account the effects of the internal hysteresis and offset voltage of the comparator. Design parameters will need to be adjusted accordingly.

Select a value for  $R_2$ . Plug in given values for  $V_{REF}$ ,  $V_{T1}$ ,  $V_{T2}$ ,  $Q$ , and  $\bar{Q}$ , and solve for  $R_1$ . For the given example,  $R_2 = 50 \text{ k}\Omega$ , and  $R_1$  is solved as  $= 8.3 \text{ k}\Omega$ .

### 8.2.2.3 Application Performance Plots

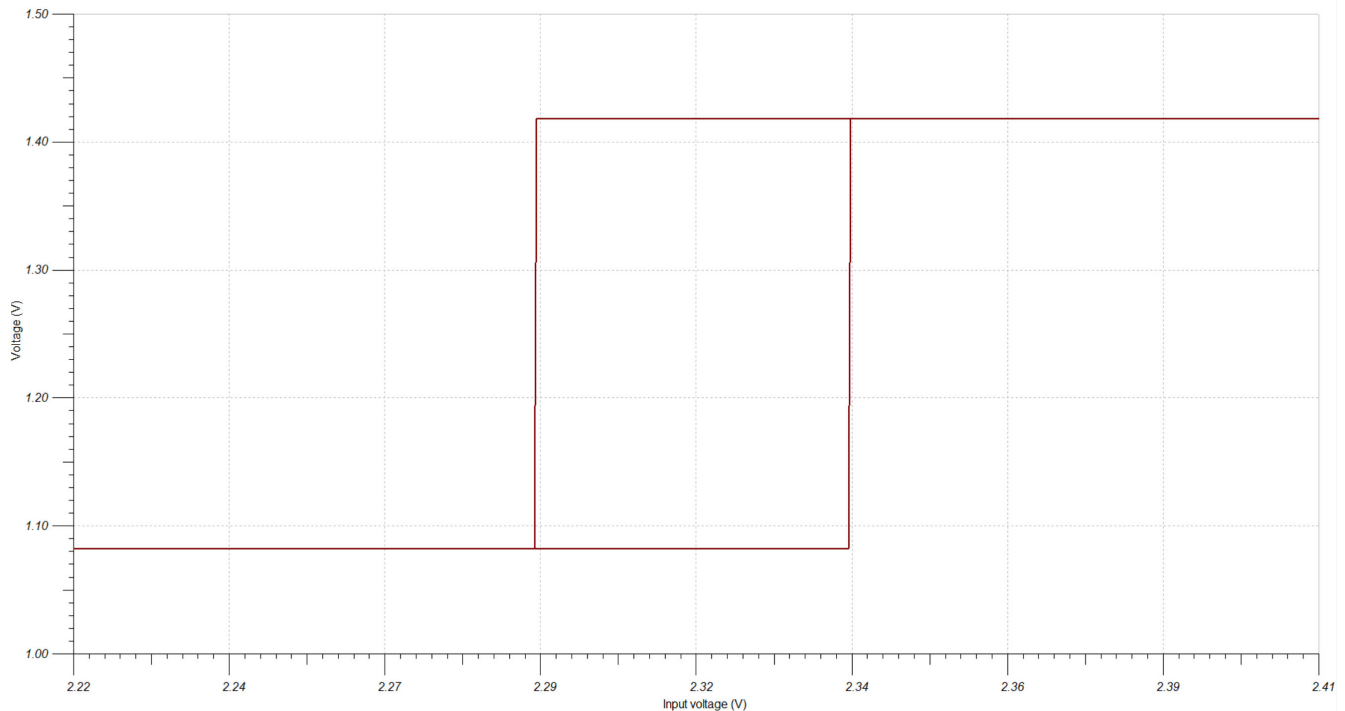


图 8-4. Hysteresis Curve for LVDS Comparator

### 8.2.3 Logic Clock Source to LVDS Transceiver

The 图 8-5 shows a logic clock source being terminated and driven with the TLV3802/TLV3811(C) across a CAT6 Cable to receive an equivalent LVDS clock signal at the receiver end.

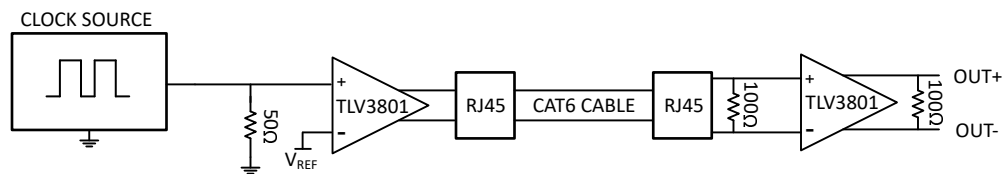


图 8-5. LVDS Clock Transceiver

### 8.2.4 External Trigger Function for Oscilloscopes

图 8-6 is a typical configuration for creating an external trigger on oscilloscopes. The user adjusts the trigger level, and a DAC converts this trigger level to a voltage the TLV380x/TLV3811(C) can use as a reference. The input voltage from an oscilloscope channel is then compared to the trigger reference voltage, and the TLV380x/TLV3811(C) sends an LVDS signal to a downstream FPGA to begin a capture. It is common to see bipolar inputs in test and measurement systems such as oscilloscopes; therefore, the TLV380x can be configured in split supply so that the inputs are in the allowable input voltage range.

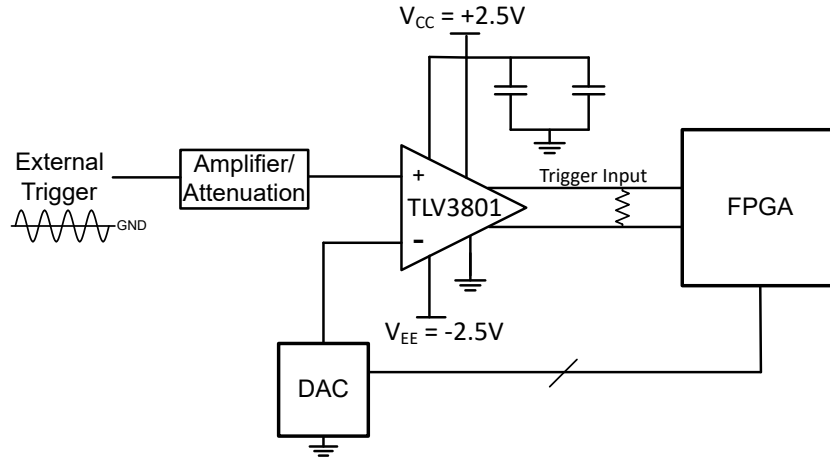


图 8-6. External Trigger Function

### 8.3 Power Supply Recommendations

The TLV380x has two separate power rails: VCC - VEE for the input stage and VCC - GND for the output stage. This allows for both single and split supply capabilities for the input stage with a separate ground reference for the LVDS output stage. Split supply operation allows users to apply both positive and negative (bipolar) voltages to the input pins.

When operating from a single supply, the supply voltage range for both the input and output stage is 2.7 V to 5.25 V. When operating from split supply rails, the supply voltage range for the input stage (VCC - VEE) is 2.7 V to 5.25 V, and the supply voltage range for the output stage (VCC - GND) is 2.4 V to 5.25 V. The output logic level is independent of the VCC and VEE levels. The TLV3811(C) is specified for operation from 2.4 V to 5.25 V and can only be operated from a single supply with both inputs and outputs referenced to GND.

Regardless of single supply or split supply operation, proper decoupling capacitors are required. It is recommended to use a scheme of multiple, low-ESR ceramic capacitors from the supply pins to the ground plane for optimum performance. A good combination would be 100 pF, 10 nF, and 1 uF with the lowest value capacitor closest to the comparator.

## 8.4 Layout

### 8.4.1 Layout Guidelines

Comparators are very sensitive to input noise. For best results, adhere to the following layout guidelines.

1. Use a printed-circuit-board (PCB) with a good, unbroken, low-inductance ground plane. Proper grounding (use of a ground plane) helps maintain specified device performance.
2. To minimize supply noise for single and split supply, place decoupling capacitor arrays as close as possible to  $V_{CC}$ .
3. On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep inputs away from the output.
4. Solder the device directly to the PCB rather than using a socket.
5. For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000 pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to propagation delay when impedance is low. The topside ground plane runs between the output and inputs.
6. Use a 100  $\Omega$  termination resistor across the device's LVDS output.
7. Use higher performance substrate materials such as Rogers.

### 8.4.2 Layout Example

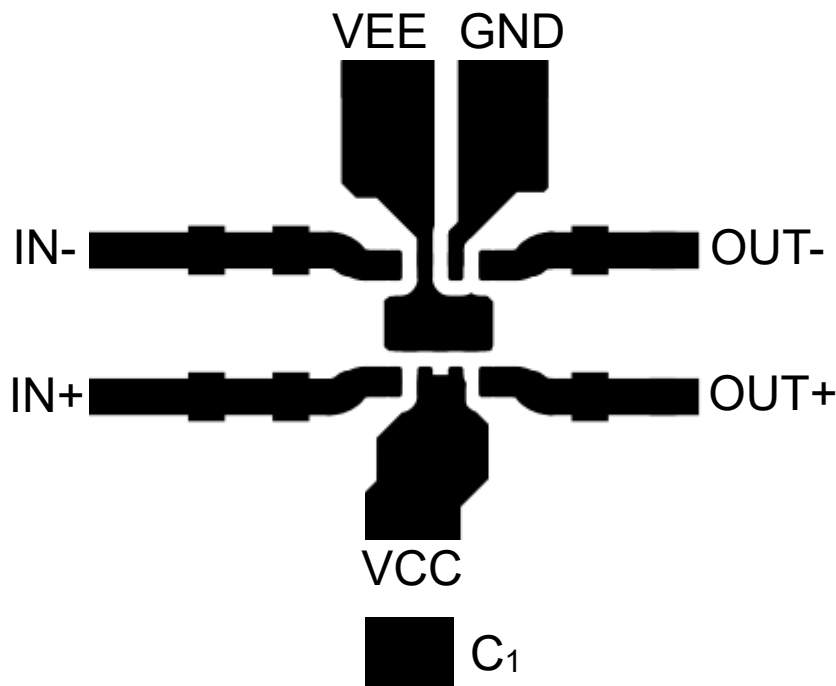


图 8-7. TLV3801EVM Layout Example

## 9 Device and Documentation Support

### 9.1 Device Support

#### 9.1.1 Development Support

*LIDAR Pulsed Time of Flight Reference Design*

### 9.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 9.3 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

### 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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### 9.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 9.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number        | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">TLV3801DSGR</a>  | Active        | Production           | WSO (DSG)   8   | 3000   LARGE T&R      | Yes         | SN                                   | Level-2-260C-1 YEAR               | -40 to 125   | 3801                |
| TLV3801DSGR.Z                | Active        | Production           | WSO (DSG)   8   | 3000   LARGE T&R      | Yes         | SN                                   | Level-2-260C-1 YEAR               | -40 to 125   | 3801                |
| <a href="#">TLV3801DSGT</a>  | Active        | Production           | WSO (DSG)   8   | 250   SMALL T&R       | Yes         | SN                                   | Level-2-260C-1 YEAR               | -40 to 125   | 3801                |
| TLV3801DSGT.Z                | Active        | Production           | WSO (DSG)   8   | 250   SMALL T&R       | Yes         | SN                                   | Level-2-260C-1 YEAR               | -40 to 125   | 3801                |
| <a href="#">TLV3802DSSR</a>  | Active        | Production           | WSO (DSS)   12  | 3000   LARGE T&R      | Yes         | SN                                   | Level-2-260C-1 YEAR               | -40 to 125   | 3802                |
| TLV3802DSSR.Z                | Active        | Production           | WSO (DSS)   12  | 3000   LARGE T&R      | Yes         | SN                                   | Level-2-260C-1 YEAR               | -40 to 125   | 3802                |
| <a href="#">TLV3811CYBGR</a> | Active        | Production           | DSBGA (YBG)   6 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | 02                  |
| <a href="#">TLV3811CYBGT</a> | Active        | Production           | DSBGA (YBG)   6 | 250   LARGE T&R       | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | 02                  |
| <a href="#">TLV3811YBGR</a>  | Active        | Production           | DSBGA (YBG)   6 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | LQ                  |
| <a href="#">TLV3811YBGT</a>  | Active        | Production           | DSBGA (YBG)   6 | 250   SMALL T&R       | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | LQ                  |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF TLV3801, TLV3802 :**

- Automotive : [TLV3801-Q1](#), [TLV3802-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLV3801DSGR  | WSO          | DSG             | 8    | 3000 | 180.0              | 8.4                | 2.2     | 2.2     | 1.2     | 4.0     | 8.0    | Q2            |
| TLV3801DSGT  | WSO          | DSG             | 8    | 250  | 179.0              | 8.4                | 2.2     | 2.2     | 1.2     | 4.0     | 8.0    | Q2            |
| TLV3802DSSR  | WSO          | DSS             | 12   | 3000 | 180.0              | 8.4                | 2.3     | 3.2     | 1.0     | 4.0     | 8.0    | Q1            |
| TLV3811CYBGR | DSBGA        | YBG             | 6    | 3000 | 180.0              | 8.4                | 0.87    | 1.27    | 0.6     | 2.0     | 8.0    | Q2            |
| TLV3811CYBGT | DSBGA        | YBG             | 6    | 250  | 180.0              | 8.4                | 0.87    | 1.27    | 0.6     | 2.0     | 8.0    | Q2            |
| TLV3811YBGT  | DSBGA        | YBG             | 6    | 250  | 180.0              | 8.4                | 0.87    | 1.27    | 0.6     | 2.0     | 8.0    | Q2            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TLV3801DSGR  | WSN          | DSG             | 8    | 3000 | 213.0       | 191.0      | 35.0        |
| TLV3801DSGT  | WSN          | DSG             | 8    | 250  | 213.0       | 191.0      | 35.0        |
| TLV3802DSSR  | WSN          | DSS             | 12   | 3000 | 213.0       | 191.0      | 35.0        |
| TLV3811CYBGR | DSBGA        | YBG             | 6    | 3000 | 182.0       | 182.0      | 20.0        |
| TLV3811CYBGT | DSBGA        | YBG             | 6    | 250  | 182.0       | 182.0      | 20.0        |
| TLV3811YBGT  | DSBGA        | YBG             | 6    | 250  | 182.0       | 182.0      | 20.0        |

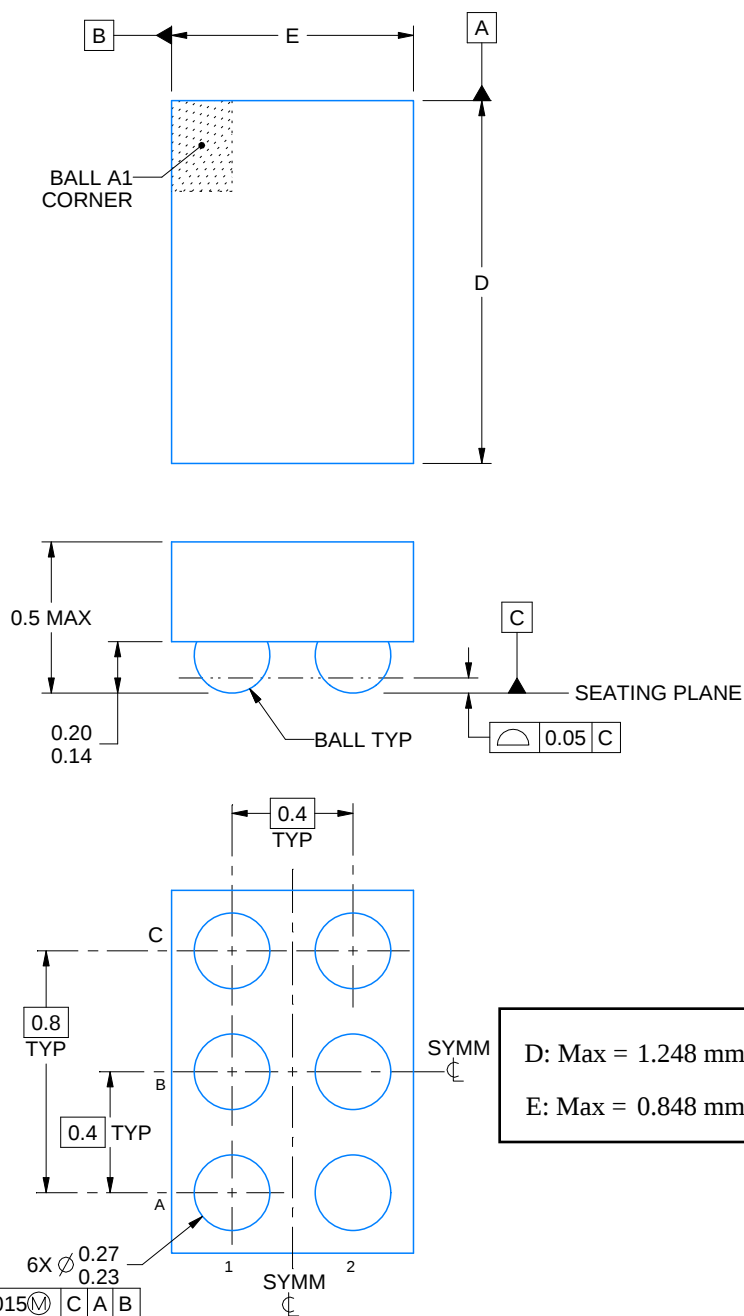
YBG0006



# PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4224328/A 05/2018

## NOTES:

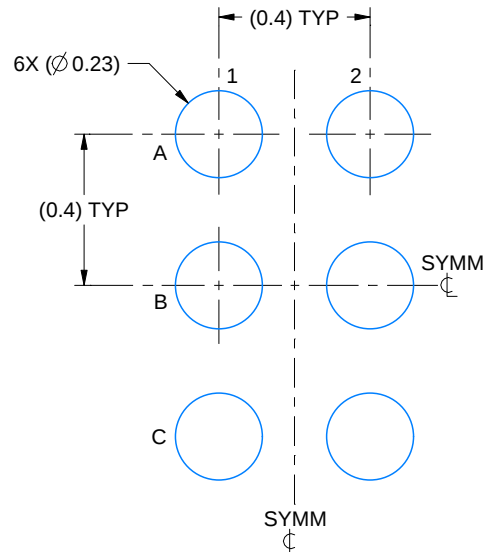
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

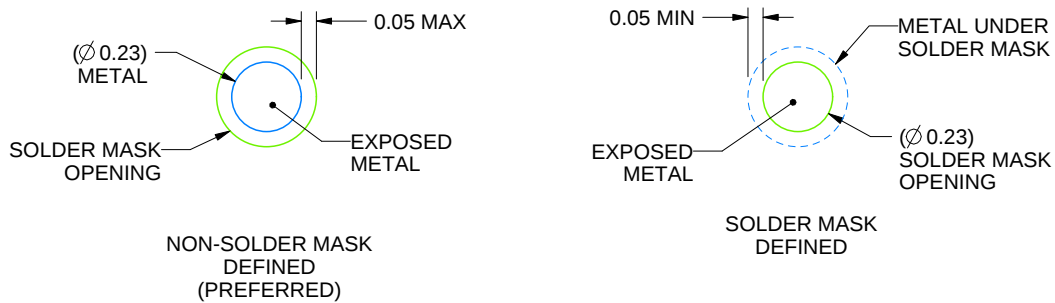
YBG0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 50X

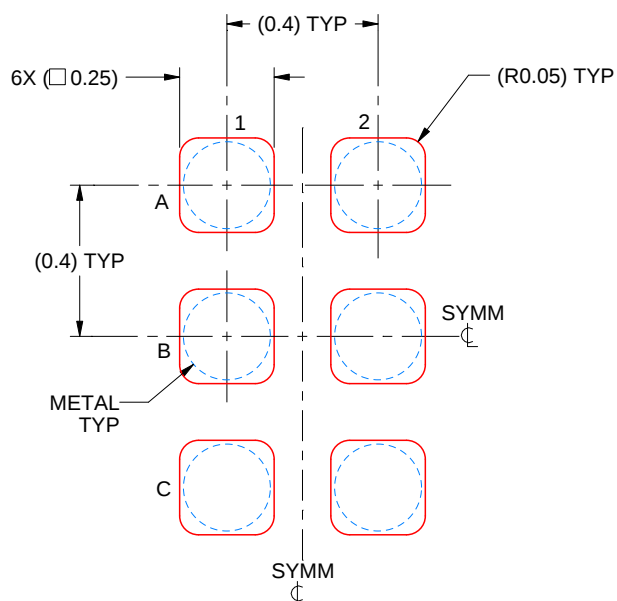


SOLDER MASK DETAILS  
NOT TO SCALE

4224328/A 05/2018

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).



SOLDER PASTE EXAMPLE  
 BASED ON 0.1 mm THICK STENCIL  
 SCALE: 50X

4224328/A 05/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

## GENERIC PACKAGE VIEW

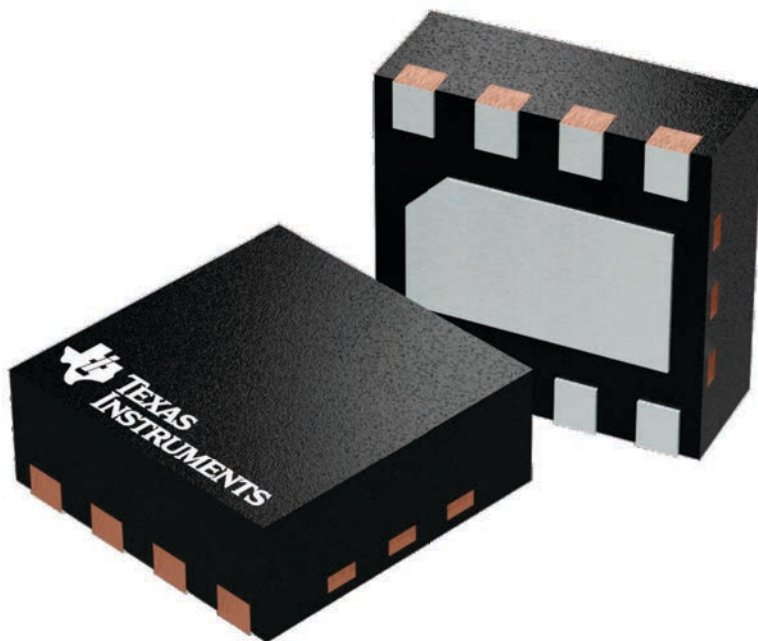
**DSG 8**

**WSON - 0.8 mm max height**

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224783/A

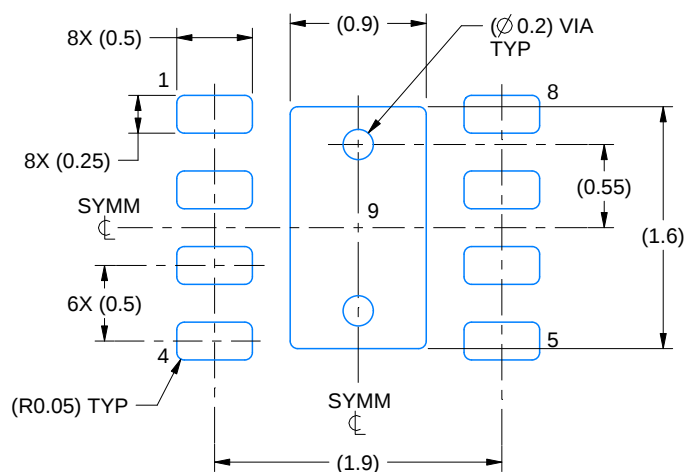


# EXAMPLE BOARD LAYOUT

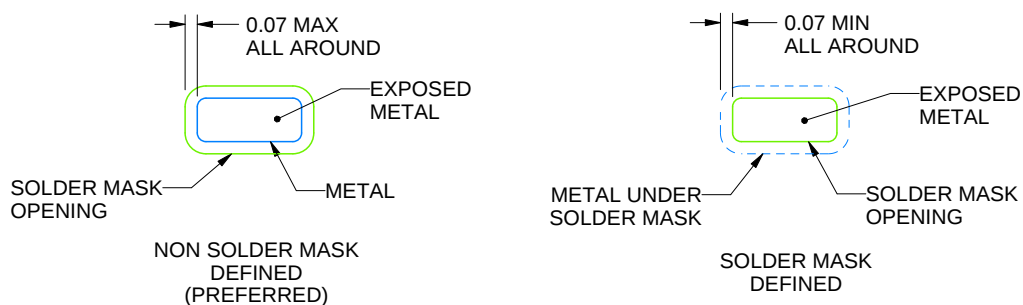
DSG0008B

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



**LAND PATTERN EXAMPLE**  
EXPOSED METAL SHOWN  
SCALE:20X



**SOLDER MASK DETAILS**

4222124/E 05/2020

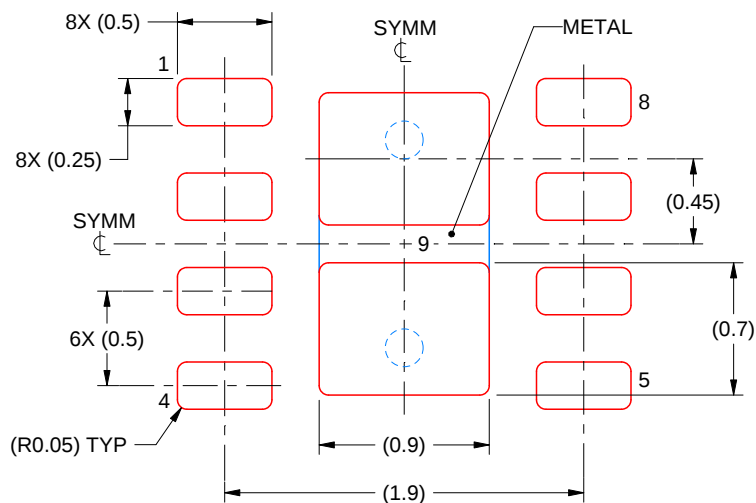
NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slue271](http://www.ti.com/lit/slue271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

**DSG0008B**

**WSN - 0.8 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



## SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:  
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:25X

4222124/E 05/2020

NOTES: (continued)

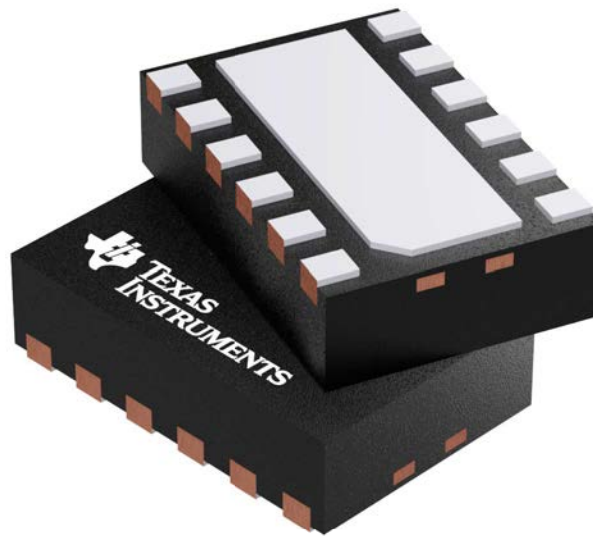
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## GENERIC PACKAGE VIEW

**DSS 12**

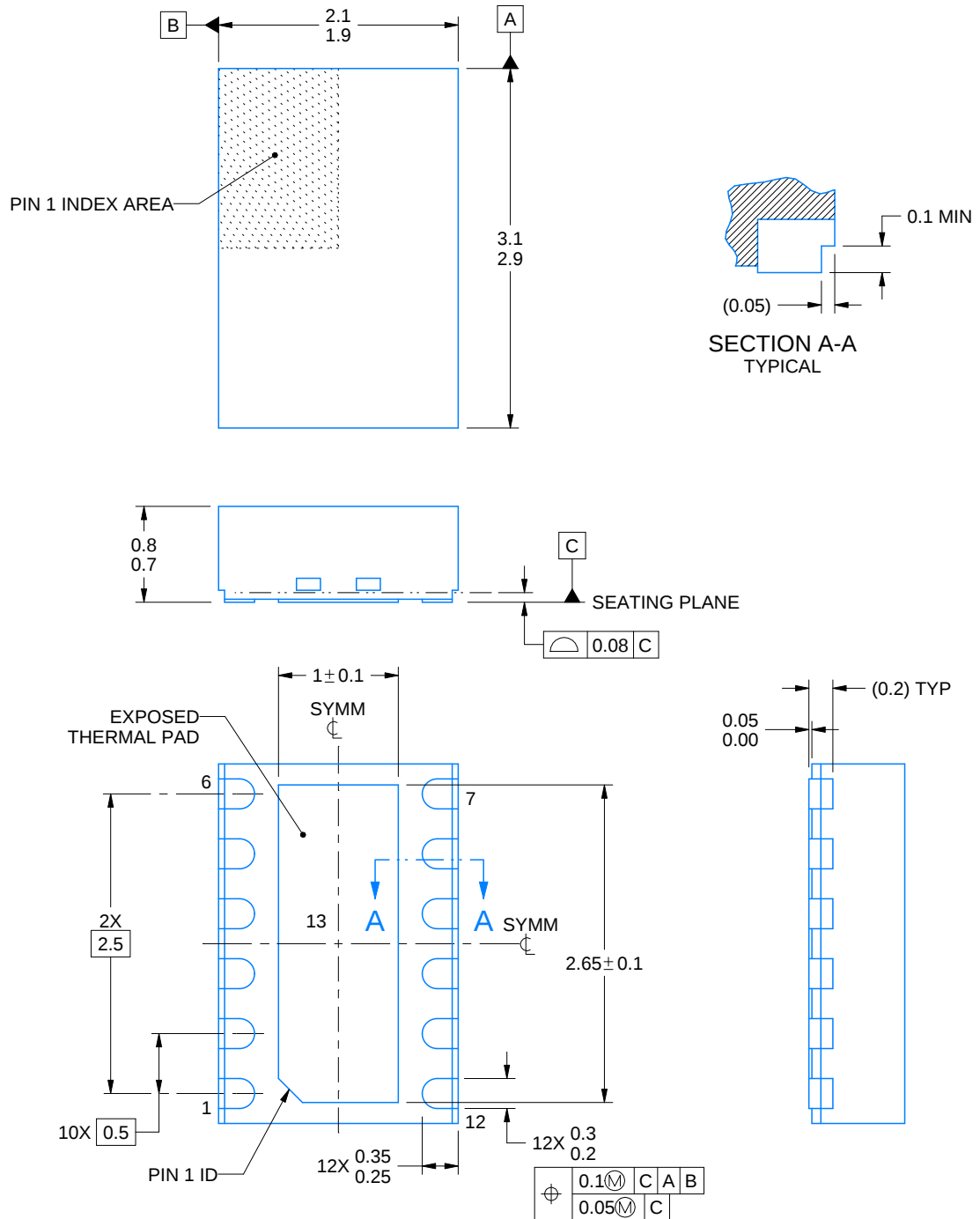
**WSON - 0.8 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4209244/D



4224220/A 02/2018

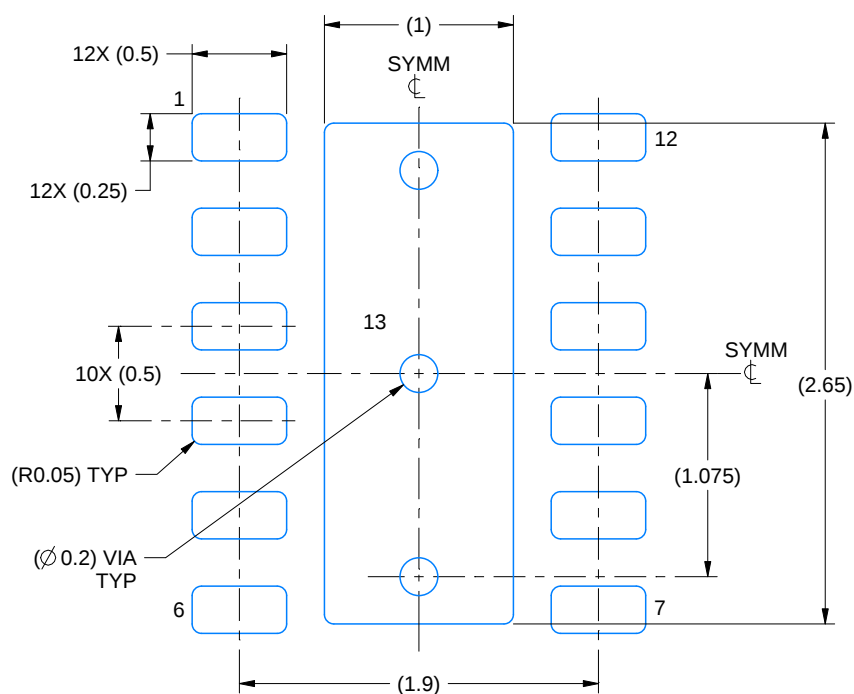
**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

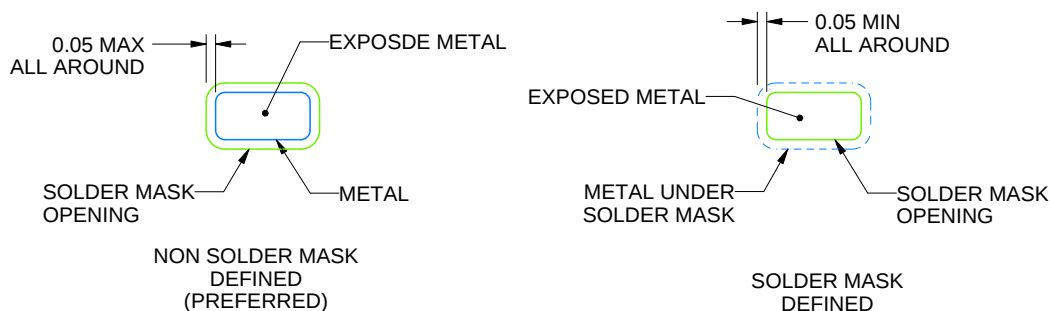
**DSS0012C**

**WSN - 0.8 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:25X



## SOLDER MASK DETAILS

4224220/A 02/2018

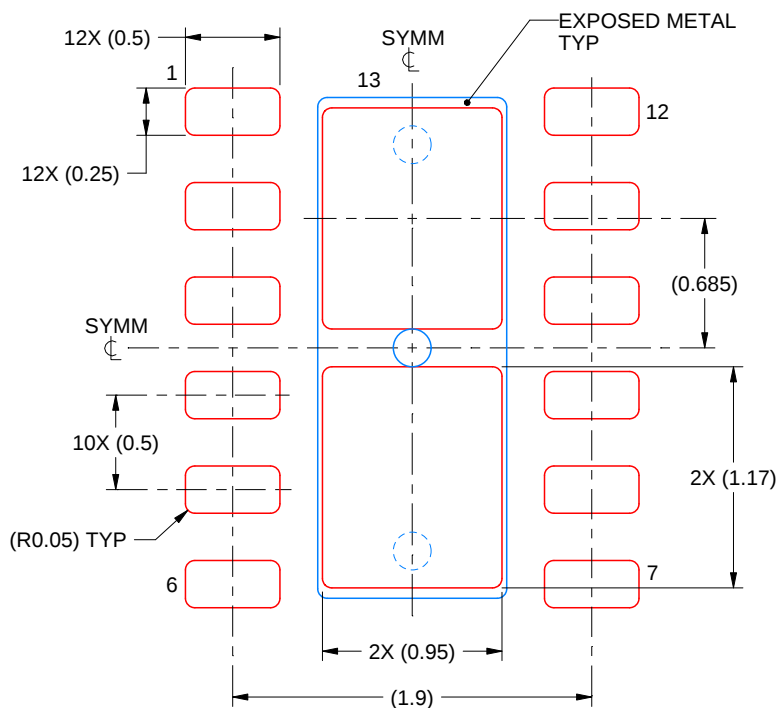
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

**DSS0012C**

**WSON - 0.8 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 13:  
83% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:25X

4224220/A 02/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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