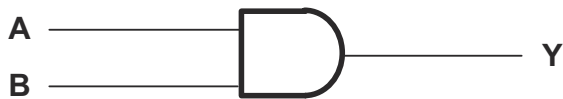


SN74AUP1G08 低功耗单路双输入正与门

1 特性

- 采用具有 0.5mm 间距的超小型 0.64mm² 封装 (DPW)
- 低静态功耗：
 $I_{CC} = 0.9 \mu A$ (最大值)
- 低动态功耗：
电压为 3.3V 时， $C_{pd} = 4.3pF$ (典型值)
- 低输入电容： $C_i = 1.5pF$ (典型值)
- 低噪声：过冲和下冲
< V_{CC} 的 10%
- I_{off} 支持带电插入、局部关断模式和后驱动保护
- 施密特触发操作可在输入端实现慢速输入转换和更佳的开关噪声抗扰度 ($V_{hys}=250mV$ ，这是 3.3V 时的典型值)
- 0.8V 至 3.6V 的宽工作 V_{CC} 范围
- 针对 3.3V 运行进行了优化
- 3.6V 耐压 I/O 支持混合模式的信号操作
- 3.3V 时， $t_{pd} = 4.3ns$ (最大值)
- 适用于点到点应用
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范的要求
- ESD 性能测试符合 JESD 22 标准
 - 2000V 人体放电模型 (A114-B, II 类)
 - 1000V 充电器件模型 (C101)



简化版原理图

2 应用

- ATCA 解决方案
- 有源噪声消除 (ANC)
- 条形码扫描仪
- 血压监护仪
- CPAP 呼吸机
- 电缆解决方案
- DLP 3D 机器视觉、高光谱成像、光纤网络和光谱分析
- 电子书
- 嵌入式 PC
- 现场变送器：温度或压力传感器
- 指纹识别
- HVAC：暖通空调
- 网络附属存储 (NAS)
- 服务器主板和电源装置 (PSU)
- 软件定义无线电 (SDR)
- 电视：高清电视 (HDTV)、LCD 电视和数字电视
- 视频通信系统
- 无线数据存取卡、耳机、键盘、鼠标和 LAN 卡
- X 射线：行李扫描仪、医疗和牙科

3 说明

此单路双输入正与门可在 0.8V 至 3.6V V_{CC} 下运行并以正逻辑执行布尔函数 $Y = A \bullet B$ or $Y = \overline{\overline{A} + \overline{B}}$ 。

器件信息

器件型号	封装 ⁽¹⁾	本体尺寸 (标称值)
SN74AUP1G08DBV	SOT-23 (5)	2.90mm x 1.60mm
SN74AUP1G08DRL	SOT (5)	1.60mm x 1.20mm
SN74AUP1G08DRY	SON (6)	1.45mm x 1.00mm
SN74AUP1G08DPW	X2SON (5)	0.80mm x 0.80mm
SN74AUP1G08YZP	DSBGA (5)	1.37mm x 0.88mm
SN74AUP1G08DCK	SC70 (5)	1.25mm x 2.00mm
SN74AUP1G08DSF	SON (6)	1.00mm x 1.00mm
SN74AUP1G08YFP	DSBGA (6)	1.16mm x 0.76mm

- (1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



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4 引脚配置和功能

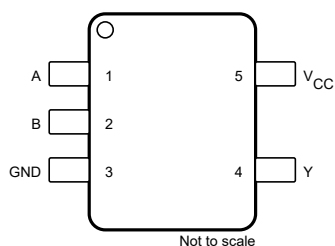
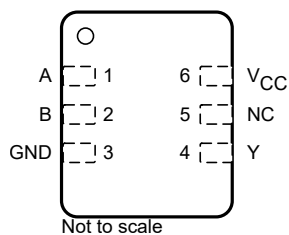
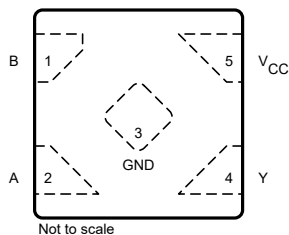


图 4-1. DRL、DCK 或 DBV 封装 5 引脚 SOT、SC70 或 SOT-23 (顶视图)



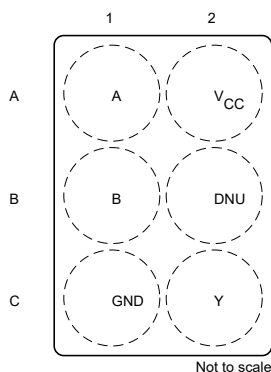
N.C. - 无内部连接

图 4-2. DRY 或 DSF 封装 6 引脚 SON (顶视图)



请参阅机械制图，了解尺寸。

图 4-3. DPW 封装 5 引脚 X2SON (顶视图)



保留 - 未使用

图 4-4. YFP 封装 6 引脚 DSBGA (顶视图)

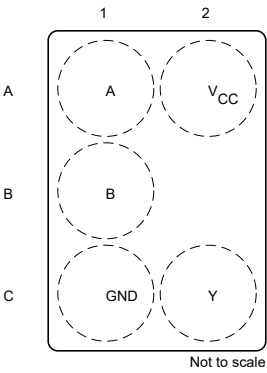


图 4-5. YZP 封装 5 引脚 DSBGA (顶视图)

表 4-1. 引脚功能

引脚						I/O	说明
名称	DRL、 DCK、DBV	DPW	DRY、DSF	YZP	YFP		
A	1	2	1	A1	A1	I	输入 A
B	2	1	2	B1	B1	I	输入 B
DNU	–	–	–	–	B2	–	请勿使用
GND	3	3	3	C1	C1	–	地
N.C.	–	–	5	–	–	–	无内部连接
V _{CC}	5	5	6	A2	A2	–	电源引脚
Y	4	4	4	C2	C2	O	输出 Y

5 规格

5.1 绝对最大额定值

在自然通风条件下的工作温度范围内测得（除非另有说明）⁽¹⁾

		最小值	最大值	单位	
V _{CC}	电源电压	-0.5	4.6	V	
V _I	输入电压 ⁽²⁾	-0.5	4.6	V	
V _O	在高阻抗或断电状态对任一输出施加的电压范围 ⁽²⁾	-0.5	4.6	V	
V _O	高电平或低电平状态下的输出电压范围 ⁽²⁾	-0.5	V _{CC} + 0.5	V	
I _{IK}	输入钳位电流	V _I < 0		-50	mA
I _{OK}	输出钳位电流	V _O < 0		-50	mA
I _O	持续输出电流			±20	mA
	通过 V _{CC} 或 GND 的持续电流			±50	mA
T _J	最大结温			150	°C
T _{stg}	贮存温度	-65	150	°C	

(1) 应力超出绝对最大额定值下列出的值可能会对器件造成永久损坏。这些仅为压力额定值，并不表示器件在这些条件下以及在建议运行条件以外的任何其他条件下能够正常运行。长时间处于绝对最大额定条件下可能会影响器件的可靠性。

(2) 如果遵守输入和输出电流额定值，有可能超过输入负电压和输出电压额定值。

5.2 ESD 等级

		值	单位
$V_{(ESD)}$	静电放电		
	人体放电模型 (HBM)，符合 ANSI/ESDA/JEDEC JS-001 标准 ⁽¹⁾	2000	V
	充电器件模型 (CDM)，符合 JEDEC 规范 JESD22-C101 ⁽²⁾	1000	

(1) JEDEC 文档 JEP155 指出：500V HBM 能够在标准 ESD 控制流程下安全生产。

(2) JEDEC 文档 JEP157 指出：250V CDM 能够在标准 ESD 控制流程下安全生产。

5.3 建议运行条件

在自然通风条件下的工作温度范围内测得（除非另有说明）⁽¹⁾

		最小值	最大值	单位
V_{CC}	电源电压	0.8	3.6	V
V_{IH}	高电平输入电压	$V_{CC} = 0.8V$	V_{CC}	V
		$V_{CC} = 1.1V$ 至 $1.95V$	$0.65 \times V_{CC}$	
		$V_{CC} = 2.3V$ 至 $2.7V$	1.6	
		$V_{CC} = 3V$ 至 $3.6V$	2	
V_{IL}	低电平输入电压	$V_{CC} = 0.8V$	0	V
		$V_{CC} = 1.1V$ 至 $1.95V$	$0.35 \times V_{CC}$	
		$V_{CC} = 2.3V$ 至 $2.7V$	0.7	
		$V_{CC} = 3V$ 至 $3.6V$	0.9	
V_I	输入电压	0	3.6	V
V_O	输出电压	0	V_{CC}	V
I_{OH}	高电平输出电流	$V_{CC} = 0.8V$	-20	mA
		$V_{CC} = 1.1V$	-1.1	
		$V_{CC} = 1.4V$	-1.7	
		$V_{CC} = 1.65$	-1.9	
		$V_{CC} = 2.3V$	-3.1	
		$V_{CC} = 3V$	-4	

5.3 建议运行条件（续）

在自然通风条件下的工作温度范围内测得（除非另有说明）⁽¹⁾

		最小值	最大值	单位
I _{OL} 低电平输出电流	V _{CC} = 0.8V		20	μA
	V _{CC} = 1.1V		1.1	mA
	V _{CC} = 1.4V		1.7	
	V _{CC} = 1.65V		1.9	
	V _{CC} = 2.3V		3.1	
	V _{CC} = 3V		4	
Δt/Δv 输入转换上升或下降速率	V _{CC} = 0.8V 至 3.6V		200	ns/V
T _A 自然通风条件下的工作温度范围		-40	85	°C

(1) 器件所有的未使用输入必须保持在 V_{CC} 或 GND 以确保器件正常运行。请参阅 TI 应用报告 [CMOS 输入缓慢变化或悬空的影响](#)，文献编号 [SCBA004](#)。

5.4 热性能信息

热指标 ⁽¹⁾	SN74AUP1G08						单位
	DBV (SOT-23)	DCK (SC70)	DRL (SOT)	DSF (SON)	DRY (SON)	DPW (X2SON)	
	5 引脚	5 引脚	5 引脚	6 引脚	6 引脚	5 引脚	
R _{θJA} 结至环境热阻	298.6	314.4	349.7	407.1	554.9	291.8	°C/W
R _{θJC(top)} 结至外壳（顶部）热阻	240.2	128.7	120.5	232	385.4	224.2	°C/W
R _{θJB} 结至电路板热阻	134.6	100.6	171.4	306.9	388.2	245.8	°C/W
Ψ _{JT} 结至顶部特征参数	114.5	7.1	10.8	40.3	159	245.6	°C/W
Ψ _{JB} 结至电路板特征参数	133.9	99.8	169.4	306	384.1	195.4	°C/W

(1) 有关新旧热指标的更多信息，请参阅 [半导体和 IC 封装热指标](#) 应用报告。

5.5 电气特性

在自然通风条件下的建议运行温度范围内测得 (除非另有说明)

参数	测试条件	V _{CC}	T _A = 25°C			T _A = -40°C 至 +85°C		单位
			最小值	典型值	最大值	最小值	最大值	
V _{OH}	I _{OH} = -20μA	0.8V 至 3.6V	V _{CC} - 0.1			V _{CC} - 0.1		V
	I _{OH} = -1.1mA	1.1V	0.75 × V _{CC}			0.7 × V _{CC}		
	I _{OH} = -1.7mA	1.4V	1.11			1.03		
	I _{OH} = -1.9mA	1.65V	1.32			1.3		
	I _{OH} = -2.3mA	2.3V	2.05			1.97		
	I _{OH} = -3.1mA		1.9			1.85		
	I _{OH} = -2.7mA	3V	2.72			2.67		
	I _{OH} = -4mA		2.6			2.55		
V _{OL}	I _{OL} = 20μA	0.8V 至 3.6V	0.1			0.1		V
	I _{OL} = 1.1mA	1.1V	0.3 × V _{CC}			0.3 × V _{CC}		
	I _{OL} = 1.7mA	1.4V	0.31			0.37		
	I _{OL} = 1.9mA	1.65V	0.31			0.35		
	I _{OL} = 2.3mA	2.3V	0.31			0.33		
	I _{OL} = 3.1mA		0.44			0.45		
	I _{OL} = 2.7mA	3V	0.31			0.33		
	I _{OL} = 4mA		0.44			0.45		
I _I A 或 B 输入	V _I = GND 至 3.6V	0V 至 3.6V	0.1			0.5		μA
I _{off}	V _I 或 V _O = 0V 至 3.6V	0V	0.2			0.6		μA
Δ I _{off}	V _I 或 V _O = 0V 至 3.6V	0V 至 0.2V	0.2			0.6		μA
I _{CC}	V _I = GND 或 (V _{CC} 至 3.6V) I _O = 0	0.8V 至 3.6V	0.5			0.9		μA
Δ I _{CC}	V _I = V _{CC} - 0.6V ⁽¹⁾ I _O = 0	3.3V	40			50		μA
C _i	V _I = V _{CC} 或 GND	0V	1.5					pF
		3.6V	1.5					
C _o	V _O = GND	0V	3					pF

(1) 一个输入电压为 V_{CC} - 0.6V , 另一个输入电压为 V_{CC} 或 GND。

5.6 开关特性 , C_L = 5pF

在自然通风条件下的建议工作温度范围内测得 (除非另有说明) (请参阅图 6-1 和图 6-2)

参数	从 (输入)	至 (输出)	V _{CC}	T _A = 25°C			T _A = -40°C 至 +85°C		单位
				最小值	典型值	最大值	最小值	最大值	
t _{pd}	A 或 B	Y	0.8V	18					ns
			1.2V ± 0.1V	2.6	7.3	12.8	2.1	15.6	
			1.5V ± 0.1V	1.4	5.2	8.7	0.9	10.3	
			1.8V ± 0.15V	1	4.2	6.6	0.5	8.2	
			2.5V ± 0.2V	1	3	4.4	0.5	5.5	
			3.3V ± 0.3V	1	2.4	3.5	0.5	4.3	

5.7 开关特性, $C_L = 10\text{pF}$

在自然通风条件下的建议工作温度范围内测得 (除非另有说明) (请参阅图 6-1 和图 6-2)

参数	从 (输入)	至 (输出)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ 至 $+85^\circ\text{C}$		单位
				最小值	典型值	最大值	最小值	最大值	
t_{pd}	A 或 B	Y	0.8V		21				ns
			$1.2\text{V} \pm 0.1\text{V}$	1.5	8.5	14.7	1	17.2	
			$1.5\text{V} \pm 0.1\text{V}$	1	6.2	10	0.5	11.3	
			$1.8\text{V} \pm 0.15\text{V}$	1	5	7.7	0.5	9	
			$2.5\text{V} \pm 0.2\text{V}$	1	3.6	5.2	0.5	6.1	
			$3.3\text{V} \pm 0.3\text{V}$	1	2.9	4.2	0.5	4.7	

5.8 开关特性, $C_L = 15\text{pF}$

在自然通风条件下的建议工作温度范围内测得 (除非另有说明) (请参阅图 6-1 和图 6-2)

参数	从 (输入)	至 (输出)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ 至 $+85^\circ\text{C}$		单位
				最小值	典型值	最大值	最小值	最大值	
t_{pd}	A 或 B	Y	0.8V		24				ns
			$1.2\text{V} \pm 0.1\text{V}$	3.6	9.9	16.3	3.1	19.9	
			$1.5\text{V} \pm 0.1\text{V}$	2.3	7.2	11.1	1.8	13.2	
			$1.8\text{V} \pm 0.15\text{V}$	1.6	5.8	8.7	1.1	10.6	
			$2.5\text{V} \pm 0.2\text{V}$	1	4.3	5.9	0.5	7.3	
			$3.3\text{V} \pm 0.3\text{V}$	1	3.4	4.8	0.5	5.9	

5.9 开关特性, $C_L = 30\text{pF}$

在自然通风条件下的建议工作温度范围内测得 (除非另有说明) (请参阅图 6-1 和图 6-2)

参数	从 (输入)	至 (输出)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ 至 $+85^\circ\text{C}$		单位
				最小值	典型值	最大值	最小值	最大值	
t_{pd}	A 或 B	Y	0.8V		32.8				ns
			$1.2\text{V} \pm 0.1\text{V}$	4.9	13.1	20.9	4.4	25.5	
			$1.5\text{V} \pm 0.1\text{V}$	3.4	9.5	14.2	2.9	16.9	
			$1.8\text{V} \pm 0.15\text{V}$	2.5	7.7	11	2	13.5	
			$2.5\text{V} \pm 0.2\text{V}$	1.8	5.7	7.6	1.3	9.4	
			$3.3\text{V} \pm 0.3\text{V}$	1.5	4.7	6.2	1	7.5	

5.10 工作特性

$T_A = 25^\circ\text{C}$

参数		测试条件	V_{CC}	典型值	单位
C_{pd}	功率耗散电容	$f = 10\text{ MHz}$	0.8 V	4	pF
			$1.2\text{ V} \pm 0.1\text{ V}$	4	
			$1.5\text{ V} \pm 0.1\text{ V}$	4	
			$1.8\text{ V} \pm 0.15\text{ V}$	4	
			$2.5\text{ V} \pm 0.2\text{ V}$	4.1	
			$3.3\text{ V} \pm 0.3\text{ V}$	4.3	

5.11 典型特性

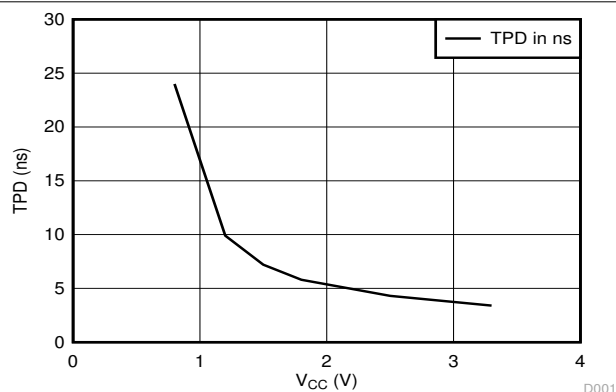


图 5-1. TPD 与 V_{CC} 间的关系 (15pF 负载)

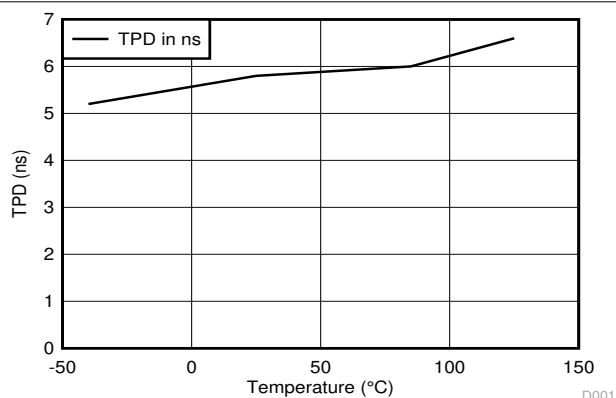
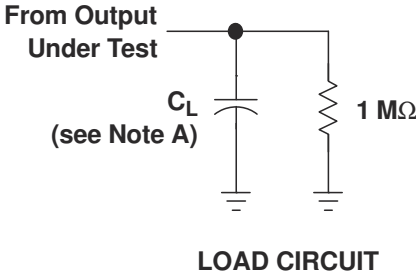


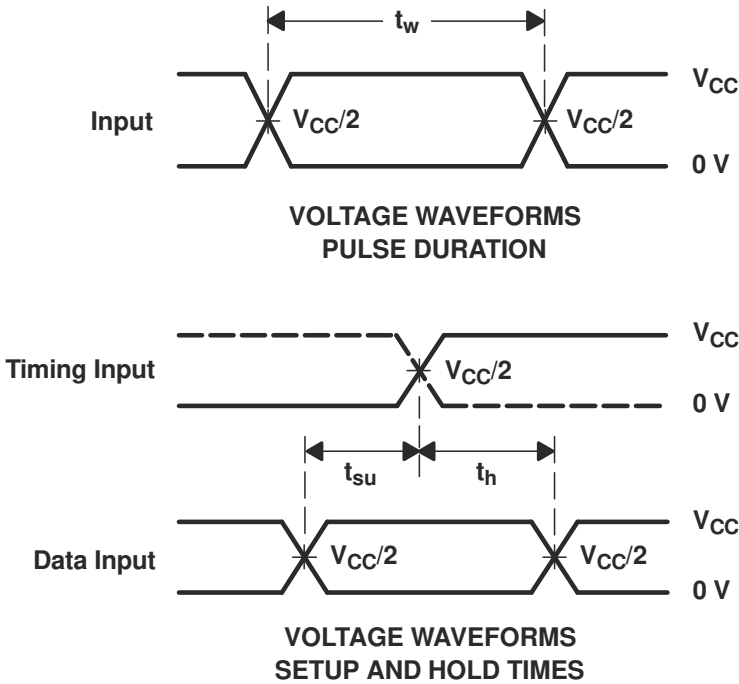
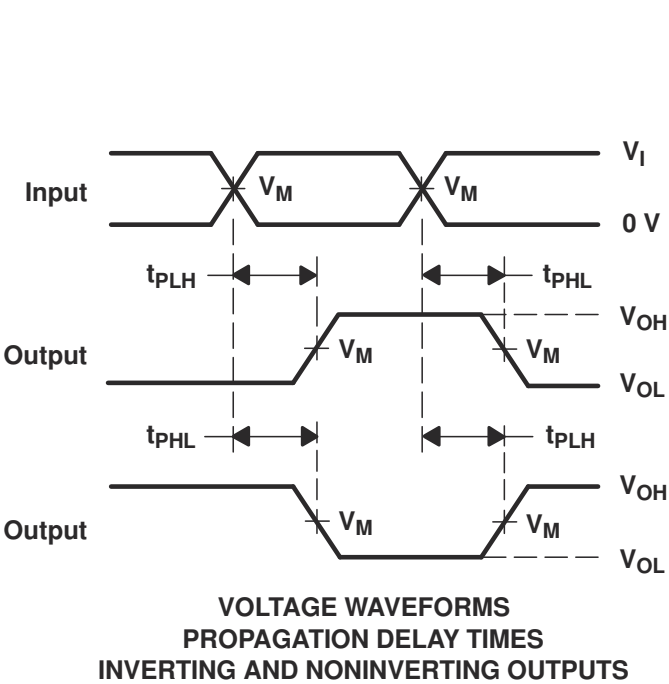
图 5-2. TPD 与温度间的关系 (1.8V、15pF 负载)

6 参数测量信息

6.1 传播延迟、建立和保持时间以及脉冲持续时间



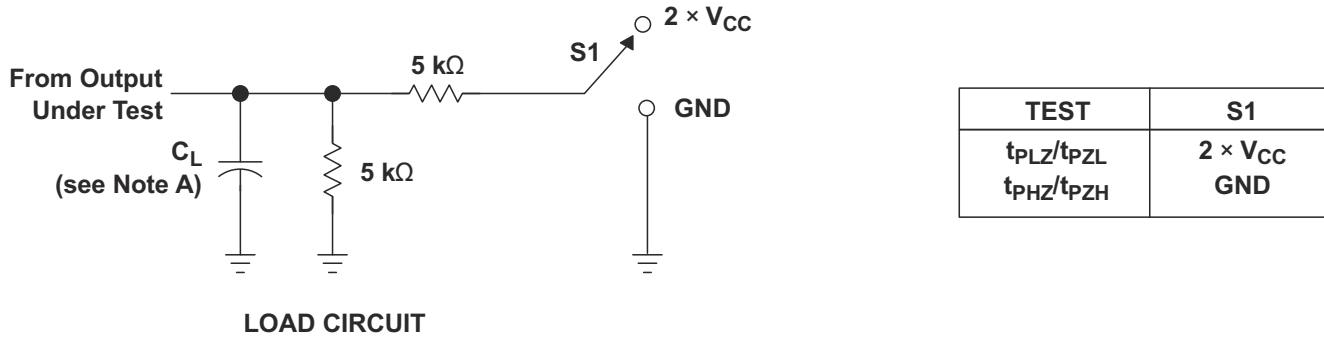
	$V_{CC} = 0.8\text{ V}$	$V_{CC} = 1.2\text{ V}$ $\pm 0.1\text{ V}$	$V_{CC} = 1.5\text{ V}$ $\pm 0.1\text{ V}$	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}



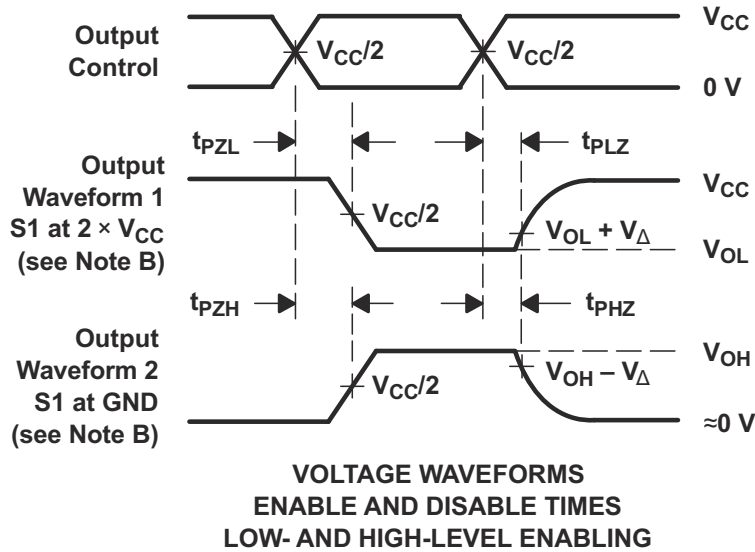
- NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, slew rate $\geq 1\text{ V/ns}$.
C. The outputs are measured one at a time, with one transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd} .
E. All parameters and waveforms are not applicable to all devices.

图 6-1. 负载电路和电压波形

6.2 启用和禁用时间



	$V_{CC} = 0.8\text{ V}$	$V_{CC} = 1.2\text{ V}$ $\pm 0.1\text{ V}$	$V_{CC} = 1.5\text{ V}$ $\pm 0.1\text{ V}$	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_{Δ}	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, slew rate $\geq 1\text{ V/ns}$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. All parameters and waveforms are not applicable to all devices.

图 6-2. 负载电路和电压波形

7 详细说明

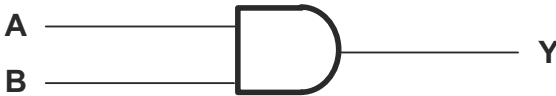
7.1 概述

此单路双输入正与门可在 0.8V 至 3.6V V_{CC} 下运行并以正逻辑执行布尔函数 $Y = A \bullet B$ or $Y = \overline{\overline{A} + \overline{B}}$ 。

AUP 系列器件的静态功耗低于 1 μ A，并采用超小型 DPW 封装。DPW 封装技术是 IC 封装中的一项重大突破。其小巧的 0.64mm² 的封装尺寸较之其他封装选项可显著节省布板空间，同时仍保留了方便制造的 0.5mm 传统引线间距。

该器件完全适合使用 I_{off} 的局部省电应用。 I_{off} 电路可禁用输出，以防在器件上电时电流回流对器件造成损坏。 I_{off} 特性还支持带电插入。

7.2 功能方框图



7.3 特性说明

- 0.8V 至 3.6V 的宽工作 V_{CC} 范围
- 3.6V 耐压 I/O 支持降压转换
- 输入迟滞可在输入端实现缓慢的输入转换和更好的开关噪声抗扰度
- I_{off} 特性允许在 V_{CC} 为 0V 时在输入和输出上产生电压
- 较慢的边沿速率实现低噪声

7.4 器件功能模式

表 7-1. 功能表

输入		输出 Y
A	B	
L	L	L
L	H	L
H	L	L
H	H	H

8 应用和实施

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 应用信息

AUP 系列是 TI 先进的解决方案，可满足电池供电便携式应用的低功耗要求。此系列可确保在 0.8V 至 3.6V 的整个 V_{CC} 范围内实现超低静态和动态功耗，从而延长电池寿命。该产品还可以保持出色的信号完整性。它具有少量内置迟滞，允许慢速或高噪声输入信号。较低的驱动可产生较慢的边沿，并防止在输出端出现过冲和下冲。

AUP 单路逻辑门系列是适用于新型较低电压微处理器（通常由 0.8V 至 1.2V 电压供电）的出色转换器，可以将仍由 3.3V 电压供电的外设驱动器和附件的电压降至新的 μC 功率级。

8.2 典型应用

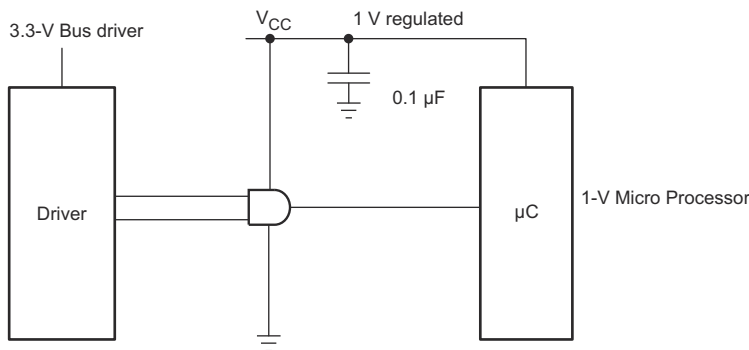


图 8-1. 典型应用原理图

8.2.1 设计要求

SN74AUP1G08 器件采用 CMOS 技术并具有平衡输出驱动。注意避免总线争用，因为它可以驱动超过最大限值的电流。

8.2.2 详细设计过程

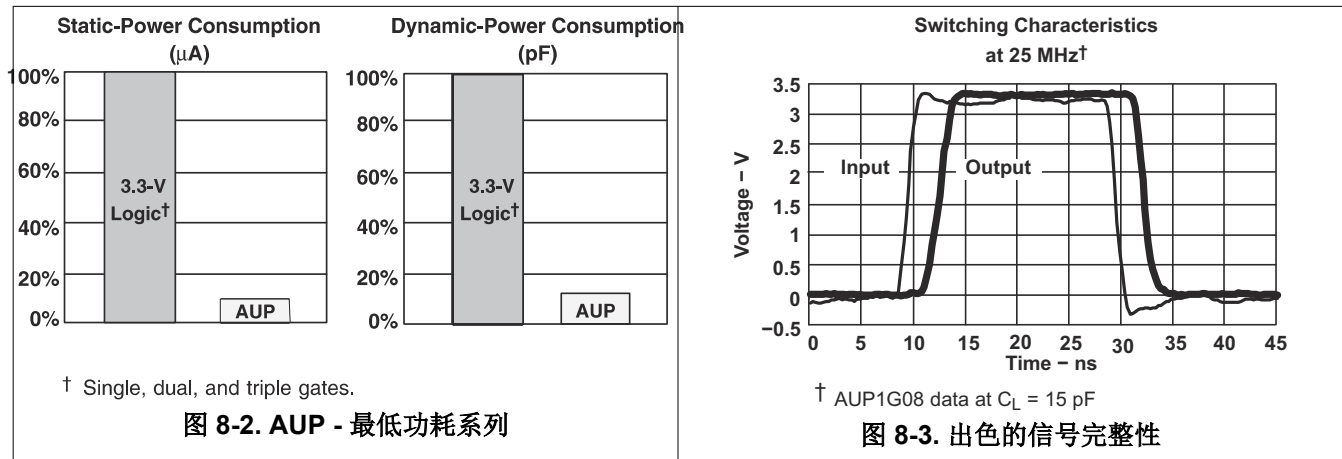
1. 建议的输入条件

- 上升时间和下降时间规格。请参阅 [建议运行条件](#) 表中的 ($\Delta t / \Delta V$)。
- 指定的高电平和低电平。请参阅 [建议工作条件](#) 表中的 (V_{IH} 和 V_{IL})。
- 输入具有过压容限，允许它们在任何有效 V_{CC} 下高达 3.6V

2. 建议的输出条件

- 输出端的负载电流不应超过 20mA，该器件的总电流不应超过 50mA。
- 输出不应被拉至高于 V_{CC}

8.2.3 应用曲线



9 电源相关建议

电源可以是 [建议运行条件](#) 表中最小和最大电源电压额定值之间的任何电压。

每个 V_{CC} 端子均应具有一个良好的旁路电容器，以防止功率干扰。对于单电源器件，建议使用 $0.1 \mu\text{F}$ ；如果有多个 V_{CC} 端子，则建议为每个电源端子使用 $0.01 \mu\text{F}$ 或 $0.022 \mu\text{F}$ 。可以并联多个旁路电容器以抑制不同的噪声频率。 $0.1 \mu\text{F}$ 和 $1 \mu\text{F}$ 通常并联使用。为了获得最佳效果，旁路电容器必须尽可能靠近电源端子安装。

10 布局

10.1 布局指南

当使用多位逻辑器件时，输入决不能悬空。

在许多情况下，数字逻辑器件的功能或部分功能未被使用（例如，当仅使用三输入与门的两个输入或仅使用 4 个缓冲门中的 3 个时）。此类输入引脚不应悬空，因为外部连接处的未定义电压会导致未定义的操作状态。[图 10-1](#) 指定了在所有情况下都必须遵守的规则。数字逻辑器件的所有未使用输入必须连接至一个高或低偏置以防止悬空。应为任何特定未使用输入应用的逻辑电平取决于器件的功能。通常，它们将连接到 GND 或 V_{CC} ，具体取决于哪种更合理或更方便。使输出悬空通常是可以接受的，除非该器件是收发器。如果该收发器有一个输出使能引脚，它会在置为有效时禁用该器件的输出部分。这不会禁用 I/O 的输入部分，因此输入在禁用后也无法悬空。

10.2 布局示例

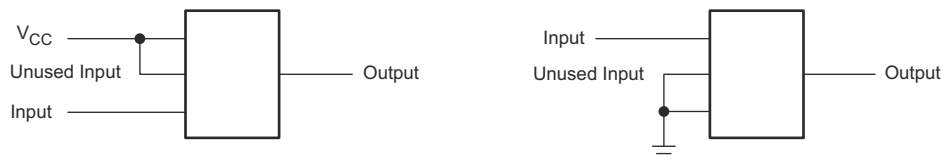


图 10-1. 布局图

11 器件和文档支持

11.1 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的[使用条款](#)。

11.3 商标

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

11.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.5 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。

12 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision P (June 2016) to Revision Q (March 2024)	Page
• 通篇更新了表格、图和交叉参考的编号格式.....	1

Changes from Revision O (June 2014) to Revision P (June 2016)	Page
• 更新了 <i>应用</i> 和 <i>器件信息</i> 表.....	1
• 更新了引脚排列图和 <i>引脚功能</i> 表.....	3
• 在 <i>绝对最大额定值</i> 中添加了贮存温度、 T_{stg} 和结温 T_J 的温度范围.....	5
• 将 <i>处理额定值</i> 更改为 ESD 等级，并将“最小值、最大值”列更改为“值”列.....	5

Changes from Revision N (November 2012) to Revision O (June 2014)	Page
• 将文档更新为新的 TI 数据表格式.....	1
• 删除了订购信息.....	1
• 添加了“应用”.....	1
• 更正了 YFP 封装图中的拼写错误.....	3
• 添加了 <i>处理额定值</i> 表.....	5
• 新增了“热性能信息”表。.....	6
• 添加了“典型特性”.....	9

Changes from Revision M (September 2012) to Revision N (November 2012)	Page
---	-------------

- 更改了 DPW 封装引脚排列.....[3](#)
-

Changes from Revision K (October 2011) to Revision L (May 2012)	Page
--	-------------

- 修订了文档，以解决封装附录问题.....[1](#)
-

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是所指定器件的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AUP1G08DBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN NIPDAU	Level-1-260C-UNLIM	-40 to 85	(H08F, H08R)
SN74AUP1G08DBVT	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU SN NIPDAU	Level-1-260C-UNLIM	-40 to 85	(H08F, H08R)
SN74AUP1G08DCKR	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU SN NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HE5, HEF, HEK, HE R) (HEH, HEP, HES)
SN74AUP1G08DCKRE4	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HE5, HEF, HEK, HE R) (HEH, HEP, HES)
SN74AUP1G08DCKT	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HE5, HER)
SN74AUP1G08DPWR	Active	Production	X2SON (DPW) 5	3000 LARGE T&R	Yes	NIPDAU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(E, E4)
SN74AUP1G08DRLR	Active	Production	SOT-5X3 (DRL) 5	4000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(HE7, HER)
SN74AUP1G08DRY2	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HE
SN74AUP1G08DRYR	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	HE
SN74AUP1G08DSF2	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU NIPDAUAG NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HE, HER) HEH
SN74AUP1G08DSFR	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU NIPDAUAG NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HE, HER) HEH
SN74AUP1G08YFPR	Active	Production	DSBGA (YFP) 6	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-	HEN
SN74AUP1G08YZPR	Active	Production	DSBGA (YZP) 5	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HEN

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

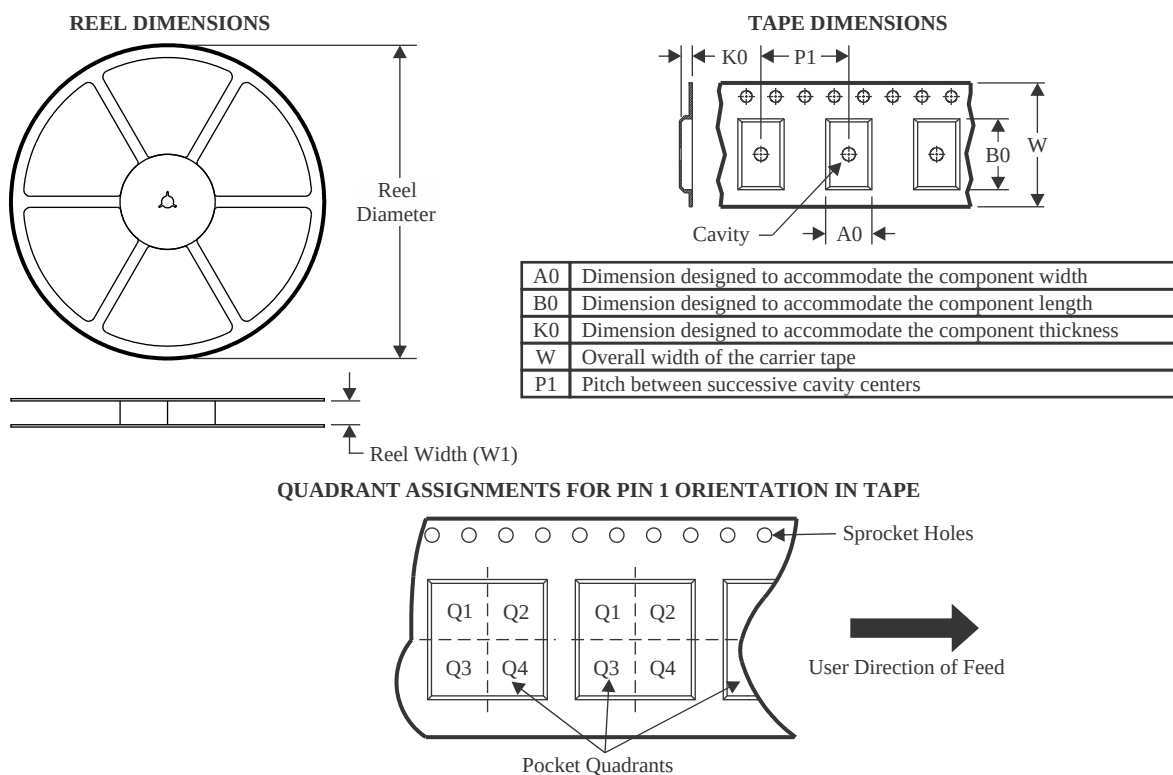
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AUP1G08 :

- Automotive : [SN74AUP1G08-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

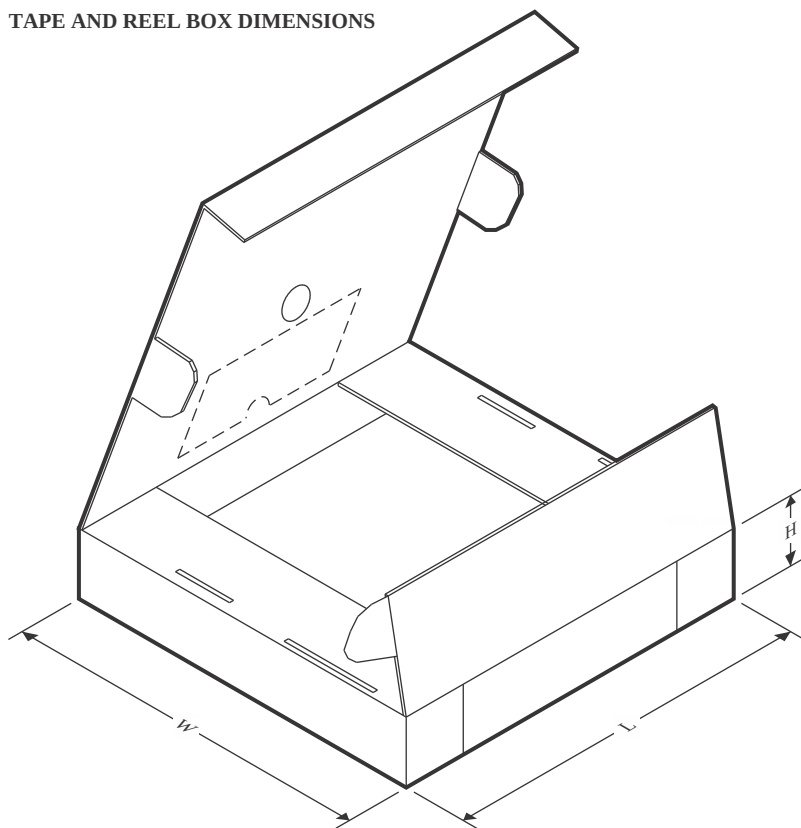
TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1G08DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AUP1G08DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AUP1G08DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AUP1G08DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AUP1G08DCKR	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74AUP1G08DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
SN74AUP1G08DCKRE4	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G08DCKT	SC70	DCK	5	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74AUP1G08DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G08DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q3
SN74AUP1G08DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74AUP1G08DRY2	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q3
SN74AUP1G08DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74AUP1G08DRYR	SON	DRY	6	5000	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
SN74AUP1G08DSF2	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q3
SN74AUP1G08DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1G08YFPR	DSBGA	YFP	6	3000	178.0	9.2	0.89	1.29	0.62	4.0	8.0	Q1
SN74AUP1G08YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

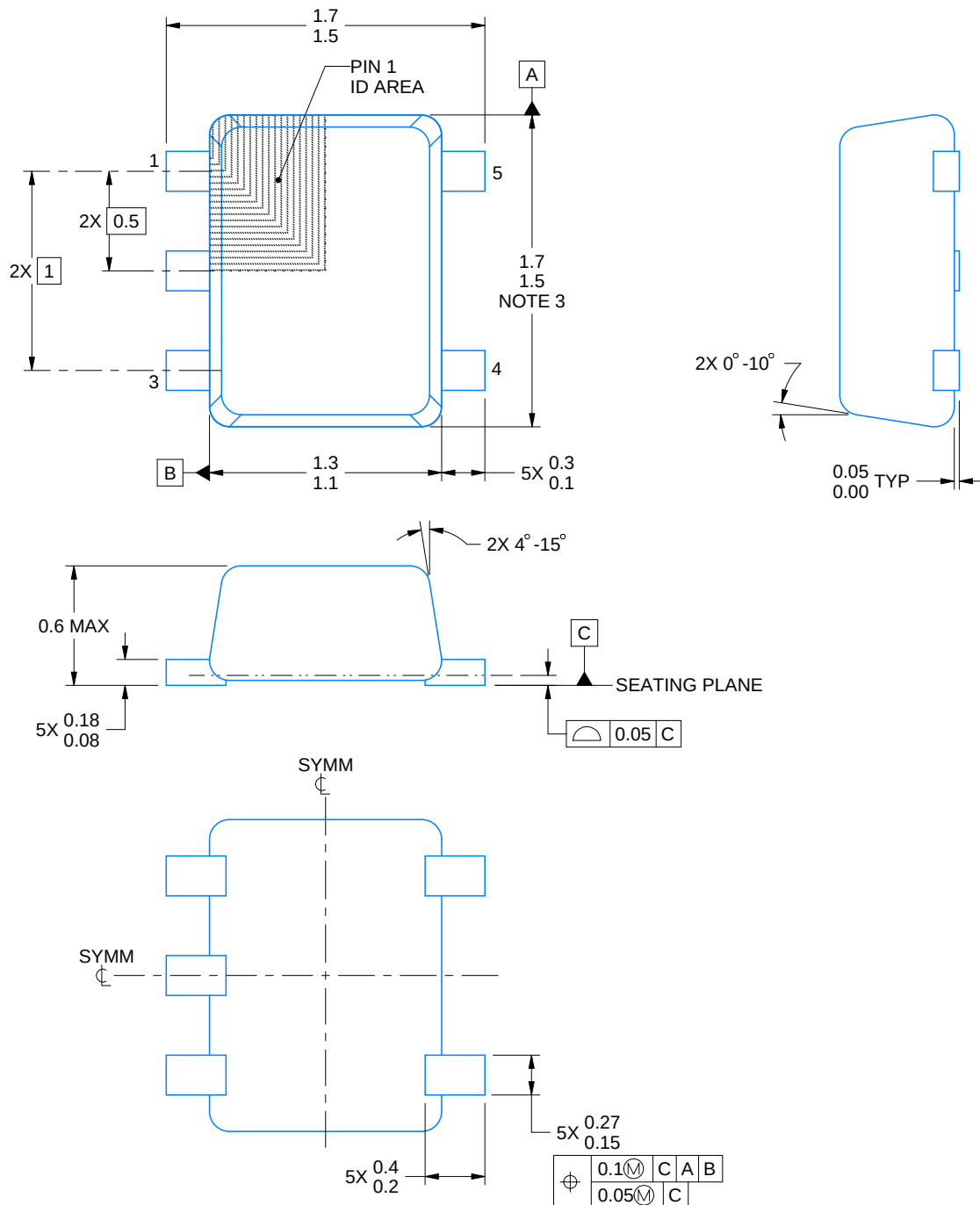
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1G08DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74AUP1G08DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74AUP1G08DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
SN74AUP1G08DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
SN74AUP1G08DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
SN74AUP1G08DCKR	SC70	DCK	5	3000	210.0	185.0	35.0
SN74AUP1G08DCKRE4	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AUP1G08DCKT	SC70	DCK	5	250	202.0	201.0	28.0
SN74AUP1G08DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74AUP1G08DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
SN74AUP1G08DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0
SN74AUP1G08DRY2	SON	DRY	6	5000	184.0	184.0	19.0
SN74AUP1G08DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74AUP1G08DRYR	SON	DRY	6	5000	202.0	201.0	28.0
SN74AUP1G08DSF2	SON	DSF	6	5000	210.0	185.0	35.0
SN74AUP1G08DSFR	SON	DSF	6	5000	210.0	185.0	35.0
SN74AUP1G08YFPR	DSBGA	YFP	6	3000	220.0	220.0	35.0
SN74AUP1G08YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0

DRL0005A

PACKAGE OUTLINE

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



4220753/E 11/2024

NOTES:

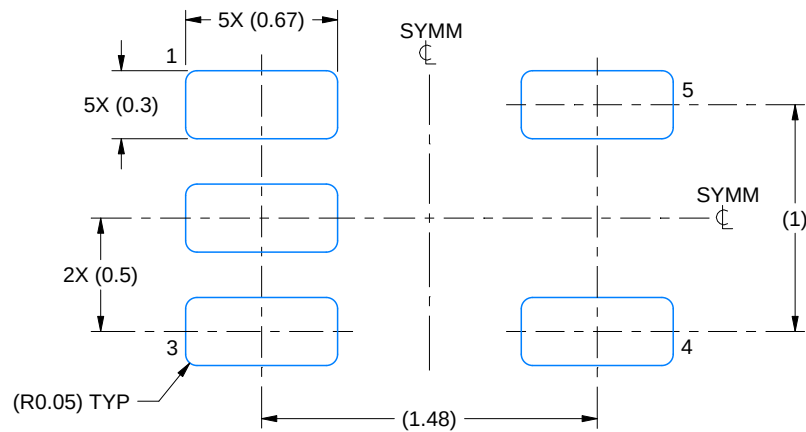
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1

EXAMPLE BOARD LAYOUT

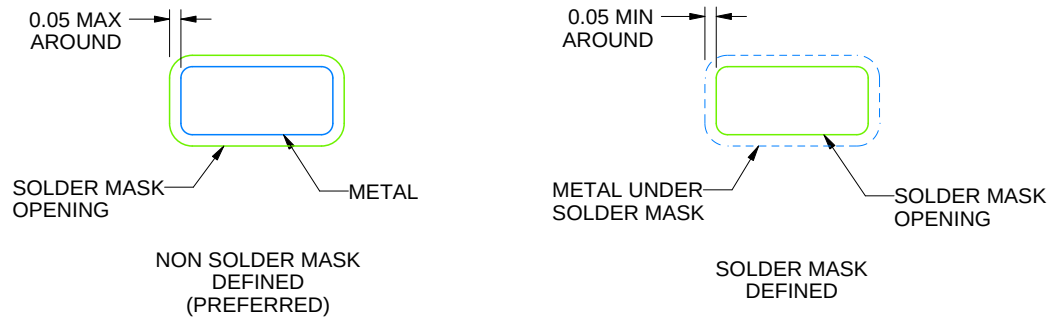
DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4220753/E 11/2024

NOTES: (continued)

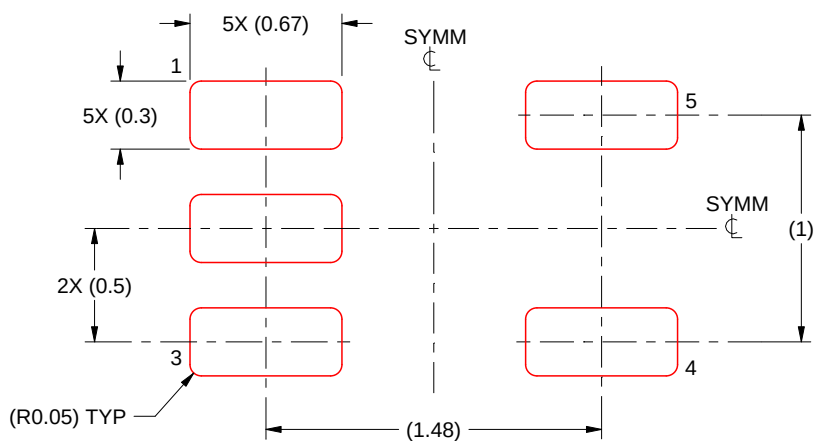
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/E 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DPW 5

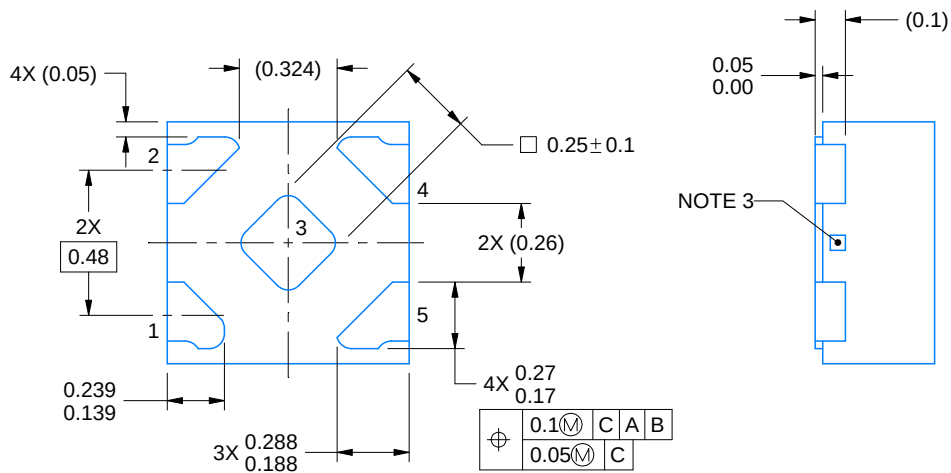
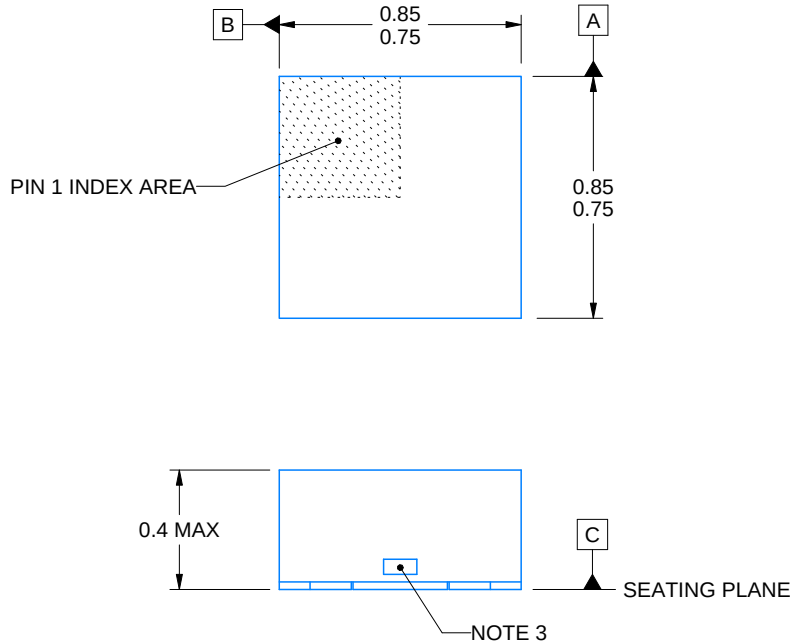
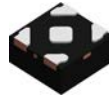
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4211218-3/D



4223102/D 03/2022

NOTES:

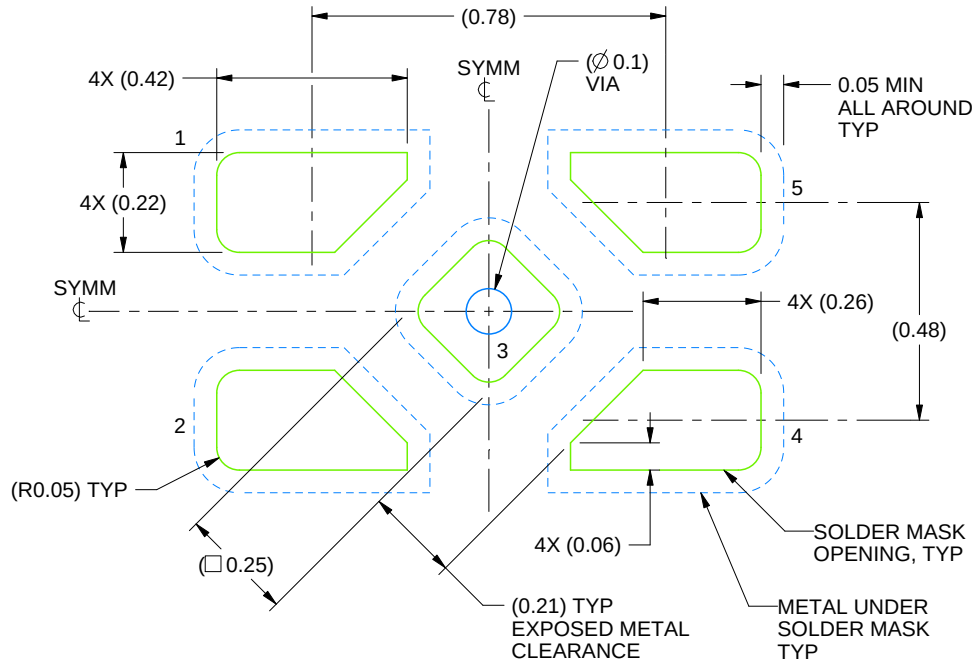
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

EXAMPLE BOARD LAYOUT

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/D 03/2022

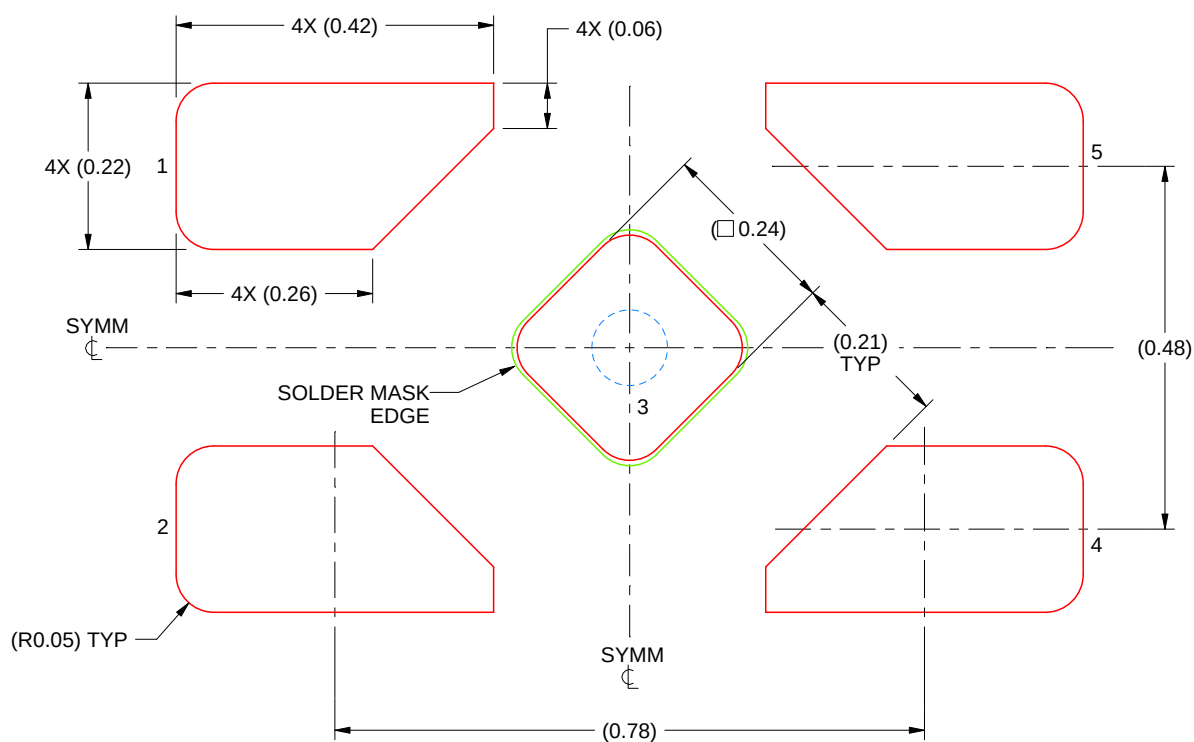
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/sluea271).

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



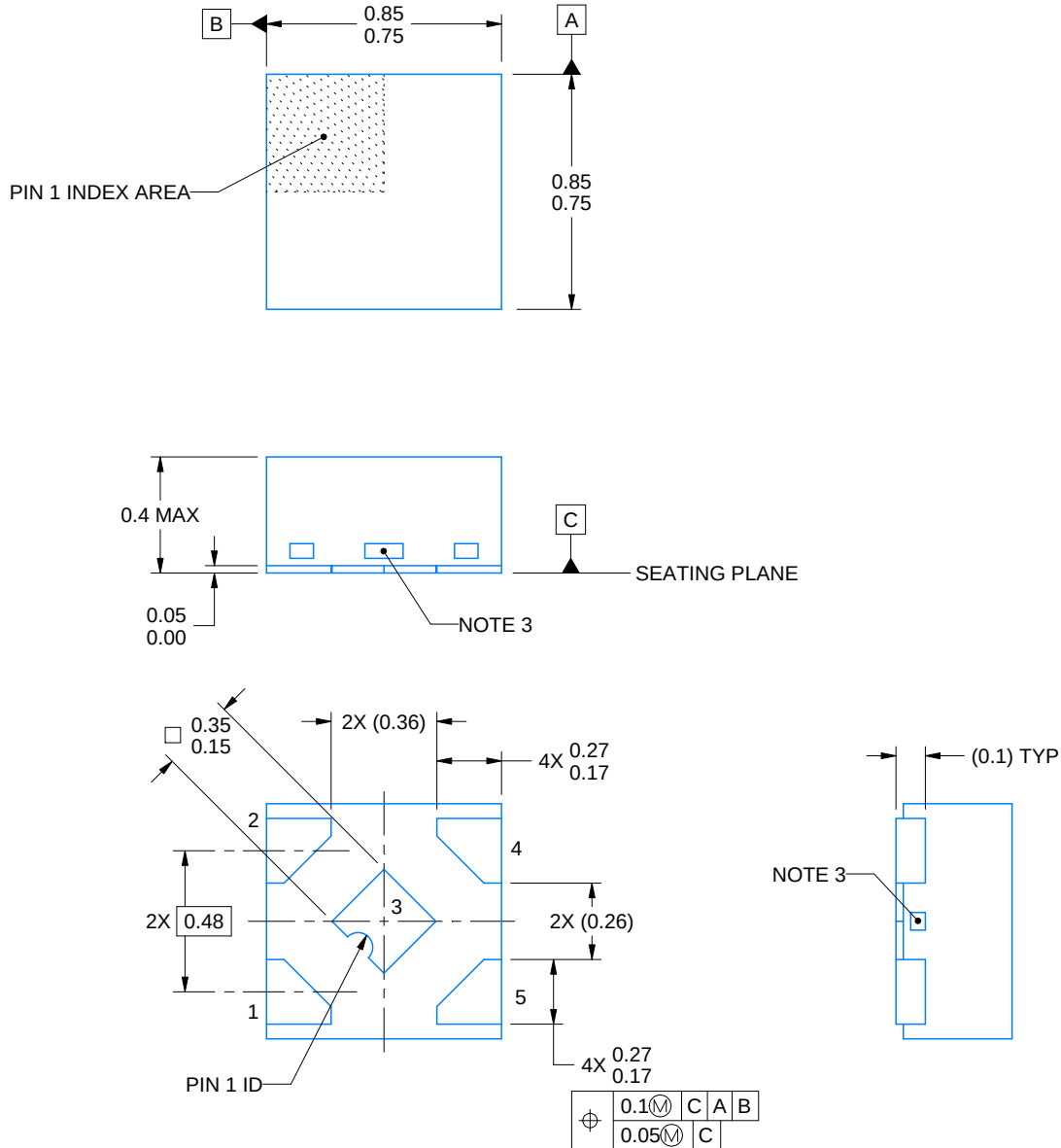
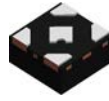
SOLDER PASTE EXAMPLE BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

4223102/D 03/2022

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



4228233/D 09/2023

NOTES:

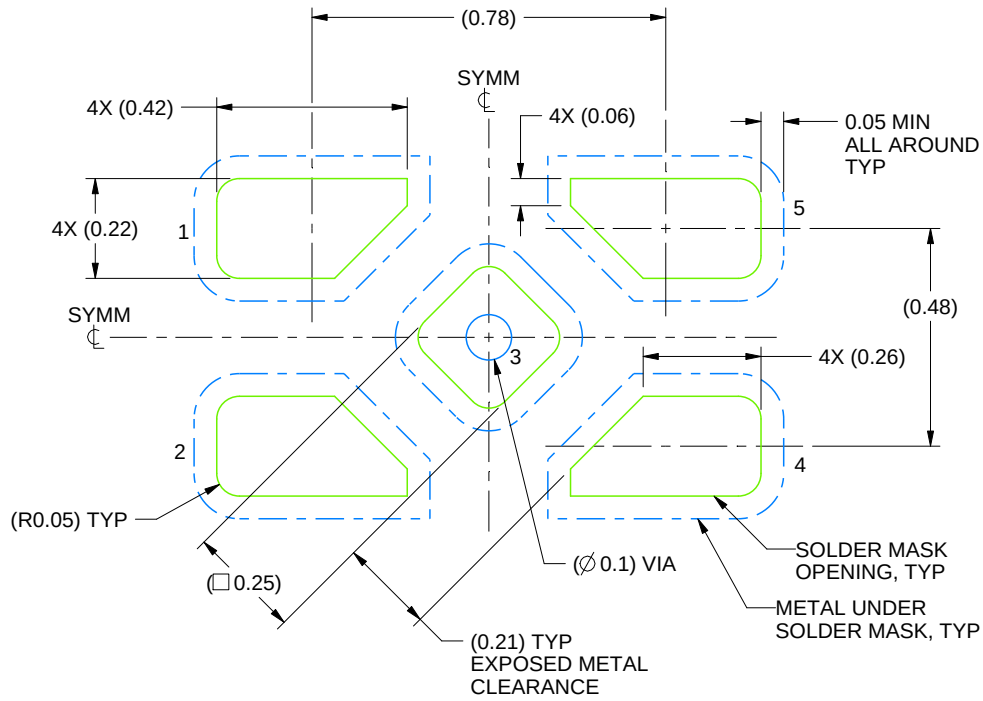
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

EXAMPLE BOARD LAYOUT

DPW0005B

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4228233/D 09/2023

NOTES: (continued)

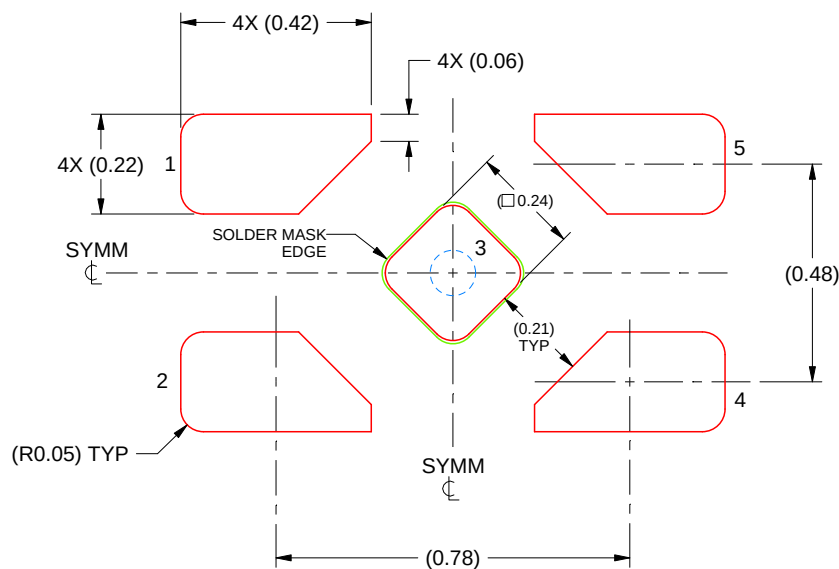
4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/sluea271).

EXAMPLE STENCIL DESIGN

DPW0005B

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 5
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:60X

4228233/D 09/2023

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

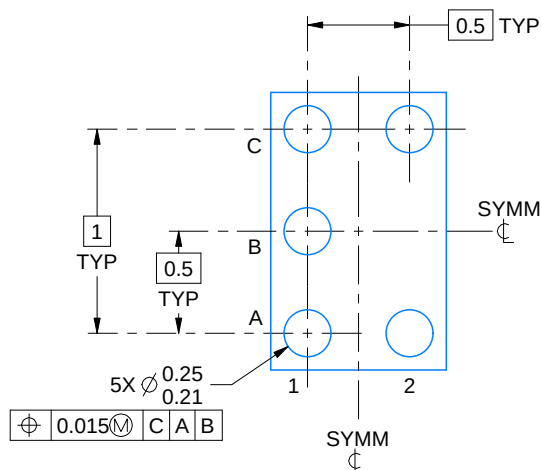
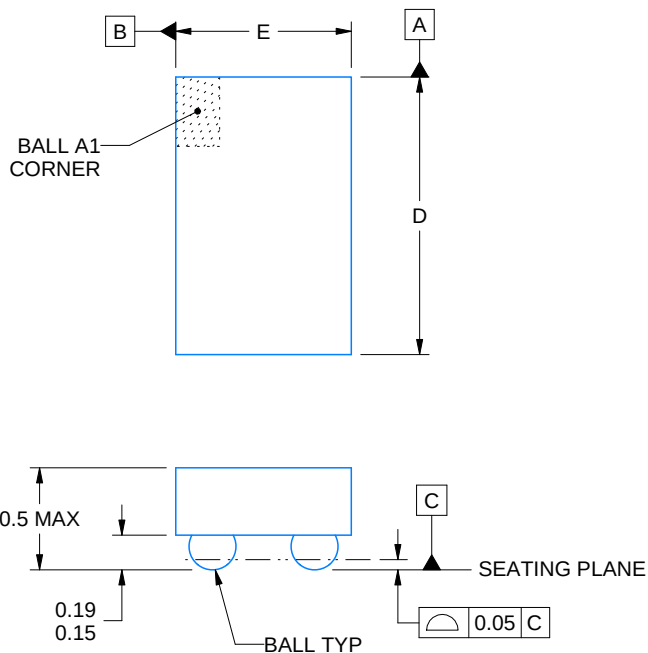
YZP0005



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.418 mm, Min = 1.358 mm
E: Max = 0.918 mm, Min = 0.858 mm

4219492/A 05/2017

NOTES:

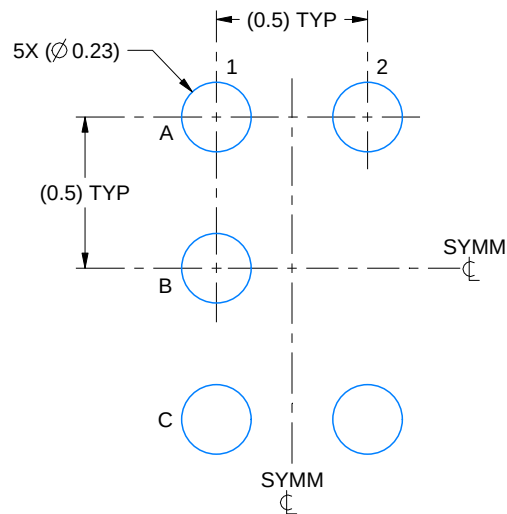
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

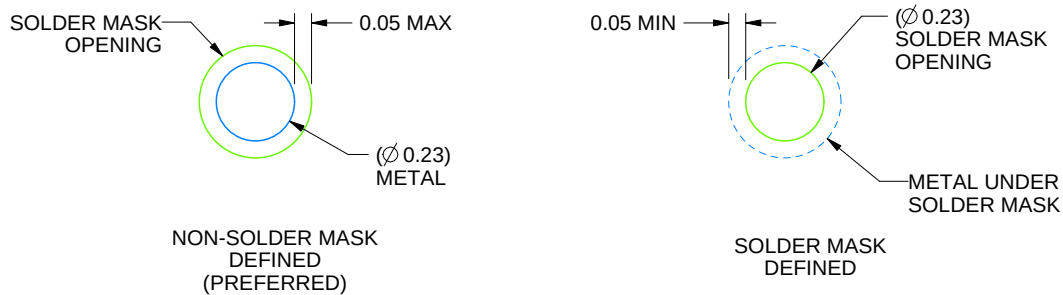
YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

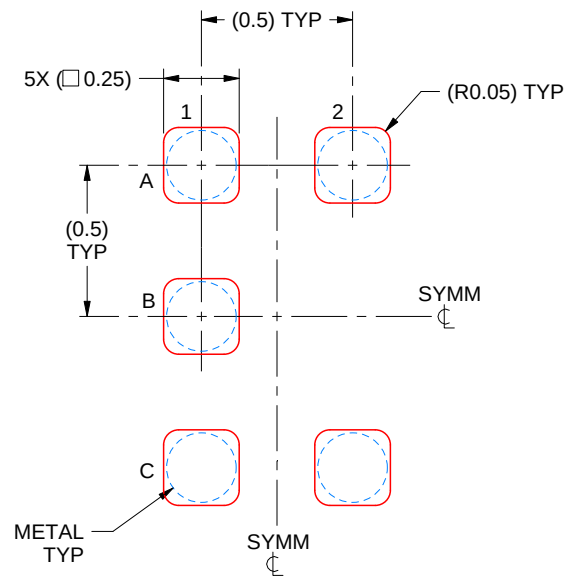
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219492/A 05/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

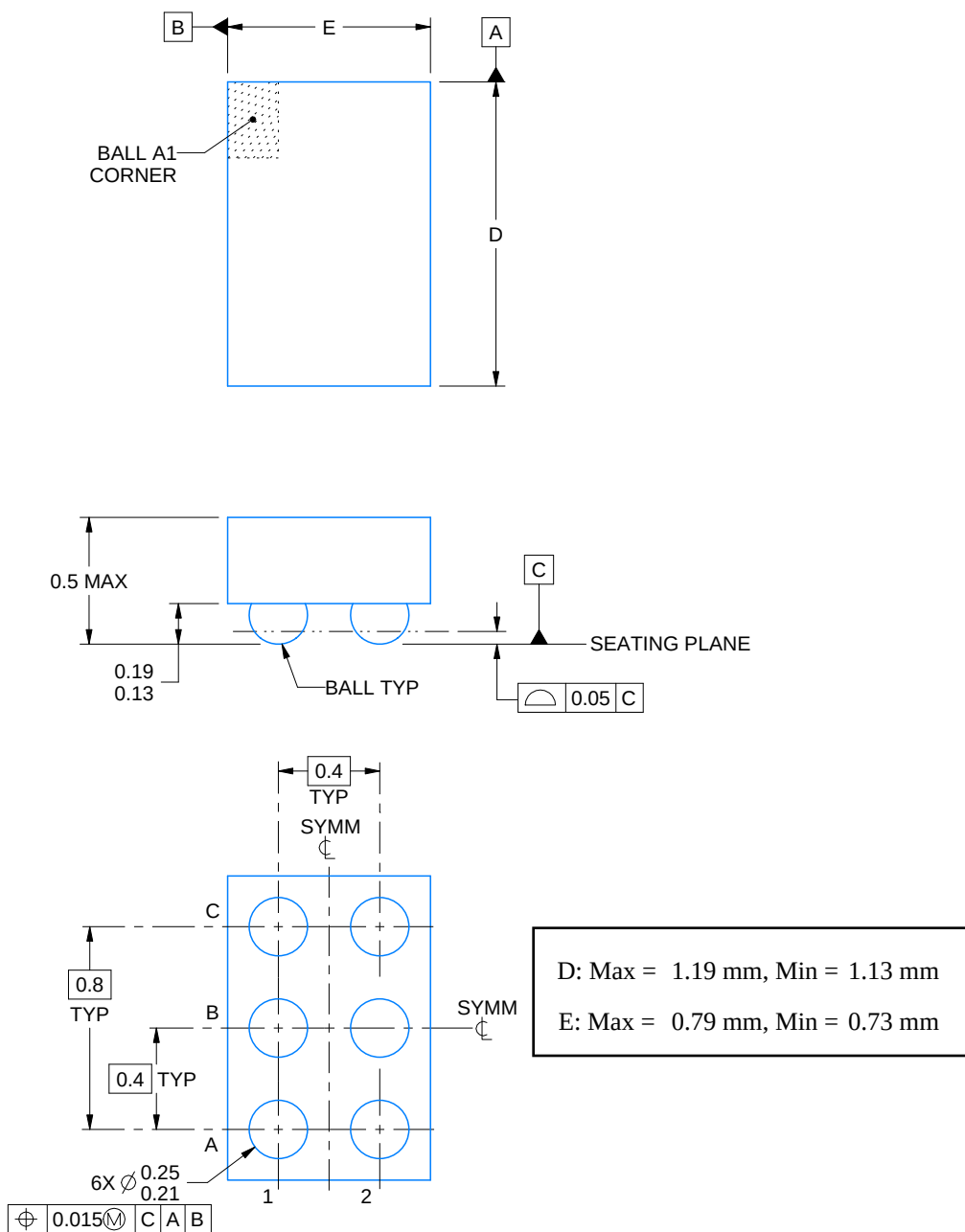
YFP0006



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4223410/A 11/2016

NOTES:

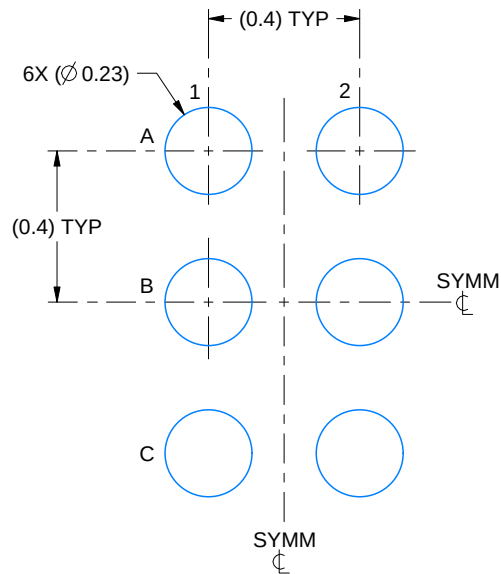
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

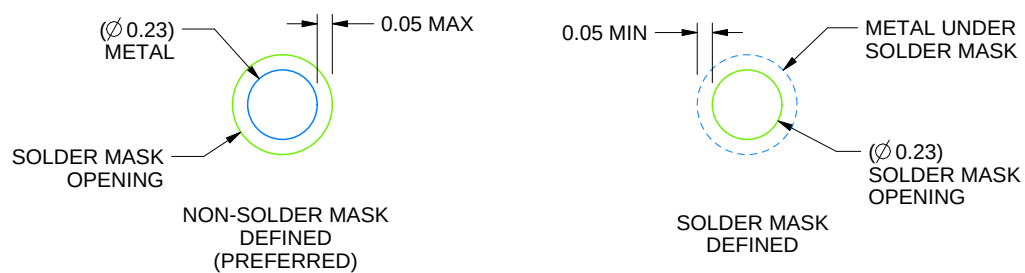
YFP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:50X



SOLDER MASK DETAILS
NOT TO SCALE

4223410/A 11/2016

NOTES: (continued)

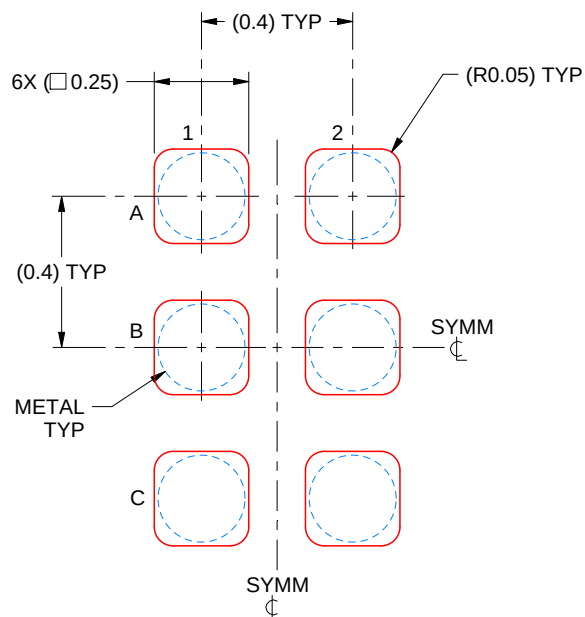
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY

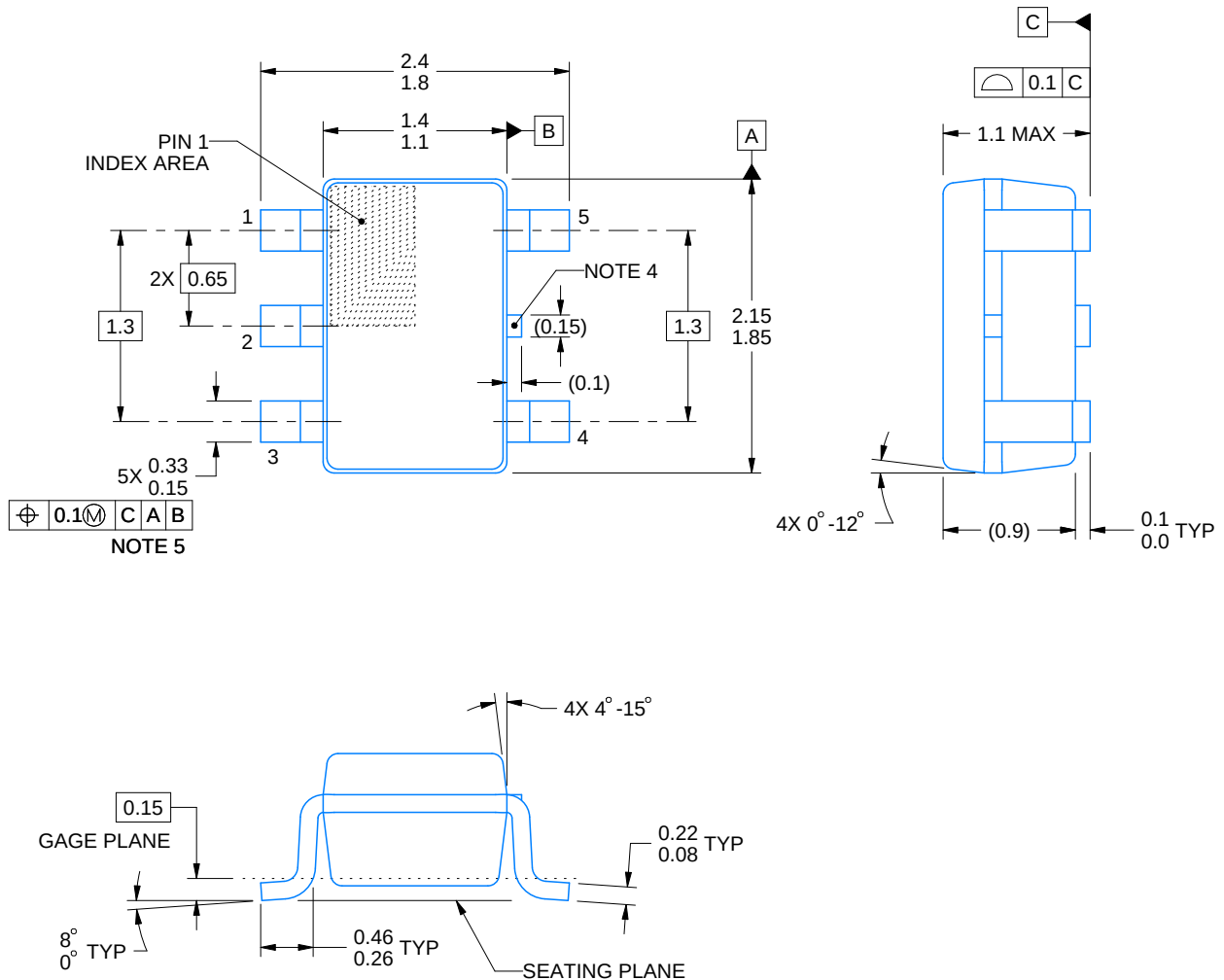


SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4223410/A 11/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



4214834/G 11/2024

NOTES:

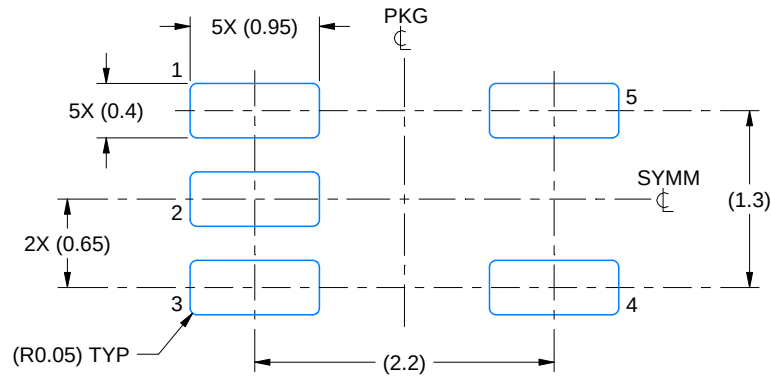
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

EXAMPLE BOARD LAYOUT

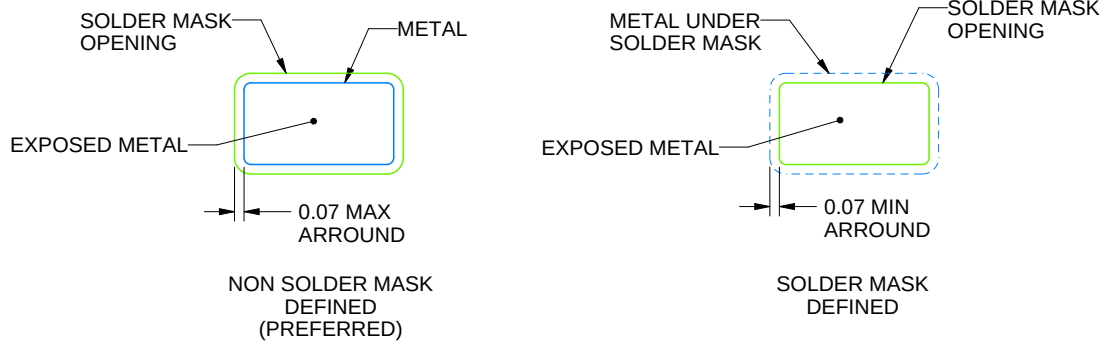
DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

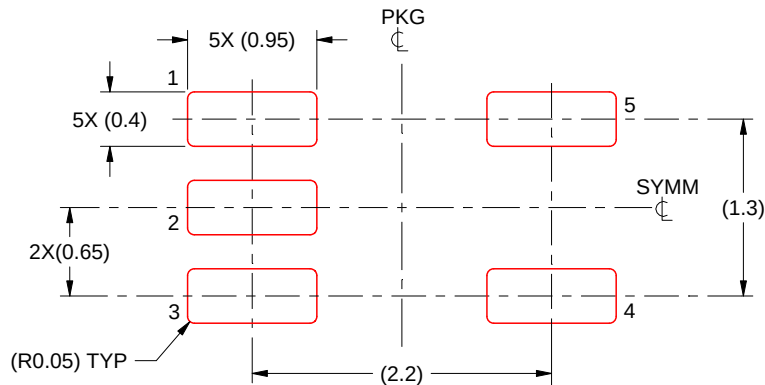


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 THICK STENCIL
 SCALE:18X

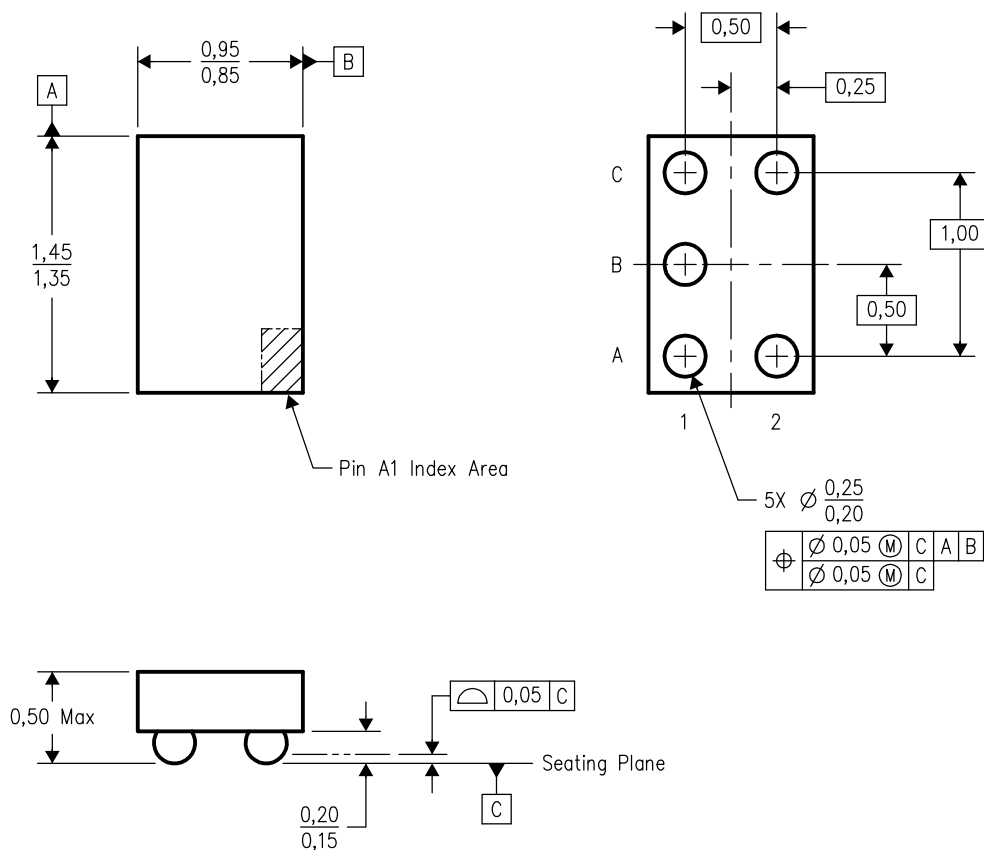
4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

YEP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



4204725-2/A 10/2002

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoStar™ package configuration.
 - D. This package is tin-lead (SnPb). Refer to the 5 YZP package (drawing 4204741) for lead-free.

NanoStar is a trademark of Texas Instruments.



SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



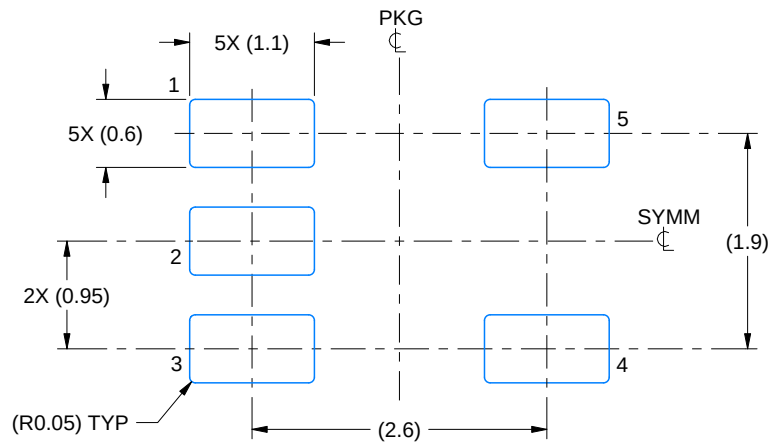
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

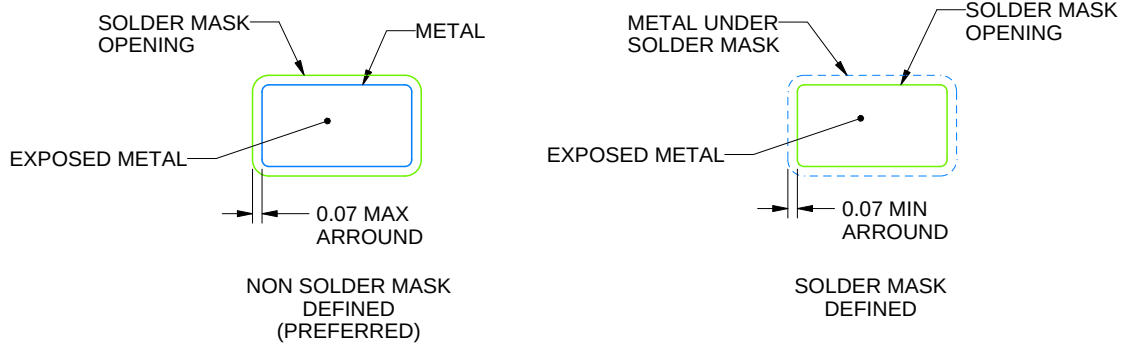
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

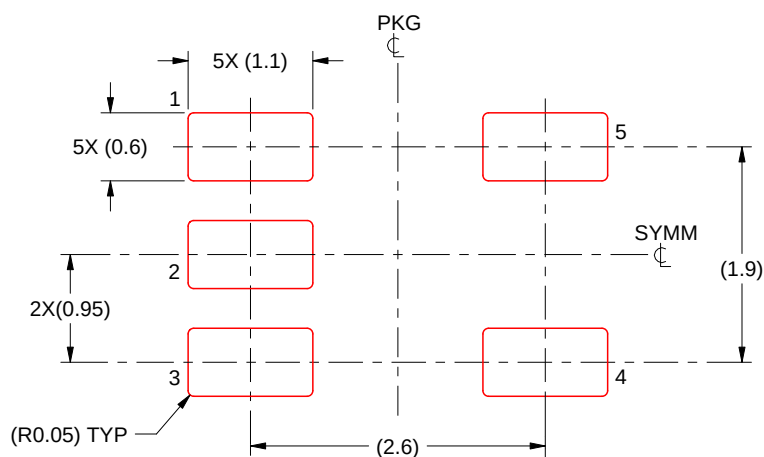
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DRY 6

USON - 0.6 mm max height

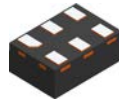
PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4207181/G

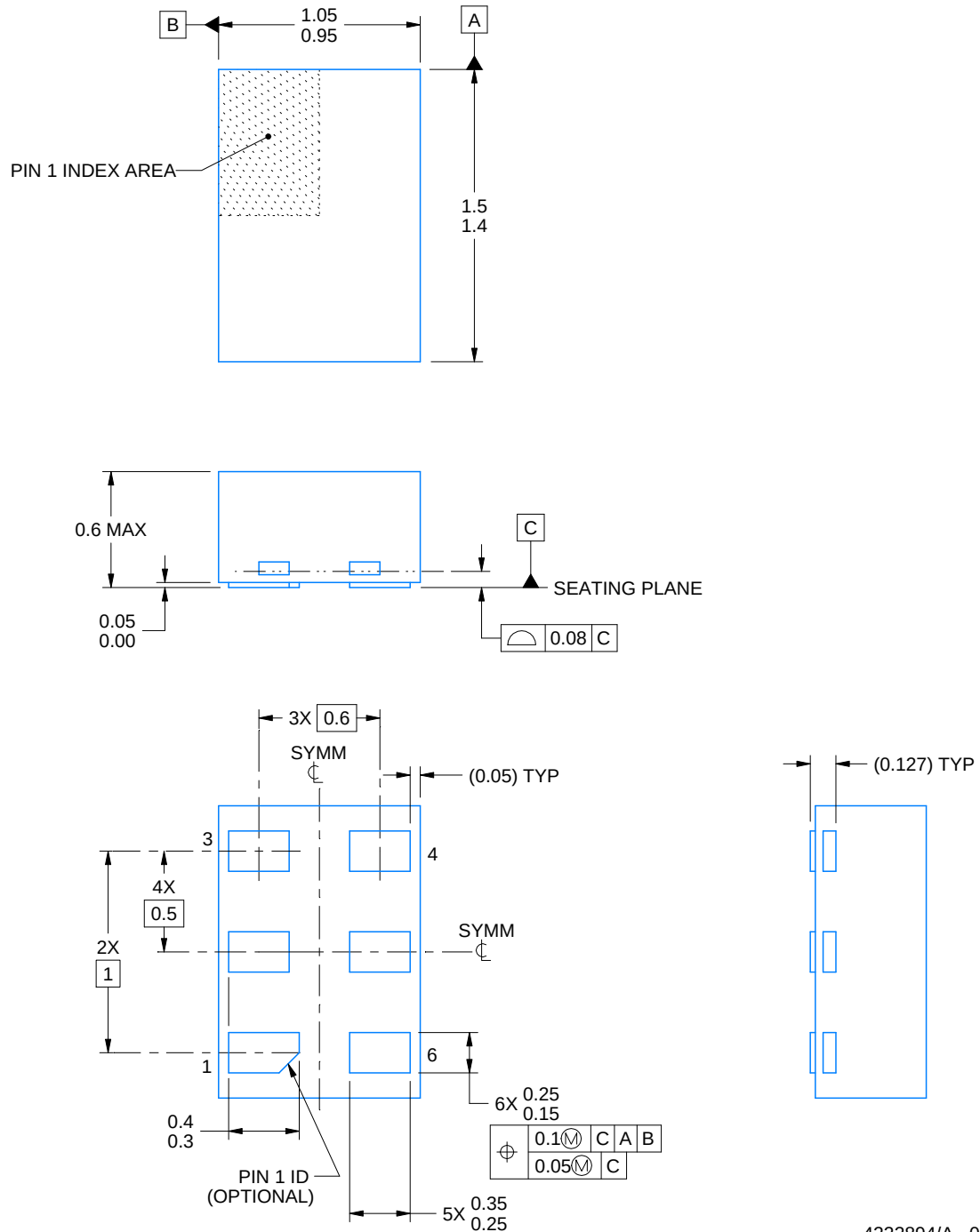
DRY0006A



PACKAGE OUTLINE

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4222894/A 01/2018

NOTES:

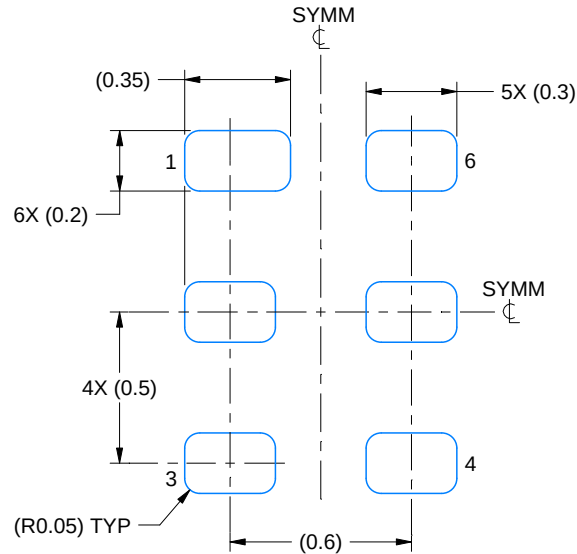
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

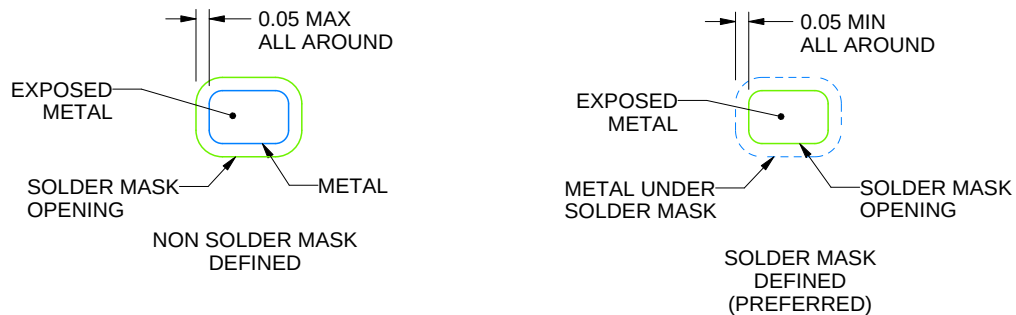
DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

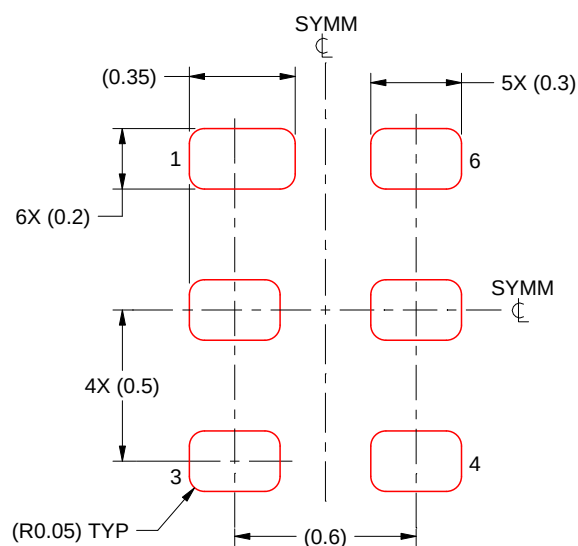
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/sluea271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

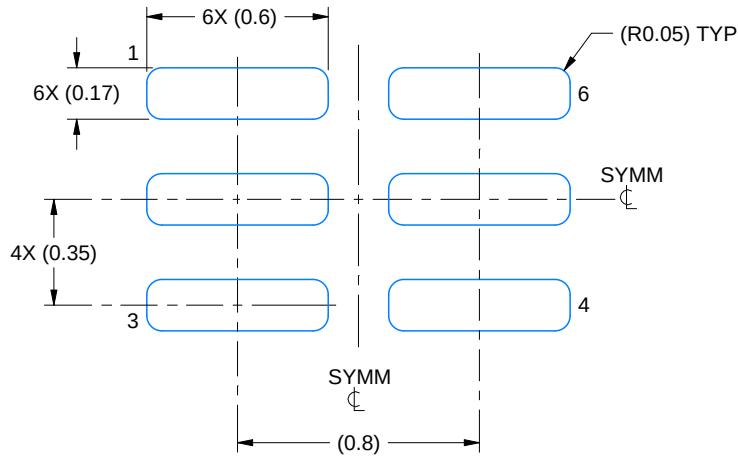
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

EXAMPLE BOARD LAYOUT

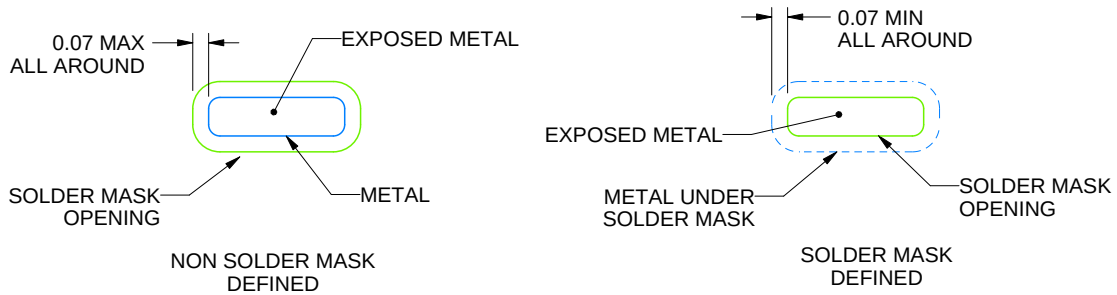
DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

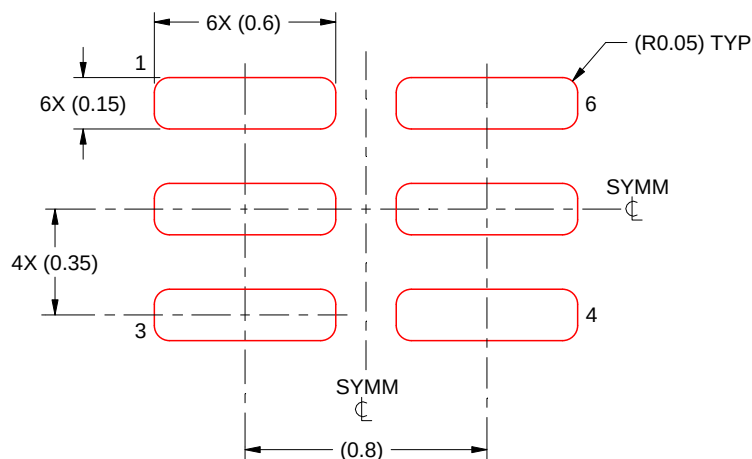
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).

EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/B 06/2022

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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