

The SN54125, SN54126, SN74125, SN74126, and SN54LS126A are obsolete and are no longer supplied.

SN54125, SN54126, SN54LS125A, SN54LS126A, SN74125, SN74126, SN74LS125A, SN74LS126A QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

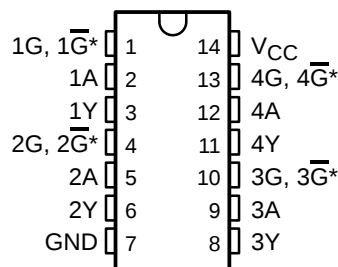
SDLS044A – DECEMBER 1983 – REVISED MARCH 2002

- Quad Bus Buffers
- 3-State Outputs
- Separate Control for Each Channel

description

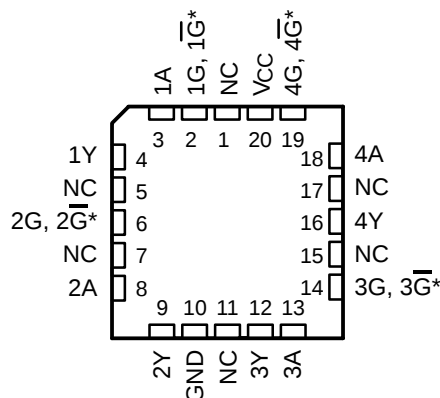
These bus buffers feature three-state outputs that, when enabled, have the low impedance characteristics of a TTL output with additional drive capability at high logic levels to permit driving heavily loaded bus lines without external pullup resistors. When disabled, both output transistors are turned off, presenting a high-impedance state to the bus so the output will act neither as a significant load nor as a driver. The '125 and 'LS125A devices' outputs are disabled when $\bar{G}$ is high. The '126 and 'LS126A devices' outputs are disabled when G is low.

SN54125, SN54126, SN54LS125A,
SN54LS126A . . . J OR W PACKAGE
SN74125, SN74126 . . . N PACKAGE
SN74LS125A, SN74LS126A . . . D, N, OR NS PACKAGE
(TOP VIEW)



* $\bar{G}$ on '125 and 'LS125A devices;
G on 126 and 'LS126A devices

SN54LS125A, SN54LS126A . . . FK PACKAGE
(TOP VIEW)



* $\bar{G}$ on '125 and 'LS125A devices;
G on 126 and 'LS126A devices
NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54125, SN54126, SN54LS125A, SN54LS126A,
 SN74125, SN74126, SN74LS125A, SN74LS126A
QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

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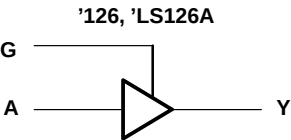
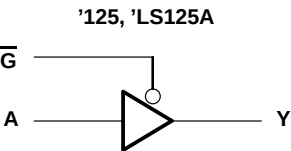
The SN54125, SN54126, SN74125, SN74126, and SN54LS126A are obsolete and are no longer supplied.

ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74LS125AN	SN74LS125AN
		Tube	SN74LS126AN	SN74LS126AN
	SOIC – D	Tube	SN74LS125AD	LS125A
		Tape and reel	SN74LS125ADR	
		Tube	SN74LS126AD	LS126A
		Tape and reel	SN74LS126ADR	
	SOP – NS	Tape and reel	SN74LS125ANSR	74LS125A
		Tape and reel	SN74LS126ANSR	74LS126A
–55°C to 125°C	CDIP – J	Tube	SN54LS125AJ	SN54LS125AJ
		Tube	SNJ54LS125AJ	SNJ54LS125AJ
	CFP – W	Tube	SNJ54LS125AW	SNJ54LS125AW
	LCCC – FK	Tube	SNJ54LS125AFK	SNJ54LS125AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

logic diagram (each gate)

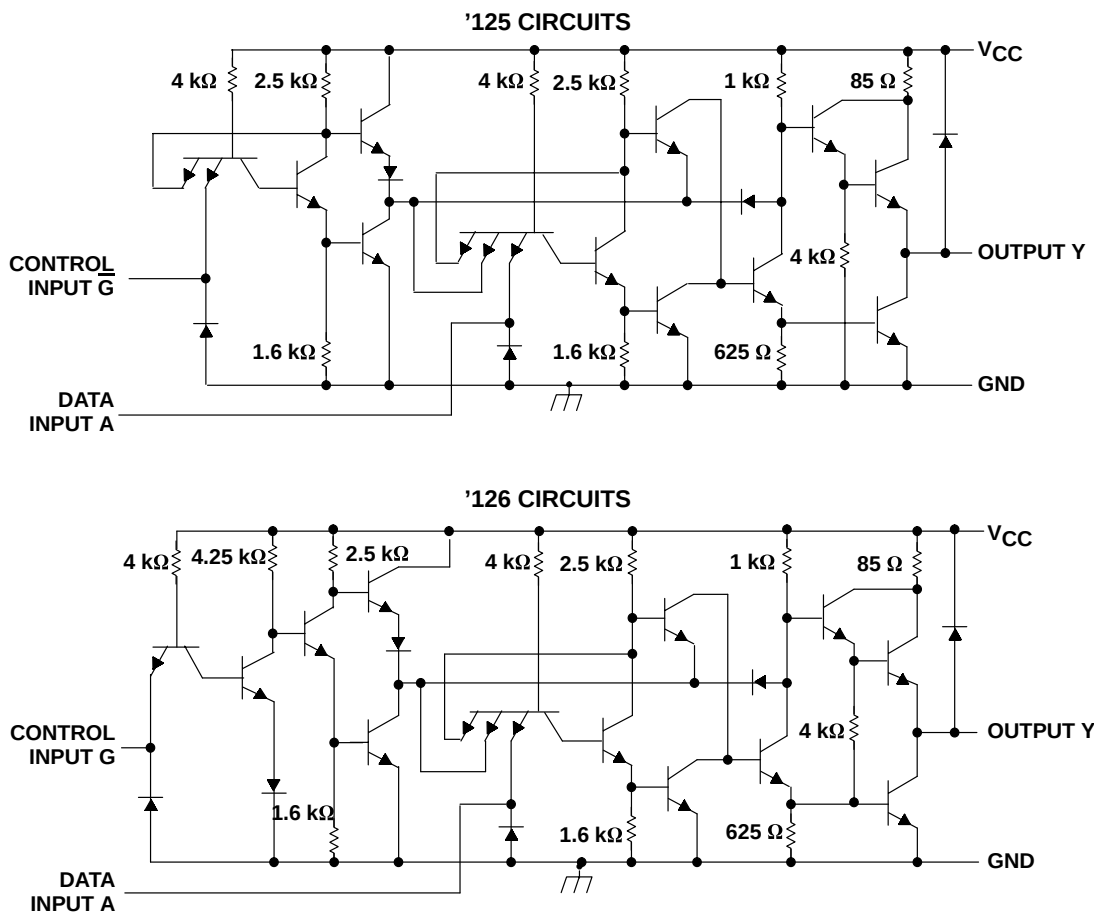


Y = A

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SN54125, SN54126, SN54LS125A, SN54LS126A, SN74125, SN74126, SN74LS125A, SN74LS126A QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS SDLS044A – DECEMBER 1983 – REVISED MARCH 2002

schematics (each gate)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†] ([']125 and [']126)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, V_I	5.5 V
Package thermal impedance, θ_{JA} (see Note 2): N package	80°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

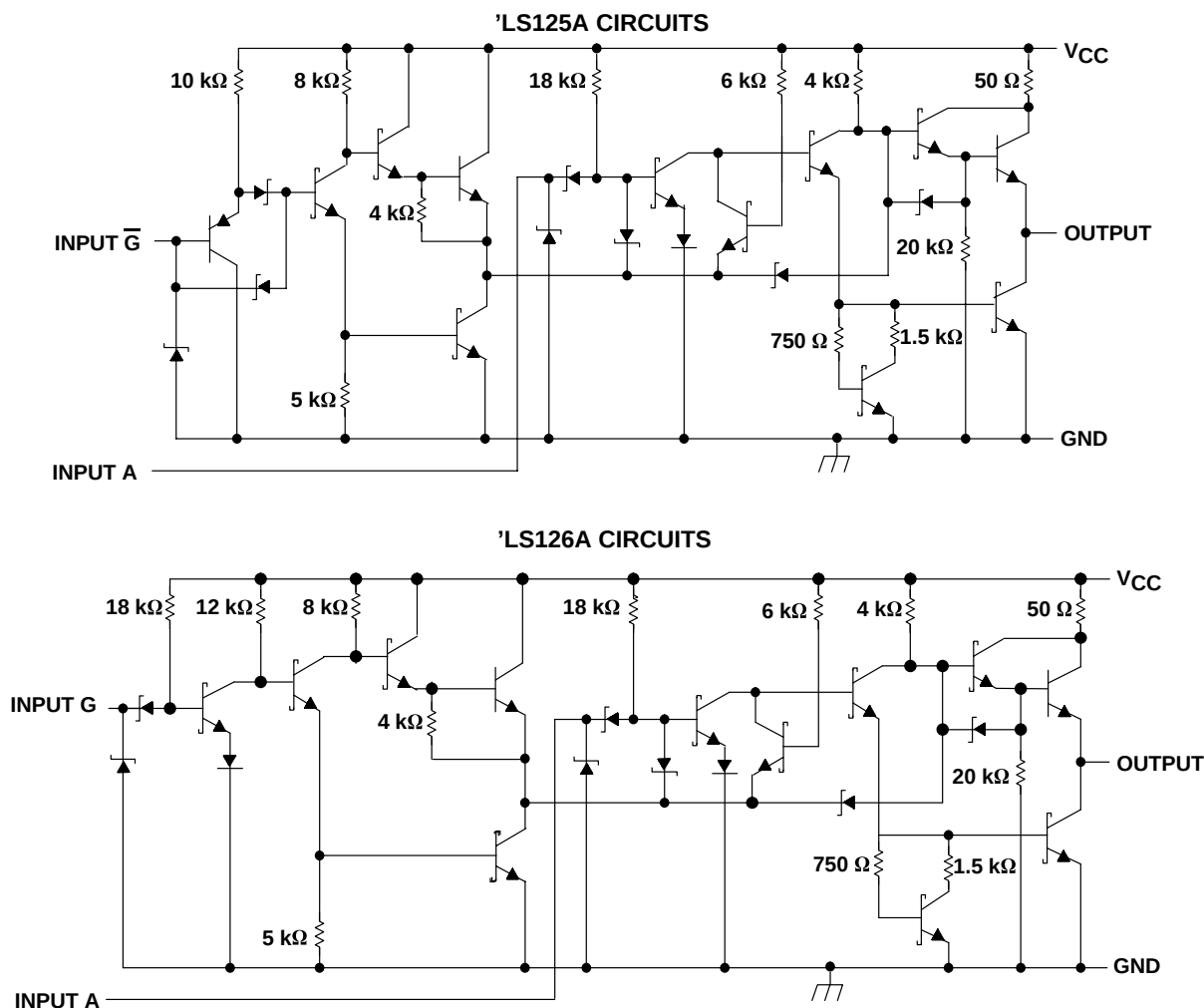
- NOTES: 1. Voltage values are with respect to network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

SN54125, SN54126, SN54LS125A, SN54LS126A, SN74125, SN74126, SN74LS125A, SN74LS126A QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

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The SN54125, SN54126, SN74125,
SN74126, and SN54LS126A are
obsolete and are no longer supplied.

schematics (each gate)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†] (**'LS125A and 'LS126A**)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, V_I	7 V
Package thermal impedance, θ_{JA} (see Note 2): D package	86°C/W
N package	80°C/W
NS package	76°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Voltage values are with respect to network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51-7.



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SN54125, SN54126, SN54LS125A, SN54LS126A, SN74125, SN74126, SN74LS125A, SN74LS126A QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

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recommended operating conditions

		SN54125 SN54126			SN74125 SN74126			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{OH}	High-level output current			–2			–5.2	mA
I _{OL}	Low-level output current			16			16	mA
T _A	Operating free-air temperature	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN54125 SN54126			SN74125 SN74126			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = –12 mA				–1.5			–1.5	V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V	I _{OH} = –2 mA	2.4	3.3					V
		I _{OH} = –5.2 mA				2.4	3.1		
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA				0.4			0.4	V
I _{OZ}	V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = 0.8 V	V _O = 2.4 V			40			40	μA
		V _O = 0.4 V			–40			–40	
I _I	V _{CC} = MAX, V _I = 6.5 V				1			1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.4 V				40			40	μA
I _{IL}	V _{CC} = MAX, V _I = 0.4 V				–1.6			–1.6	mA
I _{OS} §	V _{CC} = MAX		–30		–70	–28		–70	mA
I _{CC}	V _{CC} = MAX (see Note 3)	'125		32	54		32	54	mA
		'126		36	62		36	62	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

NOTE 3: Data inputs = 0 V; output control = 4.5 V for '125 and 0 V for '126.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

PARAMETER	TEST CONDITIONS		SN54125 SN74125			SN54126 SN74126			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t _{PLH}	R _L = 400 Ω, C _L = 50 pF			8	13		8	13	ns
t _{PHL}				12	18		12	18	
t _{PZH}	R _L = 400 Ω, C _L = 50 pF			11	17		11	18	ns
t _{PZL}				16	25		16	25	
t _{PHZ}	R _L = 400 Ω, C _L = 5 pF			5	8		10	16	ns
t _{PLZ}				7	12		12	18	



**SN54125, SN54126, SN54LS125A, SN54LS126A,
SN74125, SN74126, SN74LS125A, SN74LS126A
QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS**

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The SN54125, SN54126, SN74125,
SN74126, and SN54LS126A are
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recommended operating conditions

		SN54LS125A SN54LS126A			SN74LS125A SN74LS126A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
I _{OH}	High-level output current			–1			–2.6	mA
I _{OL}	Low-level output current			12			24	mA
T _A	Operating free-air temperature	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			SN54LS125A SN54LS126A		SN74LS125A SN74LS126A		UNIT
				MIN	TYP‡	MAX	MIN	
V _{IK}	V _{CC} = MIN, I _I = –18 mA			–1.5		–1.5		V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V	V _{IL} = 0.7 V,	I _{OH} = –1 mA	2.4				V
		V _{IL} = 0.8 V	I _{OH} = –2.6 mA			2.4		
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V	V _{IL} = 0.7 V,	I _{OL} = 12 mA	0.25	0.4			V
		V _{IL} = 0.8 V,	I _{OL} = 12 mA			0.25	0.4	
		V _{IL} = 0.8 V,	I _{OL} = 24 mA			0.35	0.5	
I _{OZ}	V _{CC} = MAX, V _{IH} = 2 V,	V _{IL} = 0.7 V	V _O = 2.4 V	20				µA
			V _O = 0.4 V	–20				
		V _{IL} = 0.8 V	V _O = 2.4 V			20		
			V _O = 0.4 V			–20		
I _I	V _{CC} = MAX, V _I = 7 V			0.1		0.1		mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V			20		20		µA
I _{IL}	V _{CC} = MAX, V _I = 0.4 V	'LS125A- $\overline{G}$ inputs		–0.2		–0.2		mA
		'LS125A-A inputs; 'LS126A All inputs		–0.4		–0.4		mA
I _{OS} §	V _{CC} = MAX			–40	–225	–40	–225	mA
I _{CC}	V _{CC} = MAX (see Note 4)	'LS125A		11	20	11	20	mA
		'LS126A		12	22	12	22	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

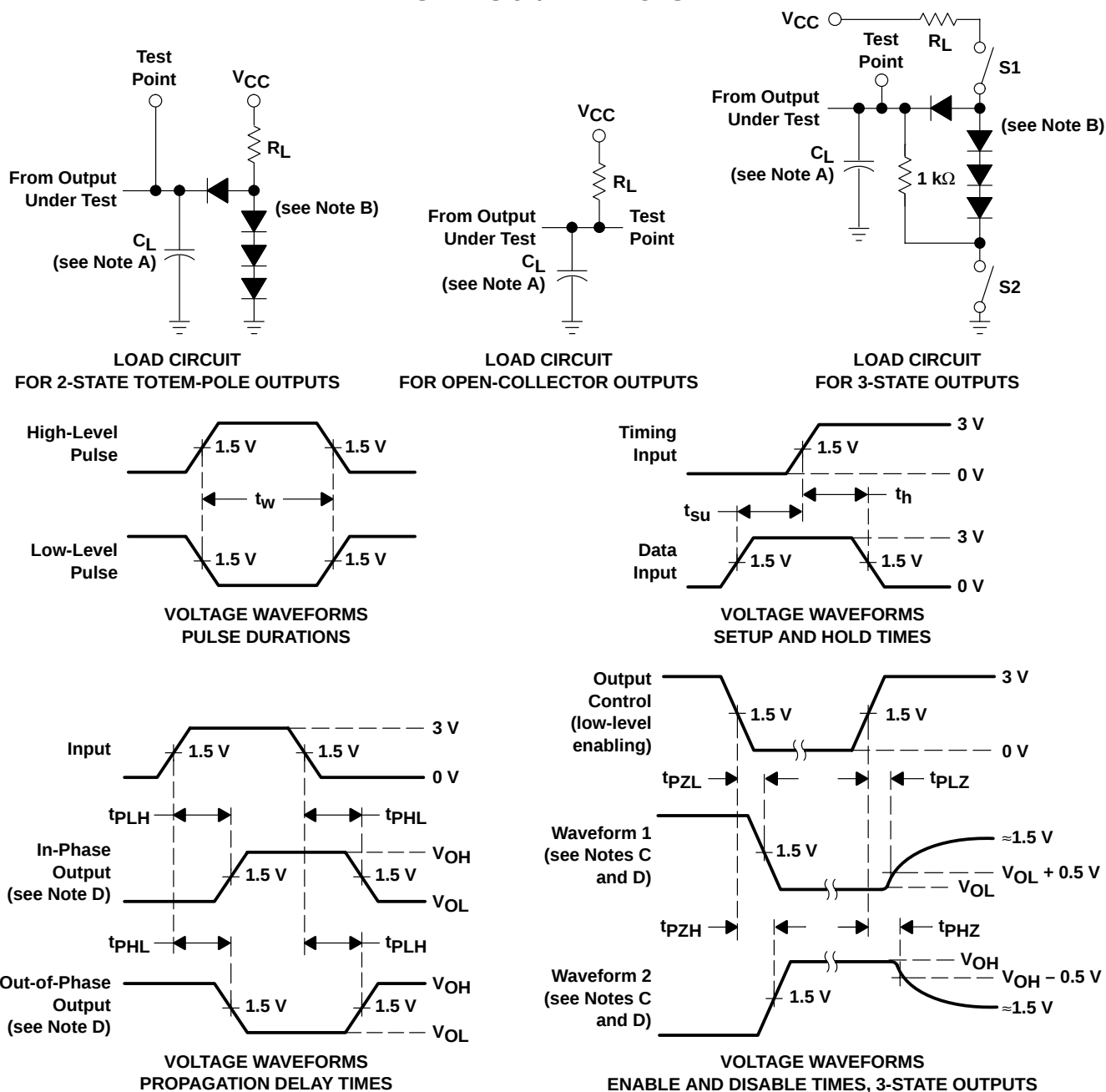
NOTE 4: Data inputs = 0 V; output control = 4.5 V for 'LS125A and 0 V for 'LS126A.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

PARAMETER	TEST CONDITIONS		SN54LS125A SN74LS125A			SN54LS126A SN74LS126A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t _{PLH}	R _L = 667 Ω, C _L = 45 pF			9	15		9	15	ns
t _{PHL}				7	18		8	18	
t _{PZH}	R _L = 667 Ω, C _L = 45 pF			12	20		16	25	ns
t _{PZL}				15	25		21	35	
t _{PHZ}	R _L = 667 Ω, C _L = 5 pF				20			25	ns
t _{PLZ}					20			25	



PARAMETER MEASUREMENT INFORMATION SERIES 54/74 DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. S1 and S2 are closed for t_{PLH} , t_{PHL} , t_{PHZ} , and t_{PLZ} ; S1 is open and S2 is closed for t_{PZH} ; S1 is closed and S2 is open for t_{PZL} .
E. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O \approx 50 \Omega$; t_r and $t_f \leq 7$ ns for Series 54/74 devices and t_r and $t_f \leq 2.5$ ns for Series 54S/74S devices.
F. The outputs are measured one at a time with one input transition per measurement.

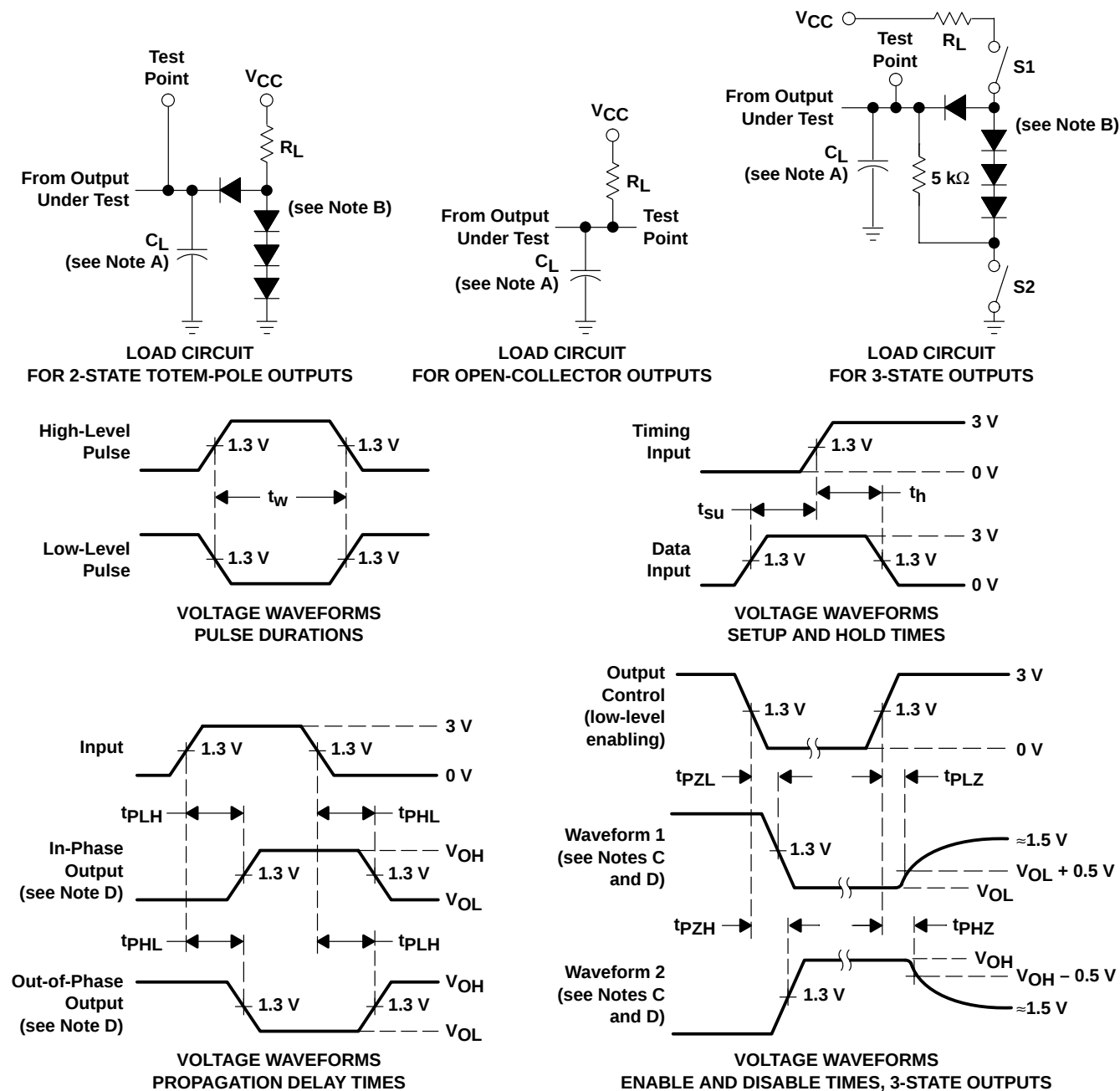
Figure 1. Load Circuits and Voltage Waveforms

**SN54125, SN54126, SN54LS125A, SN54LS126A,
SN74125, SN74126, SN74LS125A, SN74LS126A
QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS**

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**PARAMETER MEASUREMENT INFORMATION
SERIES 54LS/74LS DEVICES**



- NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. S1 and S2 are closed for t_{PLH} , t_{PHL} , t_{PHZ} , and t_{PLZ} ; S1 is open and S2 is closed for t_{PZH} ; S1 is closed and S2 is open for t_{PZL} .
E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
F. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O \approx 50 \Omega$, $t_r \leq 1.5$ ns, $t_f \leq 2.6$ ns.
G. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
JM38510/32301B2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 32301B2A
JM38510/32301BCA	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 32301BCA
JM38510/32301BDA	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 32301BDA
SN54LS125AJ	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS125AJ
SN74LS125AD	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	0 to 70	LS125A
SN74LS125ADBR	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS125A
SN74LS125ADR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS125A
SN74LS125AN	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS125AN
SN74LS125ANSR	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS125A
SN74LS126AD	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	0 to 70	LS126A
SN74LS126ADR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS126A
SN74LS126AN	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS126AN
SN74LS126ANSR	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS126A
SNJ54LS125AJ	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS125AJ
SNJ54LS125AW	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS125AW

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54LS125A, SN74LS125A :

- Catalog : [SN74LS125A](#)
- Military : [SN54LS125A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS125ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LS125ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS125ANSR	SOP	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LS126ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS126ANSR	SOP	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS125ADBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74LS125ADR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LS125ANSR	SOP	NS	14	2000	356.0	356.0	35.0
SN74LS126ADR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LS126ANSR	SOP	NS	14	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
JM38510/32301B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/32301BDA	W	CFP	14	25	506.98	26.16	6220	NA
M38510/32301B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
M38510/32301BDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74LS125AN	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS125AN	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS126AN	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS126AN	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54LS125AW	W	CFP	14	25	506.98	26.16	6220	NA

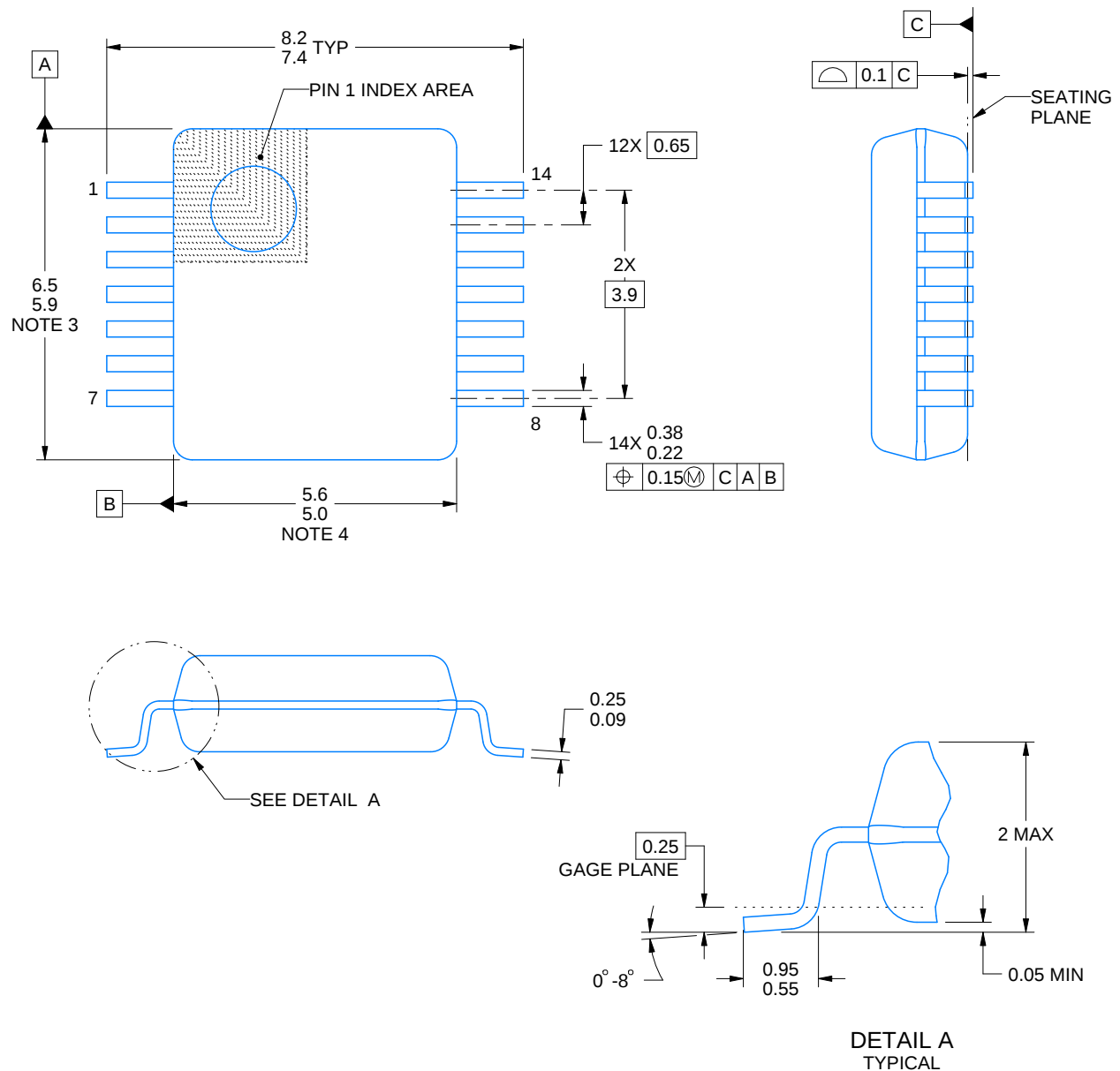
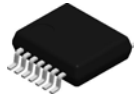
W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- This package can be hermetically sealed with a ceramic lid using glass frit.
- Index point is provided on cap for terminal identification only.
- Falls within MIL STD 1835 GDFP1-F14



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NOTES:

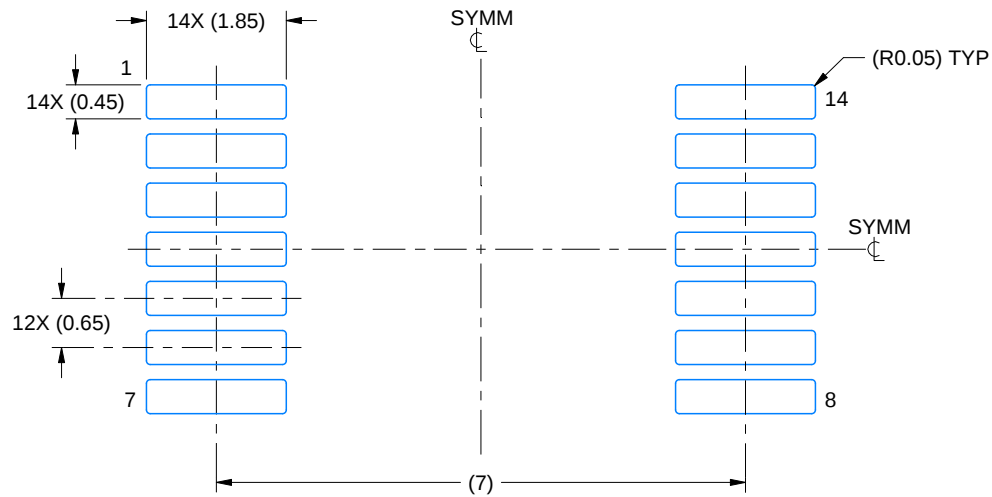
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

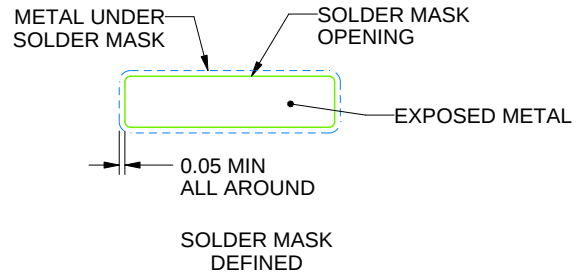
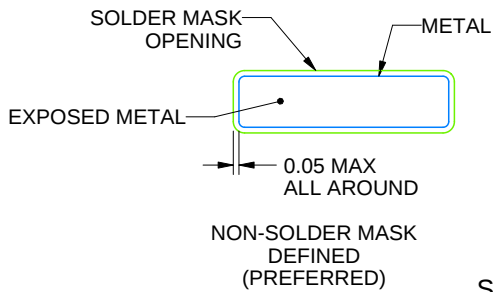
DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

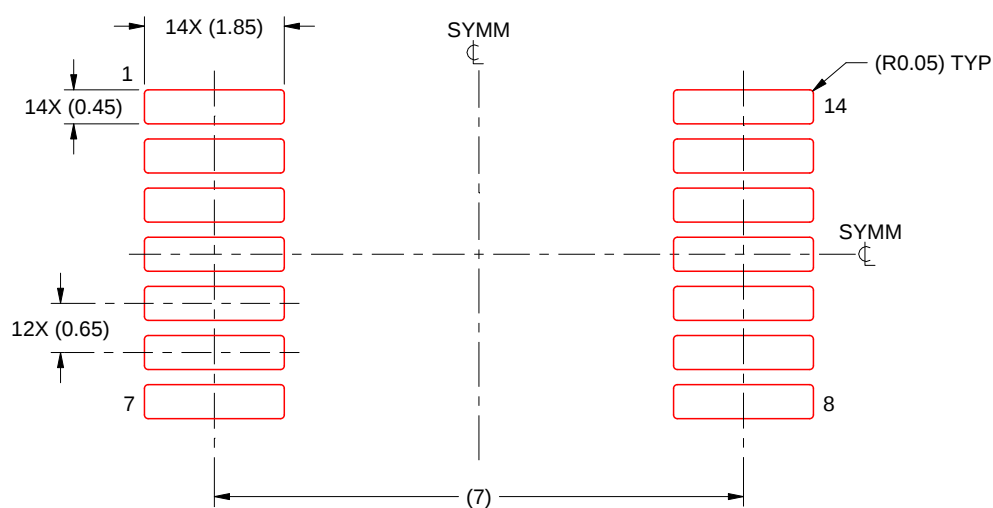
- Publication IPC-7351 may have alternate designs.
- Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

J 14

GENERIC PACKAGE VIEW

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A**PACKAGE OUTLINE****CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

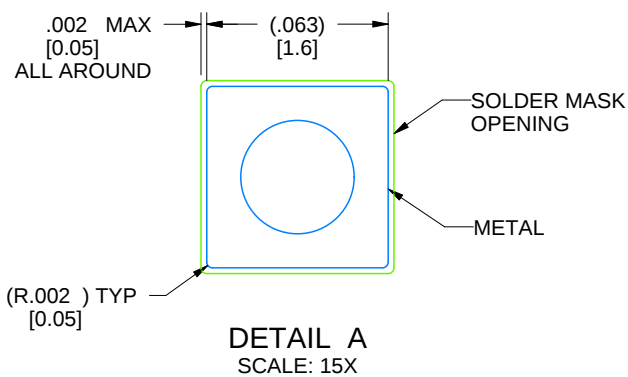
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

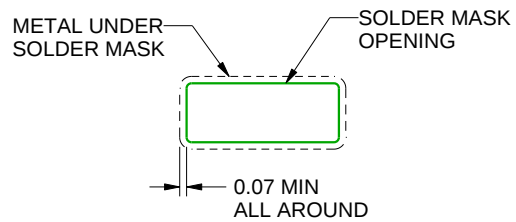
SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



NON SOLDER MASK
DEFINED



SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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